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A Three-Topology Based, Wide Input Range Switched-Capacitor DC-DC Converter with Low-Ripple and Enhanced Load Line Regulations

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***Abstract*—This paper presents a novel switched-capacitor (SC) DC-DC converter that incorporates three conversion topologies. At 100 kHz, the design is proposed to cater to wide input range, of 2.5 V to 4.5 V. Excellent accuracy and output regulation capabilities are obtained with output ripple voltage and error of ≤ 6 mV and ≤ 1.3%, respectively, when operated with a fixed output voltage of 1 V. A proportional-integral (PI) compensator is constructed for close-loop feedback compensation where it successfully enhanced both the load and line regulations. Finally, the peak efficiency of 70.76% is obtained at full load.**

Keywords—DC-DC converter; Switched-capacitor; Power Management.

I. Introduction

The accuracy of supply voltage for the subcircuits of some portable bio-electronics products such as the cardiac pacemaker and implantable biosensors is very important. In recent technology, most portable products are supplied by Li-ion battery whose supply varies from 2.5 V to 4.5 V. Since some subcircuits in the product operate at low power supply of 1 V, the need for a DC-DC converter with high accuracy has become clear.

The DC-DC converter has a primary function to provide a stable output from a time-varying voltage from battery supply. There are mainly two types of DC-DC converter, namely, the low drop-out (LDO) regulator and switched mode power supply (SMPS). LDO is not chosen in this design due to relatively low efficiency with high dependency on the input supply. Meanwhile, SMPS has two topologies, depending on its passive storage elements, namely switched inductor and switched capacitor (SC). The switched inductor has excellent efficiency but the deployment of bulky inductor makes it costly and consumes circuit area. Therefore, SC DC-DC converter is preferred for its compactness, hence cost effectiveness, and also its relatively higher efficiency.

The conventional SC converter was first introduced a few decades back with poor regulation capability due to lack of feedback mechanism. Moreover, the voltage conversion ratio is solely predetermined by the circuit structure, causing it inapplicable for wide input range converter design [1], [2].

Both the line and load regulations can be improved by adopting feedback compensator. One of the first generation of feedback mechanism called Classical Switching Scheme (CSS), utilizes on-resistance control scheme to drive the MOSFETs into the triode region of operation during the charging phase. This configuration suffered from electromagnetic interference (EMI) effect due to high current stress in the switching devices [3]. In order to reduce current spikes, the voltage-controlled current source (VCCS) scheme was developed [2], [4], [5]. In this scheme, the MOSFET is driven into saturation in order to control the charging profile of the capacitor with continuous analog input current. The VCCS is implemented using NMOS transistors for its lower on-resistance as compared to the PMOS transistors for a given transistor size. In this way, the drop-out voltage at the VCCS can be minimized to improve the input dynamic range of the converter [6].

II. SC DC-DC Converter Architecture

Fig. 1 shows a block diagram of a DC-DC converter with unity gain feedback deployed. A compensation circuit with a control-to-input transfer function of $G_c(s)$ is designed to meet the stability criteria of the system, including line and load regulations. Together with the circuit topology whose output-to-input transfer function is $G_{Vin}(s)$, it also determines the output accuracy, ripple and efficiency.

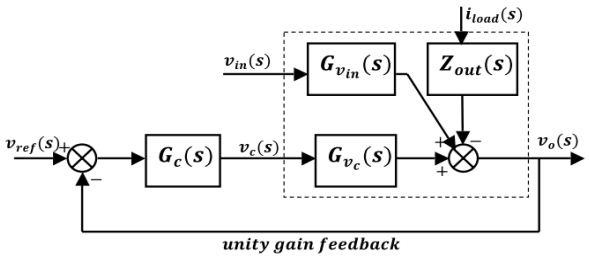

Fig. 1 Block diagram of DC-DC converter

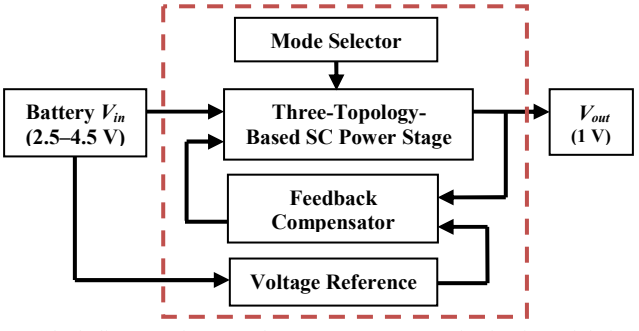

Fig. 2 Block diagram of proposed SC DC-DC converter in circuit module level

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Presented in Fig. 2 is the block diagram of our proposed SC DC-DC converter in circuit module level. The input voltage ranges from 2.5 V to 4.5 V and the output is fixed at 1 V. The SC power stage which is the main circuit block is designed to provide a choice of three circuits: 2/3, 1/2, or 1/3 conversion topologies. A mode selector is required to select the desired conversion topology for a certain input voltage. The output voltage is fed back to the input by comparing it with the reference voltage to obtain the desired output voltage of 1 V.

The schematic diagram of our proposed three-topology-based SC DC-DC converter is depicted in Fig. 3. The circuit consists of 14 switches (S1 to S14), two off-chip flying capacitors (C_{fly1} and C_{fly2}), each of $1\,\mu F$, and two VCCS's controlled by the feedback mechanism. The details of the circuit are described in this section.

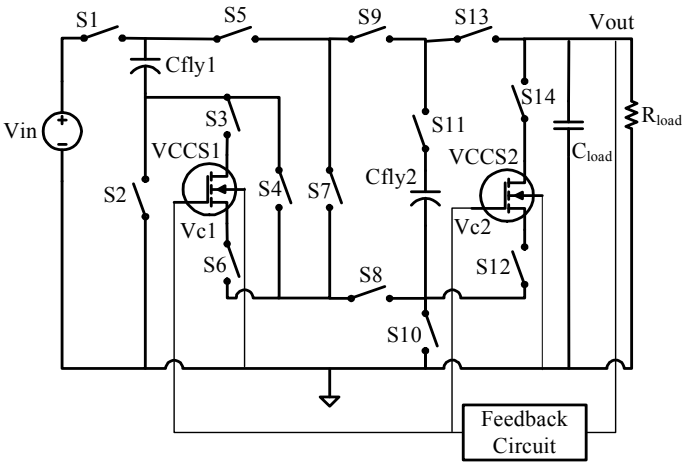

Fig. 3 Proposed SC DC-DC converter circuit configuration

A. Three-Topology-Based SC DC-DC Converter

The main power stage combines three topologies in order to achieve wider input voltage range. The topology type is identified by its ideal voltage conversion ratio (iVCR), while its voltage conversion ratio (VCR) is defined as the actual conversion ratio after the deployment of feedback mechanism. Provided that the load capacitor value is much higher than the flying capacitor (i.e. >10 times), the iVCR of certain topology can be determined using charge flow analysis [1]. The maximum efficiency, η_{max} can be obtained for varied topology using equation (1).

$$\eta_{max} = VCR / iVCR \tag{1}$$

Fig. 4 best describes the range classification of each converter topology, with its maximum efficiency. As can be seen, the maximum theoretical efficiency the proposed circuit can achieved is 75%.

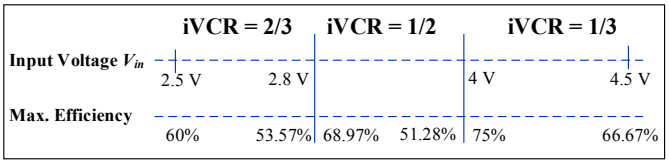

Fig. 4 Voltage range of each conversion topology with its maximum efficiency

There are two phases (i.e. ϕ_1 and ϕ_2) in each circuit topology, controlled by the switches. Non-overlapping clocks of frequency 100 kHz with dead time of 40 ns are constructed to determine the state of these switches. The detail of each conversion topology is explained as follows, and presented also in Fig. 5.

1) 2/3 conversion topology ($V_{in} \leqslant 2.8$ V):

Equation (2), given in Fig. 5, implements the charge flow analysis of 2/3 conversion topology, as described in Figs. 5(a) and 5(d), where $q_i^{(j)}$ is the amount of charge transferred by capacitor i during phase j, and vector $a^{(j)}$ is defined as an array that contains input charge, as well as the charges of all flying and output buffer capacitors during phase j.

In phase ϕ_1, if the charges at C_{fly1} and C_{fly2} are q, then by applying KCL at nodes X and Y, the charges at both input and output are obtained to be $2q$. On the other hand, the input is disconnected from the main circuit in phase ϕ_2, causing it to have zero charge with the output charge being q. Thus, the iVCR of the circuit can be verified to be 2/3 (see equation (2)).

The circuit utilizes 10 switches and two flying capacitors with VCCS2 supporting its feedback compensation. It is designated to operate when the input is not higher than 2.8 V. In the charging phase (i.e. phase ϕ_1), switches S1, S4, S9, S12, and S14 turn on, while on the discharging phase (i.e. phase ϕ_2) only switches S2, S7, and S13 are on. Also, S5 and S11 are always on with the rest of the switches being off.

2) 1/2 conversion topology ($2.8V < V_{in} < 4V$):

The *1/2* conversion topology utilizes only one flying capacitor C_{fly1} with VCCS1 as its controlled feedback. Again, if the charge at flying capacitor is q, then the charge at both the input and output during phase ϕ_1 are also q. In the discharging phase (i.e. phase ϕ_2), however, the input has no charge while the output has the same charge q as C_{fly1}. Thus, the iVCR of the circuit can be verified to be 1/2, as shown in equation (3) provided in Fig. 5.

This topology is designated for input voltage between 2.8 V and 4 V. It is commonly known as series-parallel topology. In this topology, switches S1, S3, S6, and S7 turn on during the charging phase, while switches S2, and S5 are on during discharging phase. Switches S9 and S13 are always on while the rest of the switches are completely off.

3) 1/3 conversion topology ($V_{in} \geqslant 4$ V):

The 1/3 conversion topology (refer to Figs. 5(c) and 5(f)) is designated for input voltage higher than 4 V. Similar to the 2/3 conversion topology, this topology utilizes both C_{fly1} and C_{fly2} with VCCS2 as its controlled feedback. Using similar charge flow analysis, equation (4) given in Fig. 5 verifies the conversion topology of the circuit.

During the charging phase, switches S1, S4, S7, S12, and S14 turn on, while S2, S5, S10, and S13 turn on during the discharging phase. S9 and S11 are always on and the remaining switches are completely off.

$$a^{(1)} = \left[q_{out}^{(1)} q_1^{(1)} q_2^{(1)} q_{in}^{(1)}\right] / q_{out} = \left[\begin{array}{cccc} \frac{2}{3} & \frac{1}{3} & \frac{1}{3} & \boxed{\frac{2}{3}} \end{array}\right]$$

$$a^{(2)} = \left[q_{out}^{(2)} q_1^{(2)} q_2^{(2)} q_{in}^{(2)}\right] / q_{out} = \left[\begin{array}{cccc} \frac{1}{3} & -\frac{1}{3} & -\frac{1}{3} & \boxed{0} \end{array}\right]$$

$$iVCR = \frac{q_{in}^{(1)} + q_{in}^{(2)}}{q_{out}} = \frac{2}{3} + 0 = \frac{2}{3} \quad (2)$$

$$a^{(1)} = \left[q_{out}^{(1)} q_1^{(1)} q_{in}^{(1)}\right] / q_{out} = \left[\begin{array}{ccc} \frac{1}{2} & \frac{1}{2} & \boxed{\frac{1}{2}} \end{array}\right]$$

$$a^{(2)} = \left[q_{out}^{(2)} q_1^{(2)} q_{in}^{(2)}\right] / q_{out} = \left[\begin{array}{ccc} \frac{1}{2} & -\frac{1}{2} & \boxed{0} \end{array}\right]$$

$$iVCR = \frac{q_{in}^{(1)} + q_{in}^{(2)}}{q_{out}} = \frac{1}{2} + 0 = \frac{1}{2} \quad (3)$$

$$a^{(1)} = \left[q_{out}^{(1)} q_1^{(1)} q_2^{(1)} q_{in}^{(1)}\right] / q_{out} = \left[\begin{array}{cccc} \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & \boxed{\frac{1}{3}} \end{array}\right]$$

$$a^{(2)} = \left[q_{out}^{(2)} q_1^{(2)} q_2^{(2)} q_{in}^{(2)}\right] / q_{out} = \left[\begin{array}{cccc} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} & \boxed{0} \end{array}\right]$$

$$iVCR = \frac{q_{in}^{(1)} + q_{in}^{(2)}}{q_{out}} = \frac{1}{3} + 0 = \frac{1}{3} \quad (4)$$

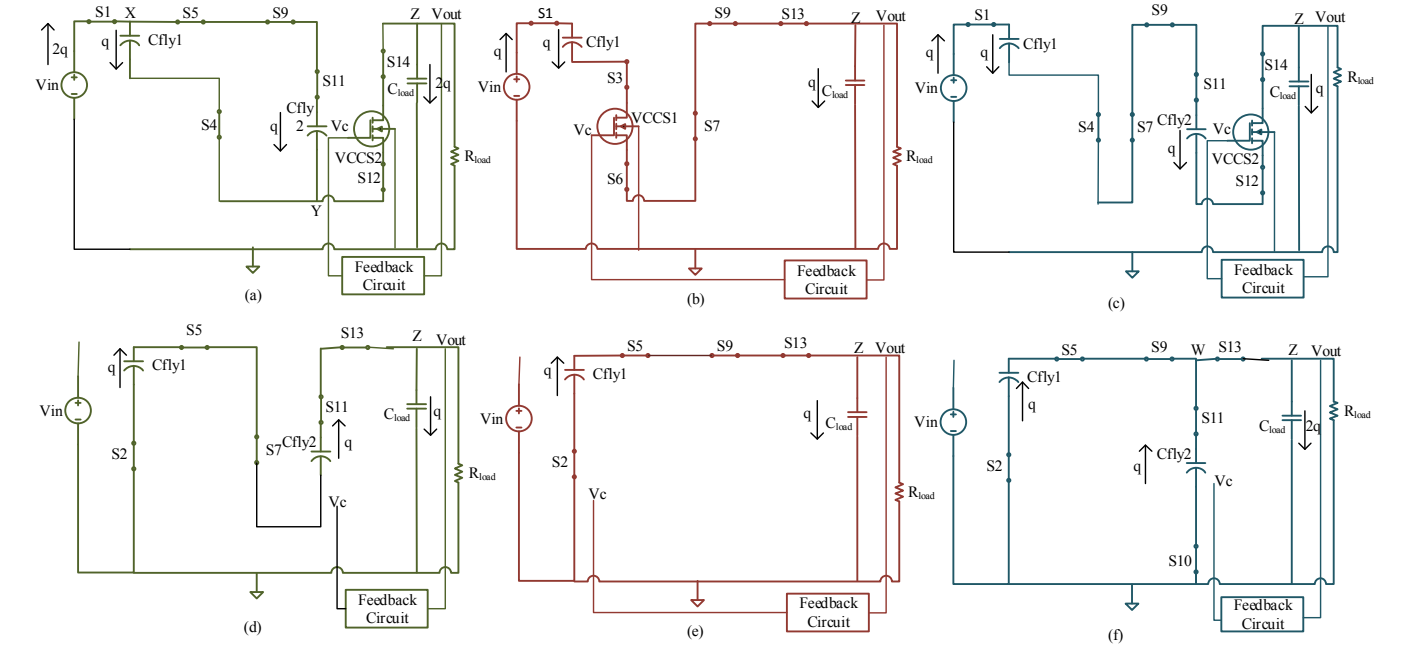

Fig. 5 Equivalent proposed circuit for each topology: (a) 2/3–charging phase, (b) 1/2-charging phase, (c) 1/3-charging phase, (d) 2/3–discharging phase, (e) 1/2-discharging phase, (f) 1/3-discharging phase

B. *Feedback Circuit*

Fig. 6 shows the proportional-integral (PI) compensator for the system. Built-in compensator is preferred for cost/area saving. Hence, all the resistors (i.e. R_{eq1} and R_{eq2}) must be replaced by switching capacitors. The switching frequency of the switched-capacitor based resistor, f_R, needs to be at least 4 times that of the switching frequency of the system [2]. In this design, f_R = 400 kHz, and C_1, C_2, R_{eq1}, and R_{eq2} are chosen to be 50 fF, 10pF, 2.5 MΩ, and 25 MΩ, respectively. Thus, the value of capacitor C_{R1} and C_{R2} can be determined using the following equations:

$$C_{R1} = \frac{1}{f_R \times R_{eq1}} = 1pF \ , \ C_{R2} = \frac{1}{f_R \times R_{eq2}} = 100fF \quad (5)$$

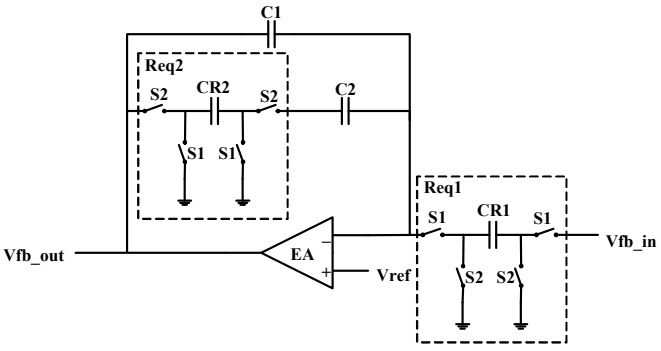

Fig. 6 Proportional Integral (PI) compensator of the SC DC-DC converter

C. *Mode Selector*

The mode selector circuit engaged in our proposed SC DC-DC converter is presented in Fig. 7. Resistors R_1, R_2, and R_3 are chosen to be R_1:R_2:R_3 = 3:2:5. If input voltage V_{in} is higher than 4 V, V_{ref} will be less than V_1 and V_2, resulting in output Q and Q' to be 1 and 0, respectively. At this instant, the circuit will work in 1/3 conversion topology. For the case of V_{in} value between 2.8 V to 4 V, V_{ref} will be less than V_2 but higher than V_1, and signal Q and Q' will be both 0, causing the circuit to work in 1/2 conversion topology. Lastly, if V_{in} is less than 2.9 V, V_{ref} is higher than V_1 and V_2. Consequently, signal Q and Q' will be 0 and 1, respectively, to cause the circuit to operate in the 2/3 conversion topology.

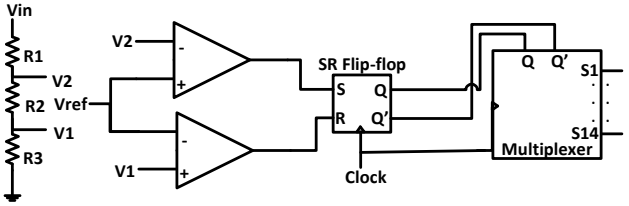

Fig. 7 Mode selector circuit

Table 1 Performance comparison with other SC DC-DC converters

Reference/year	[8]/2006	[5]/2008	[7]/2009	[2]/2010	[9]/2012	[6]/2013	this work*/2013
Process (µm)	0.5	0.35	0.35	0.35	0.35	0.35	**0.18**
V_{in} /(V)	1.8-3.5	2.5	2.9–5.5	2.4–5.5	2.7–5	1.8–5	**2.5–4.5**
V_{out} (V)	3.2	0.8–1.5	5	3.6	1.8	3.3	**1**
Load range (mA)	< 6	< 5	< 48	< 16.8	< 200	10–30	**1–10**
Flying/Load cap (µF)	1/10	3.36 nF/N.R.	1/10	1/10	1/10	1/10	**1/10**
Frequency (Hz)	90k	200 k–1 M	250k	100k	16–500k	100k	**100k**
Load Regulation (mV/mA)	9.3	NR	16.7	1	N.R.	1.82	**0.097**
Line Regulation (mV/V)	11	N.R.	9.258	N.R.	N.R.	64	**7.77**
Ripple (mV)	N.R.	110	6.254	40	< 8	50	**≤ 6**
Peak Efficiency (%)	N.R.	66.7	~85	80	87	80	**70.76**

N.R. = Not Reported; * = simulation results

III. Simulation Results

Simulation results show that the output voltage of our proposed SC DC-DC converter ranges from 995.3 mV to 1.013 V (i.e. error ⩽ 1.3%), with ripple voltage of at most 6 mV, as validated in Fig. 8. The worst ripple voltage is of 4.06% improvement from previous reported work (ref. [7]) (see Table 1). To maintain the high output accuracy, however, the circuit does suffered from slight reduction in efficiency. A peak efficiency of 70.76% is obtained at full-load as presented in Fig. 9. This is a 6.09% improvement from reported work (ref. [5]), but it is still less than ref. [9], which shares the same characteristics of a fully step-down DC-DC converter.

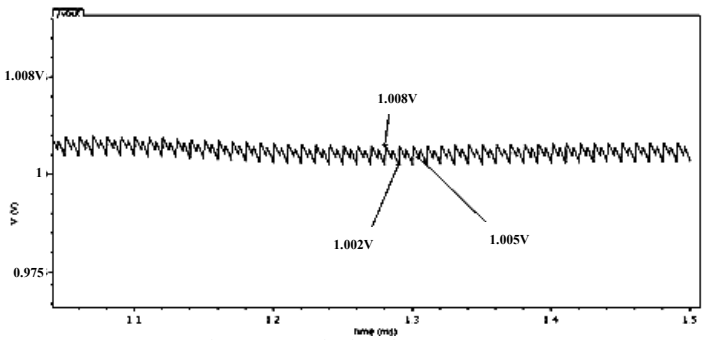

Fig. 8 Output ripple voltage at V_{in} = 2.6 V

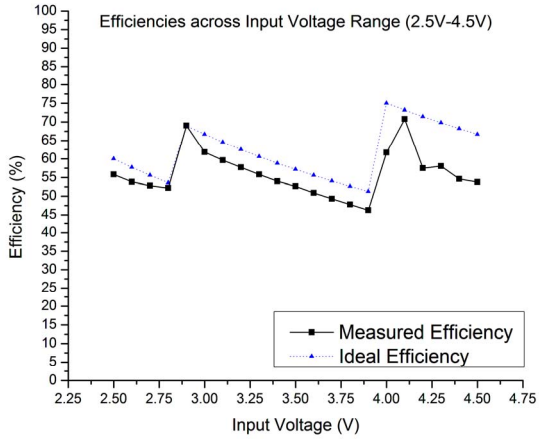

Fig. 9 Efficiency of proposed SC DC-DC converter

The output regulation shows excellent result when benchmarked against other recently reported works. The PI compensator enhances the load regulation capability at 0.097 mV/mA. Moreover, excellent line regulation was also obtained with worst value of 7.77 mV/V for the 1/3 topology. The line regulation measured at 2/3 and 1/2 topologies are 0.081 mV/V and 0.231 mV/V, respectively.

IV. Conclusions

The proposed wide-input-range SC DC-DC converter offers high accuracy and excellent regulation capability. In addition, very low ripple voltage makes the converter suitable for both digital and analog application, without the need of additional LDO which may significantly reduce the efficiency. As a trade-off, the efficiency must be slightly sacrificed to meet prominent requirement.

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