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<tr>
<th><strong>Title</strong></th>
<th>A 13.8-MHz RC Oscillator with Self-Calibration for ±0.4% Temperature Stability from -55 to 125°C</th>
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<tr>
<td><strong>Author(s)</strong></td>
<td>Wang, Jiacheng; Koh, Leong Hai; Goh, Wang Ling</td>
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Abstract—This paper articulates a novel oscillator design that can provide stable frequency operation over a wide temperature range with self-calibration technique. A simple ring oscillator is implemented to sense the temperature variation, and some digital circuits tune the output frequency according to the sensing outcomes. Simulation results show that the circuit can generate a stable frequency of 13.8MHz. The power consumption of the whole system is only 52.8µW. The temperature coefficient is less than ±0.4% ranging from -55 to 125 °C in the worst process corner whereas the supply voltage is ultra-low at 0.6V.

I. INTRODUCTION

Integrated low-frequency oscillators with excellent temperature variation performance can be used to replace crystal oscillators to reduce the size and cost of single-chip systems [1]. Furthermore, many wireless sensor networks demand a low-power on-chip real-time clock circuit. This is because the real-time clock block stay awake even though other sub-circuit blocks enter sleep mode. The frequency stability of the oscillator against temperature and supply variations is a critical specification for an on-chip oscillator.

For the past several years, many research studies of on-chip oscillator are reported [1–4]. A comparator offset cancellation is adopted in [1], whereby a very large resistor (5MΩ) is chosen which fails to optimize chip area. In [2], the voltage average feedback methods are implemented to achieve high stability in the MHz frequency. Three comparators and two additional reference voltages are implemented in [3], and a feedback loop with integrator can also maintain the frequency stability versus temperature. In [4], a pre-charge is used to compensate the delay time variation of comparators when temperature varies. On the other hand, resistors with positive and negative temperature coefficient are also implemented which requires additional masks in fabrication process. However, most of them use analog integrator feedback loop to get the stable frequency, which are power hungry and not easy to move to advanced CMOS process.

Therefore, a fully on-chip oscillator with temperature self-calibration technique is proposed in this paper. In this design, an extremely simple ring oscillator senses the temperature variation. Some digital logics and capacitor arrays are used to maintain the output frequency stability. The following section will provide the details of the proposed work. In section II, the system level architecture and circuit details are presented with comparison between the conventional architecture and proposed oscillator. And the simulation results about the proposed circuits are shown in the section III. Finally, the conclusion is given in the section IV. The whole system works under only 0.6V power supply voltage in the standard 65nm CMOS process, which achieves ultra-low-power of 52.8µW. The oscillator can generate a stable frequency at 13.8MHz. A low temperature coefficient of ±0.4% is attainable with ambient temperature ranging from −55 to 125 °C temperature variations.

II. OSCILLATOR CIRCUIT TOPOLOGY

A. Conventional Temperature Compensation Oscillator

The conventional oscillator, as shown in Fig. 1, yields an output frequency which stays invariant when temperature changes [5]. The reference current, $I_{ref}$, goes through a fixed resistor to generate a reference voltage, $V_{ref}$, for comparison. When the oscillator is in operation, a ramp voltage will be generated across the capacitors $C_1$ and $C_2$ respectively. The two capacitor will trigger when the $V_{C1}$ and $V_{C2}$ approach to $V_{ref}$.

Assume the both capacitors are the same value, it can be derived as:

$$V_{ref} = I_{ref} \cdot R = \frac{I_{ref} \cdot t}{C_{1/2}} \quad (1)$$

where $I_{ref}$ is the reference current in these current sources, and $t$ is the charging time duration for the voltage across a capacitor to rise from zero to $V_{ref}$. After simplification, the
The frequency of this oscillator is given as:

\[ f = \frac{1}{2RC_{1,2}} \]  

(2)

Unfortunately, the ramp voltage seen across the capacitors will not begin to discharge at \( V_{ref} \) due to the presence of delay time \( \tau \) and offset voltage \( V_{os} \) of the comparator. Therefore, the frequency of the oscillator varies. After considering these non-ideal parameters, the frequency is recalculated to be:

\[ f = \frac{1}{2RC_{1,2} + \frac{C_{1,2}V_{os}}{I_{ref}} + 2\tau} \]  

(3)

Furthermore, in conventional oscillator architecture, the frequency stability can be affected by mismatch found in current sources, comparator and capacitor. Hence, there are interesting techniques to mitigate these non-idealities.

**B. Proposed Oscillator Architecture**

The system architecture of this proposed oscillator is shown in Fig. 2, which consists of two parts: a main oscillator part and a temperature sensing part. The main oscillator consists of a RC oscillation pair and a comparator to generate an output frequency (\( \phi \) in Fig. 2). The other part is used to sense environment temperature variations and generate control bits to tune the frequency when the working environments vary. As shown in Fig. 2, when \( en_{cal} = 1 \), a voltage regulator begins to provide power to the simple ring oscillator. This frequency of ring oscillator varies with temperature. A counter records the ring oscillator cycles and generates some feedback bits to control the capacitors in the main oscillator.

**C. Main Oscillator Circuit**

The main oscillator circuit shown in Fig. 2 is as in the reference [1], but with two additional capacitor arrays for frequency tuning when self-calibration technique enables. In this structure, only one comparator is used and four chopper switches can cancel the comparator offset. When \( \phi = 1 \), the current \( I_{ref} \) goes through the resistor \( R \) to generate a reference voltage. This reference voltage is connected to negative input of the comparator. At the same time, a same current charges the right side capacitors \( (C+C_{array}) \). If the comparator has an offset voltage \( V_{os} \), the period of \( \phi = 1 \) will be last for \( (C+C_{array})V_{os}/I_{ref} \) longer. On the contrary, at the \( \phi = 0 \) phase, the reference voltage generated by resistor will be connected to the positive input of comparator, and the reference current charges the left side capacitors. Therefore, the duration of \( \phi = 0 \) will be decreased by the same value. Thus the comparator offset can be compensated.

In this design, the resistor is chosen to be \( 150K\Omega \) and \( C \) is \( 200fF \) for a RC oscillation time constant. The resistor \( R \) is composed of p-polysilicon resistors (complementary to absolute temperature) and n-well resistors (proportional to absolute temperature), which can compensate the resistance variation versus the temperature. The oscillation frequency can be expressed as:

\[ f = \frac{1}{2R \cdot (C+C_{array}) + 2\tau} \]  

(4)

where the parameter \( \tau \) is the loop delay from comparator logics to switches. In MHz frequency, the variation of delay time \( \tau \) will influence the output frequency. In the following section, a temperature sensing and compensation technique is proposed to compensate the frequency variation.

**D. Temperature Sensing and Compensation**

In this design, a simple inverter-based ring oscillator is implemented to sense temperature variation. Due to the ultra-low supply voltage (0.6V) in standard 65nm CMOS process, the output frequency of this ring oscillator is higher when temperature increases. The simulation result of this ring oscillator is shown in the Fig. 3 with different process corners. The Fig. 4 shows tuning algorithm of the digital compensation progress.
At first, the main on-chip oscillator generates a frequency based on the RC time constant. When the digital calibration part is enabled \( (en_{cal} = 1 \text{ in Fig. 2}) \), the ring oscillator and some digital logics begin to work. A counter records the number of ring oscillator cycles when the RC oscillator is at high voltage level. It is used to compare with the number of cycles in the room temperature which is recorded in the registers at the first time working. If the number of counter is larger than the normal one, it means that the temperature is higher. And tuning bits are generated from some digital logics and registers for feedback to the main oscillator. The capacitor array will increase the \( C \) value to reduce the oscillation frequency. As the temperature does not vary abruptly, an general purpose performance temperature sensor will do the job. But it must be monotonic to the temperature. A switched voltage regulator provides power to the ring oscillator. It can limit the current consumption at high frequency. And the control voltage \( V_{control} \) can also compensate the ring oscillator frequency variations under different process corners.

The advantages of this digital self-calibration are listed. Firstly, compared to the analog integrator loops in [2, 3], the proposed calibration loop is separated from the main oscillator. It means it can be shut down after the compensation finished. Therefore, it can save more power during a long term operation. Secondly, the self-calibration parts are mostly in the digital domain, which is suitable for the CMOS process shrinking to the advanced technologies. Furthermore, it is easy to integrate the digital part into a larger DSP or SoC system.

III. SIMULATION RESULTS

The prototype circuit of this oscillator is designed with GlobalFoundries 65nm standard CMOS process and under an ultra-low supply voltage 0.6V. In this design, each of the reference current source \( I_{ref} \) is 1\( \mu \)A. The whole power consumption is only 52.8\( \mu \)W, which consists of 16.8\( \mu \)W analog main oscillator power and 36\( \mu \)W self-calibration block power.

Fig. 5 shows the oscillation frequency variation versus temperature with different process corners at the supply voltage 0.6V. At room temperature 27°C, the standard output frequency is 13.82MHz at TT corner. From Fig. 5, the frequency variation is observed to range from 13.6MHz to 14.1MHz before calibration. After self-calibration, the frequency can be more stable at 13.81MHz to 13.87MHz, which is \( \pm 0.2\% \) after normalization. Even in the worst SS corner, the frequency variation is from 13.28MHz to 13.4MHz (less than \( \pm 0.4\% \) after normalization) after calibration.

Fig. 6 illustrates the oscillation frequency variation versus different supply voltage with digital frequency calibration. In order to keep the PTAT (proportional to absolute temperature) frequency characteristic, the supply voltage needs to be low enough to keep MOS-FETs in sub-threshold region. At room temperature 27°C, for the supply voltage ranging from 0.5 to 0.9V, the frequency varies from 13.81 MHz to 13.86 MHz after calibration at TT process corner. In the worst SS corner, it is from 13.31 to 13.4 MHz after digital compensation. The variation is \( \pm 0.8\%/V \) after normalization. From these figures,
TABLE I. PERFORMANCES SUMMARY AND COMPARISON

<table>
<thead>
<tr>
<th>Reference</th>
<th>Process (nm)</th>
<th>Temperature (°C)</th>
<th>Supply (V)</th>
<th>Frequency (MHz)</th>
<th>Power (µW)</th>
<th>Temperature Coefficient</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCAS-I 2013 [2]</td>
<td>130</td>
<td>25−200</td>
<td>2.5±1.2</td>
<td>1.7±1.9</td>
<td>100</td>
<td>±0.2%</td>
</tr>
<tr>
<td>ISSCC 2013 [3]</td>
<td>65</td>
<td>0−80</td>
<td>1±6</td>
<td>14±6</td>
<td>80</td>
<td>±0.4%</td>
</tr>
<tr>
<td>ISSCC 2009 [4]</td>
<td>180</td>
<td>−40−125</td>
<td>1.15±1.35</td>
<td>6±1</td>
<td>38.2</td>
<td>±0.25%</td>
</tr>
<tr>
<td>VLSI 2010 [6]</td>
<td>180</td>
<td>20−100</td>
<td>12±6</td>
<td>14±6</td>
<td>391</td>
<td>±0.82%</td>
</tr>
<tr>
<td>VLSI 2009 [7]</td>
<td>130</td>
<td>−20−100</td>
<td>1±6</td>
<td>14±6</td>
<td>98.4</td>
<td>±0.75%</td>
</tr>
<tr>
<td>ISSCC 2009 [8]</td>
<td>65</td>
<td>−55−125</td>
<td>1±6</td>
<td>14±6</td>
<td>45</td>
<td>±0.75%</td>
</tr>
<tr>
<td>This Work</td>
<td>65</td>
<td>−20−100</td>
<td>1±6</td>
<td>14±6</td>
<td>38.2</td>
<td>±0.25%</td>
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it shows the proposed relaxation oscillator can get a stable frequency with the temperature and supply voltage variations. Finally, Table I summarizes the performance of our on-chip oscillator compared to other ones.

IV. CONCLUSION

This paper presents a novel on-chip RC oscillator with self-calibration technique to achieve a stable output frequency with the environment temperature variation. This design is implemented in a standard 65nm CMOS process. A digital self-calibration technique is used to avoid the frequency drift. Simulation results show that the output frequency has ±0.4% variation with temperature from −55 to 125°C even in the worst process case. Moreover, the power consumption of the main oscillator yields only 16.8µW, and the whole system consumes only 52.8µW.

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REFERENCES