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3-state BTL Closed-loop PWM Class D Amplifiers

Huiqiao He • Tong Ge • Linfei Guo • Joseph S. Chang

Abstract One of the shortcomings of a number of Class D Amplifiers (CDAs) designs is their susceptibility to supply noise, quantified by Power Supply Rejection Ratio (PSRR). Reported investigations thereto to-date remain incomplete/over-simplified, particularly the assumption that the AC ground is noise-less and a simplified fully-differential integrator model. In this paper, the effect of supply noise in the AC ground to PSRR is analytically investigated, and the associated analytical expressions derived. Of specific interest, the analysis is applied to the ubiquitous 3-state Bridge-tied-load (BTL) closed-loop PWM CDA, taking into consideration not only the effect of the non-ideal AC ground, but also the effect of the resistor and capacitor mismatch based on a realistic fully-differential integrator model. Further, the PSRR analysis of 3-state BTL closed-loop CDAs has to date been limited to the single-feedback topology and in this paper, extended to the double-feedback topology. These analyses and derived equations herein are useful as they provide valuable insights to CDA designers into the PSRR mechanisms – for example, the counter-intuitive observation that the CDA with 1st-order integrators provides similar or better PSRR than the CDA with 2nd-order integrators if both CDAs are designed to the same carrier attenuation – including the effect of various circuit parameters, and ensuing trade-offs. The derived analytical expressions are verified by means of HSPICE simulations and on the basis of practical measurements on discretely-realized CDAs.

Keywords Class D Amplifiers • Bridge-Tied-Load • Carrier Generator • Power Supply Rejection Ratio • Pulse-Width-Modulation

1 Introduction

Class D Amplifiers (CDAs) [1-5] are increasingly prevalent as the audio amplifier (speakerphone) of choice for mobile devices, including smartphones, tablets, wearable electronics, etc. This is largely because of their substantially higher power-efficiency over their linear amplifier counterparts, such as Class A and Class AB amplifiers. In these mobile devices, the battery is the power source shared between many ICs and SoCs therein, whose operations induce significant noise onto the battery supply rails. As CDAs typically have their supply rails tied directly to the battery for reasons of cost (hardware simplicity) and power efficiency, their performance is degraded if their supply-noise susceptibility is poor; the supply-noise susceptibility is qualified by Power Supply Rejection Ratio (PSRR) [3,5,6]. Put simply, it is imperative for a CDA to feature high PSRR to tolerate a noisy supply rail in highly-integrated ICs and SoCs, such as high PSRR (>90dB) at 217Hz, the principle interfering GSM signal frequency. For completeness, amongst the different CDA architectures, the Pulse-Width-Modulation (PWM) CDA is the most popular CDA architecture adopted in mobile devices due to their simple hardware and relatively high fidelity. In this paper, this is the specific CDA architecture of interest.

Interestingly, in view of the imperative nature of PSRR for CDAs, reported analytical investigations in literature are incomplete and/or somewhat over-simplified. For example, investigations [6, 7] into the PSRR of PWM CDAs revealed that the important parameters affecting PSRR include the loop gain, and for single-ended and Bridge-tied-load (BTL) CDAs respectively, the design of the carrier generator and the matching between the two branches. Despite the valuable insights provided in these reported investigations, an imperative limitation is a somewhat simplified assumption, particularly that the AC ground is noise-free – an unrealistic assumption in present-day highly-integrated ICs and SoCs. Although the AC ground is recognized to be important [8, 9] to the PSRR of CDAs, their mechanisms remain uninvestigated and unreported. Put simply, as the AC ground serves as the bias point to the carrier generator and to the fully-differential
op amps for high dynamic range, the noise in the AC ground would, as expected, affect the PSRR.

Furthermore, the reported analysis [7, 9] of the PSRR of single-feedback BTL CDAs is also somewhat incomplete because it is based on an oversimplified fully-differential integrator model – modeled simply as two independent single-ended integrators. This simplified model is inadequate because the output of a fully-differential integrator depends not only on the common-mode voltage reference (i.e., AC ground) but also on the resistors and capacitors in the two branches of the integrator – specifically that there may be mismatches between the resistors and capacitors in the two branches. An investigation based on a realistic model will depict a comprehensive overview of the effect of the mismatch of each resistor pair and capacitor pair. This is pertinent because the layout of resistors and capacitors to obtain high matching can be area intensive, hence costly and if possible, avoided.

Yet further, the analysis [7] of the PSRR of BTL CDAs remain largely incomplete. Specifically, to date, only the PSRR of BTL CDAs based on the single-feedback topology has been reported while BTL CDAs based on double-feedback remain unreported. BTL CDAs based on the single-feedback and double-feedback are prevalent, and the latter is generally preferred in applications where higher fidelity is desired. Hence, PSRR is more important for the latter.

In this paper, we provide an analysis of the effect of the supply noise in the AC ground to the PSRR of open-loop PWM CDAs, and show that the PSRR, as expected, are strongly affected thereto. Analytical expressions are derived, depicting the related mechanisms. We further provide an analysis of the effect of the non-ideal AC ground and of the mismatch of the resistor pair and capacitor pair (of the two branches of the integrator) on the basis of a realistic fully-differential integrator model (vis-à-vis the simple fully-differential integrator model comprising two independent integrators). This analysis pertains to the PSRR of a 3-state BTL closed-loop CDA, and includes the derivation of analytical expressions. On the basis of said investigation, we derive the analytical equations for the PSRR of BTL CDAs based on the double-feedback topology. In general, these analyses and derived expressions are interesting as they offer valuable insights into the mechanisms of the practical circuit parameters affecting the PSRR, and possible trade-offs in the design of CDAs.

This paper is organized in the following manner. In Section 2, as a preamble to our ensuing analysis, the PSRR of three prevalent open-loop CDA structures, with various carrier generators, are reviewed and compared, and the effect of the supply noise in the AC ground analyzed. In Section 3, the analysis in Section 2 is applied to the ubiquitous 3-state BTL closed-loop PWM CDAs, taking into consideration the effect of non-ideal AC ground and mismatches of resistor pairs and capacitor pairs based on realistic fully-differential integrator model. The specific BTL CDAs of interest are those that based on the double-feedback topology where their PSRR is investigated and the associated analytical expressions derived. The important practical circuit parameters affecting the PSRR are thereafter discussed. In Section 4, the analytical derivations in Section 3 are verified on the basis of HSPICE simulations and practical measurements on discretely-realized CDAs. Finally, conclusions are drawn in Section 5.

2 Single-ended, 2-state BTL and 3-state BTL CDAs with various carrier generators

In CDAs, in part for the sake of hardware simplicity and power dissipation, the AC ground is usually realized by a voltage divider (instead of that derived from a bandgap reference) followed by a lowpass filter (whose cutoff frequency is <50Hz) [8, 9]. This simple means provides for the AC ground at −0.5V_{DD} regardless of the supply voltage - this is imperative for high dynamic range. In the following analysis, we denote the AC ground as V_{CM}:

\[
V_{CM} = \frac{V_{DD}}{2} + \frac{V_N}{A}
\]

where V_{DD} is the supply voltage, V_N is the supply noise component on the supply rail, and A is the attenuation of the supply noise in the AC ground, e.g., if A =20, the noise in the AC ground is 1/20 of that in the supply rail.

A is typically 20 and 100 at 217Hz and 1kHz respectively. These frequencies are of particular interest as they are the primary noise frequency for GSM and 4G LTE respectively. A large A at low frequency is difficult and expensive to achieve due to IC area and power dissipation constraints; in some cases, A is the limiting factor for the design of a CDA with very high PSRR (e.g. >100dB in closed loop PWM CDAs).

We will show later that depending on the architecture of the CDA and the design of the carrier generator, the supply noise in the AC ground may or may not degrade the PSRR of the open-loop CDAs. In some cases, its effect on PSRR is negligible, which translates to the relaxed design requirements for the AC ground, hence potentially smaller IC area (lower cost) and/or lower power dissipation. In other designs, on the other hand, the supply noise in the AC ground may significantly deteriorate the PSRR, and a ‘clean’ AC ground is required for high PSRR. Put simply, the AC ground should be designed with all due considerations. In view of this, we will now succinctly review the various carrier generators and in the perspective of open-loop CDAs.

Fig. 1 depicts the block diagram of three topologies of open-loop CDAs [10]: (a) single-ended, (b) 2-state BTL, and (c) 3-state (‘filterless’) BTL. All CDAs embody a carrier generator, PWM modulator, output stage, and a load (including a lowpass filter for (a) and (b), and a loudspeaker).

The three commonly used carrier generators are depicted in Fig. 2, where V_{C, I}, V_{C, II} and V_{C, III} are the carrier signals generated by Carrier Generators I, II and III, respectively. The operating mechanisms of these carrier generators are similar where by means of charging and discharging a capacitor, a triangular carrier waveform is generated as depicted in Fig. 3. By straight-forward analysis, the ideal maximum and minimum voltages of the carrier signal, V_{CH} and V_{CL}, can be ascertained and these are expressed in Fig. 2 at the bottom of the schematic of each carrier generator. Practically, due to the delay of the
comparator, \( I_D \), the practical maximum voltage of the carrier signal \( V_{CH_{Max}} \) is higher than the ideal \( V_{CH} \), and the practical minimum voltage \( V_{CL_{Min}} \) is lower than the ideal \( V_{CL} \). These are also depicted in Fig. 3.

\[
\begin{align*}
V_{CH}\_Max &= V_{CM} + I_{ref} R_C1 + \frac{t_D}{T_0} (4 I_{ref} R_C1) \\
V_{CL}\_Min &= V_{CM} - I_{ref} R_C1 - \frac{t_D}{T_0} (4 I_{ref} R_C1)
\end{align*}
\]

\[
T = T_0 + 4 \frac{t_D}{T_0} \quad T_0 = \frac{C_C}{T} 4 I_{ref} R_C1
\]

where \( T_0 \) is the ideal switching period.
Table 1: PSRR of the single-ended, 2-State BTL and 3-State BTL CDAs based on various carrier generators

<table>
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<tr>
<th>Carrier Generator</th>
<th>Single-Ended</th>
<th>2-State BTL</th>
<th>3-State BTL</th>
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<tr>
<td>Carrier Generator I</td>
<td>6</td>
<td>$-20 \log K$</td>
<td>$-20 \log K$</td>
</tr>
<tr>
<td>Carrier Generator II</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Carrier Generator III</td>
<td>$-20 \log \left( \frac{1}{A} - \frac{4}{T_0} \right) \left( 1 - \frac{4}{T_0} \right)$</td>
<td>$-20 \log \left( \frac{1}{A} - \frac{4}{T_0} \right) \left( 1 - \frac{4}{T_0} \right)$</td>
<td>$-20 \log \left( \frac{4}{T_0} \right)$</td>
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where $(V_{o1} - V_{o2})/V_{DD}$, $V_{o1}$ and $V_{o2}$ are the output offset voltages for the two branches.

Carrier Generator II

$$V_{CH,MaxII} = V_{CM} + V_{hyst} + \frac{4t_D}{T_0} V_{hyst}$$

$$V_{CL,MinII} = V_{CM} - V_{hyst} - \frac{4t_D}{T_0} V_{hyst}$$

$$T = T_0 + 4t_D$$

where $V_{hyst}$ is the hysteresis of the comparator.

Carrier Generator III

$$V_{CH,MaxIII} = \frac{V_{DD} + V_N}{G_{PWM}} + V_{CM} \frac{R_{C2}}{R_{C2} + R_{C3}} + \frac{t_D}{T_0} \frac{2V_{DD}}{G_{PWM}}$$

$$V_{CL,MinIII} = V_{CM} \frac{R_{C2}}{R_{C2} + R_{C3}} - \frac{t_D}{T_0} \frac{2V_{DD}}{G_{PWM}}$$

$$T = T_0 + \frac{V_N}{V_{DD}} T_0 + 4t_D$$

where $G_{PWM} = (R_{C2} + R_{C3})/R_{C3}$ is the gain of PWM modulator, i.e., $G_{PWM}$ is the ratio of the supply voltage to the carrier signal.

Based on the derived expressions alone and applying the method delineated in [6, 7], the PSRR of single-ended, 2-state BTL and 3-state BTL open-loop CDAs can be derived and these are tabulated in Table 1.

Using the derived expressions in Table 1 and on the basis of the following parameters: comparator delay $t_D=50\mu s$, switching period $T_0=4\mu s$ (hence the switching frequency, $1/T_0=250kHz$), normalized DC offset $K=0.01$ and $K=0.005$ for the 2-state BTL and 3-state BTL respectively, and $A=20$ (typical value at 217Hz), the PSRR of the different open-loop CDAs (Fig. 1) are obtained and tabulated in Table 2. These analytically obtained PSRR values in Table 2 are verified against HSPICE simulations. For completeness, note that the aforesaid parameters are typical in a practical design.

Table 2: Comparison of PSRR for open-loop CDAs (at 217Hz)

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<tr>
<td></td>
<td>6dB</td>
<td>40dB</td>
<td>46dB</td>
</tr>
<tr>
<td>Carr. Gen. III</td>
<td>22.8dB</td>
<td>1.4dB</td>
<td>72dB</td>
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From Tables 1 and 2, we make the following observations:

(i) As expected, because open-loop CDAs do not embody negative feedback, in general, they suffer from relatively poor PSRR.

(ii) Of the different open-loop CDAs, the 3-state BTL structure typically features the highest PSRR. This is as expected and is similarly observed in linear BTL amplifiers.

(iii) As expected, in part because of the design of the carrier generator, the noise in the AC ground has a different effect on PSRR. From eqns. (2) and (3) and from eqns. (4) and (5), it can be seen that for Carrier Generator I and II, the magnitude of that for the Carrier I and II (i.e., $V_{CH,Max}$, $V_{CL,Min}$) is independent of the supply noise; and $V_{CH,Max}$, $V_{CL,Min}$ and $V_{na}$ are AC coupled. The ‘on’ and ‘off’ periods of the output signals $(V_{SE}, V_{M1}, V_{M2}, V_{M3}, V_{M4}$ in Fig. 1) are hence independent of the noise in the AC ground and are ascertained from the intrinsic parameters, i.e., $I_{OC}$ and $R_{CL}$ for Carrier Generator I and $V_{hyst}$ for Carrier Generator II. This independence is because the noise in the AC ground does not have a feedforward path to the output of the open-loop CDAs. From eqns. (6) and (7), it can be seen that $V_{CH,Max}$ and $V_{CL,Min}$ of Carrier Generator III are dependent on a ratio (i.e., $R_{C2}/(R_{C2}+R_{C3})$) of $V_{CM}$, and that the carrier frequency, $1/T$, varies due to the supply noise. The output signal of CDAs embodying Carrier Generator III is hence affected by the AC ground and the effect of noise in the AC ground cannot be fully cancelled at the output of PWM modulator.

(iv) Of the various Carrier Generators, Carrier Generator III yields the best PSRR for the single-ended and 3-state BTL CDAs, whilst Carrier Generators I and II yields the best PSRR for 2-state BTL CDAs. This is because for single-ended and 3-state BTL CDAs with Carrier Generator III, the distortion components induced by the supply noise are in part cancelled by the distortion components in the carrier. It is worthwhile to note that although Carrier Generator III can improve the PSRR of the 3-state BTL CDA to a relatively high 72dB, it degrades the PSRR to unacceptable 1.4dB when it is embodied in the 2-state BTL CDA. Carrier Generator III is hence recommended for the single-ended and 3-state BTL CDAs but is inappropriate to the 2-state BTL CDA. Instead, Carrier Generators I and II are recommended for the 2-state BTL CDAs.

(v) For Carrier Generator III, it can be seen from Table 1 that a higher supply noise attenuation ($A$) at the AC ground results in higher PSRR - the PSRR is improved by 6.4dB (from 22.8dB to 29.2dB) when $A$ is increased from 20 to 100 for single-ended CDAs. From a practical perspective, because the lowpass filter is adopted for generating the AC ground, a larger attenuation effect appears at high frequencies, i.e., the PSRR at 1kHz may be higher than that at 217Hz due to larger $A$. 

4
3 PSRR of 3-state BTL closed-loop PWM CDAs

It was shown in Section 2 that 3-state BTL open-loop CDAs with Carrier Generator III generally feature a higher PSRR. For this reason, the 3-state BTL CDA is of specific interest herein. Further, because CDAs with higher fidelity are generally preferred (see Section 1 earlier), our analyses henceforth will be focused on the double-feedback topology where the integrators therein can be realized as either 1st-order or 2nd-order. For completeness, note that configurations other than the 3-state BTL CDA can be similarly analyzed. Consider now the 3-state double-feedback BTL CDA with 1st-order integrators in turn.

3.1 PSRR of the double-feedback BTL CDA with 1st-order integrators

In this section, the PSRR of the double-feedback BTL CDA with 1st-order integrators, denoted as PSRR_{1st}, will be first derived, followed by the interpretation of the derived mathematical expressions and the discussion about the frequency response of PSRR_{1st}.

3.1.1 Derivation of PSRR_{1st}

Fig. 4 depicts the schematic diagram of the 3-state double-feedback BTL closed-loop PWM CDA embodying 1st-order integrators. It comprises two 1st-order integrators, a 3-state BTL open-loop PWM CDA, two feedback paths and a load (loudspeaker). For reasons delineated earlier, Carrier Generator III is employed hereto.

To derive the PSRR, the block diagram of the double-feedback BTL PWM CDA is depicted in Fig. 5, where \( G_1 \) and \( G_2 \) are the transfer functions of the two branches from the input of the CDA to the input of the outer integrator (\( G_{int1} \)); \( G_3 \) and \( G_4 \) are the transfer functions from the output of the outer integrator to the input of the inner integrator (\( G_{int2} \)); and \( H_1, H_2, H_3 \) and \( H_4 \) are the feedback factors. These parameters are:

\[
G_1 = \frac{R_{fb1}}{R_1 + R_{fb1}} \tag{8}
\]
\[
H_1 = \frac{R_1}{R_1 + R_{fb1}} \tag{9}
\]

The expressions for \( G_2, G_3, G_4 \) and \( H_2, H_3, H_4 \) are respectively the same as eqns. (8) and (9) save for the subscripts.

\( G_{int1} \) and \( G_{int2} \) are respectively the transfer functions of the outer integrator and the inner integrator. To derive \( G_{int1} \) and \( G_{int2} \), Fig. 6 depicts the equivalent schematic of \( G_{int1} \) (\( G_{int2} \) can be similarly derived).

Fig. 6: The corresponding circuit of \( G_{int1} \) (from \( V_1^+ \) to \( V_2^+ \) and \( V_2^- \))

From Fig. 6, \( V_2^+ \) and \( V_2^- \) can be expressed [11] as:

\[
V_2^+ = \frac{\left(V_1^+\beta_{2a} - V_1^-\beta_{1a}\right) + 2V_{CM}\left(\frac{1}{a(f)}\right) + \beta_{2b}}{\beta_{1b} + \beta_{2b} + \frac{2}{a(f)}} \tag{10}
\]
\[
V_2^- = \frac{-\left(V_1^+\beta_{2a} - V_1^-\beta_{1a}\right) + 2V_{CM}\left(\frac{1}{a(f)}\right) + \beta_{1b}}{\beta_{1b} + \beta_{2b} + \frac{2}{a(f)}} \tag{11}
\]

\[
\beta_{1a} = \frac{1}{1 + sR_eC_{int1}} \tag{12}
\]
\[
\beta_{1b} = \frac{sR_eC_{int1}}{1 + sR_eC_{int1}} \tag{13}
\]

where \( a(f) \) is the frequency-dependent open-loop differential gain of the fully-differential op amp, \( R_e \) is the total resistance of \( R_1 \) and \( R_{fb1} \) in parallel.

Based on Fig. 6 and eqns. (10)-(13), \( G_{int1} \) can be derived as:

\[
G_{int1} = \frac{V_2^+ - V_2^-}{V_1^+ - V_1^-} \approx \frac{\beta_{1a} + \beta_{2a}}{\beta_{1b} + \beta_{2b} + \frac{2}{a(f)}} \tag{14}
\]
$G_{PWM}, N_{D1}$ and $N_{D2}$ model the 3-state BTL open-loop CDA (the shaded area in Fig.4). $G_{PWM}$ represents the gain of PWM stage, and it is a constant value. $N_{D1}$ and $N_{D2}$ are the supply noise components in the open-loop CDA induced by the noise on the carrier signal and the noise on the supply rail [6, 7]. $N_{D1}$ and $N_{D2}$ are:

$$N_{D1} = \frac{V_N}{A} \left( 1 - \frac{4\beta b}{T_0} \right) + \frac{2\beta b}{T_0} \frac{V_N}{V_{DD}} + \frac{4\beta b V_{DD}}{T_0} V_N$$  \hspace{0.5cm} (15a)

$$N_{D2} = \frac{V_N}{A} \left( 1 - \frac{4\beta b}{T_0} \right) + \frac{2\beta b}{T_0} \frac{V_N}{V_{DD}} + \frac{4\beta b V_{DD}}{T_0} V_N$$  \hspace{0.5cm} (15b)

Based on Fig. 5 and eqns. (8)-(15b), the PSRR of the double-feedback BTL CDA with 1st-order integrators can be derived as:

$$PSRR_{1st} = -20 \log(PSRR_{a,1st} + PSRR_{b,1st} + PSRR_{c,1st}) dB$$  \hspace{0.5cm} (16a)

$$PSRR_{a,1st} = \frac{1}{1 + LG} \left( \frac{2}{A} \right) * (D_{1,1st} + D_{2,1st})$$  \hspace{0.5cm} (16b)

$$PSRR_{b,1st} = \frac{1}{1 + LG} \left( \frac{N_{D1} + N_{D2}}{V_N} \right) * D_{3,1st}$$  \hspace{0.5cm} (16c)

$$PSRR_{c,1st} = \frac{1}{1 + LG} \left( \frac{N_{D1} - N_{D2}}{V_N} \right)$$  \hspace{0.5cm} (16d)

$$D_{1,1st} = G_{PWM} G_{int2} G_3 * \frac{\beta_{2b} - \beta_{1b}}{\beta_{1b} + \beta_{2b} + \frac{2}{a(f)}}$$  \hspace{0.5cm} (16e)

$$D_{2,1st} = G_{PWM} \left( \frac{\beta_{ab} - \beta_{3b}}{\beta_{3b} + \beta_{ab} + \frac{2}{a(f)}} \right)$$  \hspace{0.5cm} (16f)

$$D_{3,1st} = G_{PWM} \left( G_{int2} G_3 * \frac{H_2 \beta_{2a} - H_1 \beta_{1a}}{\beta_{1b} + \beta_{2b} + \frac{2}{a(f)}} + \frac{H_1 \beta_{4a} - H_2 \beta_{3a}}{\beta_{3b} + \beta_{4b} + \frac{2}{a(f)}} \right)$$  \hspace{0.5cm} (16g)

where $LG = G_{PWM} (G_{int1} G_{int2} G_3 H_1 + H_3 G_{int2})$ is the loop gain of the double-feedback CDA with 1st-order integrators.

$PSRR_{1st}$ will now be interpreted in the context of a practical CDA.

### 3.1.2 Interpretation of $PSRR_{1st}$ (eqns. (16a)-(16g))

It can be seen from eqns. (16a)-(16g) that $PSRR_{1st}$ for the double-feedback BTL PWM CDA with 1st-order integrators is mainly due to the following three mechanisms: 1) $PSRR_{a,1st}$ due to the non-ideal AC ground in the inner and outer integrators and the mismatches between passive components, 2) $PSRR_{b,1st}$ due to the supply noise component in each branch of the open-loop BTL PWM CDA and the mismatches in the integrators, and 3) $PSRR_{c,1st}$ due to the supply noise components in the open-loop BTL PWM CDA (specifically, the difference between the supply noise in the two branches of the open-loop BTL PWM CDA). These three mechanisms will now be delineated in turn and in the context of practical CDA design.

### Analysis on $PSRR_{a,1st}$

The non-ideal AC ground and the mismatches in the integrators contribute to the $PSRR_{a,1st}$. From eqn. (16b), it can be seen that $PSRR_{a,1st}$ consists of two items, the supply noise pertaining to $D_{1,1st}$ and pertaining to $D_{2,1st}$. The first item is the supply noise component due to the mismatch in the outer integrator and the second item is the supply noise component due to the mismatch in the inner integrator. A comparison between $D_{1,1st}$ (eqn. (16c)) and $D_{2,1st}$ (eqn. (16f)) shows that $D_{1,1st} \gg D_{2,1st}$. Practically, this means that the mismatch of the outer integrator is more critical than that of the inner integrator. Although this is somewhat unexpected but can be easily explained. This is because the $PSRR_{1st}$ due to the mismatch of the inner integrator can be attenuated by the outer integrator, hence the effect of the mismatch of the inner integrator is negligible compared to that of the outer integrator. In the perspective of practical layout, the matching of the inner integrator (including the associated passive components) can be compromised to reduce the IC area (hence reducing cost).

### Analysis on $PSRR_{b,1st}$

$PSRR_{b,1st}$ (eqn. (16c)) is due to the supply noise component induced in each branch of the open-loop BTL PWM CDA (i.e., $N_{D1}$ and $N_{D2}$). As delineated in Section 2, the noise in the open-loop BTL PWM CDA comes from the non-ideal AC ground in the carrier generator, the comparator delay and the offset voltages. This is also evident from eqns. (15a)-(15b). $PSRR_{b,1st}$ is also largely affected by the mismatches in the outer integrator and in the inner integrator, indicated by $D_{1,1st}$. Similar to $PSRR_{a,1st}$, the mismatch in the outer integrator has significantly larger effect on $PSRR_{b,1st}$, compared to the mismatch in the inner integrator.

### Analysis on $PSRR_{c,1st}$

$PSRR_{c,1st}$ (eqn. (16d)) represents the $PSRR_{1st}$ due to the DC offset between the two branches of the open-loop BTL PWM CDA (i.e., $(V_{DD}-V_{os})/V_{DD}$). It is worthwhile to note that $PSRR_{c,1st}$ is independent of the mismatches in the outer and inner integrators — this is unlike the cases of $PSRR_{a,1st}$ and $PSRR_{b,1st}$, where the $PSRR_{1st}$ depends on the mismatches in the integrators.

### 3.1.3 Frequency Response of $PSRR_{1st}$

In this section, the frequency response of $PSRR_{1st}$ will be delineated. As explained earlier, the effect of the mismatch in the inner integrator is negligible compared to that of the outer integrator, hence in the following analysis in this section, the effect of the mismatch in the inner integrator is ignored. By defining the mismatches between $R_1$ and $R_2$, $R_{fb1}$ and $R_{fb2}$, and $C_{int1}$ and $C_{int2}$ as 2% $b_1$ and 2% $c$, respectively, i.e., $R_1 = (1 - a\%) R_D$, $R_2 = (1 + a\%) R_D$, $R_{fb1} = (1 - b\%) R_{fb}$, $R_{fb2} = (1 + b\%) R_{fb}$, $C_{int1} = (1 - c\%) C_D$, $C_{int2} = (1 + c\%) C_D$ (where $R_D$, $R_{fb}$ and $C_D$ are the design values), $PSRR_{1st}$ in eqn. (16a) can be re-expressed as eqns. (17a)-(17d).
3.2 PSRR of the double-Feedback BTL CDA with 2nd-order integrators

Fig. 7 depicts the schematic of the 3-state double-feedback BTL closed-loop CDA comprising two 2nd-order integrators. The same analytical model for Fig. 4 depicted in Fig. 5, can be applied to Fig. 7; and the same analytical expression eqns. (16a)-(16g) can be derived for PSRR$_{2nd}$. The 2nd-order integrator parameters, $\beta_{1a}$, $\beta_{1b}$, for PSRR$_{2nd}$, are presented in eqns. (18) and (19), which are different from the 1st-order integrator parameters.

$$\beta_{1a} = \frac{1 + s(R_{g1}C_{int1} + R_{g1}C_{int2})}{1 + s(R_{e1}C_{int1} + R_{g1}C_{int1} + R_{g1}C_{int2}) + s^2R_{e1}R_{g1}C_{int1}C_{int2}}$$

$$\beta_{1b} = \frac{s^2R_{e1}R_{g1}C_{int1}C_{int2}}{1 + s(R_{e1}C_{int1} + R_{g1}C_{int1} + R_{g1}C_{int2}) + s^2R_{e1}R_{g1}C_{int1}C_{int2}}$$

![Fig. 7: Schematic of the double-feedback BTL CDA with 2nd-order integrators](image-url)

To delineate the frequency response of the PSRR$_{2nd}$, PSRR$_{2nd}$ can be re-derived by defining the matching of the passives as: $R_1 = (1 - a\%)R_D$, $R_2 = (1 + a\%)R_D$, $R_{fb1} = (1 - b\%)R_{fb}$, $R_{fb2} = (1 + b\%)R_{fb}$, $C_{int1} = (1 - c\%)C_D$, $C_{int3} = (1 + c\%)C_D$, $R_{g1} = (1 - d\%)R_g$, $R_{g2} = (1 + d\%)R_g$, $C_{int2} = (1 - e\%)C_D$, $C_{int4} = (1 + e\%)C_D$, where $R_D$, $R_{fb}$, $R_g$, $C_D$, and $C_D$ are the design values. PSRR$_{2nd}$ is re-expressed as eqns. (20a)-(20e).
\[ \text{PSRR}_{2nd} \approx 20 \log \left[ \frac{A}{2} \cdot G_{\text{int1}} H_1 \cdot \frac{(R_{FB} + 1) (s R_g C_{D2})}{p \cdot (1 + \alpha_p)} \right] \text{dB} \quad (20a) \]

where
\[ \alpha_p = \left| \frac{a\% - b\%}{R_{C1} r} \right| \text{p} \quad (20b) \]

\[ p = |b\% + c\%| + 2|a\% - b\%| \left(1 + \frac{C_{D2}}{C_{D1}} \right) \frac{R_g}{R_D} \quad (20c) \]

In the low frequency range \((\omega < \omega_p)\), eqn. (20a) can be simplified as:
\[ \text{PSRR}_{2nd, \text{low}} \approx 20 \log \left[ \frac{A}{2} \cdot \frac{R_{FB} + 1}{|a\% - b\%|} \right] \text{dB} \quad (20d) \]

In the high frequency range \((\omega > \omega_p)\), eqn. (20a) can be simplified as:
\[ \text{PSRR}_{2nd, \text{high}} \approx 20 \log \left[ \frac{A}{2} \cdot \frac{R_{FB} + 1}{s R_g C_{D1} \cdot p} \right] \text{dB} \quad (20e) \]

On the basis of eqns. (20a)-(20e), we make the following observations:

(i) Similar to the CDA with 1st-order integrators, the attenuation of the supply noise in the AC ground, \(A\), significantly affects the PSRR – to achieve a high PSRR, it is imperative that \(A\) is large.

(ii) From eqns. (20a)-(20e), we can see that the matching between \(R_1\) and \(R_2\) (\(a\%)\), \(R_{FB1}\) and \(R_{FB2}\) (\(b\%)\), and \(C_{\text{int1}}\) and \(C_{\text{int2}}\) (\(c\%)\) are more critical than that of \(C_{\text{int2}}\) and \(C_{\text{int3}}\) (\(d\%)\), and \(R_{C1}\) and \(R_{C2}\) (\(e\%)\). This is probably because \(R_{g1}\), \(R_{g2}\), \(C_{\text{int2}}\), and \(C_{\text{int3}}\) mainly affect the frequency response of the integrator at higher frequencies (sometimes higher than 20kHz, depending on the values of \(R_1\), \(R_2\), \(R_{FB1}\), \(R_{FB2}\), \(C_{\text{int1}}\) and \(C_{\text{int2}}\)). From a practical perspective, the layout design for \(R_{g1}\), \(R_{g2}\), \(C_{\text{int2}}\), and \(C_{\text{int3}}\) can be somewhat relaxed, hence reducing the IC area and cost.

(iii) Further, a comparison between eqns. (17c) and (20d) shows that in the low frequency range, the PSRR for the CDAs with 1st- and 2nd-order integrators are largely similar, where the PSRR is independent of the frequency and is determined by the resistor matching between \(R_1\) and \(R_2\) (\(a\%)\), and \(R_{FB1}\) and \(R_{FB2}\) (\(b\%)\).

(iv) It is interesting to notice that in the high frequency range \((\omega > \omega_p)\), the PSRR of the CDA with 2nd-order integrators decreases at a rate of ~20dB/decade, whilst its loop gain decreases at ~80dB/decade (Fig. 8). This counter-intuitive observation is because the effect of the loop gain can be in part cancelled by the mismatch components \((D_{1, 1st}, D_{2, 1st}\) and \(D_{1, 2nd}\)), as a result, PSRR\(_{2nd}\) only contain one dominant pole within the audio frequency range.

(v) Further to (iv), and from eqn. (20e), smaller mismatches (i.e., smaller \(a\%, b\%, c\%\)) and larger outer integrator gain \((G_{\text{int1}})\) result in better PSRR at high frequencies.

### 4 Verification and Results

In this section, the derived analytical expressions (i.e., eqns. (16a)-(16g), (17a)-(17d) and (20a)-(20e)) are verified by means of HSPICE simulations and on the basis of physical measurements on discretely-realized CDAs. The CDAs are realized using commercial-off-the-shelf (COTS) discrete components: TLV3502 as the comparator, THS4521ID as the differential op amp and MCP1404-E/SN as the driver. A supply \(V_{DD} = 5V\) and an 8Ω load are used. As per testing standards, for PSRR measurements, the input is grounded. The power supply with noise \((V_{DD} + V_n)\) is obtained from the Agilent Technologies N6705B DC Power Analyzer and measurements are obtained by means of the Rohde & Schwarz UPV Audio Analyzer. The measured bandwidth of the CDAs is from 20Hz to 20kHz.

The designed circuit parameters of the CDAs with the 1st- and 2nd-order integrators are tabulated in Table 3. For fair benchmarking, the parameters for the 1st- and 2nd-order integrators are selected such that the CDAs have the same carrier attenuation. It is worthwhile to note that in BTL CDAs, the dominant carrier component in the output is 2x of the carrier frequency. In this case, the carrier frequency is 250kHz, the dominant carrier component is 500kHz, and the carrier attenuation is ~14dB for both CDAs. The loop gains of the CDAs are depicted in Fig. 8 (where the DC gain of the differential op amp is 100dB and the bandwidth is 100Hz).

| Table 3: Circuit parameters of the 1st- and 2nd-order double-feedback BTL PWM CDAs |
|-----------------------------|-----------------------------|
|                            | 1st-order                  | 2nd-order                  |
| \(R_1, R_2, R_3, R_4\)     | 6kΩ                        | 6kΩ                        |
| \(R_{FB1}, R_{FB2}, R_{FB3}, R_{FB4}\) | 6kΩ                        | 6kΩ                        |
| \(R_{g1}, R_{g2}, R_{g3}, R_{g4}\) | -                          | 3kΩ                        |
| \(C_{\text{int1}}, C_{\text{int2}}, C_{\text{int3}}, C_{\text{int4}}\) | 0.5nF                      | 1nF                        |
| \(G_{PWM}\)                 | 2                          | 2                          |

![Fig. 8: Loop gains of the CDAs with 1st- and 2nd-order integrators](image-url)
Fig. 9: PSRR of the 1st- and 2nd-order CDA obtained analytically (eqns. (16a)-(16g)), and from HSPICE simulations and measurements.

Fig. 9 depicts the PSRR of the 1st- and 2nd-order CDAs against the supply noise frequency. In both designs, a%=0.1%, b%=0.2%, c%=1%, d%=0.15%, e%=1%, the same resistor and capacitor mismatches apply to the inner integrators, and A is equal to 2. On the basis of Fig. 9, we make the following observations:

(i) The analytical results largely agree with both the results obtained from simulations and from physical measurements, thereby verifying the analytical expressions derived herein.

(ii) In the low frequency range (<1.3kHz), the PSRR of both the 1st-order and 2nd-order CDAs is significantly higher (Fig. 8) and their loop gain decreases at ~20dB/decade. This is unexpected as the PSRR of the CDA with 2nd-order integrators is significantly higher and its hardware more complex. This counter-intuitive observation is because the PSRR of both CDAs in the low frequency range is determined by the component mismatches and the component mismatches of the two CDAs are similar.

(iii) In the high frequency range (1.3kHz-20kHz), the PSRR of both CDAs decreases at a rate of ~20dB/decade – although their loop gain decreases at ~40dB/decade for the CDA with 2nd-order integrators and ~80dB/decade for the CDA with 1st-order integrators. This is because, as explained earlier, the effect of loop gain is partially cancelled by the mismatch of the components (D1, D2, and D3). The PSRR decreases at ~20dB/decade.

(iv) Further to (iii), surprisingly, compared to the CDA with 2nd-order integrators, the CDA with 1st-order integrators features ~6dB higher PSRR in the high frequency range, albeit its lower loop gain. This can be explained by eqns. (17d) and (20e), where C2 in eqn. (17d) (designed value of Cint) in Fig. 4 is 0.5x C2 in eqn. (20e) (designed value of Cint) in Fig. 7) for the purpose of gaining the same carrier attenuation for both CDAs.

Fig. 10 depicts the PSRR of the CDA with 1st-order integrators for two different cases – Case 1: a%=b%=0.5%, and Case 2: a%=b%=1%. For both cases, c%=0.5%, A=2, and the same resistor and capacitor mismatches apply to the inner integrators. We note the following:

(i) The analytical results largely agree with simulations and experimental results, thereby verifying the analytical expressions derived herein.

(ii) For a%=b%, there is no corner frequency (ωp=0). This is analytically predicted by eqn. (17b).

(iii) A comparison of the PSRR for Cases 1 and 2 depicts that reducing the mismatches (a% and b%) by half would improve the PSRR by ~3dB. This insight can be obtained from eqn. (17a) and provides the CDA designer a means to trade-off some design parameters.

Fig. 11: PSRR of the CDA with 2nd-order integrators obtained analytically (eqns. (16a)-(16g)), and from HSPICE simulations and measurements.

Fig. 11 depicts the PSRR of the CDA with 2nd-order integrators, where the AC ground is at different noise levels, i.e., A=2 and A=8 (under the condition a%=b%=d%=0.2%, c%=e%=0.5%, and the same resistor and capacitor mismatches apply to the inner integrators). We note the following:

(i) As expected, the noise level on the reference, quantified by...
the noise attenuation term \( A \), has a significant effect on the overall PSRR where as expected, the higher the noise, the lower is the PSRR.

(iii) The comparison between the CDAs with \( A=2 \) and \( A=8 \) shows that a reduction of \( A \) by 4x (from \( A=8 \) to 2) would drastically reduce the PSRR by \(-12\) dB. Put simply, it is definitely worthwhile in CDA designs to embody a low-noise half-\( V_{DD} \) voltage reference to achieve high PSRR.

5 Conclusions

We have discussed the effect of the supply noise in the AC ground to the PSRR of the open-loop PWM CDAs and have ascertained the effect of the architecture of the CDA and of the carrier generator. We have also analytically investigated the PSRR of 3-state PWM BTL closed-loop PWM CDAs based on the double-feedback topology, taking into account the non-ideal AC ground and the mismatches between resistors and capacitors. Analytical expressions to model/predict the PSRR for said CDAs have been derived and subsequently verified by both simulations and hardware measurements. These derived analytical expressions have been shown to provide valuable insights to the design of CDAs.

References


