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<td>Author(s)</td>
<td>Tafti, Hossein Dehghani; Maswood, Ali Iftekhar; Konstantinou, Georgios; Pou, Josep; Townsend, Christopher D.</td>
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<tr>
<td>Date</td>
<td>2016</td>
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<tr>
<td>URL</td>
<td><a href="http://hdl.handle.net/10220/42091">http://hdl.handle.net/10220/42091</a></td>
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Low-Voltage Ride-Through Capability of Full-Row Connected Cascaded H-Bridge Converters

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Abstract—The full-row connection of dc-links provides an alternative configuration for the cascaded H-bridge (CHB) converter in large-scale grid-connected photovoltaic systems. In each stage, rather than individual strings per phase, all photovoltaic strings are connected to all phases through isolated dc/dc converters. The per-phase power imbalance issue and second-harmonic voltage of the dc-link capacitors are alleviated by using this topology. This paper studies the low-voltage ride-through (LVRT) capability of the full-row HB inverter in a grid-connected photovoltaic power plant (GCPVPP). A control algorithm is implemented for the isolated dc/dc converters which balances the capacitor voltages during voltage sags and reduces the second-harmonic voltage ripple of the dc-link capacitors. The performance of the grid-connected full-row HB inverter with LVRT capability is investigated on a 3-MVA single-row, three-level CHB topology for the GCPVPP connected to a 6.6 kV grid.

Index Terms—Photovoltaic systems, multilevel converter, full-row connected cascaded H-bridge (CHB) converter, low-voltage ride-through (LVRT), active/reactive power injection, unbalanced voltage sag.

I. INTRODUCTION

Among various renewable energy sources, photovoltaic (PV) plants are occupying an increasing share in the global power generation market. Because of the increasing tendency of installed grid-connected photovoltaic power plants (GCPVPPs), there is a requirement to use advanced converter topologies in combination with optimized control structures in order to maximize the power conversion efficiency and comply with new grid codes and standards \cite{1}--\cite{3}.

Among various multilevel converter topologies, cascaded H-bridge (CHB) converters have shown promise for large-scale GCPVPPs in several studies \cite{4}--\cite{7}, because of: a) higher power conversion efficiency due to the low switching frequency of each individual bridge, b) elimination of line-frequency bulky transformer, and c) utilization of multiple dc-links with capability of the implementation of multiple instances of maximum power point tracking algorithms. However, the conventional CHB converters suffer from two main issues:

- They require very large dc-link capacitors due to the existence of the second-harmonic voltage ripple. Each phase of the converter operates as a single-phase converter which produces double fundamental frequency in the dc-link voltage.
- Interphase and interbridge imbalances due to unequal amounts of power, that may be generated from the PV strings connected to each individual H-bridge. As a result, the injected currents to the grid, during normal grid condition, become unbalanced. Several studies have been reported on the power balancing with zero-sequence voltage injection to the phases \cite{8}--\cite{10}, however, this method requires over-rating of semiconductor devices.

A potential solution to the above issues is the connection of the individual PV strings to a common dc-link. A topology with cascaded connection of ac/ac converters has been introduced in \cite{11}, where all phases are magnetically coupled such that capacitors appear common to all phases. Although this topology eliminates second-harmonic ripples of the dc-link voltage, it requires a complicated magnetic design and high number of active components, which reduces the power conversion efficiency and increases the converter cost.

A full-row connected cascaded H-bridge topology, as shown in Fig. 1, is studied in \cite{1}. Although, the simplest configuration of this topology is presented in this figure, it can be cascaded in order to produce higher number of voltage levels. In this topology, the H-bridges of three phases are supplied with a common connection of all PV strings, which eliminates the per-phase power imbalance issue. The isolated dc/dc converters are utilized in this topology in order to isolate the H-bridges.
Switching Signals

The detailed implementation of the controller of the full-row connected CHB during grid normal condition with the injection of active power and elimination of second-harmonic voltage ripples is presented in [1]. However, a further investigation on the low-voltage ride-through (LVRT) capability of the proposed topology is required [12]. Grid codes regulate reactive power injection to the grid during voltage sags in order to enhance the voltage of the point of common coupling (PCC) during these events [13]. For voltage sags with amplitude smaller than 0.5 pu, the injected reactive current \( I_q \) is equal to the nominal current of the inverter. Therefore, no active current can be injected to the grid. During voltage sags with amplitude between 0.5 pu and 0.9 pu (referred as Sag I in this paper), \( I_q \) is smaller than the nominal current of the inverter. Therefore, the inverter is able to simultaneously inject active and reactive powers to the grid.

The purpose of this paper is to investigate the LVRT capability of the grid-connected full-row connected HB inverter (shown in Fig. 1) during Sag I. The implemented control algorithm for the dc/dc converters reduces the second-harmonic dc-link voltage ripples and balances the capacitor voltages during voltage sags. The performance of the full-row connected HB converter is investigated on a simulated 3-MVA GCPVPP during both normal and voltage sag conditions. The impact of the dc/dc stage in the balancing of the capacitor voltages and reduction of the second order harmonic is also demonstrated.

II. CONTROLLER ALGORITHM FOR FULL-ROW CONNECTED HB INVERTER DURING VOLTAGE SAGS

Two controllers, one for dc/dc conversion stage and one for the grid-connected HB inverter, are required for the operation of the GCPVPP. Each of these controllers require separate control strategies, which are specific for the grid operating condition (i.e. during normal operation or during network disturbances such as voltage sags).

The control schematic of the grid-connected H-bridge converter is presented in Fig. 2(a). Firstly, the amount of d-axis current reference \( I^*_d \) is calculated by regulating the average capacitor voltages \( \bar{v}_{dc} \) to its reference value \( v^*_{dc} \). \( \bar{v}_{dc} \) is calculated as \( (v_{dc-a} + v_{dc-b} + v_{dc-c})/3 \). Subsequently, the average active power reference is calculated by multiplying \( I^*_d \) and \( |v^*_{pcc}| \). The average reactive power reference \( Q^* \) is computed through grid codes. Based on the active/reactive power references and the instantaneous PCC voltages, the current reference can be calculated using the instantaneous power theory [14]. Proportional resonant (PR) current controllers with anti-windup are implemented in \( \alpha \beta \) frame in order to ensure the zero sequence voltage during unbalanced voltage sags [15]. Finally, the computed voltage references are fed into the phase-shifted pulse-width-modulation algorithm for generating CHB switching signals. An individual capacitor voltage balancing is also implemented based on [6] to ensure the operation of all capacitors within their nominal range.

The control algorithm of the isolated dc/dc converters, depicted in Fig. 2(b), consists of three control loops. The first loop is responsible for the extraction of maximum power from the PV string during grid normal operation or required power reference during voltage sags.

The second loop is implemented for the reduction of the second-harmonic voltage ripple and balancing capacitor voltages during both grid normal and voltage sag conditions. This is achieved by comparing the average voltage of capacitors of all phases \( \bar{v}_{dc} \) with the instantaneous dc-link voltage of that phase \( v_{dc-x} \), which \( x \) is referred to phase a, b or c).

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**TABLE I**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
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<tr>
<td>Three phase nominal power</td>
<td>( P_{nom} )</td>
<td>3 MW</td>
</tr>
<tr>
<td>Grid voltage</td>
<td>( v_{pcc} )</td>
<td>6.6 kV rms</td>
</tr>
<tr>
<td>Inductor filter</td>
<td>( L_f )</td>
<td>14 mF</td>
</tr>
<tr>
<td>dc-link voltage</td>
<td>( v_{dc} )</td>
<td>6.6 kV</td>
</tr>
<tr>
<td>dc-link capacitor</td>
<td>( C )</td>
<td>3 mF</td>
</tr>
<tr>
<td>Carrier frequency</td>
<td>( f_{car} )</td>
<td>600 Hz</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>( f_{sw} )</td>
<td>3600 Hz</td>
</tr>
<tr>
<td>PV Filter capacitance</td>
<td>( C_{p-f} )</td>
<td>3 mF</td>
</tr>
<tr>
<td>dc/dc converter turns ratio</td>
<td></td>
<td>1 (PV) : 10 (CHB)</td>
</tr>
<tr>
<td>dc/dc converter switching frequency</td>
<td>( f_{sw-dcdc} )</td>
<td>10 kHz</td>
</tr>
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</table>
Fig. 3. Operation of full-row connected HB inverter during grid Normal condition: (a) Three-phase grid voltages ($v_{pcc}$), (b) inverter three-phase currents ($i_{abc}$), (c) injected active/reactive power ($p/q$), (d) dc-link capacitor voltages ($v_{dc}$) and (e) PV string voltage ($v_{pv}$).

as depicted in Fig. 2(b). This control loop is implemented using a proportional controller with a proportional gain of $K_1$. If $v_{dc-x}$ is larger than $v_{dc}$, the duty cycle ($D$) of the dc/dc converter is reduced in order to decrease the injected power to that capacitor and reduce its voltage. On the other hand, if $v_{dc-x}$ is smaller than $v_{dc}$, $D$ is increased, which as a consequence, larger power in injected from the PV string to the capacitor to increase its voltage. This results in the reduction of the capacitor voltage ripples which can eventually lead to a decrease in the size of the CHB dc-link capacitors. Finally, the third loop is responsible for sharing equal power between capacitors of different phases which balances the injected power to all phases.

III. EVALUATION RESULTS

The GCPVPP with CHB inverter (Fig. 1) is modeled using Matlab/Simulink and PLECS toolbox. The parameters of the simulated full-row connected HB converter are listed in Table I. The performance of the proposed controller is evaluated during grid normal operation and results are shown in Fig. 3. According to the three-phase grid voltages and the injected currents, shown in Fig. 3(a) and (b), it can be observed that the inverter operates with unity power factor during normal condition, and consequently the injected reactive power to the grid is zero. Due to the implementation of the dc/dc converter controller, the dc-link capacitor voltage ripple is smaller than 50 V ($0.7\%$ of the capacitor average voltage), which is approximately four times smaller compared to the voltage ripple with deactivation of the second control loop. The controller transfers the voltage oscillation from dc-link capacitors to the PV string and an oscillation of approximately 150 V exists in the PV string voltage (Fig. 3(e)). Although, the extracted power from PV string is reduced due to its voltage ripple, the size of dc-link capacitors can be reduced.

The performance of the controller during a single phase
importance of the voltage balancing controller in the balancing with three control loops is implemented in order to balance the plant (GCPVPP). A control algorithm for the dc/dc converters full-row connection of a grid-connected photovoltaic power. The effectiveness of the voltage balancing controller is presented in Fig. 5. In this case study, the voltage balancing controller (second control loop of the dc/dc converter controller) is deactivated during the voltage sag. Before the voltage sag, the capacitors are balanced. However, the capacitor voltages are deviating from each other during Sag I. The voltage sag is cleared at $t = 0.18\, s$ and the voltage balancing controller is activated at this moment. Accordingly, capacitor voltages become balanced in less than $0.03\, s$. This case study proves the importance of the voltage balancing controller in the balancing of capacitor voltages during voltage sags. The first control loop is responsible to extract the maximum power the PV string, while the second-harmonic voltage ripple of the dc-link capacitors is reduced due to the implementation of the second control loop. Finally, the third loop balances the injected power to all phases by sharing equal power between capacitors of different phases. The performance of the HB inverter with full-row connection is evaluated on a simulated 3-MVA GCPVPP during voltage sags and results show the LVRT capability of this topology which makes it interesting for large-scale GCPVPPs.

### REFERENCES


