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Comparison of Bipolar Sub-Modules for the Alternate Arm Converter

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Abstract

The alternate arm converter (AAC) is an emerging dc-fault tolerant multilevel converter topology aimed at high-power and HVDC applications. This paper addresses the suitability of modular multilevel converter (MMC) submodules (SMs) for the AAC. Bipolar SMs are applicable for AACS depending on the complexity, controllability, device count, and operating losses. However, only the full-bridge SM (FB-SM) and the cross-connected SM (CC-SM) are fully controllable and functional in AACS. Based on the loss analysis of FB-SM- and CC-SM-based AAC with different device configurations, it is shown that: i) complex SM structures do not benefit the operation of AAC, and ii) the FB-SM provides the most functional advantages in an AAC.

Keywords: Alternate arm converter, cross-connected submodules, losses, identical semiconductor devices.
1. Introduction

Research on dc-fault tolerant multilevel converters has gained noticeable attention over recent years [1, 2, 3], and the alternate arm converter (AAC) [4], a hybrid topology of the two-level converter and the modular multilevel converter (MMC) is such an emerging multilevel converter topology. Since its introduction [5], the modular multilevel converter (MMC) has become the state-of-the-art in high-voltage direct current (HVDC) systems and medium voltage applications [6]. Apart from the inherited features of multilevel voltage source converters (VSCs), additional features of the MMC and its hybrid topologies in high-power applications include: i) modularity, ii) scalability, iii) ability to handle wide power and voltage ratings, iv) relative simplicity of submodule (SM) capacitor voltage balancing, and v) redundant configuration [7]. Owing to the large number of voltage levels, MMCs provide near sinusoidal output voltages and currents with low harmonic distortion.

The MMC topology shown in Fig. 1(a) consists of \( N \) series connected SMs per arm, and two inductors (\( L \)) connecting the two arms to form one phase-leg. SM capacitor voltage balancing, circulating current control, and arm energy balancing are the key control requirements of MMCs. A variety of modulation methods [2, 8, 9] can be applied to MMC-based topologies, and the staircase modulation techniques are the most efficient over the alternatives as the number of voltage levels increases [10]. Different strategies can also be applied for SM capacitor voltage balancing [11, 12] where the most commonly used is based on a ‘sort and select’ algorithm. Two major circulating current control techniques based on stationary reference frame with proportional-resonant (PR) controllers [13, 14], and double-frequency rotating reference frame with decoupled current control [15] are applicable to MMCs.

MMC SMs can be divided in two categories based on the capability to generate negative voltage levels in the output. Unipolar SMs generate only positive voltage levels, and bipolar SMs generate both positive and negative voltage levels [16]. One of the major drawbacks of MMCs based on unipolar SMs [17] is the lack of dc-fault handling capability. The use of bipolar SMs in MMCs offers voltage blocking capability during dc-faults. A variety of SM configurations [16, 17] are available for MMCs which can offer additional functionalities and dc-fault tolerant capability at the cost of increased semiconductor device count and higher losses.

The AAC [4], shown in Fig. 1(b), consists of bipolar and fully controllable SMs which provide the blocking voltage during dc-faults [18] and has been introduced in order to address the dc-fault handling issues of the MMC. The structure of the AAC maintains traits of the MMC structure with the addition of director switches (DSs) in the upper and lower arms as shown in Fig. 1(b). Owing to the use of bipolar SMs, the AAC can generate peak ac voltages above the dc-link voltage up to a maximum ac peak voltage of \( 4/\pi \) times the dc-link voltage, (as it will be demonstrated in Section 2). This is called “sweet-spot” [4] operation, and is defined as the operating point where the net energy exchange within the arms is equal to zero. Non-sweet-spot operation leads to non-zero net energy exchange within the AAC arms, causing deviations in the steady-state SM capacitor voltages.

The arm energy regulation and the upper/lower arm energy balancing can be achieved using overlap period based methods [19, 20] or current injection methods [21, 22]. Arm energy balancing of the AAC at non-sweet-spot operation is challenging due to the al-
ternate operation of the DSs. The arms of an AAC phase-leg alternatively conduct the
total phase current during each half of the voltage cycle. Hence, the energy has to be
exchanged between the two arms by overlapping the operation of two DSs [19] or by
injecting a zero-sequence current. Zero-sequence voltage injection can also be utilized to
change the span of overlap period and ac voltage push-up period [21]. Additionally, use
of an star-connected transformer at the ac-side of the AAC with a neutral connection
to the dc-side allows the zero-sequence current to transfer energy between AAC arms
and the dc-side [22]. The non-zero net energy exchange at non-sweet-spot operation and
the zero-current switching of the director switches should also be considered in AAC SM
capacitor sizing [23] and arm inductor sizing [24].

The similar structural characteristics between MMCs and AACs in terms of the topol-
ogy and SM capacitor voltage sorting and balancing [18, 12], make it feasible to apply
MMC SMs to the AAC depending on their: i) suitability, ii) full controllability, iii) com-
plexity, iv) ease of capacitor voltage balancing, and v) component count [16, 17]. Al-
though there are several bipolar SM configurations in addition to the FB-SM, only the
cross-connected SM (CC-SM) is suitable for the AAC, as it offers the fully controllable
bipolar operation with full voltage blocking capability [16].

Existing literature evaluates the fitness of different SM configurations for MMCs,
based on the circuit complexity, capacitor voltage balancing capability, and SM losses
[16, 17, 25]. A CC-SM-based generalized SM structure is proposed for AACs in [26]
using nonidentical switching devices, and the device count is reduced compared to the
FB-SM-based AAC. Although the CC-SM with nonidentical switching devices reduces
the device count, it becomes less modular in device-level, which adds to the overall
complexity. Moreover, CC-SMs with different switching device configurations leads to
significant differences in AAC losses. Although bipolar SMs are proposed as applicable
to AACs, the suitability of those SMs for the AAC is yet to be investigated subject to
complexity, voltage balancing, and operating losses. The aim of this paper is to provide

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Figure 1: MMC and AAC circuit configurations; (a) MMC phase-leg and (b) AAC phase-leg.
a comparison and loss analysis of bipolar SMs for the AAC, investigating the relative merits of complex bipolar SM structures for AACS.

The paper is organized in the following manner. Section 2 provides an overview of the basic operating principles of the AAC, and a description of applicable SMs is presented in Section 3. Simulation results of FB-SM- and CC-SM-based AACS are demonstrated in Section 4. Section 5 offers an evaluation of the losses in CC-SM and FB-SM-based AACS, demonstrating impact of identical and nonidentical switching devices on the losses of CC-SMs. Section 6 summarizes the conclusions of the work.

2. AAC Operating Principles

A. Structure

The single-phase AAC topology is shown in Fig. 1(b). Each phase-leg of the AAC consists of two arms with N series-connected SMs, one inductor (L), and a director switch (DS) per arm. A single dc-source is utilized on the dc-side of the three-phase AAC topology. The SM, which is the basic building block of the AAC, is based on bipolar configurations [16, 17].

The AAC topology has a similar structure to the MMC as shown in Fig. 1 with the exception of the DSs (DS_u and DS_l). The DSs operate alternatively during the positive and negative half-cycles of the reference waveform (v_{am}) of the output voltage:

\[ v_{am} = m_a \cos(\omega t), \]  

respectively. The duty-ratios of the upper and lower arms (d_u and d_l) are then defined as:

\[ d_u = 1 - v_{am}, \]  

\[ d_l = 1 + v_{am}, \]

where the duty-ratios are limited to |d_u,l| ≤ 1, and define the number of SMs (n_u and n_l) of the arm to be inserted. When the AAC operates above the dc-link voltage (m_a > 1), the duty-ratios become negative for a small period. The negative sign of the duty ratios represents the insertion of SMs in the opposite direction.

Owing to the alternate operation of the two arms of an AAC phase-leg, only one arm carries the total output current,

\[ i_a = \hat{I}_a \cos(\omega t + \phi). \]

There is no continuous current component circulating within the AAC phase-leg, limiting the energy exchange between the upper and lower arms of the AAC.

B. Current Control and Arm Energy Balancing

An overlap period can be defined in order to exchange the energy between upper and lower arms. During the overlap period both DS_u and DS_l are closed, and a circulating current i_{circ} flows within the phase-leg in addition to the arm currents in upper and lower arms. The overlap period can be evenly distributed around the zero-crossing points of v_{am}, by varying the operation of the DSs accordingly. The operation during the overlap
period mimics the MMC operation [22]. Thus, the upper and lower arm currents ($i_u$ and $i_l$) during the overlap period can be defined as:

\[
    i_u = \frac{i_a}{2} + i_{\text{circ}}, \quad \text{and}
\]

\[
    i_l = \frac{i_a}{2} - i_{\text{circ}}.
\]  

Unlike the MMC, flexibility of arm energy balancing is limited by the length of this overlap period. The energy balancing flexibility can be increased by utilizing a longer overlap period at which, more energy can be exchanged between the upper and lower arms. SM capacitor energy can be regulated by appropriately controlling the circulating current during the overlap period [19]. However, longer overlap periods can lead to output voltage distortions due to the limited number of SMs per arm [20]. In order to avoid such distortions, SM voltages in the upper and lower arms should be sufficient to synthesize the output voltage well-below and above zero, respectively. Moreover, the availability of additional control voltages in the upper and lower arms is necessary in order to control the circulating current and for energy balancing. Therefore, the overlap period based energy balancing capability of the AAC fully depends on the number of SMs ($N$) in each of the arms.

In AACs, $N$ is chosen to provide dc-fault tolerant capability by blocking the ac peak voltage, and calculated based on the ac-side peak voltage $\hat{V}_a$ and the nominal voltage of the SM capacitors $V_C$ as:

\[
    N = \left\lceil \frac{\hat{V}_a}{V_C} \right\rceil.
\]  

Based on the selection of $N$, the maximum achievable overlap period which avoids output voltage distortions is limited by the redundant voltage ($V_r$),

\[
    V_r = NV_C - \frac{V_{dc}}{2}.
\]  

This redundant voltage is an important parameter and in order to provide higher flexibility to overlap period based energy control, redundant SMs can purposely be included in the arms [7].

The net energy exchanged by the SMs of one arm within each half-cycle should be kept at zero, in order to maintain the SM capacitor voltages at the reference. Assuming balanced operation of the AAC with SM voltage balancing algorithm and an ideal converter, the net energy absorbed by all the SMs of an arm can be calculated using the difference between dc-link energy and the ac-side energy exchanged by the arm current. Defining the converter output voltage as:

\[
    v_a = v_{am} \frac{V_{dc}}{2} = m_a \frac{V_{dc}}{2} \cos(\omega t),
\]  

and considering that the arm current and the output phase current are similar within a half-cycle based on the assumption of a negligible overlap period, the exchanged energy in the dc-link $E_{dc}$ and the ac-side $E_{ac}$ can be determined using (4) and (9) as:

\[
    E_{dc} = \int_{-\frac{T}{4}}^{\frac{T}{4}} \frac{V_{dc} I_a}{2} \cos(\omega t + \phi) \, dt,
\]  

\[
    E_{ac} = \int_{-\frac{T}{4}}^{\frac{T}{4}} \frac{V_{dc} I_a}{2} \cos(\omega t + \phi) \, dt,
\]
\[ E_{ac} = \int_{-\frac{T}{4}}^{\frac{T}{4}} \frac{m_a V_{dc} I_a}{2} \cos(\omega t) \cos(\omega t + \phi) \, dt, \]  

(11)

where \( T \) and \( \phi \) are the fundamental period and the phase angle, respectively. Hence, the net energy absorbed by the arm capacitors can be determined from (10) and (11) as:

\[ E_{dc} = E_{ac} = \frac{\pi V_{dc} I_a \cos \phi}{4\omega} \left( \frac{4}{\pi} - m_a \right). \]  

(12)

Eq. (12) shows that, the net energy exchanged by SM capacitors becomes zero only at \( m_a = 4/\pi \). Hence, the natural energy balance of AAC arms exists only at one operating point \((m_a = 4/\pi)\). This is called the “sweet-spot” [4], and the maximum ac peak voltage is produced at this operating point. When the operating point moves away \((m_a < 4/\pi)\) from the sweet-spot, the net exchanged energy of the SMs increases resulting in voltage imbalance. Therefore, energy balancing control becomes relatively difficult due to the high excessive SM energy.

The negative voltage polarity of the bipolar SMs is important only for operating points where \( m_a \geq 1 \). The SMs are negatively inserted around the peak of the reference voltage waveform, and the excessive energy in the SMs is reduced by allowing the arm current to discharge the SM capacitors outside the overlap period. However, as the operating point moves away from the sweet-spot, the time which the SM capacitors are negatively inserted is reduced. Hence, the discharging time of the SM capacitors is also reduced, while increasing the effort of SM energy control based on overlap current control. When the operating point reduces below the unity modulation index, the discharge time of the SM capacitors outside the overlap period becomes zero, and SM energy has to be fully controlled during the overlap period. This involves large changes in the arm currents with high gradients due to the short overlap time, that may lead to output current and voltage distortions.

C. SM Voltage Balancing

AAC capacitor voltage balancing can be achieved by adopting methods used in MMCs. Phase-shifted carrier based pulse-width-modulation (PS-PWM) offers voltage balancing among the SMs without an additional sorting stage [1]. However, PS-PWM becomes complex as the number of SMs increases. Most commonly used SM voltage balancing methods are based on “sort and select” algorithms, which involve sorting of the SM capacitor voltages and selection based on the arm current direction [18].

3. SM Configurations for AACs

AACs require SMs which can generate both positive and negative voltage levels, in order to push the output voltage above the dc-link voltage during normal operation. Based on [16, 17], the only suitable SMs include FB-SM and CC-SM. The characteristics of the two SM types, and the adoption of the MMC restricted voltages balancing algorithm [12] to the AAC is described here.
A. FB-SM

The FB-SM, shown in Fig. 2(a), has a simple structure including one capacitor shared by two side-by-side legs. One leg operates as a half-bridge SM (HB-SM) while the other leg defines the output voltage polarity by operating in a single state. The single capacitor configuration of the FB-SM allows the use of HB-SM sorting algorithms for capacitor voltage balancing of the FB-SM-based AAC.

Considering the FB-SM as a combination of one HB-SM \((S_1 \text{ and } S_2(=\bar{S}_1))\), and two single state switching devices \((S_3 \text{ and } S_4(=\bar{S}_3))\), restricted voltage balancing algorithm of
the HB-SMs can be applied with slight modifications to the inputs and output. Fig. 3(a) shows the modified restricted voltage balancing algorithm adopted to an upper arm of the FB-SM-based AAC phase-leg, where \( \Delta K \) is the offset constant of the SM capacitor voltages. The polarity of the arm current input \( (i_u) \) is defined based on the operation of single state devices which is reflected in Fig. 3(a) by the polarity of the duty-ratio \( (d_u) \).

The switching signals \( (S_{1uj}) \) provided to the legs operating as HB-SMs are obtained by negating \( S_j \) based on the polarity of \( d_u \), and the signals \( (S_{3uj}) \) to single state switches are directly determined by the polarity of \( d_u \). Similarly, the voltage balancing of the lower arm can be achieved by considering the \( n_u \rightarrow n_l, v_{Cuj} \rightarrow v_{Clj}, \) and \( i_u \rightarrow -i_l \), referring to Fig. 1(b).

B. CC-SM

The CC-SM structure, shown in Fig. 2(b), consists of two HB-SMs cross-connected on the dc-side using single state switches \( (S_3 \) and \( S_4 (= S_3) \)). Due to the cross-connection, the CC-SM is capable of generating a symmetrical multilevel bipolar voltage waveform at the output. The two pair of switches \( S_1, S_2 (= S_1) \) and \( S_5, S_6 (= S_5) \) operate as two HB-SMs, where the single state switches operate based on the output voltage polarity of the SM.

The restricted voltage balancing algorithm of the HB-SMs can be applied to the CC-SM-based AAC (Fig. 3(b)). Similarly to FB-SM, the polarity of the arm current input is defined based on the polarity of the duty-ratio \( (d_u) \). The switching signals \( (S_{1uj} \) and \( S_{3uj}) \) to the legs operating as HB-SMs are determined based on \( S_j \) and the polarity of \( d_u \), whereas the switching signals \( (S_{3uj}) \) to single state switches are directly based on \( d_u \). The restricted voltage balancing of the lower arm can be achieved by considering \( n_u \rightarrow n_l, v_{Cuj} \rightarrow v_{Clj}, \) and \( i_u \rightarrow -i_l \), referring to Fig. 1(b).

The maximum voltage applied across each single state switch is the total voltage of the two capacitors \( (C_1 \) and \( C_2) \). Hence, the voltage rating of the single state switches should be at least twice the voltage rating of the other switches \( S_1, S_2, S_5, \) and \( S_6 \) \( (V_C) \), in order to withstand a voltage of \( 2V_C \). The voltage rating of the cross-connection can be satisfied using different devices; the device count of the CC-SM depends on those device ratings. Each cross-connection can be made either with multiple devices which have a lower voltage rating (i.e two devices with a rating of \( V_C \) for a CC-SM with identical devices), or with a single device which has a voltage rating of \( 2V_C \) [26]. The former ensures device-level modularity of the CC-SM but with higher device count. The latter leads to an asymmetric CC-SM structure with a relatively low device count but with a less-modular structure.

The semiconductor device losses depend on both the device count and device ratings. Although a higher device count of the modular CC-SM structure can lead to increased losses as the number of voltage levels increase, a less modular structure with higher device ratings may result in comparatively higher losses despite the low device count. Moreover, the asymmetric device structure adds to the overall complexity of the SM, especially with a large number of voltage levels. Thus, there is a trade-off between the CC-SM with identical devices, and the asymmetric CC-SM structure. Therefore, losses of the different CC-SM structures based on the device count and device ratings will be analyzed in the following section, and compared against the FB-SM.
4. Simulation Results

In order to evaluate the operational losses in FB-SM-based and CC-SM-based AACS, three-phase grid-connected AACS (17-level) are simulated in MATLAB-Simulink and PLECS. Fig. 4 shows the schematic diagram of the simulation. Table 1 provides the simulation parameters. The FB-SM-based AAC and the CC-SM-based AAC have $N = 8$ FB-SMs per arm and $N = 4$ CC-SMs per arm, respectively. The 17-level AAC simulation models are developed by adopting the CIGRE benchmark MMC test system [27] for $N = 8$ and $N = 4$ SMs with a voltage rating of 35 kV per SM capacitor. SM capacitance is determined by limiting the stored energy of the AAC to one third of the stored energy of an MMC with similar power ratings based on [23].

Table 1: Simulation Parameters of the Grid-Connected AAC

<table>
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<th>Parameter</th>
<th>Value</th>
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<tr>
<td>Rated Power</td>
<td>400 MVA</td>
</tr>
<tr>
<td>Number of SMs/臂 (N)</td>
<td>8 (FB-SM), 4 (CC-SM)</td>
</tr>
<tr>
<td>DC-Link Voltage ($V_{dc}$)</td>
<td>400 ($\pm$200) kV</td>
</tr>
<tr>
<td>SM Capacitance ($C$)</td>
<td>150 $\mu$F</td>
</tr>
<tr>
<td>SM Capacitor Voltage ($V_C$)</td>
<td>35 kV</td>
</tr>
<tr>
<td>Arm Inductance ($L$)</td>
<td>0.019 pu</td>
</tr>
<tr>
<td>Transformer Leakage Inductance</td>
<td>0.045 pu</td>
</tr>
<tr>
<td>Transformer Resistance</td>
<td>0.0015 pu</td>
</tr>
<tr>
<td>Transformer Ratio</td>
<td>1.218</td>
</tr>
<tr>
<td>Grid Voltage (for $m_a = 4/\pi$)</td>
<td>380 kV</td>
</tr>
<tr>
<td>Carrier frequency ($f_c$)</td>
<td>7.2 kHz</td>
</tr>
<tr>
<td>System frequency ($f$)</td>
<td>50 Hz</td>
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Operation at different power factors is achieved while maintaining a fixed current equal to the rated current at the sweet-spot. When the AAC operates away from the sweet-spot, overlap period control \cite{13} and circulating current control \cite{24} mechanisms must be applied, in order to maintain the SM capacitor voltages at the rated voltage. When the converter operates near the sweet-spot, no major influence due to the absence of these controllers is expected.

Fig. 5(a) and (b) show the steady-state output voltage and current for the near sweet-spot operation of the FB-SM-based AAC. The output voltages are 17-level waveforms. The steady-state upper and lower arm SM capacitor voltages of phase $a$ are shown in Fig. 5(c). Fig. 5(d) provides the upper and lower arm currents of the phase-leg $a$ of FB-SM-based AAC. The upper and lower arm SM capacitor voltage are balanced demonstrating the successful operation of the restricted voltage balancing algorithm \cite{12} for FB-SM-based AACs (Fig. 5(a)). SM capacitor voltages are maintained at the rated voltage (35 kV) by employing an overlap period based circulating current control.

Near sweet-spot steady-state operation of the CC-SM-based AAC is similar to the near sweet-spot operation of FB-SM-based AAC shown in Fig. 5. Subsequently, Fig. 6
shows the steady-state SM capacitor voltages and arm currents of the phase $a$ of CC-SM-based AAC, and output voltages and currents. The upper and lower arm SM capacitor voltages (Fig. 6(c)) demonstrates the successful operation of the modified restricted voltage balancing algorithm of Fig. 3(b) in CC-SM-based AACs. Similarly as in the FB-SM-based AAC, a circulating current control method is utilized, in order to regulate the SM capacitor voltages to the rated value ($35 \text{kV}$).

Non-sweet-spot operation of the AAC is important as the sweet-spot operation is not applicable in practical applications at all times. Moreover, the ability to operate at different power factors is also important. Fig. 7 demonstrates the results for non-sweet-spot operation of the CC-SM-based AAC ($m_a = 0.9$) with 0.7-lagging power factor. The three-phase output voltages and currents are shown in Fig. 7(a) and (b) while the SM capacitor voltages and the arm currents of phase $a$ are shown in Fig. 7(c) and (d), respectively. The balanced capacitor voltages demonstrate the performance of the balancing algorithm in low power factor and non-sweet-spot operation. The operation of FB-SM-based AAC at this operating point is also similar to the operation of CC-SM-based AAC. Arm currents are subjected to rapid changes during the overlap period.
as shown in Fig. 7(d). These arm current variations affect and distort the three-phase output currents (Fig. 7(b)) at relatively low operating points and low power factors.

5. Loss Evaluation and Comparison

In order to investigate the suitability of the CC-SM for AACs over the FB-SM, the losses in FB-SM- and CC-SM-based AACs are compared while modeling the SMs using identical semiconductor devices. In order to study the losses considering the device count and the single state switching device ratings, the loss profiles of two distinct insulated-gate bipolar transistor (IGBT) and diode modules are analyzed. Based on those two IGBT modules, losses of the two CC-SM configurations are compared and the conclusions are illustrated.

A. FB-SM-Based AAC Losses and CC-SM-Based AAC Losses

The FB-SM-based and CC-SM-based AACs of Section 4 are simulated for loss analysis with PLECS thermal modeling. One SM in each upper and lower arm of both AACs are
Table 2: Specifications of IGBT Modules

<table>
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<tr>
<th>#</th>
<th>Model No. (ABB)</th>
<th>( V_{CE} )</th>
<th>( I_C )</th>
<th>( I_{C_{max}} )</th>
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<tr>
<td>1</td>
<td>5SNA 0800N330100</td>
<td>3.3 kV</td>
<td>800 A</td>
<td>1600 A</td>
</tr>
<tr>
<td>2</td>
<td>5SNA 0750G650300</td>
<td>6.5 kV</td>
<td>750 A</td>
<td>1500 A</td>
</tr>
</tbody>
</table>

Figure 8: Comparison of the normalized losses per two FB-SMs with losses per one CC-SM of the AAC, operating at different power factors; (a) conduction loss, and (b) switching loss.

modeled with the loss characteristics of the IGBT Module-1 given in Table 2. The voltage ratings of the switches at each position in FB-SM (Fig. 2(a)) and CC-SM (Fig. 2(c)) are defined by the nominal capacitor voltage (35kV). Module-2 can be considered as a double rated device for Module-1. Hence, the voltage rating of 35 kV is matched by connecting twelve IGBT modules (3.3 kV) in series.

The steady-state conduction and switching losses per FB-SM and per CC-SM for the near sweet-spot operation \((m_a = 1.26)\) are calculated while changing the power factor from 0.7-lagging to 0.7-leading. As the FB-SM-based AAC has double the SMs, the comparison is performed for two FB-SMs vs one CC-SM in Fig. 8. All loss components are normalized to the total loss of FB-SM-based AAC and given in per-unit scale. The results show that the losses in the CC-SM-based AAC are identical to the FB-SM-based AAC, when the CC-SM is configured with identical semiconductor devices.

Similarly, the conduction and switching loss against the power factor are calculated for non-sweet-spot operating points within the range \(0.8 \leq m_a < 1.26\). Fig. 9 shows the normalized conduction, switching, and total losses per SM of the FB-SM-based AAC, respectively. The trend of conduction losses against the power factor is almost uniform for \(m_a > 1.1\). At lower operating points \((m_a < 1.1)\), conduction losses relatively increase.
Figure 9: Variation of normalized losses per SM of the FB-SM-based AAC with the power factor and the modulation index; (a) conduction loss, (b) switching loss, and (c) total loss.

Conduction losses depend on the resistance of the conduction path (i.e. number of transistors and diodes in series) and the arm currents. In a FB-SM-based AAC arm, the average number of conducting switches increases while the average number of conducting diodes decreases as the modulation index increases, and the total number of conducting devices remains unchanged. Hence, the effective arm resistance over a half-cycle becomes larger for higher modulation indices.

However, when the AAC operates away from the sweet-spot with an overlap period, the circulating current increases to achieve energy balancing. If the circulating current is in the discharging direction of the SM capacitors, the current flows through switches only for lagging power factor operation.
Figure 10: Losses per SM of the CC-SM-based AAC.

(referring to Fig. 2). Moreover, as the overlap period applies around the zero-crossing points of the output voltage reference waveform, almost all the SMs are inserted in the positive voltage polarity. Therefore, when the AAC operates at lower modulation indices, during the overlap period, almost all the conducting devices of both upper arm and lower arm of a phase-leg are switches. This leads to higher conduction losses at lower modulation indices as shown in Fig. 9(a).

In contrast to lagging power factor operation, the SM capacitors are further discharged by the arm current outside the overlap period when the power factor is leading. Hence, the overlap circulating current is relatively larger for lagging power factor operation and, the increased conduction losses during the overlap period lead to higher overall conduction losses (Fig. 9(a)). This phenomenon is insignificant at higher modulation indices.
indices ($m_a > 1.1$) due to the low excess energy in the SMs.

The switching losses against the power factor (Fig. 8(b)) do not significantly vary with the modulation index as shown in Fig. 9(b). The switching losses are slightly increased around unity modulation index. Bipolar operation of the FB-SMs is required only when $m_a > 1$. When the FB-SM-based AAC operates close to unity modulation index, the number of switching transitions of the single state switches becomes frequent, due to the marginal bipolar operation of the SMs. This leads to slightly higher switching losses around unity modulation index operation. When the operating point moves towards the sweet-spot, switching transitions of the single state switches becomes less frequent due to the longer ac voltage push-up period (the time period corresponds to $v_{am} > 1$). Hence, the switching losses slightly decrease for $m_a > 1$ (Fig. 9(b)).

Similarly to the loss analysis of the FB-SM-based AAC, the losses are calculated for the different operating points of the CC-SM-based AAC considering both lagging and leading power factor. Fig. 10(a), (b), and (c) provide the normalized conduction, switching, and total losses per SM of the CC-SM based-AAC, respectively. The conduction and switching losses of the CC-SM-based AAC is similar to the corresponding losses in FB-SM-based Aacs.

The FB-SM and the CC-SM operate as a combination of HB-SMs and single state switches. A similar analysis applies to the CC-SM based AAC. Figs. 9 and 10 show that the use of CC-SM for AACs over the FB-SM does not offer advantages in terms of losses or simplicity of the SM structure. The total losses shown in Figs. 9(c) and 10(c) demonstrate that both AAC types have better performance at comparatively higher modulation indices ($m_a > 1.1$), especially with lagging power factor operation.

B. Impact of Nonidentical Devices on Losses in CC-SM

Based on the two modules of Table 2, the CC-SM can be configured in three ways as; C1) Identical 6.5 kV IGBT modules ($8 \times 6.5$ kV devices), C2) Identical 3.3 kV IGBT modules ($8 \times 3.3$ kV devices), and C3) Mixed IGBT modules [26] ($4 \times 3.3$ kV devices and $2 \times 6.5$ kV devices).

C1 has SM capacitor voltages up to 6.5 kV while the other two configurations up to 3.3 kV. The three resultant Aacs generate similar multilevel output voltages but C1 with less number of levels compared to others. The difference between C2 and C3 lies in the structure of cross-connections. Hence, the conduction and switching losses of these two configurations (specifically in the cross-connections) should be compared and can be analyzed using the on-state/forward characteristics and switching energy loss profiles of the IGBT and the diode in each module (Table 2).

Fig. 11 shows the switching energy losses of the IGBT and diode of each module. The switching losses of the IGBT with a higher voltage rating (6.5 kV) are several times (more than twice) the equivalent switching losses of the IGBT with lower voltage rating (3.3 kV). Moreover, the turn-off energy loss of the diode in Module-1 (3.3 kV) is slightly below half the equivalent energy loss of the diode in Module-2 (6.5 kV). Based on the details in the data sheets, the conduction losses of the IGBTs of two modules are approximately similar and the conduction loss of the diode in Module-2 is higher than individual but lower than twice the conduction loss of the diode in Module-1.

Based on Fig. 11 C1 exhibits the highest switching losses and it is not comparable with other two configurations as the SM capacitor voltage rating differs. C2 and C3 have
the same capacitor voltage rating and comparable losses. Although C3 has a lower device count, switching losses are still higher than C2 due to the significantly high switching energy losses in the 6.5 kV IGBT and diode module as shown in Fig. 11 but, the conduction losses of C3 are lower than C2. However, the higher switching loss of C3 adds to the overall losses of the AAC, despite the lower conduction losses.

Fig. 12 demonstrates the per-SM normalized losses at each switch position of C2 and C3 for unity power factor operation of the AAC. The voltage rating at each switch position (Fig. 2(b)) of both C2 and C3 is matched by series-connecting the relevant IGBT modules. Switching losses are increased and the conduction losses are reduced for the cross-connected devices of C3. However, overall SM loss of C3 is increased compared to C2, due to the significant increment of switching losses at S3 regardless of the reduced total loss at S4. The switching energy losses are dominantly increased compared to the conduction losses when the voltage rating of the semiconductor device becomes higher. Hence, the CC-SM with identical devices is a better choice over the mixed device configuration.

6. Conclusion

The AAC is an emerging dc-fault tolerant multilevel converter topology. Despite its similarities with the MMC, due to the requirement for fully controllable bipolar SMs, only FB-SM and CC-SM can be utilised in the AAC. In this paper a loss analysis of
FB-SM-based AACS and CC-SM-based AACS are presented. The steady-state results of the AAC models demonstrate the identical operation of the two different SMs in the AAC.

Based on the presented analysis and loss comparison, the CC-SM does not offer any advantage over the FB-SM in the AAC. The loss analysis of different operating points demonstrates the comparatively better performance of the AAC at relatively higher modulation indices and for lagging power factor operation. Further loss analysis of CC-SM with identical and nonidentical semiconductor devices shows that, the switching losses are dramatically increased regardless of the conduction losses (hence the total loss) when the higher rated devices are used for cross-connections, adding to the complexity. Unlike the MMC, the CC-SM is not a better alternative for the AAC as it does not offer advantages in terms of losses, complexity. It is therefore recommended that AACS consider only FB-SMs in their circuit configuration.

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