<table>
<thead>
<tr>
<th>Title</th>
<th>Predicting house price with a memristor-based artificial neural network</th>
</tr>
</thead>
<tbody>
<tr>
<td>Author(s)</td>
<td>Wang, J. J.; Hu, S. G.; Zhan, X. T.; Luo, Q.; Yu, Q.; Liu, Zhen; Chen, Tu Pei; Yin, Y.; Hosaka, Sumio; Liu, Y.</td>
</tr>
<tr>
<td>Date</td>
<td>2018</td>
</tr>
<tr>
<td>URL</td>
<td><a href="http://hdl.handle.net/10220/45488">http://hdl.handle.net/10220/45488</a></td>
</tr>
<tr>
<td>Rights</td>
<td>© 2018 IEEE. Translations and content mining are permitted for academic research only. Personal use is also permitted, but republication/redistribution requires IEEE permission. See <a href="http://www.ieee.org/publications_standards/publications/rights/index.html">http://www.ieee.org/publications_standards/publications/rights/index.html</a> for more information.</td>
</tr>
</tbody>
</table>
Predicting House Price With a Memristor-Based Artificial Neural Network

J. J. WANG¹, S. G. HU¹, X. T. ZHAN¹, Q. LUO¹, Q. YU¹, ZHEN LIU², T. P. CHEN³, Y. YIN⁴, SUMIO HOSAKA⁴, AND Y. LIU¹

¹State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 610054, China
²School of Materials and Energy, Guangdong University of Technology, Guangzhou 510006, China
³School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798
⁴Graduate School of Engineering, Gunma University, Kiryu 376-8515, Japan

Corresponding author: Y. Liu (yliu1975@uestc.edu.cn)

This work was supported in part by NSFC under Project 61774028 and Project 61771097, in part by the Fundamental Research Funds for the Central Universities under Project ZYGX2016Z007, and in part by the Opening Project of Science and Technology on Reliability Physics and Application Technology of the Electronic Component Laboratory under Project ZHD201602.

ABSTRACT Synaptic memristor has attracted much attention for its potential applications in artificial neural networks (ANNs). However useful applications in real life with such memristor-based networks have seldom been reported. In this paper, an ANN based on memristors is designed to learn a multi-variable regression model with a back-propagation algorithm. A weight unit circuit based on memristor, which can be programed as an excitatory synapse or inhibitory synapse, is introduced. The weight of the electronic synapse is determined by the conductance of the memristor, and the current of the synapse follows the charge-dependent relationship. The ANN has the ability to learn from labeled samples and make predictions after online training. As an example, the ANN was used to learn a regression model of the house prices of several Boston towns in the USA and the predicted results are found to be close to the target data.

INDEX TERMS House price predicting, neural network, memristor, memristive synapse.

I. INTRODUCTION

The idea of building an artificial brain has existed for a long time. Artificial neural network (ANN) is a possible method to realize artificial intelligence. Until now, researchers have made many amazing achievements in the applications like pattern recognition [1]–[3], face detection [4], [5], learning cat concept from cat videos in the internet [6], classifying [7], and playing Go game [8]. However, most of these works were implemented with CPUs and GPUs. Both have separated memories and processors and consume a large amount of energy [8]. Another way to realize artificial intelligence is to design a customized integrated circuit (IC), which consumes much less power and works in a high speed [7], [9]. However, the customized IC has difficulties in online training, and usually, the neural network in the customized IC [10] has to be trained with the help of von-Neumann computers. In 1983, Michalski proposed a machine that can learn from labeled samples [11]. In 1986, Rumelhart introduced a back-propagation (BP) algorithm to train ANN online automatically [12], [13]. In 1971, Chua [14] predicted the fourth basic circuit element, namely, the memristor, which was later demonstrated in laboratory by Strukov et al. [15] in 2008.

Subsequently, some studies showed that memristors could be used as electronic synapses in ANN [16], [18]. For example, ANN consisting of neurons and memristor-based synapses was used to mimic the associate function of human brain [16], [19].

In this work, a multi-layer feed-forward neural network has been designed using memristors as electronic synapses to realize automatic online training. Memristor weights of the ANN can be adjusted by the BP algorithm to build up a regression model spontaneously, which is different from the classification model realized with memristor-based network in [1]. The trained ANN has been used to predict the house price of several Boston towns in the US, and the predicted result is close to the target data.

II. SIMULATION AND METHODS

A. THE ARCHITECTURE OF ANN

The house price predicting system is illustrated in Figure 1. The ANN used in the house price predicting system is constructed with memristor synapses. The relevant labeled information (i.e. a labeled data includes thirteen parameters and its corresponding target house price) is used to train
J. J. Wang et al.: Predicting House Price With a Memristor-Based ANN

**FIGURE 1.** Schematic illustration of the house price predicting system. Thirteen parameters are considered to predict the house price, and the abbreviations of these parameters in the “Input” module are explained in Supplementary Table 1.

The ANN learns to predict the house price and then does the prediction with the unlabeled information (i.e., an unlabeled data includes only thirteen parameters). Abbreviations for the relevant parameters in the input module are explained in Supplementary Table 1.

**FIGURE 2.** Schematic of the two layer forward neural network (a), weight matrices in hidden layer (b) and output layer (c), and circuit schematic of the weight unit with a memristor (d).

As shown in Figure 2(b), $V_{bpi}$ is the back propagation voltage applied to the $i^{th}$ line in $V$, while $V_{xj}$ is the input voltage applied to the $j^{th}$ column in $V$. As shown in Figure 2(c), $V_{bp}$ is the back propagation voltage, and $V_{hi}$ is the voltage transferred from the hidden layer to the $i^{th}$ column in $W$. $V_{fix}$ is a constant voltage applied to $b_1$ and $b_2$. The circuit of the weight unit with one memristor is illustrated in Figure 2(d). All of the circuits shown in Figure 2 are designed and simulated with Cadence and MATLAB, respectively.

**FIGURE 3.** Schematic illustration of the network connection in the hidden layer.

As shown in Figure 3, the weight matrix element $v_{ij}$ ($i = 1, 2, \ldots, m$; and $j = 1, 2, 3, \ldots, n$) is connected to the input vector $x_j (j = 1, 2, \ldots, n)$ in $X$. The $i^{th}$ Neuron of the hidden layer ($N_i^{(Hidden)}$) collects the currents $i_{ij}$ ($j = 1, 2, 3, \ldots, n$) from the weight units $v_{ij} (j = 1, 2, 3, \ldots, n)$, and the currents are integrated in the membrane potential capacitor $C_{MEM_i}^{(Hidden)} (i = 1, 2, \ldots, m)$ connected to the transfer function module $f_1$. The output $h$ of the neuron is determined by $f_1$ according to

$$W = (w_{ij})_{1 \times m}$$  \hspace{1cm} (2)

$$b_1 = (\gamma_1, \gamma_2, \ldots, \gamma_j, \ldots, \gamma_n)$$  \hspace{1cm} (3)

$$b_2 = (\theta)$$  \hspace{1cm} (4)
Equations (5) and (6).

\[ h = f_1 \left( V \cdot X + b_1 \right) \]  
\[ h_1 = f_1(\beta_1 + \gamma_1) \]

where \( f_1(x) = \frac{1}{1+e^{-x}} \).

\( \beta_i = \sum_{j=1}^{n} (v_{ij} \cdot x_j) \) is the sum of the synaptic currents flowing through all membranes of \( N_i^{(Hidden)} \); and \( \gamma_i \) is the possible leak current of the \( i \)th membrane of \( N_i^{(Hidden)} \).

### FIGURE 4. Schematic illustration of the network connection in the output layer.

There is only one neuron \( N^{(output)} \) in the output layer which collects currents from the weight units \( w_{ij} \) \((j = 1, 2, \ldots, m)\), as shown in Figure 4. The linear-function module \( f_2(x) \) converts voltage of the membrane potential capacitor \( C_{MEM} \) to the final output \( \hat{y} \) according to Eqs. (7) and (8).

\[ \hat{y} = f_2(W \cdot h + b_2) \]  
\[ \hat{y} = f_2(\alpha + \theta) \]

where \( f_2(x) = cx \) and \( c \) is a constant. \( \hat{y} \) can also be rewritten as

\[ \hat{y} = f_2(\alpha + \theta) \]

where \( \alpha = \sum_{j=1}^{m} (w_{ij} \cdot h_j) \) is the sum of synaptic currents which flow through the membranes of \( N^{(Output)} \); and \( \theta \) is the possible leak current of the membrane of \( N^{(Output)} \).

### B. WEIGHT UNIT DESIGN BASED ON MEMRISTOR

The memristor was predicted by Chua according to the symmetry of circuit theory [14]. In this work, we adopt the memristor model reported in [18]. Supplementary Notes 1 and Supplementary Figure 1 present the details of electrical characteristics of the memristor model used in this work. Voltage pulses above \( v_{ih} \) can also be used to adjust the conductance of memristor as well as the weight. In this work, \( v_{ih} \) is set to 0.5 V.

Weight matrix contains weight units and biasing units as shown in Figure 2(b) and Figure 2(c), respectively. The biasing unit is similar to the weight unit except that its magnitude is fixed at 0.5 V. As shown in Figure 2(d), the memristor-based weight unit consists of two switches, a memristor, a micro current detector and a multi-output current mirror. The memristance (i.e., the resistance of the memristor) can be adjusted to an appropriate magnitude by the voltage across the memristor. The multiplication can be realized by obtaining the current flowing through the memristor which is driven by the voltage pulse. In order to avoid convergence of the ANN to a local minimum point, the memristances of the memristors are set to random values in a uniform distribution during system initialization. When the current sink is connected to the output, a positive weight is obtained; when the current source is connected to the output, a negative weight is obtained.

In the training mode, the back propagation pulse amplitude is fixed at 0.5 V. The switches at the anode and cathode of one memristor can change the polarity of the voltage pulse. When the weight is positive, positive pulses can increase the conductance of the memristor as well as the weight, while negative pulses can reduce the conductance and also the weight. The detailed circuit design for the whole ANN is discussed in Supplementary Note 2 and Supplementary Figure 2.

### C. TRAINING AND PREDICTING METHOD

In the training mode, the ANN is able to adjust the weight online automatically based on the BP algorithm. The square of the error between the target result \( y^k \) and the predicted output \( \hat{y}^k \) is connected to the output, a negative weight is obtained.

\[ E_k = \frac{1}{2} (y_k - \hat{y}_k)^2 \]

\[ \Delta v_{ij} = -\eta_1 \frac{\partial E_k}{\partial v_{ij}} \]

\[ \Delta \gamma_j = -\eta_1 \frac{\partial E_k}{\partial \gamma_j} \]

\[ \Delta w_{ij} = -\eta_2 \frac{\partial E_k}{\partial w_{ij}} \]

\[ \Delta \theta = -\eta_2 \frac{\partial E_k}{\partial \theta} \]

The partial derivatives to \( E_k \) are used to calculate the change of weight (i.e., \( \Delta v_{ij}, \Delta w_{ij}, \Delta \gamma_j \) and \( \Delta \theta \)). The derivative of \( f_1 \) is expressed by Equation (10), and the derivative of \( f_2 \) is equal to the constant \( c \). According to the chain derivative method, the partial derivative can be calculated according to Equation (11).

\[ \frac{d}{dx} f_1(\alpha) = f_1(\alpha) \cdot (1 - f_1(\alpha)) \]

\[ \frac{\partial E_k}{\partial w_{ij}} = \frac{\partial E_k}{\partial y^k} \frac{\partial y^k}{\partial \alpha} \frac{\partial \alpha}{\partial w_{ij}} \]

where \( \frac{\partial \alpha}{\partial w_{ij}} = h_j \).

By defining \( g = \frac{\partial E_k}{\partial \alpha} \frac{\partial y^k}{\partial \alpha} = c \cdot (y^k - \hat{y}^k) \), the following expression can be obtained:

\[ \frac{\partial E_k}{\partial v_{ij}} = \left( \frac{\partial E_k}{\partial \hat{y}^k} \frac{\partial \hat{y}^k}{\partial \alpha} \frac{\partial \alpha}{\partial h_i} \right) \cdot \left( \frac{\partial h_i}{\partial \beta_j} \frac{\partial \beta_j}{\partial \hat{y}^k} \right) \]

\[ = (g \cdot w_{ij}) \cdot h_i \cdot x_j \]
By setting $e_h = \frac{\partial E_k}{\partial V_k} = \frac{\partial E_k}{\partial h_i} \cdot \frac{\partial h_i}{\partial y_k} = (g_{ij} \cdot w_{1i}) \cdot h_j (1 - h_j)$, Equation series (13) can be obtained:

$$
\begin{align*}
\Delta v_{ij} &= \eta_1 e_h \cdot x_j \\
\Delta y_k &= -\eta_1 e_h \\
\Delta w_{ij} &= -\eta_2 g \cdot h_j \\
\Delta \theta_j &= \eta_2 g \\
\end{align*}
$$

In the training mode, the initial output $\hat{y}^k$ is calculated by the ANN, and the teacher’s signals are applied to the output layer. With the BP algorithm, the weight of the output layer is updated, and the weight of the hidden layer is updated according to Equation series (13).

In the circuit design, the difference between the output $\hat{y}^k$ and the teacher’s signal $y^k$ can be represented by the BP signal $(\hat{y}^k - y^k)$. Then the BP signal modulates the delay time.

By applying the teacher’s signal, the feed-forward signal $h_j$ of the hidden layer is generated again. The implementation of the BP algorithm is based on the linear increase segment of the STDP rule (Supplementary Figure 3(i)) [18], [19]. The voltage of the pre-synapse is modulated by the amplitude, while the voltage of the post-synapse with amplitude $V_{th}$ is modulated by the delay time. When the delay time is zero, the voltages on both the anode and cathode are the same such that the voltage across the memristor is zero. If the delay time is longer than 1 ms, it is considered as positive; otherwise it is negative. When the delay time is positive, the voltage during the delay time at the transient edge is beyond the threshold voltage, and the memristance changes following Equation (14). The change of memristance is proportional to both the delay time and amplitude of the post-synapse voltage. Neglecting the high order series of Equation (15), $\Delta M$ is proportional to the product of delay time $t_d$ and $V_{pre-syn}$.

$$
\begin{align*}
\Delta M_{ij}(t_d, V_{pre-syn}) &= \int_0^{t_d} f(V_{pre-syn} - V_{th}) dt \\
&= \int_0^{t_d} I_0 e^{V_{th}} \left( e^{V_{pre-syn} + V_{th}} - e^{V_0} \right) dt \\
\end{align*}
$$

where $t_d = A_m \cdot (\hat{y}^k - y^k)$ and $V_{pre-syn} = h_j \cdot V_{th}$.

Then

$$
\begin{align*}
\Delta M_{ij}(t_d, V_{pre-syn}) &= \int_0^{t_d} I_0 e^{V_{th}} \left( e^{V_{pre-syn} + V_{th}} - e^{V_0} \right) dt \\
&\approx \int_0^{t_d} I_0 e^{V_{th}} \left( 1 + \frac{V_{pre-syn} - V_0}{V_0} - 1 \right) dt \\
&= I_0 e^{V_{th}} \cdot \frac{V_{pre-syn} - V_0}{V_0} \cdot t_d \\
&= I_0 e^{V_{th}} \cdot \left( h_j \cdot V_{th} \right) \cdot A_m \cdot (\hat{y}^k - y^k) \\
&= A_p \cdot h_j \cdot (\hat{y}^k - y^k) \\
\end{align*}
$$

III. RESULTS

The input layer generates the amplitude-modulated signal, while the hidden layer generates the waveform which is modulated by the delay time $t_d$ based on Equation series (13). $t_d$ can be generated by an analog multiplier which produces the output $t_{ij} = A_m \cdot (g \cdot w_{1i}) \cdot h_j (1 - h_i)$. In this case, the change of $M_{ij}$ follows

$$
\Delta M_{ij}(t_d, V_{pre-syn}) = A_p \cdot g \cdot w_{1i} \cdot h_j (1 - h_i) \\
$$

In the predicting mode, the input module converts the input data vector $x = \left( x_1, x_2, \ldots, x_j, \ldots, x_k \right)$, $k \in \{1, 2, \ldots, N\}$ to individual voltage pulses whose levels are proportional to the input data $x_j$. The voltage pulses are applied to the anodes of the first weight matrix unit (the $V_{pb}$ is set to 0 V), and the voltage pulses are multiplied with the corresponding weights to output current signals. The currents are collected by $C_{MEM}(Hidden)$ ($i = 1, 2, \ldots, m$) of the neuron in the hidden layer. In the output layer, $C_{MEM}(Output)$ is used in a way similar to that of $C_{MEM}(Hidden)$ to collect the currents, and the output is finally obtained by the conversion from the current to voltage signal by the linear function module $f_2$.

![Figure 5](image-url)
BP algorithm to make the outputs close to the target prices during the training process.

The mean square error (MSE) loss function (\( \text{Loss function} = \sum_{k=1}^{N} (y_k - \hat{y}_k)^2 \)) is used to estimate the performance of the network. The loss function decreases gradually with the increase of training epoch, and reaches a saturation value of \(~0.24\) after \(~50\) epochs, indicating successfully learning of house price prediction, as shown in figure 5(d). The error histogram is roughly concentrated to zero after 200 training epochs, as shown in Figure 5(b).

Finally, the parameters of the test set, which are not used to train the model, are fed to the trained ANN, and the error histogram is showed in Figure 5(c). The errors between the predicted prices and the target prices are small and distribute in a very narrow region (about \([-0.25, 0.25]\)), which again proves that the trained ANN is able to precisely predict the house prices.

![Figure 6](image)

**FIGURE 6.** (a) Predicted house price with parameters from the training set and test set, respectively; (b) comparison between the predicted price and the target price. The values are normalized to the highest house price. The target prices are obtained from [20].

Figure 6(a) shows the target house prices, the prices predicted with the parameters from both the training and test set after training. Figure 6(b) shows the relation between the target prices and the predicted prices. As illustrated in the figure, the departures from the linear regression line \( y = x \) (dash line in Figure 6(b)) is small, indicating that the prediction is reliable.

**IV. CONCLUSIONS**

In this paper, a 2-layer feed-forward neural network is designed using memristors as synapses. The weights of synapses can be adjusted online by the pulse voltage with BP algorithm. The ANN has the ability to learn to predict the house price under training mode, and then can successfully predict the house price in the predicting mode. The ANN was trained with the house price samples of several Boston towns in the US to make predictions, and the predicted results are found to be close to the target data.

**REFERENCES**


J. J. Wang received the B.S. degree in microelectronics from the University of Electronic Science and Technology of China, Chengdu, China, where he is currently pursuing the Ph.D. degree. His current research interests include thin-film transistor, nonvolatile memory devices, and their applications in artificial intelligence.

S. G. Hu received the Ph.D. degree in microelectronics from the University of Electronic Science and Technology of China, Chengdu, China. He has been an Associate Professor with the University of Electronic Science and Technology of China, since 2016. His current research interests include neuromorphic devices, chips, and systems.

X. T. Zhan received the B.S. degree in microelectronics from the University of Electronic Science and Technology of China, Chengdu, China, where he is currently pursuing the M.S. degree. His current research interests include thin-film transistor, nonvolatile memory devices, and their applications in artificial intelligence.

Q. Luo received the Ph.D. degree in microelectronics and solid-state electronics from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2007. He is currently an Associate Professor with the School of Microelectronics and Solid-State Electronics, UESTC. His current research interests include the fabrication of GaN-based HEMT and Si-based MOSFET devices.

Q. Yu received the Ph.D. degree from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2010. He is currently a Professor and the Vice Dean with the School of Microelectronics and Solid-State Electronics, UESTC.

T. P. Chen received the Ph.D. degree from The University of Hong Kong, Hong Kong, in 1994. He is currently an Associate Professor with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore.

Y. Yin received the Ph.D. degree in microelectronics and solid-state electronics from Shanghai Jiao Tong University, China. He has been an Assistant Professor with Gunma University, Japan, since 2008. His current research interests include micro/nano-electronic devices for future’s IoT and AI, renewable energy, and nano-fabrication.

Zhen Liu was born in Changsha, China, in 1983. He received the Ph.D. degree from the School of Electrical and Electronic Engineering, NTU, in 2011. He is currently an Associate Professor with the School of Materials and Energy, Guangdong University of Technology. His research interests include the electrical and optoelectronic properties of metal-dielectric nanocomposites and their device applications.

Y. Liu received the B.Sc. degree in microelectronics from Jilin University, Changchun, China, in 1998, and the Ph.D. degree from Nanyang Technological University, Singapore, in 2005. In 2008, he joined the School of Microelectronics, University of Electronic Science and Technology of China (UESTC), Chengdu, China, as a Full Professor. He has authored or co-authored over 130 peer-reviewed journal papers and over 100 conference papers. His current research interests include memristor neural network systems and neuromorphic ICs. In 2006, he was the recipient of the prestigious Singapore Millennium Foundation Fellowship.