Title	9.3–10.4-GHz-band cross-coupled complementary oscillator with low phase-noise performance(Published version)
Author(s)	Lin, Jia; Ma, Jianguo; Yeo, Kiat Seng; Do, Manh Anh
Citation	Lin, J., Ma, J. G., Yeo, K. S., & Do, M. A. (2004). 9.3–10.4-GHz-band cross-coupled complementary oscillator with low phase-noise performance. IEEE Transactions on Microwave Theory and Techniques, 52(4), 1273-1278.
Date	2004
URL	http://hdl.handle.net/10220/4562
Rights	

9.3–10.4-GHz-Band Cross-Coupled Complementary Oscillator With Low Phase-Noise Performance

Lin Jia, Jian-Guo Ma, *Senior Member, IEEE*, Kiat Seng Yeo, and Manh Anh Do

***Abstract*—A fully integrated 10-GHz-band voltage-controlled oscillator (VCO) has been designed and fabricated using commercial 0.18-μm CMOS technology. The complementary cross-coupled differential topology is adopted in the design. The measured phase-noise is around −89 dBc/Hz at the offset frequency of 100 kHz from the center frequency of 9.83 GHz, the output frequency tuning range of the fabricated VCO is 1.1 GHz ranging from 9.3 to 10.4 GHz, and the power consumption of the core VCO circuit is 5.8 mW. The design is the first one that adopts the complementary cross-coupled circuit structure for 10-GHz-band oscillators, and whose performances of the VCO are the best ones for 10-GHz-band oscillators, compared with the 10-GHz-band CMOS oscillators reported earlier.**

***Index Terms*—Complementary cross-coupled differential topology, LC tank voltage-controlled oscillator (VCO), linear time variant (LTV), lower phase noise, lower power consumption, RF integrated circuit (RFIC), wide tuning range, 0.18-μm CMOS technology.**

I. Introduction

In RECENT years, the 10-GHz-band optical communication system (SONET) market has been growing rapidly and moving toward high data-rate applications. High-frequency low phase-noise oscillators are important to the building blocks in a transceiver design for these applications. CMOS processes typically achieve f_T in excess of 50 GHz to make the processes an alternative for the low-noise RF circuit operating at these higher frequencies [3]–[5]. CMOS oscillators with integrated inductors and p+/n-well varactor are well suited for such applications. Even though a significant amount of research has been carried out in the past, the CMOS voltage-controlled oscillator (VCO) operating in such a high-frequency band is still a challenge for RF integrated circuit (RFIC) designers since more stringent requirements are imposed on VCOs at higher frequencies. The main issue for recent VCO research is to achieve a monolithic integration between low phase noise with a wide frequency tuning range and low power consumption at given operating frequencies. Two papers had been reported on 10-GHz-band VCO adopted CMOS technologies, one is an *LC* delay line VCO with a 225-MHz tuning range, −75-dBc/Hz phase nose at the 100-kHz offset frequency and 70-mW power consumption [1], the other one is the ring-coupled quadrature VCO with 2.5-GHz tuning range, −80-dBc/Hz phase noise at 100-kHz offset frequency, and 45-mW power consumption [2].

Manuscript received August 26, 2003; revised November 25, 2003.

The authors are with the Centre for Integrated Circuits and Systems, Nanyang Technological University, Singapore, 639798 (e-mail: ejgma@ntu.edu.sg).

Digital Object Identifier 10.1109/TMTT.2004.825621

This paper describes a fully integrated CMOS *LC* VCO designed and fabricated by a 0.18-μm CMOS technology operated at 10 GHz. The design is based on the cross-coupled complementary oscillator configuration with around a 1.1-GHz tuning range, from 9.3 to 10.4 GHz, low phase noise of −89 dBc/Hz at the offset frequency of 100 kHz as the oscillation frequency is 9.83 GHz, and the power consumption of the core circuit is 5.8 mW. To our knowledge, the performances of this design are better than that of the reported 10-GHz-band CMOS oscillators in the literature.

II. Circuit Design and Theory

The circuit diagram is shown in Fig. 1(a). A fully integrated complementary cross-coupled configuration is chosen because of the following advantages [6].

- The complementary structure offers higher transconductance at a given current, which results in faster switching of a cross-coupled differential pair.
- It performs better rise- and fall-time symmetry, which results in less upconversion of $1/f$ noise with the other low-frequency noise sources.
- The dc voltage dropping across the channel is larger for the all-NMOS structure since the dc value of the drain voltage is $V_{\rm dd}$. There is, therefore, a stronger velocity saturation and a larger γ.

It is well known that the active devices (NMOS1, NMOS2, PMOS1, and PMOS2) serve as the negative resistor to compensate for the energy loss from the tank due to the tank effective resistor. The cross-coupled VCO operates as switches [3]. Firstly, the oscillator forces $V_{\rm GD}$ of the NMOS transistors are noted to be equal in magnitudes, but with opposite signs to generate a differential voltage across the resonator. At the differential zero voltage, four switching transistors (NMOS1, NMOS2, PMOS1, and PMOS2) are all in the saturation region and form a small-signal negative conductance that breed the startup of the oscillation. As the differential oscillation voltage crosses $V_{{\rm th},n}$ (the threshold voltage of NMOS), $V_{\rm GD}$ (the voltage difference between gate-to-source voltage and drain-to-source voltage) of NMOS1 exceeds $+V_{{\rm th},n}$, forcing it into the triode region, $V_{\rm GD}$ of NMOS2 falls below $+V_{{\rm th},n}$, driving the device into a deeper saturation region, and then NMOS2 turns off.

Simultaneously, as the falling differential oscillation voltage crosses $-V_{{\rm th},p}$ (the threshold voltage of PMOS, a negative value in our design), $V_{\rm DG}$ (the voltage difference between source-to-gate voltage and source-to-drain voltage of PMOS2) exceeds $-V_{{\rm th},p}$, forcing it into the triode region, at the same time, $V_{\rm DG}$ of PMOS1 forces itself into deeper saturation, and

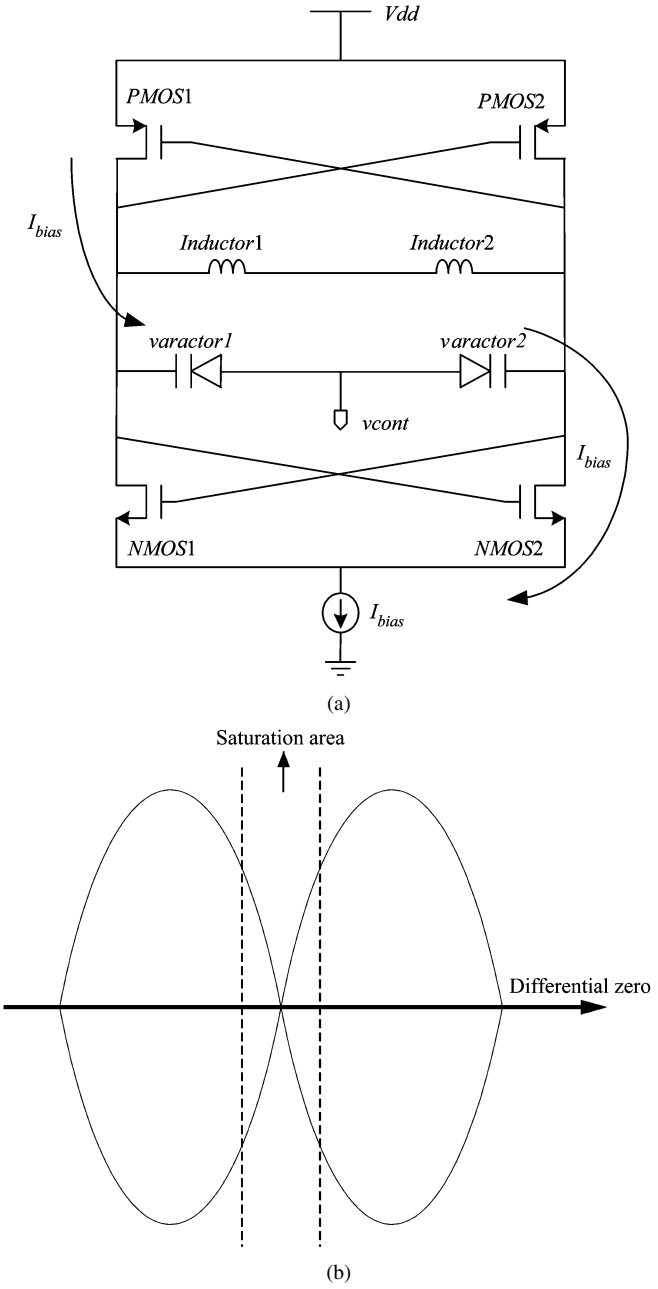

Fig. 1. (a) Schematic of the cross-coupled complementary *LC* VCO with the parasitic elements. (b) Differential zero.

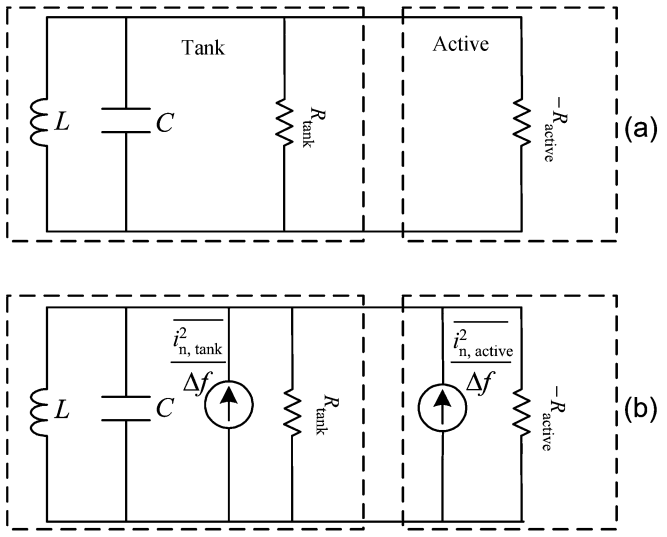

Fig. 2. Equivalent circuit of the *LC* tank VCO. (a) Without a noise source. (b) With noise sources.

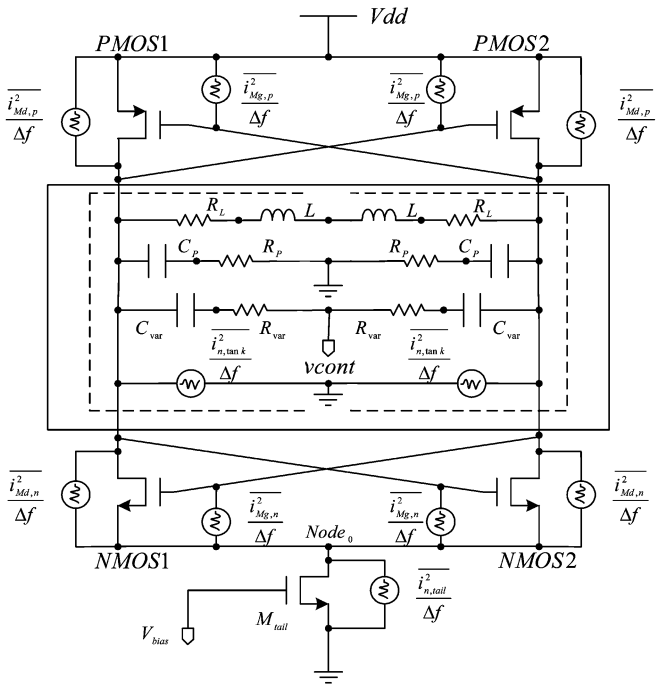

Fig. 3. Complementary *LC* tank VCO with the total noise sources.

then PMOS1 turns off. Thus, the complementary *LC* tank VCO operates when both NMOS and PMOS pairs are all in the saturation region beforehand, then NMOS1 and PMOS2 are at the off states, while other NMOS2 and PMOS1 are at the on states. Such a switching process is periodical throughout the operation of the VCO depicted in Fig. 1(b). The current $I_{\rm bias}$, as indicated in Fig. 1(a), drives the *LC* tank VCO into the stable operation.

III. Phase-Noise Analysis

A. Associate Noise Sources of LC Tank VCO

Fig. 2 depicts the total noise sources existing in an *LC* tank VCO. In general, those noise sources are viewed as the three main contributions of the equivalent positive resistor $R_{\rm tank}$ and the equivalent negative resistor $-R_{\rm active}$, as shown in Fig. 2, and the contribution of the tail transistor's equivalent resistor $R_{\rm tail}$, as shown in Fig. 3. The power spectral densities (PSDs) of these noise sources are required to evaluate the phase noise of the oscillator through linear time variant (LTV) methodology.

1) Noise Sources of the Tank: The main noise sources existing in the tank are shown in Fig. 3. The effective resistance of the tank is expressed [6] as follows:

$$R_{\rm tank} \approx R_L + R_{\rm var} + \frac{1}{R_p(\omega_0 C_{\rm var})^2} \tag{1}$$

where R_L and $R_{\rm var}$ are the series resistance of the inductor and the varactor, respectively, R_p is the substrate resistance of the inductor, and $C_{\rm var}$ is the capacitance of the varactor.

The noise contribution from the effective resistance of the tank is presented by the following current PSD:

$$\frac{\overline{i^2_{n,\tan k}}}{\Delta f} = \frac{4kT}{R_{\tan k}}. \tag{2}$$

2) Noise Sources of the Active Devices: The current PSD of $R_{\rm active}, (\overline{i^2_{n,\rm active}})/\Delta f)$ can be modeled [5] as follows:

$$\frac{\overline{i^2_{n,\rm active}}}{\Delta f} = \frac{\overline{i^2_{Md,n}}}{\Delta f} + \frac{\overline{i^2_{Md,p}}}{\Delta f} + \frac{\overline{i^2_{Mg,n}}}{\Delta f} + \frac{\overline{i^2_{Mg,p}}}{\Delta f}. \tag{3}$$

Here, $(\overline{i^2_{Md}})/(\Delta f)$ and $(\overline{i^2_{Mg}})/(\Delta f)$ are the channel induced noise and gate induced noise of the MOS devices, respectively, and they are modeled by [6]

$$\frac{\overline{i^2_{Md}}}{\Delta f} = 4kT\gamma g_{d0} \tag{4}$$

$$\frac{\overline{i^2_{Mg}}}{\Delta f} = 4kT\delta g_g, \qquad \text{where } g_g = \frac{\omega^2 C^2_{\rm gs}}{5g_{d0}} \tag{5}$$

where g_{d0} and g_g are the output conductance and transconductance of the MOS devices when they work in the saturation region; for this case, the zero crossing of the differential tank voltage is used to evaluate g_{d0} and g_g [3]. $\gamma \approx 2$ for a short channel transistor, hence, $\delta \approx 2\gamma = 4$ [6].

Therefore, the total noises of the active devices in the *LC* tank VCO can be expressed as follows:

$$\begin{aligned}\frac{\overline{i^2_{n,\rm active}}}{\Delta f} &= \left(\frac{\overline{i^2_{Md,n}}}{\Delta f} + \frac{\overline{i^2_{Md,p}}}{\Delta f} + \frac{\overline{i^2_{Mg,n}}}{\Delta f} + \frac{\overline{i^2_{Mg,p}}}{\Delta f}\right) \\ &= \Big(4kT\gamma g_{d0,n} + 4kT\delta g_{g,n} + 4kT\gamma g_{d0,p} + 4kT\delta g_{g,p}\Big).\end{aligned} \tag{6}$$

3) Noise Source of the Tail Transistor: The tail current source is operated at the double frequency of the oscillation frequency of the *LC* tank VCO since the tail node $(\rm Node_0)$ is pulled up when each one of the differential NMOS and PMOS turns on. According to [6], the noise of the tail current source in the vicinity of ω_0 has no effect on the differential noise current, and results in less up-conversion of the $1/f$ noise [6]. In addition, the main noise contribution caused by the tail transistor is the flick noise, i.e., one enlarges the area of this transistor, but keeps the same aspect ratio to reduce the $1/f$ noise. Hence, it can be neglected in our analysis.

Hence, the total noise of the *LC* tank VCO can be expressed by [7]

$$\begin{aligned}\sum \frac{\overline{i^2_n}}{\Delta f} &= \frac{\overline{i^2_{n,\rm active}}}{\Delta f} + \frac{\overline{i^2_{n,\rm tank}}}{\Delta f} \\ &= \Big(4kT\gamma g_{d0,n} + 4kT\delta g_{g,n} + 4kT\gamma g_{d0,p} + 4kT\delta g_{g,p}\Big) \\ &\quad + \frac{4kT}{R_{\rm tank}}.\end{aligned} \tag{7}$$

B. Calculation of the Phase-Noise Using LTV Analysis

Phase noise of an oscillator due to arbitrary noise source is given by [9], [10]

$$\Phi(t) = \int_{-\infty}^{\infty} h_\Phi(t,\tau) i(\tau) = \frac{1}{q_{\max}} \int_{-\infty}^{\infty} \Gamma(\omega_0\tau) i(\tau)\, d\tau \tag{8}$$

where $i(\tau)$ is the current impulse injected at the node of the circuit, and $\Gamma(\omega_0\tau)$ is the impulse sensitivity function (ISF). The ISF is essentially a transfer function between an arbitrary noise source and an excess phase at the output of the oscillator. $q_{\max}$ is the maximum charge swing, and $q_{\max} = C_{\rm node}V_{\max}$, where $V_{\max}$ is the voltage swing across the capacitor at the node of the circuit.

It can be derived from (8) that the phase noise of an oscillator due to thermal noise is [9], [10]

$$L(\Delta\omega) = 10\log\left(\frac{\Gamma^2_{\rm rms}}{q^2_{\max}} \cdot \frac{\sum \frac{\overline{i^2_n}}{\Delta f}}{2\cdot(\Delta\omega)^2}\right) \tag{9}$$

and the single-side bandwidth (SSB) phase noise of an oscillator due to flicker noise is

$$L(\Delta\omega) = 10\log\left(\frac{c^2_0}{q^2_{\max}} \cdot \frac{\sum \frac{\overline{i^2_n}}{\Delta f}}{8\cdot(\Delta\omega)^2} \cdot \frac{\omega_{1/f}}{\Delta\omega}\right). \tag{10}$$

The quantity $\Gamma_{\rm rms}$ is the rms value of the ISF. In this study, all ISFs were obtained using Spectre Time Simulations (periodic steady state) by injecting a small current pulse into an oscillator node over one oscillation cycle, and observing the output phase shifts several cycles later.

In general, these noise sources are cyclostationary because of the periodic changes in current and voltages of the active devices. Consequently, the cyclostationary nature of the noise sources must be considered in a completive analysis. The ISF contains only the sensitivity to noise as a function of time, but it does not reveal the information on the time duration, for which a noise source is present. Hence, the effective ISF is given by [9]

$$\Gamma_{\rm rms,eff}(x) = \Gamma(x)_{\rm rms} \times \alpha(x) \tag{11}$$

where $\alpha(x)$ represents the noise modulation function (NMF) [7].

In this design, the simulated ISF with an injected charge of 0.1 pC is shown in Fig. 4(a). The NMOS and PMOS NMFs are presented in Fig. 4(b), and the effective ISFs are shown in Fig. 4(c). According to (11), the effective $\Gamma_{\rm rms}$ of all active devices' noise sources $\Gamma_{{\rm rms},n,\rm eff} = 0.19$ and $\Gamma_{{\rm rms},p,\rm eff} = 0.15$ are obtained, respectively, when the *LC* VCO operates at 9.83 GHz.

Therefore, the phase noise of -93 dBc/Hz at the offset frequency of 100 kHz is calculated by (9). As such, the phase noises of -95 and -89 dBc/Hz are calculated when the VCO operates at 9.3 and 10.4 GHz, respectively. The noise contributions of all noise sources existing in *LC* tank VCO and the effective ISF of the active device are summarized in Table I. The PSD of the active devices (NMOS and PMOS) is much bigger than that of the tank. Hence, the noises from the active devices

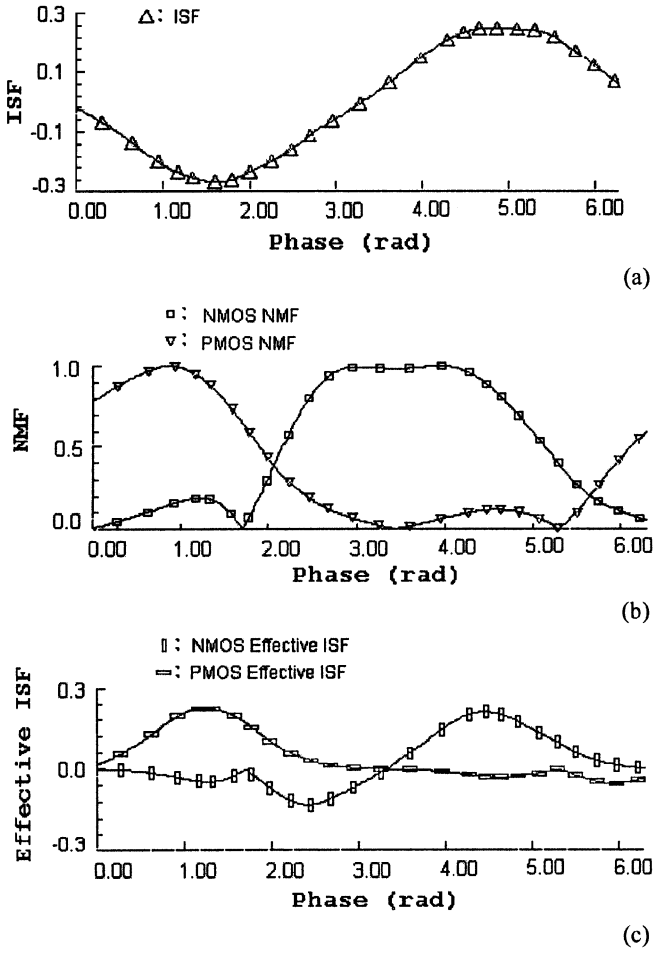

Fig. 4. (a) ISF ($\Gamma_{\rm rms}(x)$) of NMOS and PMOS. (b) NMF ($\alpha(x)$) of NMOS and PMOS. (c) Effective ISF ($\Gamma_{\rm rms,eff}(x)$) of NMOS and PMOS.

TABLE I
PSD OF ALL NOISE SOURCES AND EFFECTIVE ISF

Noise Source	PSD (A^2/Hz)	Γ_{rms}
NMOS	2.86e-22	$\Gamma_{rms,n,eff} = 0.19$
PMOS	1.41e-22	$\Gamma_{rms,p,eff} = 0.15$
Tank	8.1e-23	$\Gamma_{rms} = 0.28$

are the main contributors to the phase noise of the VCO, and all parameters in Table I are used to calculate the phase noise by (9).

IV. EXPERIMENTAL RESULTS

A commercial 0.18-μm CMOS process (CSM 0.18-μm technology) is used to design and implement the project. Six metal layers are used in this process. The technology has a cutoff frequency f_T of 58 GHz, a maximum frequency $f_{\max}$ of 67 GHz [11], and the supply voltage of 1.8 V. Inductors are implemented by stacking the fifth metal layer and top metal layer (sixth metal layer) to prevent the loss of the metal and substrate. The simulation of this inductor predicts an inductance of 0.5 nH and an effective Q value of 10 at 9.83-GHz operation frequency, which is shown in Fig. 5. The p+/n-well diode varactor of the design

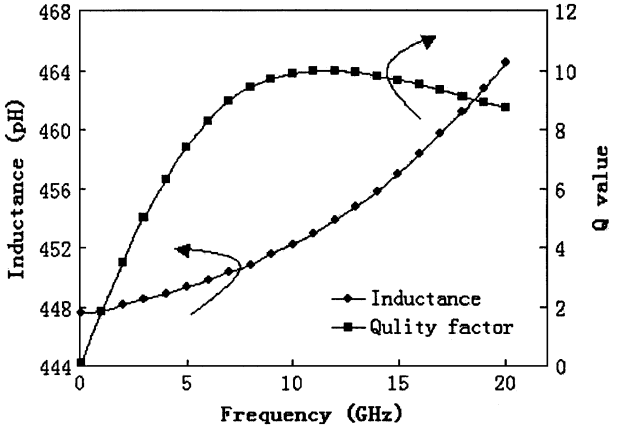

Fig. 5. Simulated inductance and Q value of the inductor.

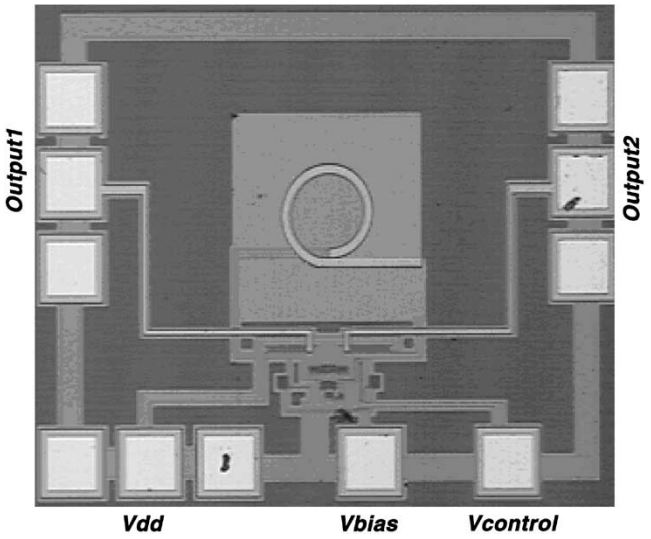

Fig. 6. Die photograph of the *LC* oscillator.

incorporates an capacitance of $\mathrm{C_{var}} = 0.5$ pF with the Q value of around 38 at 9.83 GHz, and the dynamic range $\mathrm{C_{max}}/\mathrm{C_{min}}$ is approximately 2.5 with $0\ \mathrm{V} < V_{\rm var} < 4\ \mathrm{V}$ [11].

The area of the die is approximately 0.5×0.6 mm ^{2}, as shown in Fig. 6. The VCO is measured on the wafer level. A ground–signal–ground (GSG) RF probe is used at the output of the oscillator (output1 or output2, as shown in Fig. 6). The GPG dc probe connected to the bias network is adopted for power supply $V_{\rm dd}$ to filter the original noise from the dc supply equipment HP4142.

The phase noise and PSD have been measured using an HP8564E spectrum analyzer, whose phase-noise characteristic for the 9.83-GHz oscillator is shown in Fig. 7. The phase noise is -91 dBc/Hz at the 100-kHz offset frequency away from the oscillator center frequency of 9.3 GHz, -89 dBc/Hz at the 100-kHz offset frequency away from the oscillation frequency of 9.83 GHz, and -84 dBc/Hz at the 100-kHz offset frequency away from the oscillation frequency of 10.4 GHz.

The figure-of-merit (FoM) characteristic is expressed as [12]

$$\mathrm{FoM} = 10\log\left[\left(\frac{f_0}{\Delta f}\right)^2 \frac{1}{L(\lambda)\,P_{\rm supply}}\right]. \qquad (12)$$

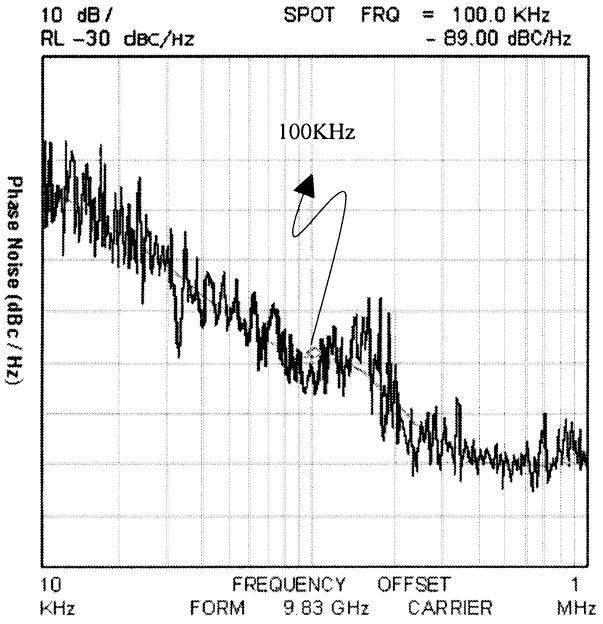

Fig. 7. Measured phase noise at 9.83 GHz.

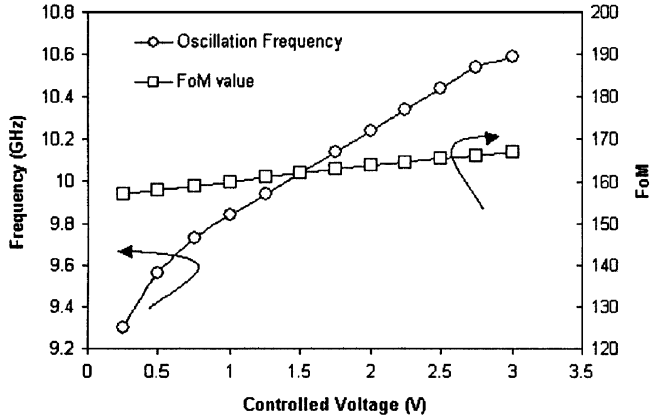

Fig. 8. Tuning characteristics and FoM of the VCO.

TABLE II
SUMMARIZATION OF THE VCO PERFORMANCE

Items	Measured	LTV method
Supply Voltage	1.8V	1.8V
Core circuit power supply	5.8mW	5.6mW
Center Frequency	9.83 GHz	10.2GHz
Tuning Range	11.2%	15.6%
Phase-noise (f_0=9.3GHz, @100kHz)	-91dBc/Hz	-95 dBc/Hz
Phase-noise (f_0=9.83GHz, @100kHz)	-89dBc/Hz	-93 dBc/Hz
Phase-noise (f_0=10.4 GHz, @100kHz)	-84dBc/Hz	-89 dBc/Hz

Here, f_0 is the oscillation frequency of the VCO given by $f_0 = (1/2\pi(\sqrt{LC})$ [6], Δf is the offset frequency, and P_{supply} is the power consumption. Fig. 8 depicts the curves of the oscillation frequency and FoM versus the controlled voltage (which is the voltage difference between the cathode and anode of the pn varactors) from measurement, the tuning range around 1.1 GHz and FoM value of 165 at 9.83-GHz operation frequency are achieved.

The phase-noise performances from the measurement and LTV method for a 9.83-GHz VCO are summarized in Table II. The phase noise using LTV analysis has a good agreement compared to the measured phase noise at the 100-kHz offset frequency, and the maximum difference between both is approximately 5 dBc/Hz. The performance of the 10-GHz VCO is an excellent one for 0.18-μm CMOS technology compared with the reported results in the literature.

V. CONCLUSION

A 1.1-GHz tuning range from a 9.3–10.4-GHz VCO with the low phase noise of -89 dBc/Hz at an offset frequency of 100 kHz away from the center frequency of 9.83 GHz has been designed and fabricated by using Chartered Semiconductor Manufacturing (CSM) 0.18-μm technology. The power consumption of the core circuit of the VCO is 5.8 mW, and the output peak-to-peak voltage is around 1.1 V. Thus far, this design is the first one to adopt complementary cross-coupled differential for a 10-GHz-band CMOS VCO, and the performance of the designed VCO is the best one for a 10-GHz CMOS VCO. Furthermore, this design is very useful for the 10-Gb/s clock and data recovery integrated circuit (IC) and SONET communication applications.

ACKNOWLEDGMENT

The authors would like to thank the foundry of Chartered Semiconductor Manufacturing (CSM), Singapore, for supporting the die fabrication of the designs.

REFERENCES

[1] J. E. Rogers and J. R. Long, "A 10 Gb/s CDR/DEMUX with *LC* delay line VCO in 0.18 μm CMOS," in *Int. Solid-State Circuits Conf.*, 2002, pp. 204–205.

[2] T. P. Liu, "1.5 V 10–12.5 GHz integrated CMOS oscillators," in *VLSI Circuit Tech. Dig. Symp.*, 1999, pp. 55–56.

[3] T. Cho, E. Dukatz, M. Mack, D. MacNally, M. Marringa, S. Metha, C. Nilsion, L. Plouvier, and S. Rabii, "A single-chip CMOS direct-conversion transceiver for 900 MHz spread-spectrum digital cordless phones," in *Int. Solid-State Circuits Conf.*, 1999, pp. 228–229.

[4] H. Samavati, H. Rategh, and T. H. Lee, "A fully integrated 5 GHz CMOS wireless LAN receiver," in *Int. Solid-State Circuits Conf.*, 2001, pp. 208–209.

[5] F. O. Eynde, J. Schmit, V. Charlier, R. Alexande, C. Sturman, K. Coffin, B. Mollekens, J. Craninckx, S. Terrijin, A. Monterastelli, S. Beerens, P. Goetshalckx, M. Ingels, D. Joos, S. Guncer, and A. Pontioglu, "A fully integrated single-chip SOC for Bluetooth," in *Int. Solid-State Circuits Conf.*, 2001, pp. 196–197.

[6] A. Hajimiri and T. H. Lee, *The Design of Low Noise Oscillators*. Boston, MA: Kluwer, 1999.

[7] D. Ham and A. Hajimiri, "Concepts and methods in optimization of integrated *LC* VCOs," *IEEE J. Solid-State Circuits*, vol. 36, pp. 896–909, June 2001.

[8] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, U.K.: Cambridge Univ. Press.

[9] A. Hajimiri and T. H. Lee, "A general theory of phase-noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, pp. 179–194, Feb. 1998.

[10] ——, "Design issues in CMOS differential *LC* oscillators," *IEEE J. Solid-State Circuits*, vol. 34, pp. 717–724, May 1999.

[11] *0.18 μm Process Design Manual*, Chartered Semiconductor Manufacturing, Singapore, 2002, pp. 1–120.

[12] P. Kinget, *Integrated GHz Voltage Controlled Oscillators*. Norwell, MA: Kluwer, 1999, pp. 353–381.

[13] J. Craninckx and M. Steyaert, "Low-noise voltage-controlled oscillator using enhanced *LC* tanks," *IEEE Trans. Circuits Syst. II*, vol. 42, pp. 794–804, Dec. 1995.

Lin Jia received the B.S. degree in semiconductor physics and devices from the Shenyang Polytechnic University, Shenyang, China, in 1991, the M.S. degree in semiconductor physics from JiLin University, Changchun, China, in 1994, and is currently working toward the Ph.D. degree at the Nanyang Technological University, Singapore.

In 1994, she joined the Beijing Power Electronics Research and Development Center (BPEC), where she was a Device Modeling and Simulation Engineer. From 1998 to 2001, she was a Senior Modeling and Simulation Engineer with the Digital DNA Laboratory, Motorola, Beijing, China, where she was involved with deep-submicrometer CMOS. Since 2001, she has been a Research Associate with the Centre for Integrated Circuits and Systems (CICS), Nanyang Technological University, where she is involved with the research and design of RFIC building blocks by deep-submicrometer CMOS technology, BiCMOS technology, and the phase noise reduction technique and its implementation in RF CMOS VCOs.

Jian-Guo Ma (M'96–SM'97) received the B.Sc. and M.Sc. degrees (with honors) from the Lanzhou University of China, Lanzhou, China, in 1982 and 1988, respectively, and the Doctoral degree in engineering from the Gerhard-Mercator University, Duisburg, Germany, in 1996.

Prior to joining the Nanyang Technological University, Singapore, in 1997, he was with the Technical University of Nova Scotia, Halifax, NS, Canada. He is currently an Associate Professor and Director of the Center for Integrated Circuits and Systems, Nanyang Technological University. He has authored or coauthored over 130 technical papers and two books. He holds six patents in CMOS RFICs. His research interests are RFIC designs for wireless applications, RF characterization and modeling of semiconductor devices, RF interconnects and packaging, system-on-a-chip (SoC) and applications, and electromagnetic compatibility/electromagnetic interference (EMC/EMI) in RFICs.

Kiat Seng Yeo received the B.E. degree in electronics (with honors) and Ph.D. degree in electrical engineering from the Nanyang Technological University, Singapore, in 1993 and 1996, respectively.

In 1996, he joined the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, as a Lecturer, and became an Assistant Professor in 1999 and an Associate Professor in 2002. He provides consulting to statutory boards and multinational corporations in the areas of semiconductor devices and electronic circuit design. He has been extensively involved in the modeling and fabrication of small MOS/bipolar integrated technologies over the last ten years. His research interests also include the design of new circuits and systems (based on scaled technologies) for low-voltage low-power applications, RFIC design, IC design of BiCMOS/CMOS multiple-valued logic circuits, domino logic, and memories, and device characterization of deep submicrometer MOSFETs.

Manh Anh Do received the B.E. degree in electronics (with honors) and Ph.D. degree in electrical engineering from the University of Canterbury, Canterbury, New Zealand, in 1973 and 1977, respectively.

From 1977 to 1989, he was a Research and Design Engineer and Production Manager with Radio Engineering Ltd., a Research Scientist with the Fisheries Research Centre, and a Senior Lecturer with the National University of Singapore. In 1989, he joined the School of Electrical and Electronic Engineering, Nanyang Technological University (NTU), Singapore, as a Senior Lecturer, and became an Associate Professor in 1996 and a Professor in 2001. Since 1995, he has been Head of the Division of Circuits and Systems, School of Electrical and Electronic Engineering, NTU. He has been a consultant for numerous projects in the Singapore electronic industry, and was the principal consultant for the design, testing, and implementation of the $200 million Electronic Road Pricing (ERP) island-wide project in Singapore from 1990 to 2001. His current research interests are digital and mobile communications, RFIC design, mixed-signal circuits, and intelligent transport systems. He has specialized in sonar design, biomedical engineering, and signal processing.

Dr. Do is a Chartered Engineer in the U.K. and a Professional Engineer in Singapore. He is a Fellow of the Institution of Electrical Engineers (IEE), U.K.