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OPTICAL AND ELECTRONIC LOGIC GATE WITH ORTHOGONAL INPUTS

XU CAI

SCHOOL OF MATERIALS SCIENCE AND ENGINEERING

2018
OPTICAL AND ELECTRONIC LOGIC GATE WITH ORTHOGONAL INPUTS

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SCHOOL OF MATERIALS SCIENCE AND ENGINEERING

A thesis submitted to the Nanyang Technological University in partial fulfillment of the requirement for the degree of Doctor of Philosophy

2018
Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research and has not been submitted for a higher degree to any other University or Institution.

17/01/2018

Date

Xu Cai
Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

17/01/2018

Date

Chen Xiaodong
Authorship Attribution Statement

This thesis contains material from a paper (plan to be) published in the following peer-reviewed journal where I was the first and/or corresponding author.

Chapter 4 is (plan to be) published as Cai Xu, Zhihua Liu, Xiaotian Wang, Yaqing Liu, Zhiyuan Liu and Xiaodong Chen*. Optoelectronic self-destructive memory device based on multi-segmented nanorods. The paper is currently under preparation.

The contributions of the co-authors are as follows:

- Prof. Xiaodong Chen provided the initial project direction and edited the manuscript drafts.
- I prepared the manuscript drafts. The manuscript was revised by Dr. Zhihua Liu and Dr. Xiaotian Wang.
- I co-designed the study with Prof. Xiaodong Chen and performed all the laboratory work at the School of Materials Science and Engineering. I also analyzed the data.
- Dr. Yaqing Liu assisted the concept design of self-destructive memory device, he generated the idea of using schematic diagram illustrating the information self-destructive process.
- Dr. Zhiyuan Liu assisted part of the SEM image collection and EDX analysis.
Abstract

Logic gate is the fundamental for computational operation. With the fast development of information technology, it is necessary to develop the logic operation system at micro or nanoscale. At the meantime exploring different kinds of output signal and incorporating various inputs could significantly extend the potential application of logic gate.

This thesis aims to explore both optical and electronic logic gate function with orthogonal inputs, and realize the functions at micro or nanoscale. Our thesis starts from the hypothesis that by employing one system which is sensitive to orthogonal external inputs (optical, electrical and electrochemical), loading different inputs could generate outputs and realize the logic operation. The output value depends on the input and the output signal could be controlled by properly designing the system and materials involved. Another objective is to achieve the logic gates with stable output, even without continuous input provided. Hence, the logic operation does not rely on durative power supply. Memristors and orthogonally switchable molecules were used in the current study toward this goal.

Two contributions of the thesis include developing the electronic logic gate and the optical logic gate in novel approaches.

Firstly, the electronic logic gate has been successfully demonstrated based on the integration of single nanorod based optoelectronic memory device and electrically switchable memory devices. The memristor based circuit does not rely on continuous input to generate output. Thus, it performs the function of both information storage and logic operation. To achieve such kind of logic gate, firstly the optoelectronic memory device has been developed based on single nanorod device. The device was fabricated based on the photo-sensitive semiconductor CdS. By properly engineering the material interface, the photocurrent can be maintained after removing optical stimulation. Unlike the tradition memory device, the single nanorod based resistive switching memory could keep photocurrent persistently but the information could still be compulsively erased after a
specific time horizon. Thus, it demonstrated the function of both information storage (memory) and information protection (self-destructive). The optoelectronic memory device was integrated with an electrically switchable resistive switching memory thereafter to demonstrate the memristor based logic gate function. Due to the characteristics of two components employed, the circuit realized three levels of functions: the fundamental “OR” logic gate, the memorable logic gate and the self-locking logic gate.

Secondly, the optical logic gate was designed to generate distinct plasmonic output signal by transforming the orthogonal inputs. The device was prepared by assembling the organometallic molecules, which is responsive to both light illumination and electrochemical stimulation, to the plasmonic active gold nanoparticle arrays. The output signal, which is the plasmon resonance, can be tuned as a result of molecular switch under different stimulations. Thus, the plasmonic logic function has been successfully demonstrated in solid state, and by molecular modulation for the first time.
Lay Summary

The information technology developed rapidly nowadays. The logic gate is the fundamental component for computation. This thesis aims to develop new types of logic functions. The main innovations are listed as below:

Firstly, the intensive information processing rose up the requirement of developing smaller size components. Thus, if the logic gate function can be realized at micro or even nanoscale it could contribute to the objective significantly. In the current thesis, some advanced technologies were utilized to realize the size minimization.

Secondly, the logic gate generally accept electrical inputs, and generate electrical outputs. Thus, there is an opportunity for diversification. For the inputs, if the logic gate could accept different signals, it will be able to be operated under different conditions. For example, if the element is sensitive to light illumination, the logic gate could accept light and then transform it to the output signal. This could extend the application. Additionally, if the logic gate can generate output on top of the electrical signals, the computation is able to be performed in innovative ways.

Thirdly, the common logic gate is computed under the electrical power supply. It is interesting to develop a component that could perform both logic computation and information storage function. Thus, here in this thesis the memory device is utilized to construct logic gate. The memory device is widely used in information storage. A memory device based logic gate could generate continuous output with only one time input. Thus, the information can be maintained without continuous power supply.

In this thesis the above mentioned innovations have been realized. The logic function can be performed with two different kinds of inputs. Additionally, two output signals, optical and electrical, have been demonstrated.
Acknowledgements

Firstly, I thank the financial support from Singapore Ministry of Education Academic Research Fund (AcRF) Tier 2. With their financial funding support the equipment and materials are possible to be purchased in order to conduct the experiment and finish this thesis.

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I would like to show my gratefulness to our collaborator, Professor Stephane Rigaut from University of Rennes, his group helped me to synthesize the organic molecules and organometallic molecules. Part of this thesis is done based on the unique switching characteristics of such molecules.
I would also like to say thanks to all our group members. Thanks to their sharing of new ideas and experimental tools on each group meeting and sub-group meeting. Without their kindly support, this study is unable to be completed. Especially, I would like to thank to my colleagues Dr. Wang Xiaotian, Dr. Liu Yaqing, Dr. Liu Zhihua, Dr. Meng Fanben, Dr. Zhu Bowen, Dr. Liu Yuanjun, Dr. Qianpeng, Dr. Li Bin, Dr. Yu Jiancan, Dr. He Ke, Dr. Wang Juan, Dr. Yang Hui, Dr. Tang Yuxin, Dr. Cai Pingqiang, Dr. Hu Benhui, Dr. Wang Ting, Dr. Wang Hong, Dr. Wang Hua, Dr. Wang Wei, Dr. Liu Zhiyuan, Mr. Lv Zhisheng, Miss Chen Geng, Miss Jiang Ying, Miss Guo Xintong, Miss Wang Ting, Miss Cui Yajing, Miss Luo Yifei, Mr. Wei Jiaqi. Thanks to their continuously idea sharing, experimental details discussing and valuable suggestions for my thesis writing.

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# Table of Contents

Abstract ........................................................................................................................................................................... i

Lay Summary ........................................................................................................................................................................ iii

Acknowledgements .................................................................................................................................................................. v

Table of Contents ............................................................................................................................................................... vii

Table Captions ........................................................................................................................................................................ xiii

Figure Captions ....................................................................................................................................................................... xv

Abbreviations ......................................................................................................................................................................... xxix

## Chapter 1  Introduction ..................................................................................................................................................... 1

1.1 Hypothesis/Problem Statement ........................................................................................................................................ 2

1.1.1 Memory Devices Based Electronic Logic Gate with Orthogonal Inputs ................................................................. 2

1.1.2 Plasmonic Logic Gate with Orthogonal Inputs ........................................................................................................... 6

1.2 Objectives and Scope ........................................................................................................................................................ 10

1.3 Dissertation Overview ....................................................................................................................................................... 10

1.4 Findings and Outcomes ....................................................................................................................................................... 12

References ............................................................................................................................................................................... 13

## Chapter 2  Literature Review ............................................................................................................................................. 17

2.1 Overview .............................................................................................................................................................................. 18
2.1.1 Memristor-based Electronic Logic Gate .......................................................... 18
  2.1.1.1 Memristor ................................................................................................. 18
  2.1.1.2 Optically Switching Memory Device ......................................................... 23
  2.1.1.3 Memristor Based Electronic Logic Gate .................................................... 25
2.1.2 Fundamentals for Nanoscale Optical Logic Gate ........................................... 30
  2.1.2.1 Molecular Logic Gate ................................................................................ 30
  2.1.2.2 Controlling Plasmon Resonance by Modulating Molecular Antenna...... 34
2.2 Questions to answer based on literature-electronic logic gate............................... 39
2.3 Questions to answer based on literature-optical logic gate ................................... 41
2.4 PhD in context of literature .................................................................................. 41
References .................................................................................................................. 42

Chapter 3 Experimental Methodology ..................................................................... 49
3.1 Rationale for Selection .......................................................................................... 50
3.2 Preparation of electronic logic gate with orthogonal inputs ............................... 52
  3.2.1 Method to fabricate single nanorod based optoelectronic memory device...... 52
  3.2.2 Logic Function Realization .......................................................................... 57
3.3 Fabrication of optical logic gate with orthogonal inputs ...................................... 58
  3.3.1 Method to fabricate plasmonic-active substrate ........................................... 59
  3.3.2 Assembly of organic/organometallic molecules .......................................... 60
3.4 Characterization and experimental setup for logic performance measurement ...... 61
  3.4.1 Characterization and electric measurements for the single nanorod device and
      electronic logic gate ......................................................................................... 61
  3.4.2 Characterization and Measurements for Optical Logic Gate ......................... 62
Chapter 4  Optoelectronic Self-destructive Memory Device Based on Multi-segmented Nanorods ................................................................. 65

4.1 Introduction ........................................................................................................... 66
4.2 Materials and Methods .......................................................................................... 71
  4.2.1 Electrochemical Deposition of Nanorod .......................................................... 71
  4.2.2 Nanorod Device Characterization .................................................................... 72
  4.2.3 Controlling the Formation of Interface ............................................................ 73
4.3 Principle Outcomes ............................................................................................... 75
  4.3.1 Surface Plasmon Resonance Enhanced Photocurrent ....................................... 75
  4.3.2 Controllable Persistent Photocurrent for Optoelectronic Memory Device ........ 80
  4.3.3 Controllable Multi-addressable Characteristics ............................................... 83
  4.3.4 Demonstration of Self-Destructive Memory Behavior for Information Protection ................................................................. 88
4.4 Conclusion .............................................................................................................. 93
Reference .................................................................................................................... 93

Chapter 5  Optically and Electrically Configurable Memory for Programmable Logic Gate with Orthogonal Inputs ................................................................. 99

5.1 Introduction ........................................................................................................... 100
5.2 Materials and Methods ......................................................................................... 102
  5.2.1 Setup of Electronic Logic Gate with Orthogonal Inputs .................................... 102
  5.2.2 Device characterization ..................................................................................... 103
5.3 Principle Outcomes ............................................................................................... 104
5.3.1 Performance for Single Memory Component ........................................ 104
5.3.2 Demonstration of Logic Function for Different Inputs ............................... 108
5.3.3 Discussion on the Function of Logic Gate ............................................. 112
5.4 Conclusion ........................................................................................................ 115
References ............................................................................................................. 116

Chapter 6 Developing Plasmonic Logic Gate by Orthogonally Modulating

Organometallic Molecules ......................................................................................... 119

6.1 Introduction ........................................................................................................... 120
6.2 Materials and Methods ....................................................................................... 123
  6.2.1 Molecule synthetic procedures ................................................................. 123
  6.2.2 Fabrication of Plasmonic Active Substrate ............................................... 123
  6.2.3 Assembly of Molecules and Controllable Molecular State Switch .......... 124
6.3 Principle Outcomes ............................................................................................. 125
  6.3.1 Controlling Plasmon Resonance by Optically Switching the Organic Molecules ........................................................................................................ 125
  6.3.2 Demonstration of Plasmonic Logic Gate by Orthogonally Tuning the States of Organometallic Molecules ................................................................................................. 133
6.4 Conclusion ........................................................................................................... 140
References ............................................................................................................. 141

Chapter 7 Discussion and Future Work .................................................................. 145

7.1 General Discussion ............................................................................................. 146
7.2 Reconnaissance Work for Future Work ............................................................ 148
  7.2.1 Demonstration of Logic Function in Single Device ................................... 148
Table of Contents

7.2.2 Time Dependent Automatic Hierarchical Storage ........................................ 150
7.2.3 Plasmonics in Tunable Gap Structure ......................................................... 153
7.3 Conclusion ........................................................................................................ 155
References ............................................................................................................... 156
Table Captions

Table 2.1 Comparison between IMPLY and MAGIC memristor based logic gate[^39].

Table 4.1. Performance summary of nano-photodetectors and memory devices.
Figure Captions

Figure 1.1 (a) the seven most common types of logic gates and their logic meanings. (b) the truth table of different types of logic gates.

Figure 1.2 Typical logic gates performed by integration of memristors: (a) The AND gate, (b) The OR gate, (c) the NOT gate, (d) the NOR gate and (e) the NAND gate[4].

Figure 1.3 Proposed design of logic circuit with orthogonal inputs.

Figure 1.4 (a) The schematic to illustrate the design of 1D multi-segmented nanorod heterostructure and the hypothetical electrons/holes migration. (b) the hypothetical photocurrent change upon light illumination and after light off.

Figure 1.5 (a) Mechanism of circuit design: upon illumination, the OPD will trigger a redistribution of voltage in the two devices. Meanwhile, the threshold change will cause a non-volatile resistance change in ORS. (b) current-voltage characteristics of OPD under dark and upon light illumination with different incident light intensities. (c) current-voltage characteristics of ORS. (d) current-voltage characteristics of whole circuit under different illumination conditions. (e) the writing process of 16 different resistance states (4-bit) have been demonstrated[18].

Figure 1.6 The molecule switch induced nanodevice based logic gates (a) schematic that illustrate the experiment setup. The nanogap structure was prepared by electrochemical approach, the molecules are self-assembled to bridge the gap. (b) switching mechanism for the molecule with one DTE unit and two Ru systems. (c) experimental demonstration of the OR gate with two inputs. The molecule can be switched either by UV light or by electrochemical stimulation. The molecules can be switched back with visible light. (d) switching mechanism for the molecule with two DTE unit and three Ru systems. e) experimental demonstration of the AND/OR gate with three inputs. The molecule can be
switched either by UV light or by two steps sequential electrochemical stimulations. The molecules can be switched back with visible light[34].

**Figure 1.7** Schematic illustrating the plasmonic logic gate function.

**Figure 2.1.** (a) The four fundamental elements to connect six mathematical relations. (b) the current-voltage relationship of a resistive memory device demonstrated in the Pt-TiO$_2$-Pt sandwiched structure[2].

**Figure 2.2** (a), (b) Typical current–voltage characteristics of resistive memory device working under filamentary and distributed switching mechanisms. c) current–voltage characteristics of the resistive switching memory device working with both switching mechanisms. (d), (e), (f) the schematic diagram shows the switching mechanism of filamentary, distributed and combined, respectively[4].

**Figure 2.3** The structure design and performance measurement results of memory devices prepared by various materials. (a) The representative of metal-oxide based resistive switching memory designed in Pt-TiO$_{2-x}$-Pt sandwich structure[12]. (b) the characterization and device performance of amorphous silicon based memory[14]. (c) schematic and stability of polymer based resistive switching memory[13]. (d) the SEM image and current-voltage characteristics of carbon based memory device[16]. (e) The representative of bio-material based multi-level resistive switching memory, prepared by Ag-sericin-Au sandwich structure[19,20].

**Figure 2.4** Tunable resistive switching behavior in memory devices by (a) magnetic field[21], (b) temperature[22] and (c) chemical stimulations[23].

**Figure 2.5.** (a) I-V curve of device under 1min, 5min and 10min light illumination. Inset: I-V curve measured in the dark. (b) Retention of the ON/OFF states[27].

**Figure 2.6.** Optically controllable memory device based on (a) Al$_2$O$_3$[27]. (b) BiMnO$_3$[29].
Figure 2.7. (a) The Atomic Force Microscope (AFM) image of memristive crossbar array nanocircuit. (b) the ideal current-voltage characteristics of single memristive and the resistive states operation. (c) illustration of IMP operation with two voltage pulses: $V_{\text{COND}}$ and $V_{\text{SET}}$, which are applied to switch p and q, respectively. The right side figure shows the truth table for IMP operation. (d) the colored curve shows the voltages applied (blue for p and red for q. The number is the value input, while the results can be read out correspondingly\textsuperscript{[33]}.

Figure 2.8. MAGIC gate with NOR function in a crossbar array\textsuperscript{[39]}.

Figure 2.9. (a) Schematic diagram illustrating the device design and operation. From top to bottom, it is constructed with: Co ferromagnetic electrode, a thin layer of AlOx tunnel barrier, the Alq3 organic semiconductor and the La$_{0.7}$Sr$_{0.3}$MnO$_3$ ferromagnetic electrode at the bottom. (b) the resistance measured with different magnetic field intensity under various voltage. A high enough voltage bias can destroy the GMR effect. (c) the resistance and GMR under different voltage. (d) and (e) demonstration of the implication (IMP) logic function in this device\textsuperscript{[40]}.

Figure 2.10. The mimic computational process with molecular logic. The currently available substrates are summarized, the chemical reagent and/or testing environmental conditions which is able to influence the output are listed. Similar to the traditional semiconductor based logic gate, the molecular logic gate can response to a number of different inputs and generate output. Unlike the electronic logic, the output can vary in a board range\textsuperscript{[52]}.

Figure 2.11. (a) The schematic diagram illustrating the fundamental OR logic gate, which is established by combination action of dsDNA-AuNRs and ERs. Controlling the interaction of ERs and dsDNA the logic operation can be realized. (b) The output of different logic functions is the ratio of absorption intensity at 510 nm and 885 nm. Controlling the operation of inputs, the logic functions can be demonstrated as OR, NOT,
Figure 2.12. (a) The schematic explains the molecule switch operation. The four different states: 1o, 1c, 1c²⁺ and 1c⁺, can be achieved by applying different stimulations. (b) UV-Vis spectroscopy of the on state molecule and the off state molecule, explaining the wavelength to drive switch. (c) the CV curve of 1o state molecules under two consecutive scans and the close state molecules. (d) UV-Vis-NIR spectroscopy of different states by applying specific electrochemical stimulations[54].

Figure 2.13. (a) Extinction spectra of gold particle measured in air (black), after coated with a layer of PEDOT film with oxidized state (blue) and after coated with a PEDOT film with reduced state[66]. (b) The plasmon resonance shift under different electrochemical stimulations. The inset illustrate the operation for plasmon resonance switch of the Au nanoparticle arrays on ITO substrate, and covered by PANI[67].

Figure 2.14. (a) Structure and electrochemical switching mechanism of the dithiolaneterminated bistable rotaxane (b) schematic diagram illustrating plasmon resonance shift with different states of molecules. (c) extinction of molecule before (green) and after (red) the TTF station oxidation. (d) numerical calculation of extinction and refractivity change corresponding to (c). (e) and (f) extinction spectra of Au-molecule and Au nanodisk systems for the initial state, before and after oxidation[68].

Figure 2.15. The operations to induce molecular switch by controlling the incident light wavelength in (a) azobenzenes (AB), (b) spiropyrans (SPs) and (c) dithienylethenes (DTEs)[77].

Figure 2.16. (a) Schematic diagram shows the azobenzenes bonding to the gold nanoprisms and switch between cis and trans states under UV light and blue light illumination. (b) SPR extinction spectrum for Au-molecule hybrid structure. The red curve
shows the situation for molecule in trans state while the green one represent the state in cis. (c) The LSPR peak shift by repeatedly tune the molecular states[64].

**Figure 3.1.** (a) SEM image of an Au-Ni/NiO-CdS-Ni/NiO-Au device, the red dash line is the scanning trace of EDX analysis. (b) EDX elemental line-scanning analysis of a single Au-Ni/NiO-CdS-Ni/NiO-Au nanorod.

**Figure 3.2.** (a) The gold particle array fabricated by photolithography with diameter of 5 μm (b) The board extinction peak made it difficult to compare SPR shift between various molecular states.

**Figure 3.3.** (a) AAO membrane with silver back layer. (b) protocol of electrochemical deposition along AAO membrane. (1) commercially available AAO template. (2) sliver layer evaporated on the back side of AAO membrane. (3) sacrificial silver layer deposited in order to make sure the connection to the evaporated backing is clean. (4) deposit multi-segment nanorods in sequence. (5) remove the Ag layer, solve the AAO membrane and get dispersed nanorods.

**Figure 3.4.** (a) Schematic of photolithography fabrication of micro-electrodes. (b) the micro-electrodes pattern prepared following the steps shown in Figure 3.4a, the inset is the magnified microscope image of single electrode pattern.

**Figure 3.5.** (a) Schematic of e-beam lithography. (b) the Au-Ni-Au-Ni/NiO-CdS-Ni/NiO-Au-Ni-Au single nanorod heterostructure device engineered using the procedure in Figure 3.5a.

**Figure 3.6.** (a) Micro-electrodes patterned on PET substrate by photolithography. (b) the nanodevice written on PET substrate by e-beam lithography.

**Figure 3.7.** The schematic illustrating the ZIF-8 based memory device. The Ag patterns, ZIF-8 and Si act as top electrode, switching layer and bottom electrode, respectively.
Figure 3.8. (a) The experimental procedure of AAO membrane with PMMA holder transferred to the ITO substrate, followed by PMMA solving, thermo-evaporation and removal of membrane. (b) the SEM image of ultra-thin AAO membrane covered on the surface of ITO. (c) the nanoparticle arrays obtained after thermo-evaporation. The inset is magnified image of the relatively homogenous nanoparticle arrays.

Figure 3.9. The chemical reactions to form covalent Au-S bond between Au and (a) organic molecule, (b) organometallic molecule.

Figure 3.10. The (a) Keithley 4200-SCS and (b) HAL-320W xenon lamp used in current experiment.

Figure 3.11 UV-Vis spectrophotometer used in current study to collect extinction spectrum from the Au-organic/organometallic molecules hybrid structure.

Figure 4.1 The decay curve of photoconductivity after light off in SrTiO$_3$/LaAlO$_3$ heterogeneous interface$^{[9]}$.

Figure 4.2 (a) ZnO/SrTiO$_3$ nanorod based optically switchable memory device, after light removal, the photocurrent can be kept for a long time. (b) ZnO nanorod arrays based memory device, without light irradiation, the device performs typical semiconductor characteristics. Under light illumination, it demonstrates memory behavior. (c) ITO/CeO$_{2-x}$/AlO$_y$/Al based memory. The device can be optically written and information can be erased by applying a reverse voltage bias. However, the ON/OFF ratio is not desired.

Figure 4.3. Fabrication strategy of multi-segmented nanorod devices by electrochemical deposition and the subsequent e-beam lithography.

Figure 4.4. SEM images of (a), (b) Au-Ni-Au-Ni/NiO-Cds-Ni/NiO-Au-Ni-Au, (c), (d) Au-Ni-Au-Cds-Au-Ni-Au and (e), (f) Au-Ni-Cds-Ni-Au nanorod devices prepared by electrochemical deposition followed by electron-beam lithography (EBL). (a), (c), (e) are
the images for devices connected to microelectrodes while (b), (d), (f) are the magnified images for the inner, effective segments.

**Figure 4.5.** XPS spectra of (a), (b) Ni 2p and O 1s thin film deposited by nickel plating solution without adding KCl and KOH. (c), (d) Ni 2p and O 1s thin film deposited by nickel plating solution adding 0.1 M KCl and 1 mM KOH.

**Figure 4.6.** (a) The current-voltage characteristics of Au-CdS-Au and pure CdS nanorod measures at dark and under light illumination. The incident white light intensity is 1000 mW/cm². (b) the statistical study of photocurrent of Au-CdS-Au and pure CdS nanorod with a fixed voltage bias of 0.5 V, with 1000 mW/cm² white light irradiation.

**Figure 4.7.** Schematics of the three energy transfer mechanisms from SPR metal to the nearby semiconductor (a) Direct Electrons Transfer (DET). (b) Local Electromagnetic Field Enhance (LEMF). (c) Resonant Energy Transfer (RET).

**Figure 4.8.** Statistical study of the photocurrent distribution of 20 nano-devices with the structure of Au-CdS-Au and Au-Ni/NiO-CdS-Ni/NiO-Au, respectively. The incident light intensity is 1000 mW/cm² and the applied voltage bias is 0.5 V.

**Figure 4.9.** (a) Transient photocurrent measurement for Au-CdS-Au, Au-Ni/NiO-CdS-Ni/NiO-Au, Au-Ni-CdS-Ni-Au and pure CdS single nanorod devices under the applied voltage bias of 0.5 V. (b) Typical I-V characteristics of Au-Ni/NiO-CdS-Ni/NiO-Au measured in the dark, after illuminated for 300 s and after turn off light for different times.

**Figure 4.10.** (a) A typical whole photocurrent damping curve for Au-Ni/NiO-CdS-Ni/NiO-Au nanorod after remove light illumination. (b) Repeating photocurrent change by periodically turn on and turn off light illumination in 30 cycles.

**Figure 4.11.** The model to explain persistent photocurrent in Au-Ni/NiO-CdS-Ni/NiO-Au nanorod device: (a) Energy level diagram for NiO and CdS before they contact. (b) Fermi
level re-alignment and internal electric field formation after contact. (c) movement of holes and electrons upon light illumination.

**Figure 4.12.** The peak photocurrent-incident light intensity relationship in the Au-Ni/NiO-CdS-Ni/NiO-Au single nanorod devices. The applied voltage bias is 0.5 V.

**Figure 4.13.** Demonstration of the “0”, “1” and “2” states in the optically switchable memory device by applying different incident light intensity of 3000 mW/cm² and 10 mW/cm². The former one drove the peak current to 5 µA while the latter one lead to a peak current of 10 nA.

**Figure 4.14.** The damping curves of Au-Ni/NiO-CdS-Ni/NiO-Au single nanorod device which was illuminated to generate different photocurrent by control the incident light intensities. It demonstrates the ability for current memory device to show the multi-addressable characteristics.

**Figure 4.15.** The demonstration of binary information storage system by utilizing the driving factors of peak photocurrent and damping time.

**Figure 4.16.** Experimental and exponential fitted time dependent photocurrent decay curves within (a) $10^0$ s-$10^2$ s. (b) $10^2$ s-$10^3$ s. (c) $>10^3$ s, the solid and dash lines represent the experimental and fitted curves, respectively. (d) The extracted $\tau$ values for different groups of samples within various time horizons. Group 1, 2, 3, 4 and 5 represents samples with peak photocurrent of 1 nA, 10 nA, 100 nA, 1 µA and 5 µA, respectively.

**Figure 4.17.** Schematic diagram to demonstrate the experimental process of optically write the information of “NTU” by eight-bit codes of the American Standard Code for Information Interchange, the inset shows a typical single nanorod device in one single unit.

**Figure 4.18.** The demodulating process of the word “NTU” according to the ASCII codes before illumination, after shined light illumination, and after 5 min, 10 min, 20 min and 30 min from light off.
**Figure 4.19.** (a) The current-time curves illustrating the original state and the write, read and erase process of the Au-Ni/NiO-CdS-Ni/NiO-Au nanorod device on flexible substrate. (b) the cycling performance of Au-Ni/NiO-CdS-Ni/NiO-Au nanorod device on flexible substrate before and after bending for 100 cycles.

**Figure 5.1.** Schematic diagram illustrate the operation and purposed functions of the memristor-based logic circuit. The circuit was established by parallelly connect the optoelectronic memory device to the electric memory device. The logic circuit was proposed to demonstrate three levels of functions: the basic “OR” gate function, the memorable logic gate function (one time input, continuous output) and self-locking logic gate function (output compulsive to be “1” within blocking stage under “1, 1” input).

**Figure 5.2** Schematic illustrating the logic circuit setup by integrate the single nanorod device based optoelectronic memory and the sandwich structure based Ag-ZIF-8-Si electric memory device.

**Figure 5.3** SEM image of Ag-ZIF 8-Si sandwiched memory from (a) cross view and (b) top view of the device arrays.

**Figure 5.4** A typical current-time characteristics for the individual Au-Ni-Au-Ni/NiO-CdS-Ni/NiO-Au-Ni-Au single nanorod device. The device was firstly exposed to 1000 mW/cm² white light for 2 min to reach the peak current. Then the light was turned off and damping process of photocurrent was recorded. The voltage bias was fixed at 0.5 V during the whole measuring process.

**Figure 5.5** A typical current-voltage characteristics for the Ag/ZIF-8/Si memory device in voltage sweeping mode. The compliance current was set to be (a) $1 \times 10^{-3}$ A and (b) $1 \times 10^{-4}$ A for the purpose of prevent device from breakdown and provide a desired ON/OFF ratio.

**Figure 5.6** (a) The HRS and LRS distributions of resistance recorded in different devices. The read voltage was set to be 300 mV. (b) the device to device variation of set and reset
voltage, which are statistically collected from 25 devices. (c) the HRS and LRS switching operations in 30 cycles, with the read voltage of 300 mV. (d) Statistical result for set and reset voltage in 30 measuring cycles.

**Figure 5.7** The characteristics of resistance retention in HRS and LRS at a constant 300 mV read out voltage in $10^3$ s in air, at room temperature. The resistance in different resistance states shows no significant fluctuation.

**Figure 5.8** The logic circuit inputs for “electrical 1, optical 0” and the corresponding output (current) detected.

**Figure 5.9** The logic circuit inputs for “electrical 0, optical 1” and the corresponding detected output current.

**Figure 5.10** The logic circuit inputs for “electric 1, optical 1”. The optical and electrical inputs and the corresponding output current at different points.

**Figure 5.11** Summary of the function of logic circuit constructed by parallelly connect the single nanorod based optoelectronic memory device to the ZIF-8 based electric resistive switching memory. The “OR” logic gate function, the memorable logic gate function and the self-locking logic gate function, were realized in specific scenarios.

**Figure 5.12** Summary of the logic gate functions with the multi-level conductance taken into consideration. (a) The levels of conductivity were re-defined to “2”, “1” and “0”, corresponding to the output current range of $10^{-7}$ A-$10^{-4}$ A, $10^{-10}$ A-$10^{-7}$ A and $<10^{-10}$ A, respectively. (b) the revised truth table with output “2”, “1” and “0”. The electric inputs E1 and E2 represent the set and reset voltage bias, respectively. The “0” and “1” inputs for E2 is defined as apply and not apply the reset voltage, respectively.
Figure 6.1 The examples illustrating factors that can influence the SPR characteristics: (a) the size effect\textsuperscript{[13]}, (b) the aspect ratio effect\textsuperscript{[10]}, (c) the shape effect\textsuperscript{[11]} and (d) the dielectric environment effect\textsuperscript{[12]}.

Figure 6.2 Schematic diagram illustrating the hypothesis of plasmonic logic gate design: the organometallic molecules were firstly assembled to the plasmonic active substrate. The output extinction signal can be detected. By orthogonally tuning the molecular states (open and close), the configuration will change accordingly, result in the dielectric environment variation. Hence, it is proposed that the LSPR spectrum can be shifted under orthogonal stimulations. The plasmonic logic function concept can be demonstrated with such design.

Figure 6.3 The AFM image of nanoparticle array prepared by thermo-evaporation with the ultra-thin AAO membrane as shadow mask.

Figure 6.4 Schematic diagram explaining the whole experimental procedure. The cleaned substrate was immersed into the THF solution in which the organic/organometallic molecules was dissolved. After left in the solution overnight it was rinsed and placed in a cube to apply the light irradiation/electrochemical potential. The extinction spectrum was measured under different molecular states.

Figure 6.5 The chemical structures of the DTE based organic molecule in (a) open state and (b) close state. The molecular switch can be achieved by applying incident light with different wavelength. The open to close state switch can be triggered under 360 nm light irradiation while the reverse switch can be done by applying 650 nm visible light.

Figure 6.6 (a) the extinction spectrum of THF solution with the DTE based organic molecules dissolved. The black curve represent the open (initial) state molecule while the red curve shows the close state molecule. (b) The appearance difference between the two distinct molecular states. The photo on the left hand side is the open state molecule solved in THF solution while the right hand side photo shows the close state molecule in solution.
Figure 6.7 The extinction characteristics of unmodified Au nanoparticle substrate that measured in the dark, and with continuous UV/visible light irradiation.

Figure 6.8 The relationship between Au nanoparticle array thickness and the range of LSPR peak shift in organic molecule modified Au substrate.

Figure 6.9 (a) The SPR characteristics of unmodified Au nanoparticle array (blue), the array with close state DTE based organic molecules assembled (black), and with open state DTE based organic molecules assembled (red). (b) The magnified resonance curve for Au-open state molecule and Au-close state molecule. (c) The repeated SPR shift realized by light illumination. The resonance peak shift back and forth with the change of incident light wavelength.

Figure 6.10 The operation and molecular switching mechanism for the organometallic molecule. The molecular switch from open form to close form can be achieved by applying UV light and/or electrochemical oxidization with subsequent reduction voltage bias, while the reverse switch can be achieved by applying 700 nm visible light.

Figure 6.11 (a) the extinction spectrum of organometallic molecules in liquid state. The black curve represent the open (initial) state molecule while the red curve shows the close state molecule. (b) The appearance difference between the two distinct molecular states.

Figure 6.12 (a) CV scanned in CH$_2$Cl$_2$ solution with 0.2 M Bu$_4$NPF$_6$ for the open form molecule (black curve) and close form molecule (red curve). (b) The switching operation to manipulate the molecular state between o/c$^{2+}$/ c$^+$/c.

Figure 6.13 (a) The LSPR of nanoparticle array with close state ruthenium based organometallic molecules assembled (blue), and after the molecule switched with visible light (red). (b) The repeated LSPR switch with light illumination. The resonance peak shift back and forth with the change of incident light wavelength.
Figure 6.14 (a) The LSPR characteristics detected with open form molecules, and after shined UV light and/or applied electrochemical stimulation to switch the molecule to close state. (b) the repeated LSPR shift with light illumination or electrochemical stimulation. The resonance peak shift back and forth with the change of external inputs. (c) the concept of plasmonic “OR” logic gate, with orthogonal inputs. The output is the LSPR peak position. (d) the output value of plasmonic logic gate in the device tested in above experiment.

Figure 7.1 (a) The structure of floating nanodot gate memory fabricated by CdS FET and Au nanodots. The curves show the $I_{DS} - V_{GS}$ characteristics of device operated under ±1, ±3, ±5 V windows. (b) The read/write/erase operations by applying 5 V and -5 V voltage bias with 200 ms duration$^{[1]}$.

Figure 7.2 (a) The typical I-V characteristics for an Au-CdS-ITO sandwich structure. The CdS was electrochemically deposited on the ITO substrate, and Au layer was evaporated subsequently. (b) The design of Au-Ni/NiO-CdS-ITO sandwiched structure that is expected to demonstrate the logic function.

Figure 7.3 (a) The chemical structure of DAE, with open form and close form. (b) the $I_{DS} - V_{GS}$ characteristics for the open and close form of DAE. (c) the multi-level conductance of device obtained by gradually irradiate the DAE. (d) the $I_{DS}$-time curve for the device measured with 3 ns laser pulse. The current decreased gradually and generated multi-level conductance for 8 bit information storage$^{[3]}$.

Figure 7.4 (a) The circuit design illustrated the concept realization of automatic hierarchical information storage. The optoelectronic memory device will be integrated with electric memory device by series connection. The initial current can be adjusted with incident light intensity. (b) the hypothesis that information can be stored to different levels at different time, and realize the hierarchical storage based on the timeliness of information.
Figure 7.5 (a) The design of bowtie nanoantenna arrays and the process of coating hydrogel. (b) and (c) the SEM images of the Au nanoantenna arrays with and without coating a layer of hydrogel. (d) the reflection measurement under different temperature for the array without hydrogel. (e) the reflection measured by changing temperature on the bowtie nanoantenna arrays with hydrogel coated.

Figure 7.6 (a) The design of tunable gap structure for the purpose of controlling plasmon resonance characteristics. The Au-Ni-Au nanoparticle array structure was fabricated on a glass substrate. The structure was coated with hydrogel and then with the Ni layer etched the gap structure can be tuned with temperature change, which will result in the hydrogel tuned between collapse and swollen state with significant thickness variation. (b) the simulated transmission for the gap size of 10 nm (black) and 50 nm (red). The coupling peak disappears with the gap widening and reappear when it gets narrowed. (c) dimension of the nanostructure for simulation. The period is 460 nm and diameter is 150 nm.
### Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
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<tbody>
<tr>
<td>DTE</td>
<td>Dithienylethene</td>
</tr>
<tr>
<td>HRS</td>
<td>High Resistance State</td>
</tr>
<tr>
<td>LRS</td>
<td>Low Resistance State</td>
</tr>
<tr>
<td>SEM</td>
<td>Scanning Electron Microscopy</td>
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<tr>
<td>AFM</td>
<td>Atomic force microscope</td>
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<tr>
<td>PET</td>
<td>Polyethylene terephthalate</td>
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<tr>
<td>PMMA</td>
<td>Polymethyl methacrylate</td>
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<tr>
<td>EBL</td>
<td>Electron-beam lithography</td>
</tr>
<tr>
<td>PPC</td>
<td>Persistent Photocurrent</td>
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<tr>
<td>SPR</td>
<td>Surface Plasmon Resonance</td>
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<td>LSPR</td>
<td>Localized Surface Plasmon Resonance</td>
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Chapter 1

Introduction

Logic gate was invented by Claude Shannon in 1936 in his Master’s thesis. From that on, the computational operation of Boolean logic was completed. With the development of information technology, several issues need to be settled in order to satisfy the computation requirement. First, the miniaturization of electric circuits is a main trend of modern computing system. Realizing desired logic function at micro and nanoscale is a must to overcome the bottleneck. Second, properly store data in non-volatile memory system to protect time to time electric power off or lost. Third, traditional frequency limitation of silicon based electronics are reached, incorporating new inputs is critical for the computation technology. At the same time, employing orthogonal inputs can significantly extend the application of logic circuit, which has been investigated intensively in the past decades. Finally, although electrical signal dominates the output of conventional logic gate, recent reports introduced optical, chemical and magnetic outputs as promising alternatives for logic circuits development. Taking the general trends into consideration, here in this thesis, the study on non-volatile logic gates with orthogonal inputs (electrical, electrochemical and optical) will be introduced to improve the applicability of logic functions. To well address the data storage issue in real world, components with stable output were used to perform both logic value storage and logic operation.
1.1 Hypothesis/Problem Statement

1.1.1 Memory Devices Based Electronic Logic Gate with Orthogonal Inputs

After logic gate invented by Claude Shannon in 1936 in his Master’s thesis\cite{1}, it was developed quickly and the computational operation of Boolean logic was completed\cite{2}. The current logic gates are mainly operated by involving diodes or transistors to work as electric switches. The seven most common types of logic gates (AND, NAND, NOT, OR, NOR, EOR and ENOR), and their corresponding truth tables, are shown in Figure 1.1.

![Figure 1.1](image)

**Figure 1.1** (a) the seven most common types of logic gates and their logic meanings. (b) the truth table of different types of logic gates.

However, the conventional logic gates did not address the problem of logic value storage, it relies on continuous power supply to finish the logic operation. To solve the data storage issue as well as maintain the logic operation functions, especially at the time of power loss (i.e. when laptop batteries ran out or cell phone turns off)\cite{3}, in recent years people started to consider employing memristor-based nonvolatile
logic circuits. A typical logic function based on memristor is shown in Figure 1.2. It is interesting to note that in such type of logic circuits, the logic operation is realized by integration of individual memristors. Each single memristor act as both logic value storage and logic operation component.

Figure 1.2 Typical logic gates performed by integration of memristors: (a) The AND gate, (b) The OR gate, (c) the NOT gate, (d) the NOR gate and (e) the NAND gate. 

[Diagram of logic gates]
Inspired by this design, the hypothesis of current study starts from employing the memory devices, which are sensitive to both optical and electrical stimuli to realize logic operations. Due to the natural property of memory device, the system output will be independent of continuous power supply. Thus, the logic value storage purpose can be achieved at the meantime of logic operation. Figure 1.3 is the schematic of purposed logic circuit.

Although the electrically switchable memory devices were investigated intensively and lots of materials are readily available\cite{5-10}, the investigation on optically switchable memory devices are still limited, which is the main barrier of engineering the logic gate. The challenges for developing optically controllable memory devices include the limitation of highly sensitive photo-responsive materials and strategy of controlling the duration of photocurrent. Thus, the first step is to find an approach to fabricate the optical memory devices.

Figure 1.3 Proposed design of logic circuit with orthogonal inputs.

The strategy of fabricating optoelectronic memory device is proposed in Figure 1.4. The 1D multi-segmented Au-Ni/NiO-CdS-Ni/NiO-Au nanorod is prepared by electrochemical deposition\cite{11,12}. The electrochemical deposition can allow us to assemble various components and heterogeneous interfaces along the axial direction, and, in turn, engineering the energy band structure along the charge transport pathways\cite{13,14}. Au can enhance the light absorption and prevent the charge recombination in CdS, while CdS has good absorption to visible light\cite{15-17}.
which allow us to achieve significant ON/OFF ratio. Moreover, by controlling the composition of plating solution, the NiO/CdS interface can be successfully formed. The duration of photocurrent can be significantly extend with such design of interface by controlling the migration of photogenerated carriers (see Figure 1.4a), result in a long-time persistent photocurrent, as shown in Figure 1.4b. Thus, the device can be optically switched to low resistance state (LRS) and shows good retention characteristics in a relative long time after illumination removed.

![Figure 1.4](image)

**Figure 1.4 (a)** The schematic to illustrate the design of 1D multi-segmented nanorod heterostructure and the hypothetical electrons/holes migration. (b) the hypothetical photocurrent change upon light illumination and after light off.

With the obtained nanorod device the objective is to design and engineer the electronic logic gate with orthogonal inputs via integration. Regarding to the integration-driven function realization, one example is illustrated in Figure 1.5. The organic photodiode (OPD) and the organic resistive switching devices (ORS) are connected in series to form a circuit, in which the current pass through can be controlled by light illumination. As a result, the current of photodiode is the compliance current of the whole circuit. By tuning the photocurrent of OPD (via controlling the incident light intensity), the resistive switching memory device can be switched to different levels and demonstrated a multi-level data storage system. Inspired by such design our current research aims to develop a system that could be
controlled by multiple stimuli, and employing the logic operation as the output of integrated circuit.

**Figure 1.5** (a) Mechanism of circuit design: upon illumination, the OPD will trigger a redistribution of voltage in the two devices. Meanwhile, the threshold change will cause a non-volatile resistance change in ORS. (b) current-voltage characteristics of OPD under dark and upon light illumination with different incident light intensities. (c) current-voltage characteristics of ORS. (d) current-voltage characteristics of whole circuit under different illumination conditions. (e) the writing process of 16 different resistance states (4-bit) have been demonstrated\textsuperscript{[18]}.

### 1.1.2 Plasmonic Logic Gate with Orthogonal Inputs

The traditional logic computation were dominated by silicon based flow of charges
manipulation\textsuperscript{[19]}. The past improvement of lithography resolution enables the quick development of computation complexity and the speed developed exponentially under Moore’s law. However, after the microelectronic revolution, the electric computation seems to face a bottleneck. With the data intensive information processing nowadays, optical computing is becoming attractive\textsuperscript{[19]}. The system with optical output have three main advantages. First, it allows highly localized information encoding (the transverse spatial resolution limit in optical circuits is roughly the wavelength of the light, which is smaller than 1 μm, so a 1mm\textsuperscript{2} area allows 10\textsuperscript{6} optical elements to be packed in). Second, the fast development of nanophotonics provides an opportunity for revolution in photonics technology, making it possible to precisely create features far smaller than wavelength of light. When conventional scaling in CMOS processors is approaching its physical limits, optical computation may give an alternative for information technology. Third, optoelectronic technologies, including electrical to optical (lasers and modulators) and optical to electrical (detectors) transduction, will be simpler and cheaper (since optical communications have begun penetrating the markets for shorter links in local area networks)\textsuperscript{[20,21]}. Incorporating the source availability, long distance controllability and board applicability\textsuperscript{[22,23]} of optical signal, it could open a new window for information technology development.

One approach to decrease the scale of optical system comes from molecular logic gate. The Boolean logic operation, with the function of AND, OR, XOR, NAND, NOR, INHIBIT, half-adder, and half-subtractor\textsuperscript{[24]}, have been performed on different kinds of molecules. However, for traditional molecular logic gates, there are several key drawbacks. 1) Most of the logic gates are not resettable\textsuperscript{[25]}, which means they are only workable in one time operation. 2) The systems incorporated fluorescent signal as output and small molecules or large biomolecules as input, which increased the complexity of instrument set up and detecting cost\textsuperscript{[25-28]}. 3) A large part of the investigations were performed in liquid state, with the external stimulations such as light irradiation\textsuperscript{[20,30]}, temperature\textsuperscript{[31]} and chemical reaction\textsuperscript{[32]}. In such system, electrical inputs cannot be involved.
Herein the hypothesis is proposed to use orthogonally modulable molecules as switching activator. The suitable nanostructure will be prepared as both the plasmonic-active substrate and electrical contacts, pushing to realize the SPR switch in the solid state. At the meantime, optical and electrochemical inputs can be combined to tune the state of molecules. With the expected shift of LSPR, a plasmonic logic gate can be demonstrated.

In previous studies, the orthogonally switchable organometallic molecules were assembled to the nanogap structure (Figure 1.6) to fabricate the nanodevice$^{33,34}$. Under UV light illumination, the Dithienylethene (DTE) unit can be switched from non-conjugated open state to a $\pi$-conjugated closed state. The reaction is reversible under visible (700 nm) light illumination. More interestingly, combining a ruthenium carbon-reach system, the molecule is able to undergo the radical coupling with electrochemical stimulation. The molecule can be switched from open state to close state with electrochemical voltage bias. Thus, a multi-functional switching mechanism with multicolor optical and electrochromism molecular system has been successfully demonstrated. It is also found that in this system, after molecules immobilized in the nanogap, the device demonstrated tunable conductivity. The open state molecule represents a high resistance state (HRS), while the close state represents low resistance state (LRS). An orthogonally tunable logic gate with electrical output has been achieved.

To illustrate the hypothesis of using this organometallic molecule to prepare orthogonally switchable plasmonic logic gate, the design is presented in Figure 1.7. Firstly, the molecules are modified with one side sulfur linker. To form the Au-S bond it can be assembled to a prepared Au nanoparticle array based substrate. As a result, a plasmonic absorption spectrum can be detected for the Au-organometallic molecule hybrid system. Afterwards, external stimulations, including UV/visible light illumination and/or electrochemical stimulation will be applied to the system, and repeatedly switch the molecules between open state and close state. A resettable logic function with SPR shift as output is expected to be demonstrated.
Figure 1.6 The molecule switch induced nanodevice based logic gates (a) schematic that illustrate the experiment setup. The nanogap structure was prepared by electrochemical approach, the molecules are self-assembled to bridge the gap. (b) switching mechanism for the molecule with one DTE unit and two Ru systems. (c) experimental demonstration of the OR gate with two inputs. The molecule can be switched either by UV light or by electrochemical stimulation. The molecules can be switched back with visible light. (d) switching mechanism for the molecule with two DTE unit and three Ru systems. e) experimental demonstration of the AND/OR gate with three inputs. The molecule can be switched either by UV light or by two steps sequential electrochemical stimulations. The molecules can be switched back with visible light^{34}. 
Introduction

Chapter 1

1.2 Objectives and Scope

This thesis addresses the systematic study of design, fabricate and demonstration of electrical and optical logic gates with orthogonally inputs that have not been achieved previously. It will start from the fabrication of optoelectronic memory device, and illustrate how the memristor-based logic gate can be achieve through integration. For the optical logic gate, the mechanism of molecular switch, experimental setup, and the phenomena detected will be discussed in detail. The thesis will include experimental details, results, discussions and relative theories to make sure all conclusions are experimentally repeatable and scientifically solid.

1.3 Dissertation Overview

The thesis includes seven chapters. The details of contents are listed as following:

Chapter 1 addresses the outline of the overall thesis. Firstly the importance of developing logic circuit with multiple outputs and orthogonal inputs will be explained. Then the illustration of hypothesis of: 1) developing optoelectronic

Figure 1.7 Schematic illustrating the plasmonic logic gate function.
memory device and achieve memristor-based logic gate via integration and 2) developing plasmonic logic gate via orthogonal molecular switching will be presented. The goals and scopes of this investigation are briefly summarized as well.

Chapter 2 gives the literature review on the background of orthogonally controllable logic gate. It will start from reviewing the recent studies which focus on using multiple external stimulations to tune the output of logic circuits. For the electronic logic gate, the recent progress of optically switchable memory devices will be reviewed first, followed by the literatures of memristor-based logic gate investigations to address the hypothesis. For the optical logic gate, the investigations on molecular logic gate will be discussed. And the plasmon resonance shift activated by molecular switching will be review as the fundamental of current research.

Chapter 3 provides the detailed experiment procedures. It will start from introducing the electrochemical deposition strategy, which is the core technology of fabricating the optoelectronic memory devices. The integration of memory devices for logic gate will be explained as well. Lastly, the strategy of fabricating plasmonic-active substrate, assemble organometallic molecules and experiment processes to detect output signal, will be presented.

Chapter 4 systematically studies the fabrication, characterization and demonstration of the optoelectronic memory devices. The detailed experiment to control the interface formation will be discussed. The property and controllability of the optoelectronic memory device will be illustrated with experimental observations. Finally, the potential real world application of such device will be demonstrated.

Chapter 5 provides the details on electronic logic gate with orthogonal inputs via integration. Combining the optoelectronic memory device developed in Chapter 4 and the readily available electrically switchable memory devices, the construction and demonstration of memristor based logic gate will be introduced. The different
functions achieved with single optical input, single electrical input and combination of both will be discussed with experimental observations.

Chapter 6 will systematically study the plasmonic logic gate, starting from molecular switching mechanism. The plasmonic-active substrate will be prepared first. LSPR switching phenomena was detected with illumination in organic molecules and with optical and/or electrochemical stimulation in organometallic molecules. The theoretical basis will also be provided to explain the phenomena.

Chapter 7 will make conclusion for the overall study and make some recommendations for future related works.

1.4 Findings and Outcomes

The investigation of electrical and optical logic gate with orthogonal inputs led to novel outcomes by:

For the first time the optoelectronic self-destructive memory device based on multi-segmented nanorods was successfully developed. It provides a new window for single nanoscale device to demonstrate memory behavior with optical stimulation.

A memristor-based logic gate was developed by integration of optoelectronic and electrical memory devices. This ensures the logic system to be responsive to multiple stimulations. At the meantime, unique functions have been realized.

A plasmonic logic gate was demonstrated by incorporating the multi-responsive organometallic molecules to the plasmonic-active substrate. For the first time it is proved that the plasmon resonance shift can be achieved by tuning the molecular state via orthogonal stimuli.
References

Chapter 2

Literature Review

As discussed previously, with the development of information technology, computational operation of Boolean logic, as a fundamental building block of computer science, is attracting significant attentions. Several scientific and practical questions need to be addressed. First, the non-volatile output is significant to ensure output stability. Second, logic gate with multiple inputs can enhance its flexibility. Third, multiple outputs of logic gates can contribute to the extension of application. Finally, it is desired to achieve the logic functions at micro and even nanoscale to make a breakthrough toward to bottleneck of Moore’s law. In this chapter the recent findings in memristor-based electronic logic circuits and the fundamentals to engineer optical (plasmonic) logic gate will be discussed. The literature review includes the optically switchable memory device, the integration of logic circuits and the molecule level manipulation toward logic function in detail.
2.1 Overview

Logic function is one of the most fundamental operation in computer science. In Chapter 1 the basic logic functions has been introduced. In order to maintain the output stability as well as decrease the reliability to continuous inputs, non-volatile elements should be utilized in the system construction. In this section the relevant studies that could contribute to the current optical and electronic logic gate will be reviewed. The electronical non-volatile logic gate is memristor based. Thus, the background for memristor, especially optically switchable memories, will be introduced. For the optical logic gate, the literature will be separated to the molecular logic gate and molecular switching induced SPR shift.

2.1.1 Memristor-based Electronic Logic Gate

2.1.1.1 Memristor

In 1971, Leon Chua found that there should be six mathematical relations to connect the four fundamental physical variables: current i, voltage v, charge q and magnetic flux $\psi^{[1]}$. Base on the symmetry shown in Figure 2.1a, he predicted that there should be a fundamental element to link the magnetic flux $\psi$ to the charge $q$. In 2008, Williams et al.$^{[2]}$ firstly demonstrate the properties of memristor using titanium dioxide thin film. After that, following resistor, capacitor and inductor, memristor became the fourth fundamental two-terminal circuit element. Williams demonstrated the most common type of memristor-the resistive switching memory. In a typical resistive switching memory, the resistance can be switched between High Resistance State (HRS) and Low Resistance State (LRS) when applying a voltage on the electrodes. Figure 2.1b shows a typical resistive switching memory. By switch the status between HRS and LRS, information can be stored as “0” or “1”. Nowadays, memory device is an essential element in integrated circuits and a core component in data storage.
Figure 2.1. (a) The four fundamental elements to connect six mathematical relations. (b) the current-voltage relationship of a resistive memory device demonstrated in the Pt-TiO$_2$-Pt sandwiched structure$^{[2]}$.

Typically, the mechanism to explain physical resistive switching behavior can be ascribed to two models: filamentary resistive switching and distributed resistive switching$^{[3,4]}$. The former switching model is driven by forming a filament, which is conductive across the insulator or semiconductor. It can be resulted from the metallic ions$^{[3,5,6]}$ or oxygen vacancies$^{[3,7,8]}$ migration under the applied voltage bias. With a positive voltage, the oxidized metallic ions drift under electric field, forming a conductive filament path the make the resistive memory switch to the ON state. On the contrary, with a negative voltage bias, the resistive switching memory goes back to the OFF state under the dissolution along the conductive bridge. The distributed resistive switching mechanism can be explained as the diffusion effect at the interface$^{[9]}$. Basically, the conductive bridge was not completely formed. This phenomena can be activated by a relative low voltage bias, reduces the energy consumption. However, in most cases the device cannot obtain a desired ON/OFF ratio, since the conductivity difference of the device in the two different states are limited. Interestingly, the combination of both switching mechanisms has also been studied, under which a new current–voltage characteristics, was found. In Figure 2.2 the typical I-V characteristics and the schematic illustrating the different kinds of switching mechanisms, are presented.
Figure 2.2 (a), (b) Typical current–voltage characteristics of resistive memory device working under filamentary and distributed switching mechanisms. c) current–voltage characteristics of the resistive switching memory device working with both switching mechanisms. (d), (e), (f) the schematic diagram shows the switching mechanism of filamentary, distributed and combined, respectively \(^4\).

In a typical memory device, the switching mechanisms, either filamentary or distributed, is activated by external voltage bias and has low correlation with the material of switching layer. Thus, in recent years numerous materials were found to demonstrate memory behavior including metal oxide\(^{10-12}\), polymer\(^{13}\), amorphous silicon\(^{14,15}\), carbon\(^{16}\) and bio-materials\(^{17-20}\). Usually, these materials have their own merits in real world application. For example, utilizing the amorphous silicon as switching layer the performance of memory devices can be improved. At the meantime it could extend the application in conventional or hybrid nano/CMOS architectures. For biomaterials, their advantages comes from the low costs, biocompatibility and environment friendly. In Figure 2.3 some kinds of
materials proved to demonstrate the memory characteristics, and their respective performance, are summarized.

![Figure 2.3](image-url)

**Figure 2.3** The structure design and performance measurement results of memory devices prepared by various materials. (a) The representative of metal-oxide based resistive switching memory designed in Pt-TiO$_{2-x}$-Pt sandwich structure$^{[12]}$, (b) the characterization and device performance of amorphous silicon based memory$^{[14]}$, (c) schematic and stability of polymer based resistive switching memory$^{[13]}$, (d) the SEM image and current-voltage characteristics of carbon based memory device$^{[16]}$, (e) The representative of bio-material based multi-level resistive switching memory, prepared by Ag-sericin-Au sandwich structure$^{[19,20]}$.

On top of exploring suitable materials for active switching layer, extending the potential applications by incorporating new stimuli has also attracted rising interests. Traditionally, voltage bias dominates the external stimulus that leading to memory switching. However, once a new stimulus could be utilized to control the
resistive memory, the device application can be extended significantly. The current available publications have already reported magnetic field, temperature, chemical stimulation and light illumination as the new stimulus to tune the characteristics of resistive memory device. In 1997, A. Asamitsu et al.\cite{21} reported the finding of magnetic field intensity tunable memory behavior in Pr\(_{1-x}\)Ca\(_x\)MnO\(_3\) (\(x=0.3\)), which is shown in Figure 2.4a. The temperature dependent CuOx and NiO switching behavior was modeled by Ugo Russo et al.\cite{22}. The switching characteristics varied significantly with the changed temperature (Figure 2.4b). Recently Liu and co-workers\cite{23} demonstrated that in the metal-organic framework (MOF) based electrical switchable memory devices, the performance can be mediated by alcohol and the mechanism was ascribed to the supramolecular interactions between alcohols in the ZIF-crystals (Figure 2.4c).

![Figure 2.4](image_url)

**Figure 2.4** Tunable resistive switching behavior in memory devices by (a) magnetic field\cite{21}, (b) temperature\cite{22} and (c) chemical stimulations\cite{23}.

On top of the above mentioned stimulations, light illumination could also be involved to modulate device performance. More importantly, compare to the
traditional electrical stimulations, light illumination has several unique advantages. First, light is one of the easiest obtained resource in nature. Second, light illumination can be controlled remotely, if a specific travelling path is secured. These merits make it attractive and relevant investigations were performed in recent years. Since it is one of the key building blocks for the current thesis, in the following section the literatures of optically switching memory device will be reviewed separately.

### 2.1.1.2 Optically switching Memory Device

The reported optically switching memory device can be classified into three categories. In the first category, the light illumination was applied to tune the properties, such as set/reset voltage, ON/OFF ratio and I-V characteristics of device. One typical work comes from the DNA based light controllable “write-once, read-many-times (WORM)” memory device. Upon light irradiation the device can be set to LRS as a result of the combined action of light and voltage. However, the device cannot be reset and hence is regarded as WORM memory device. The current-voltage curve and ON/OFF state stability are shown in Figure. 2.5.

![Figure 2.5](image-url)

**Figure 2.5.** (a) I-V curve of device under 1min, 5min and 10min light illumination. Inset: I-V curve measured in the dark. (b) Retention of the ON/OFF states.

Another study, which is more close to the typical and resettable resistive memory device, was reported in 2012 by M. Ungureanu et. al. The Pd-Al₂O₃-SiO₂
structure was engineered to achieve the light controllable resistive switching characteristics. Unlike the previous DNA based device, this memory can be set to LRS and reset to HRS by controlling the voltage bias. Interestingly, this system is responsive to light irradiation. Under UV or IR illumination, the I-V curve changed significantly compare to that measured in the dark. The conductivity of device is correlated to the light intensity. Higher incident light intensity will lead to better conductivity. The schematic and experimental data are summarized in Figure 2.6a. Similar case comes from BiMnO$_3$ nanowire arrays based memory device\[^{28}\]. In the Ag/BiMnO$_3$/Ti structure, the resistance of both HRS and LRS changed according to light illumination (Figure 2.6b).

**Figure 2.6.** Optically controllable memory device based on (a) Al$_2$O$_3$\[^{27}\]. (b) BiMnO$_3$\[^{29}\].

The second category of optical memory device combines both light irradiation and voltage bias to activate the memory behavior. In this area the first finding was
reported by Jinjoo Park et al.\cite{29,30} in 2012, the light controllable resistive memory device was designed based on the ZnO nanorod arrays with Au outer shell. It is interesting that when the experiment was performed without light illumination, the ZnO nanorod arrays presents a typical semiconductor curve, and a classical I-V characteristics appears upon light illumination. The resistive switching mechanism is ascribed to the electrochemical redox process associated with the formation and annihilation of conductive filaments established by the oxygen vacancies\cite{31}.

In the third category of optical memory device, the incident light was used as an information writing tool. This mechanism is completely different from the traditional device, in which voltage bias was used to activate the resistance switch. Typical examples include the ITO/CeO_{2-x}/AlOy/Al junction structure by R. Li et al.\cite{31} and ZnO/SrTiO_{3} (STO) by T. Wu et. al\cite{32}. In the former case, the authors achieved “optically write” and “electrically erase”, which means the resistive memory device can be set by light illumination and be erased by applying a reverse voltage. The latter case was performed on ZnO/SrTiO_{3} (STO) heterostructure, it is interesting to find that in the control experiment, the photocurrent of ZnO and STO quickly return back to the original state, while in the ZnO/STO heterostructure, the photocurrent only decrease 1 order within the same time, resulted in a persistent photocurrent. The persistent photocurrent is the fundamental to establish the optoelectronic memory device. Thus, a more detailed discussion will be presented in Chapter 4.

2.1.1.3 Memristor Based Electronic Logic Gate

With the development of memristor, on top of its natural function of data storage, it has also been developed quickly toward other applications. One of these applications is memristor based logic circuits. Here the current publications are divided into two categories: the first category focus on integrating the memristor into the CMOS circuit, and the logic functions have been presented. The second category engages new stimulation to demonstrate logic operation based on single device.
When the memristor is integrated into CMOS circuit, one outcome can be the stateful logic. One example of stateful logic is material implication (IMPLY) \(^{[33-38]}\). The strategy is to establish the logic circuit in a memristive crossbar array. In this kind of logic circuit, both input and output of the logic gate will be stored. To implement such logic function, voltage activation is required to be performed at different locations of the circuit. **Figure 2.7** is a case of stateful logic based on memristor which was reported by Julien Borghetti et al.\(^{[33]}\) in 2010.

**Figure 2.7.** (a) The Atomic Force Microscope (AFM) image of memristive crossbar array nanocircuit. (b) the ideal current-voltage characteristics of single memristive and the resistive states operation. (c) illustration of IMP operation with two voltage pulses: \(V_{\text{COND}}\) and \(V_{\text{SET}}\), which are applied to switch p and q, respectively. The right side figure shows the truth table for IMP operation. (d) the colored curve shows the voltages applied (blue for p and red for q. The number is the value input, while the results can be read out correspondingly\(^{[33]}\).

On the other hand, to solve the problem that simultaneous voltage pulses need to be performed at different positions of the circuit and at the same time to store the logic value purely based on the dedicated output, memristor-aided logic (MAGIC) has been studied. The MAGIC is a memristors only approach, which means only memristors are involved in the logic circuit. In a MAGIC circuit, the state is
represented as a resistance. The HRS and LRS are corresponding to “OFF” and “ON”, respectively. With the initial logic state works as the input of memristors, the output is the state of whole logic circuit. **Figure 2.8** shows the design of a MAGIC NOR gate constructed with the crossbar array published by Shahar Kvatinsky et al.\textsuperscript{[39]}. The two-inputs gate with NOR logic function can be achieved in row i, where two inputs, in1 and in2 are utilized as the starting state in columns j+1 and j, respective. Column j−1 is the output. Within the crossbar, the schematic is shown in **Figure 2.8b**. The voltage was applied at the gateway V\textsubscript{0}, while column j−1 is connected to ground.

![Figure 2.8. MAGIC gate with NOR function in a crossbar array\textsuperscript{[39]}.](image)

There are several differences between stateful logic gate and MAGIC logic gate. Firstly, the stateful (IMPLY) logic gate requires addition electronic components (i.e. resistor) while MAGIC is purely memrisistor based. Secondly, the IMPLY gate cannot separate input and output, while it can be achieved in MAGIC logic. Lastly, the MAGIC logic gate has an advantage of logical completion, while IMPLY logic
requires the writing of 0 (FALSE requirement) to a memristor for NOR operation. \textbf{Table 2.1} is a summary of the comparison.

\begin{table}[h]
\centering
\begin{tabular}{|c|c|c|}
\hline
 & \textbf{IMPLY} & \textbf{MAGIC} \\
\hline
No. of voltages & 2 ($V_{SET}$, $V_{COND}$) & 1 ($V_{th}$) \\
Separate input and output & No & Yes \\
Basic functions & IMPLY (+ FALSE) & OR, AND, NOR, NAND, NOT \\
No. of memristors for NOR/NAND & 3 (+ a resistor) & 3 \\
No. of clock cycles for NOR/NAND & 4 & 2 \\
Within memory & Yes & Yes (for NOR) \\
Logically complete & Requires FALSE & Yes (NOR, NAND) \\
\hline
\end{tabular}
\caption{Comparison between IMPLY and MAGIC memristor based logic gate\cite{39}.}
\end{table}

Both the two types of memristor based logic gates are designed and operated based on electrical memory devices. Hence, the circuit outputs relies on the electrical inputs (voltage). Moreover, the studies are closely related to the design of CMOS. From materials science view, there are also efforts to employ a new stimulus and explore the application of single device. One example comes from Mirko Prezioso et al.\cite{40}, whom reported the magnetically tunable memory device based logic gate. The device was fabricated by Tris(8-hydroxyquinoline)-aluminium(III) (Alq3) and was operated with spin-polarized electrodes. Due to the giant magnetoresistance (GMR) effect, the device is responsive to both magnetic and electrical inputs. When the applied voltage reaches the threshold, the GMR effect can be destroyed. As a result, an implication (IMP) logic function can be demonstrated in a single memory device. The output value is “0” only when the device is operated with magnetic input and without electrical input. In all other cases, the output is 1. \textbf{Figure 2.9} summarized the device design, device performance and truth table of this single memory based logic gate.
Figure 2.9. (a) Schematic diagram illustrating the device design and operation. From top to bottom, it is constructed with: Co ferromagnetic electrode, a thin layer of AlOx tunnel barrier, the Alq3 organic semiconductor and the La0.7Sr0.3MnO3 ferromagnetic electrode at the bottom. (b) the resistance measured with different magnetic field intensity under various voltage. A high enough voltage bias can destroy the GMR effect. (c) the resistance and GMR under different voltage. (d) and (e) demonstration of the implication (IMP) logic function in this device\[^{[40]}\].

To summarize, in this section the latest development of memristor has been reviewed. To extend the application of the fundamental element, different investigations were performed, especially on exploring new stimulations that are able to control the device performance. The optoelectronic memory device, as an
important component in the current thesis, has been reviewed separately. Lastly, to address the memristor based logic function, currently there are lots of studies to integrate memristor into CMOS and demonstrate different logic output. At the meantime, people are also paying efforts to exploring memory device based logic function in single circuit. Applying orthogonal inputs to the memory device (or circuit) could help to develop new solutions. In Chapter 4 and Chapter 5. The study on developing optoelectronic memory devices and incorporating the orthogonal inputs to the circuit, and in turn, realizing logic operations, will be presented.

2.1.2 Fundamentals for Nanoscale Optical Logic Gate

As mentioned in Chapter 1, the hypothesis is to combine the plasmonic-active substrate and the orthogonally tunable molecules to develop a system that is responsive to multiple inputs. In order to engineer the optical (plasmonic in specific) logic gate, there are two core problems need to be settled. First, the design requires a molecule that is multi-responsive. Second, the hypothesis aims to develop a new kind of output, which is plasmon resonance. Thus, the solution needs to be developed in order to integrate the molecules to the plasmonic platform. Following this logic, in this section firstly the relevant investigations on molecular logic gate will be reviewed. After that the strategies to tune SPR properties by combining antennas in the hybrid system, will be introduced.

2.1.2.1 Molecular Logic Gate

The molecular logic opens a new window to perform logic functions at nanoscale, which is its most important strength compare to the larger semiconductor system. In reality, although the semiconductor based logic gate has been well established, the molecular computation is also matured nowadays. Importantly, it is somehow difficult to define molecular logic based on the same criteria as that for semiconductor because naturally there are lots of differences on the input and output of them\cite{41,42}. Typically in a semiconductor logic system, the output should be “0” or “1”, corresponding to different states of electric parameters (i.e.
resistance). However, in molecular logic, the output varies in a broad range. It can be fluorescence\(^{43-45}\), current\(^{46-48}\), color change\(^{49-51}\) and so forth. In Figure 2.10 the reagent, condition, substrate and readout of molecular logic is presented.

**Figure 2.10.** The mimic computational process with molecular logic. The currently available substrates are summarized, the chemical reagent and/or testing environmental conditions which is able to influence the output are listed. Similar to the traditional semiconductor based logic gate, the molecular logic gate can response to a number of different inputs and generate output. Unlike the electronic logic, the output can vary in a broad range\(^{52}\).

Basically, in molecular logic gate, people can program different logic functions by controlling the inputs. For example, Roger M. Pallares et al.\(^{53}\) demonstrated multiple logic gate platforms by binding estrogen receptors (ERs) to the dsDNA on the gold nanorods. At the meantime, two different kinds of human ER (ER\(_\alpha\) and ER\(_\beta\)) were incorporated in the experiment. Determined by the sequential interactions between ERs and dsDNA, the platform can perform six different kinds
of logic functions (OR, NOT, IMPLY, BUFFER, TRUE and FALSE), as shown in Figure 2.11b. Additionally, integrating single logic gate unit the system can perform complex logic functions. For example, combining the above mentioned OR and NOT single logic gate, the NOR logic operation can be realized, as shown in Figure 2.11c. Note that in this study the logic output can be controlled by properly select the base solution and additives.

![Figure 2.11](image)

**Figure 2.11.** (a) The schematic diagram illustrating the fundamental OR logic gate, which is established by combination action of dsDNA-AuNRs and ERs. Controlling the interaction of ERs and dsDNA the logic operation can be realized. (b) The output of different logic functions is the ratio of absorption intensity at 510 nm and 885 nm. Controlling the operation of inputs, the logic functions can be demonstrated as OR, NOT, IMPLY, BUFFER, TRUE and FALSE. (c) The integration of single OR and NOT logic function to demonstrate the NOR logic operation[53].

Based on the information from Figure 2.10, it can be observed that the molecular logic gate can start with various inputs and generate different outputs. In this thesis, the main focus is to incorporating orthogonal inputs to generate output. A desired candidate must be multi-responsive toward this objective. Thus, below the organometallic molecules will be introduced, especially on its molecular state logic
operation. In the work reported by Liu et al.\cite{54}, the organometallic molecules, which includes carbon-rich ruthenium and diarylethene (DTE) units, have been synthesized. The DTE unit is an ideal candidate for the photochromic switching between the non-conjugated structure (open state) and \( \pi \)-conjugated structure (close state). At the meantime, the carbon-rich ruthenium complexes have excellent ability to promote the coupling of metal centers and the organic ligands when they are combined into the system. Hence, in theory, the molecular switch can be achieved by optical and/or electrochemical stimulations. In Figure 2.12a the operation to activate molecular switch is shown. With 350 nm UV irradiation, or applying an oxidation and subsequent reduction voltage bias, the molecule can be switched to the \( \pi \)-conjugated close form. The process is reversible when a 700 nm visible light illumination is applied. The molecular switch can be proved by the UV-vis absorption spectra change. For the molecules in open state, the absorption peak appears at around 346 nm while the peak for close form is around 652 nm. More interestingly, the molecular switch can generate four different states by precisely controlling electrochemical stimulation. The \( 1o, 1c, 1c^{2+} \) as well as the \( 1c^+ \) states, can be achieved under different oxidation and reduction operation, which can be seen in Figure 2.12c.

Based on the switching mechanism of the organometallic molecules, in 2014, Meng et al.\cite{55} assembled the molecules into the nanogap structure which was fabricated using the on-wire lithography approach. The engineered molecular device underwent the electric measurement. The light illumination and the electrochemical stimulation were applied to the nanodevice. With the repeated switching of molecular states, the conductivity of device went back and forth, forming the “0” state (high resistance state) and “1” state (low resistance state), respectively. Interestingly, the molecule based nanodevice demonstrate the two inputs OR logic function and three inputs AND & OR logic function, as shown in Figure 1.5. This is a case that utilize the molecular logic function to generate logic operation in molecular electronics.
Figure 2.12. (a) The schematic explains the molecule switch operation. The four different states: 1o, 1c, 1c\(^{2+}\) and 1c\(^{+}\), can be achieved by applying different stimulations. (b) UV-Vis spectroscopy of the on state molecule and the off state molecule, explaining the wavelength to drive switch. (c) the CV curve of 1o state molecules under two consecutive scans and the close state molecules. (d) UV-Vis-NIR spectroscopy of different states by applying specific electrochemical stimulations\(^{[54]}\).

2.1.2.2 Controlling Plasmon Resonance by Modulating Molecular Antenna

Surface plasmon resonance (SPR) is the resonant oscillation of conduction electrons at the interface between negative and positive permittivity material activated by incident light. When surface plasmon is confined to a size that is comparable to the wavelength of light, the free electrons of particle participate in the collective oscillation, result in localized surface plasmon (LSP). Two important effects of LSP are: 1) the electric fields near the surface of can be enhanced significantly, the enhancement is greatest at the surface and rapidly falling off with
distance. 2) the extinction of particle optical reaches maximum at the plasmon resonant frequency, for noble metals it occurs at the wavelength of visible light\[^{56}\]. There are several factors that could influence the LSPR properties. These factors include: size\[^{57,58}\], aspect ratio\[^{59-61}\], shape\[^{62}\] and dielectric environment\[^{63}\]. In Chapter 6 a detailed discussion will be provided.

One of the strategy to shift the plasmon resonance is to form a layer of molecular antenna on the plasmonic-active substrate. With the switching of molecular states the SPR of modified plasmonic platform can be tuned. A generally accepted explanation for this phenomena is that the dielectric environment changed with the molecular switch\[^{64,65}\].

Before the finding of molecular switch driven SPR shift, the SPR characteristics tuned by conductive polymer was reported. Verena Stockhausen et al.\[^{66}\] reported the giant plasmon resonance shift in their system which combined the Au nanoparticle arrays and poly(3,4-ethylenedioxythiophene) (PEDOT). Controlling the electrochemical stimulation, the PEDOT switched between oxidization state and reduction state. As a result, the SPR peak was tuned significantly. The explanation was related to the variation of dielectric function and supported by numerical studies. Another case comes from Yann Leroux et al.\[^{67}\]’s publication. Their investigation was based on the Au nanoparticle arrays, which were covered by a layer of polyaniline (PANI). Similarly, by oxidizing and reducing the PANI, SPR peak of the hybrid structure shifts accordingly. Moreover, it is found that under different electrochemical voltage bias, the plasmon resonance can be tuned gradually, as shown in Figure 2.13b.
Figure 2.13. (a) Extinction spectra of gold particle measured in air (black), after coated with a layer of PEDOT film with oxidized state (blue) and after coated with a PEDOT film with reduced state[66]. (b) The plasmon resonance shift under different electrochemical stimulations. The inset illustrate the operation for plasmon resonance switch of the Au nanoparticle arrays on ITO substrate, and covered by PANI[67].

On top of realizing SPR switch by electrochemically tuning the states of conductive polymer, another approach is to use single layer molecules. The variation of molecular states could result in conformational change of molecules. As a result, the dielectric environment varies and SPR characteristics shifts accordingly. Compare to the conductive polymer layer, the SPR shift resulted from molecular switch is generally weaker. However, the advantage is that the system can be operated at nanoscale. In recent years, a number of studies have been reported on the switchable molecules coated nanostructures. External stimuli, such as chemical reaction and light illumination, were applied to the system. The SPR change can be detected by controllably tune the molecular state.

The molecular switching stimulations include the chemical reaction and light illumination. One typical case of the chemical reaction induced SPR variation was performed on the bistable rotaxanes covered Au nanodisk arrays[68], as shown in Figure 2.14a. For the molecules in ground state of $1^{4+}$, the ring of CBPQT$^{4+}$ will have higher affinity and prefer to reside at the tetrathiafulvalene (TTF) station. However, with oxidation of TTF, the CBPQT$^{4+}$ will lose the affinity for the TTF$^{2+}$ (oxidized state), and moves close to the dioxynaphthalene (DNP) station. This will
result in completely different electronic properties and absorption characteristics, which is shown in Figure 2.14c. Upon oxidation, the Au-molecule hybrid system showed a 9.5 nm red shift for the SPR peak, and the variation is reversible.

Figure 2.14. (a) Structure and electrochemical switching mechanism of the dithiolaneterminated bistable rotaxane (b) schematic diagram illustrating plasmon resonance shift with different states of molecules. (c) extinction of molecule before (green) and after (red) the TTF station oxidation. (d) numerical calculation of extinction and refractivité change corresponding to (c). (e) and (f) extinction spectra of Au-molecule and Au nanodisk systems for the initial state, before and after oxidation[68].
For the latter type, the molecular switching mechanism is based on the photo switchable units in the molecules. Two categories of molecules can undergo such state switch. For the first category of molecules, the isomers are stable for both states. The different molecular states can be achieved by various incident light wavelength. Typical examples of such kind of molecules is dithienylethenes (DTEs). For the second category, one of the molecular state is metastable, and the state can exist only when incident light with specific wavelength is continuously provided. The examples of such kind of molecules include azobenzenes (AB) and spiropyrans (SPs). In Figure 2.15, the wavelength induced molecular switch for DTE, AB and SPs, are summarized.

![Figure 2.15](image)

**Figure 2.15.** The operations to induce molecular switch by controlling the incident light wavelength in (a) azobenzenes (AB), (b) spiropyrans (SPs) and (c) dithienylethenes (DTEs).

Interestingly, after modifying the plasmonic active substrate with photo switchable molecules, the SPR shift can be detected according to specific light illumination condition. One example in this area is from Gayatri K. Joshi et al. The azobenzenes were attached to the gold nanoprisms. With photoisomerization the azobenzenes switch between the cis and trans states. The SPR extinction spectrum changes with the molecular switching operation. With trans state azobenzenes, the
SPR shift toward longer wavelength while it shows blue shift as a result of the molecule switch back to cis. In a cyclic testing, the LSPR peak shifted back and forth, a 21 nm peak shift was detected in the repeatability measurement procedure. The effects of azobenzene conformational change was explained as the reason of SPR shift. For cis and trans states there are 0.6 nm difference in thickness, this will result in local dielectric environment variation and contributed to the SPR shift. The enhanced resonance energy transfer between the Au nanoprisms substrate and the attached azobenzene with trans conformation is considered as another contribution to red shift.

![Figure 2.16. (a) Schematic diagram shows the azobenzenes bonding to the gold nanoprisms and switch between cis and trans states under UV light and blue light illumination. (b) SPR extinction spectrum for Au-molecule hybrid structure. The red curve shows the situation for molecule in trans state while the green one represent the state in cis. (c) The LSPR peak shift by repeatedly tune the molecular states[64].](image)

**Figure 2.16.** (a) Schematic diagram shows the azobenzenes bonding to the gold nanoprisms and switch between cis and trans states under UV light and blue light illumination. (b) SPR extinction spectrum for Au-molecule hybrid structure. The red curve shows the situation for molecule in trans state while the green one represent the state in cis. (c) The LSPR peak shift by repeatedly tune the molecular states[64].

### 2.2 Questions to answer based on literature-electronic logic gate

Based on the literature review mentioned above, people developed different approaches to employ new stimuli on top of voltage bias to control the
characteristics of memory devices. Especially, the optically switchable memory devices have been discussed in detail. However, there are still questions that are open to be answered and new applications pending to be explored.

First, optical memory device is switched with the enhancement of photocurrent driven by external light illumination. Is it possible to employ SPR active metals in the nanostructure, and as a result, to enhance the photocurrent and achieve desired properties in the memory device?

Second, the memory devices developed in previously studies were all binary devices in which the resistive switch and information storage were realized between “0” state and “1” state. In order to improve the information storage capacity, multi-addressable characteristics can be employed and properly utilized. Hence, is it possible to achieve perfectly distinguishable multiple states in the system?

Third, traditionally, the memory devices are operated based on the “read-write-erase” process. The information can be erased by applying a reverse voltage bias or UV light. However, the process is selective. Here the open question is that whether it is possible to develop a “compulsorily” erase mechanism, under which the information erase happens spontaneously and the memory device can act as both information storage and information protection component?

Finally, the memory devices based electronic logic gate has been reviewed. The question is that whether people can perform the logic operations based on orthogonal inputs?

The first three questions focus on the strategy of developing optically switchable memory devices, while the last one aims to extend the potential applications by combining the optoelectronic memory device and electrical memory device.
2.3 Questions to answer based on literature-optical logic gate

Based on the literatures reviewed above, it can be found that the logic operations can be realized at molecular level. Various approaches were applied to tune the states of molecules and in turn, achieving different outputs. Meanwhile, it has also been reviewed that after incorporating external stimulus tunable molecules to the plasmonic-active substrates, people can detect SPR shift with tuning molecular states. Thus, one potential question in this section is that whether the “molecular logic operation” and “molecular switch induced SPR shift” can be integrated. On one hand the objective is to find out a molecule that is responsive to multiple external stimulations, and is able to demonstrate logic operation. On the other hand, combining the molecules to the plasmonic-active substrate, whether the multiple stimulations induced SPR shift can be demonstrated?

2.4 PhD in context of literature

In the current thesis, the realization of logic function at micro and nanoscale will be systematically investigated. The logic functions with stable electrical and optical output will be studied. The main contributions are as following.

First, the self-destructive optoelectronic memory device will be established based on multi-segmented single nanorod device. In this memory device, the SPR effect from noble metal will be combined into the photo-sensitive semiconductor in order to enhance the photocurrent. As a result, a more desired ON/OFF ratio can be achieved. Meanwhile, with controllable engineering of the segments along the axial of 1D nanorod, the migration of electrons and holes can be controlled so that the recombination of electron/hole pairs can be prohibited. As a result, the photocurrent can be maintained and demonstrate information storage characteristics. Of course, due to the spontaneous process that the photocurrent will eventually return to the initial state, it demonstrates the concept of “self-destructive” memory characteristics as well.
Second, the optoelectronic memory device was parallel connected to the electrical memory device to ensure the logic circuit is sensitive for orthogonal inputs. Under various external stimulations the circuit output can be tuned accordingly. As a result, unique logic functions have been demonstration under different combinations of stimulations (electrical only, optical only or both). Especially, due to the unique characteristics demonstrated in optoelectronic memory device (the automatic and compulsory erase mechanism), the logic circuit can demonstrate the self-locking characteristics.

Finally, the organometallic molecules will be attached to the plasmonic-active substrate. The molecular states can be tuned by light (UV) illumination, electrochemical oxidation/reduction cycle or both. With the molecular state variation the LSPR will shift accordingly. An “OR” logic function with plasmonic output has been demonstrated at nanoscale. This is the first time that multiple stimulations were applied to tune the SPR characteristics.

References


Chapter 3

Experimental Methodology

In this chapter, the design, preparation and characterization methodology of both electrical and optical logic gate with orthogonal inputs will be introduced. For the electronic logic gate, it will start from the fabrication of optically switchable memory device. The devices were fabricated by electrochemical deposition in an anodic aluminum oxide (AAO) membrane. Followed by the photolithography and e-beam lithography the single nanorod based memory device can be prepared. Finally, the single nanorod based device will be parallelly connected to a ZIF-8 based electrically switchable memory device to demonstrate the logic function. In the optical logic gate, firstly the ultra-thin AAO membrane is utilized as a template. The thermo-evaporation process was taken to fabricate the plasmonic-active gold nanoparticle arrays thereafter. Finally, the organometallic molecules were self-assembled to the surface of nano-arrays. Under external orthogonal stimulations (electrochemical and optical) the plasmonic logic functions can be demonstrated at nanoscale.
3.1 Rationale for Selection

The explanation of rationale of selection will be started from the key focus of nanostructure fabrication in order to achieve desired properties. For the electronic logic gate, as mentioned in Chapter 1 and Chapter 2, optically stimulated memory device is the key component while the investigations in this area is still limited currently. To keep the photocurrent after external stimulation removed, and thus store information in a persistent time horizon, the recombination of electron/hole pairs would be prohibited. In this way, the engineering of material interface is critical.

Figure 3.1. (a) SEM image of an Au-Ni/NiO-CdS-Ni/NiO-Au device, the red dash line is the scanning trace of EDX analysis. (b) EDX elemental line-scanning analysis of a single Au-Ni/NiO-CdS-Ni/NiO-Au nanorod.

In the current study, the self-destructive optoelectronic memory device will be prepared based on Au-Ni/NiO-CdS-Ni/NiO-Au single nanorod heterostructure, as shown in Figure 3.1. The 1D multi-segmented nanorod structures can allow people to assemble various components and heterogeneous interfaces along the axial direction, and, as a result, engineering the energy band structure along the charge transport pathways\textsuperscript{1,2}. Au is able to enhance the light absorption and prevent the charge recombination in CdS\textsuperscript{3-5}, while CdS has good absorption to visible light\textsuperscript{6,7}. Moreover, by controlling the composition of plating solution, the NiO/CdS
interface can be formed, which ensures the electrons and holes movement to be controlled via the design of Fermi level. As a result, the recombination of electron/hole pairs can be restricted.

For the optical logic gate with orthogonal inputs, the experiment was performed on an organometallic molecules modified plasmonic-active substrate. The key components include the substrate and molecules. As the output will be detected from UV extinction, the substrate needs to satisfy two requirements: 1) the individual nanoparticle should have relative small size so that the extinction peak before and after shift could be comparable. Thus, the technologies such as photolithography, which engineers micro-size array should be avoided, as shown in Figure 3.2, and 2) the plasmonic-active substrate should be fabricated in large scale in order to ensure the detectability. Thus, small area manufacturing strategies, such as e-beam lithography, can be excluded. In the current study, ultra-thin AAO template based thermo-evaporation was selected. Applying this methodology\cite{8,9}, the gold nanoparticle arrays can be prepared on 2cm*2cm area using a single step approach. At the meantime, since the electrochemically fabricated AAO membrane has relatively homogenous pore size, the desired homogenous nanostructure can be manufactured. The details will be discussed in the following sections.

![Figure 3.2](image.png)

**Figure 3.2.** (a) The gold particle array fabricated by photolithography with diameter of 5 μm (b) The board extinction peak made it difficult to compare SPR shift between various molecular states.
3.2 Preparation of electronic logic gate with orthogonal inputs

The fabrication of electronic logic gate includes two steps:

1) To engineer single nanorod base optoelectronic memory device.

2) To parallelly connect the optoelectronic memory device to a traditional electrical memory device.

In short, the fabrication of single nanorod device includes electrochemical deposition in an AAO membrane, followed by photolithography to prepare the micro-electrode and e-beam lithography to fabricate the nanodevice. The electrical memory device was prepared on an Ag-Metal–Organic Framework (MOF)-Si sandwiched structure. Finally, the two memory components were parallelly connected in order to receive external orthogonal inputs.

3.2.1 Method to fabricate single nanorod based optoelectronic memory device

The process starts from electrochemical deposition of 1D nanorod heterostructure in a commercially available AAO membrane\textsuperscript{[10-12]}. The process is summarized in Figure 3.3. The anodic aluminum oxide (AAO) membrane is used as the template. Firstly, the membrane was evaporated with 300 nm silver thin layer on the back side in order to make it conductive (Figure 3.3a). Then the AAO is immersed in the plating solution and taking sequential electrochemical deposition. The Pt electrode is taken as counter electrode while Ag/AgCl acts as reference electrode. In the first step, a thick layer of Ag is deposited in order to make sure the following layers grow within the pores (to calibrate the roughness between the conductive Ag layer and the pores). After that, the Au, Ni/NiO and CdS segments can be deposited accordingly. The applied voltage for Ag, Au, Ni/NiO and CdS are -800mv, -900mv, -850mv and -2500mv, respectively\textsuperscript{[13]}. The length of each segment can be controlled by limit the charge quantity. 2500 mC, 3000 mC, 10000 mC and 6000
mC are the charge quantify for 1μm length of Ag, Au, Ni/NiO and CdS, respectively. When the plating solution is changed to deposit the next segment, carefully rinse the pool and Pt counter electrode is needed. It is worthy to note that in the Ni segment depositing process, 1 mM KOH and 0.1 M KCl were added to the Ni plating solution in order to obtain the Ni/NiO, the detailed mechanism of NiO forming will be discussed in Chapter 4. Prior to the electrochemical deposition of CdS, the solution was heated to 85°C and use magnetic stirring to fully dissolve the sulfur[14].

![Figure 3.3](image)

**Figure 3.3.** (a) AAO membrane with silver back layer. (b) protocol of electrochemical deposition along AAO membrane. (1) commercially available AAO template. (2) sliver layer evaporated on the back side of AAO membrane. (3) sacrificial silver layer deposited in order to make sure the connection to the evaporated backing is clean. (4) deposit multi-segment nanorods in sequence. (5) remove the Ag layer, solve the AAO membrane and get dispersed nanorods.

The backing Ag layer on AAO membrane can be removed by methanol: hydrogen peroxide: ammonium hydrogen solution=4:1:1 solution. After that the membrane
is placed in 3 M NaOH solution for 1h to solve the template. Then rinse the sample 3 times by DI water and 3 times by ethanol, the nanorod solution can be successfully prepared.

In the nanodevice fabrication procedure, the two ends of nanorod need to be connected to the external electrode in order to test the electronic properties. Two powerful and widely-used nanofabrication techniques, photolithography and electron beam lithography (EBL), were taken in sequence to achieve such objective.

![Photolithography Process](image)

**Figure 3.4.** (a) Schematic of photolithography fabrication of micro-electrodes. (b) the micro-electrodes pattern prepared following the steps shown in Figure 3.4a, the inset is the magnified microscope image of single electrode pattern.

Photolithography is taken to fabricate the outer layer of microelectrode. The process includes three steps. Firstly, the silicon wafers with 600 nm SiO$_2$ were sonicated in acetone and ethanol for 30 min, respectively. After dried by N$_2$ the wafers were spin coated a layer of AZ1518 photoresist. The speed of spin coater was 500 rpm for 5 s and 3000 rpm for 45 s. Then the wafers were dried in an oven for 3 min at 95 °C. Secondly, the wafers with photoresist were exposed to UV light using a mask aligner (SUSS MJB4 Mask aligner) and developed using AZ319 MIF, the developing time was 20 s. At last, 10 nm Cr and 100 nm Au was evaporated on the
wafer. Afterwards the wafers were immersed into acetone solution for 1 h for liftoff. The photolithography process and the prepared micro-electrodes are shown in Figure 3.4.

After obtaining the microelectrode pattern, the electrochemically deposited nanorods were casted onto the silicon wafers with prefabricated electrodes using a droplet. Briefly, the suspension of nanorods prepared by electrochemical deposition was diluted 100 times. 5μL of diluted solution was transferred from the tube to a piece of silicon wafer (with microelectrodes). At the meantime the wafer is placed on an oven (55 ℃) to accelerate the evaporation of ethanol. After drying the suspension of nanorods, single nanorod will be spread on the surface of silicon wafer. Then a layer of 950 C7 PMMA with about 1 μm thickness was spin coated on the chips. The speed of spin coater was 500 rpm for 5 s and 3000 rpm for 45 s. After spin coating the wafers were placed on an oven for 4 min at 180 ℃. E-beam lithography was taken subsequently on a FESEM (JEOL JSM-7600SEM, Tokyo, Japan), connected by the Raith SEM lithography kits at 20 kV accelerating voltage and 94 pA beam current (note that the e-beam lithography is selective, only single nanorod at a proper position will be connected to the microelectrode). After developed with 1:3 MIBK/IPA solution for 15 s and immersed in IPA solution for 15 s, the substrates were evaporated by 10 nm Cr and 500 nm Au. After remove the PMMA by acetone and dry the substrate by N2, the nano-devices were successfully prepared. Figure 3.5 is the schematic of e-beam lithography and the device obtained.
Figure 3.5. (a) Schematic of e-beam lithography. (b) the Au-Ni-Au-Ni/NiO-CdS-Ni/NiO-Au-Ni-Au single nanorod heterostructure device engineered using the procedure in Figure 3.5a.

On top of the nanodevices engineered on silicon wafer, the process can also be taken on the transparent and mechanically flexible Polyethylene terephthalate (PET) substrate. The key notifications of PET based device fabrication are: 1) During the spin coating process both for photolithography and e-beam lithography, the mechanically bendable substrate should be hold on an flat substrate to avoid any strains. 2) After spin coat a layer of 950 C7 PMMA on the flexible substrate, before taking e-beam lithography, a layer of 15 nm Au should be evaporated on the surface. This is because the electron beam will cause serious strain on the surface of PET and the writing path will change accordingly without protection. With a thin layer of gold the PET surface became more rigid to perform e-beam lithography. After patterning, the gold layer can be removed with I₂/KI solution. The developing and PMMA removal process is same with that on the common silicon wafer. Figure 3.6 shows the patterns on the PET substrate which was prepared by photolithography and the nanodevice on flexible PET engineered with e-beam lithography.
3.2.2 Logic Function Realization

The logic function was realized by parallelly connect the above mentioned single nanorod based optoelectronic memory device to an Ag-MOF (ZIF-8)-Si\textsuperscript{[15-17]} sandwiched structure based electrical memory device. The ZIF-8 based memory device was engineered as follows: first, a rigid conductive silicon wafer was selected as the substrate. Si substrates were cleaned in the H\textsubscript{2}SO\textsubscript{4}:H\textsubscript{2}O\textsubscript{2}=3:1 piranha solution for 45 min, followed by rinsing in DI water and subsequent drying with N\textsubscript{2}. The wafers undergoes oxygen plasma for 3 min. Afterwards 25 mM of Zn(NO\textsubscript{3})\textsubscript{2} •6H\textsubscript{2}O and 50 mM of 2-methylimidazole methanolic stock solutions, which was prepared in advance was used. The silicon wafers were immersed into the mixed solution for half an hour at room temperature for ZIF-8 film growth purpose. Finally, the samples were rinsed with methanol, dried with N\textsubscript{2}. At last, a 150 nm silver layer was evaporated on the top surface of film with a shadow mask to fabricate the top electrode. In Figure 3.7 the structure of ZIF-8 based memory device is presented.

The prepared ZIF-8 based electrically switchable memory device was connected to the single nanorod based optoelectronic memory device to form a circuit, the brief setup schematic is shown in Figure 1.3. The circuit got power supply from the
probe station (Keithley 4200-SCS). Due to the parallel connection, the voltage on ZIF-8 based electrically switchable memory equals to the nanorod based optoelectronic memory device. With consistent power applied on the circuit, a 300W xenon lamp provides light illumination on the optoelectronic memory device. The output of logic circuit are monitored with multiple external stimuli.

![Figure 3.7](image)

**Figure 3.7.** The schematic illustrating the ZIF-8 based memory device. The Ag patterns, ZIF-8 and Si act as top electrode, switching layer and bottom electrode, respectively.

### 3.3 Fabrication of optical logic gate with orthogonal inputs

The optical logic gate with orthogonal inputs will be engineered with two steps:

1) Fabricate plasmonic active substrate in a relative large area, and with relatively homogenous arrangement.

2) Assemble the organic molecules, which is responsive to optical stimulation, and the organometallic molecules, which is responsive to orthogonal external inputs, to the surface of arrays prepared in step 1.
3.3.1 Method to fabricate plasmonic-active substrate

The plasmonic-active substrate was fabricated using thermo-evaporation, with an ultra-thin AAO membrane covered on the Indium Tin Oxide (ITO) surface. The period, pore diameter and thickness of membrane are 125 nm, 80 nm, and 130 nm, respectively. The AAO membrane was purchased from a company, the manufacturing details can be found in previous publication[8].

The AAO membrane need to be transferred to the ITO substrate surface and then undergoes thermo-evaporation. Figure 3.8a illustrates the process. First, the 3 cm*1 cm ITO pieces were cleaned by sonicating in acetone, ethanol and DI water for 30 min, respectively. After dried by N2 the substrates undergoes oxygen plasma for 3 min, the power was 30%, in order to make the surface hydrophilic. The AAO membrane was hold on a PMMA and was free-standing initially. After that DI water droplet was spread on the ITO surface, and placing the AAO membrane (with PMMA holder) on the substrate. After drying with filter paper half of the membrane was immersed in acetone solution for 3 min. Then the sample was taken out of acetone, dried in air, rotated for 180°. Then the rest half of sample was immersed into the acetone solution for 3 min. After the PMMA completely dissolved the sample was dried in air and repeatedly cleaned in acetone solution for 3 times. Finally, the AAO membrane can be closely attached to the surface of ITO substrate. Figure 3.8b shows the SEM image of ITO substrate with AAO covered on the surface.

The ITO substrate with AAO membrane then underwent the thermo-evaporation. During the evaporation, the gold particles pass through the pores and attached to ITO surface. After evaporation the AAO membrane was removed using a tape. In the current experiment, 20 nm gold particles were deposited. Figure 3.8c shows the nanoparticle arrays obtained. To find out the optimal parameter for detecting SPR peak shift, 40 nm, 60 nm and 80 nm particles were also prepared for control experiment.
Figure 3.8. (a) The experimental procedure of AAO membrane with PMMA holder transferred to the ITO substrate, followed by PMMA solving, thermo-evaporation and removal of membrane. (b) the SEM image of ultra-thin AAO membrane covered on the surface of ITO. (c) the nanoparticle arrays obtained after thermo-evaporation. The inset is magnified image of the relatively homogenous nanoparticle arrays.

3.3.2 Assembly of organic/organometallic molecules

The organic/organometallic molecules were self-assembled to Au nanoparticle arrays, forming Au-organic/organometallic molecules hybrid structures, and demonstrate the logic functions at nanoscale. The detailed information of molecule synthesis will be discussed in Chapter 6. Figure 3.9 shows the chemical reaction for the self-assemble process. Stable chemical reaction between plasmonic-active Au nanoparticle arrays and the organic/organometallic molecules can be formed by the Au-S bond\(^{18,19}\). The molecules were modified with thiol ends in one side which work as anchor group. The self-assembly process is as following: the prepared substrate with Au nanoparticle arrays underwent the oxygen plasma for 3 min, the
Experimental Methodology

power was 30%, in order to clean the surface and remove contaminations. After that the substrate was rinsed by ethanol and dried with N₂. At the meantime 10 mL degassed tetrahydrofuran (THF) solution was prepared, with molecules dissolved in advance. The substrate was immersed into the THF solution overnight, under N₂ protection. NH₄OH (28% of NH₃, 5 μL) was dropped into the THF solution in order to deprotect the thiol. At last, the sample was taken out of the solution, rinsed with THF and ethanol, and dried with N₂.

![Figure 3.9](image)

**Figure 3.9.** The chemical reactions to form covalent Au-S bond between Au and (a) organic molecule, (b) organometallic molecule.

3.4 Characterization and experimental setup for logic performance measurement

3.4.1 Characterization and electrical measurements for the single nanorod device and electronic logic gate

The nanorod structures were observed under FESEM (JEOL JSM-7600SEM, Tokyo, Japan). The elements of nanorod are analyzed using EDX analysis software on the same equipment.
The electrical performance (i.e. the current-voltage and current-time relationship) of nanorod based optoelectronic memory device and the electronic logic gate, was measured on a probe station (Keithley 4200-SCS). The light illumination was applied with a 320W xenon lamp. The incident light intensity was determined by applying a light intensity meter. **Figure 3.10** shows the Keithley 4200 and HAL-320W xenon lamp applied in the current equipment.

![Figure 3.10](image)

**Figure 3.10.** The (a) Keithley 4200-SCS and (b) HAL-320W xenon lamp used in current experiment.

### 3.4.2 Characterization and Measurements for Optical Logic Gate

The plasmonic active Au nano-arrays were observed under FESEM (JEOL JSM-7600SEM, Tokyo, Japan). The morphology was characterized by Atomic Force Microscopy (AFM) (PiroPlus from Molecular Imaging, Agilent Technology). The absorption spectrum was collected from the UV-Vis spectrophotometer (UV-2550, SHIMADZU, **Figure 3.11**). To switch the molecules from open state to close state, a 360 nm band pass filter was applied to HAL-320W xenon lamp, and the illumination lasted for 30 min. The electrochemical switch for organometallic molecules was taken with the Pt electrode as counter electrode, Ag/AgCl as reference electrode and ITO as working electrode. For the reverse step, a 650 nm/700 nm band pass filter was applied to HAL-320W xenon lamp and the sample was irradiated for 1 h in order to switch the molecules back to open state.
Figure 3.11 UV-Vis spectrophotometer used in current study to collect extinction spectrum from the Au-organic/organometallic molecules hybrid structure.

References


Chapter 4

Optoelectronic Self-destructive Memory Device Based on Multi-segmented Nanorods

As discussed in previous chapters, it is critical to develop the optically switchable memory device in order to achieve the memory device based logic function with orthogonal inputs. Currently a large amount of investigations on electrically switchable memory devices, regarding to the switching mechanism, materials selection and the performance improvement can be found. However, studies on the optically controllable memory device is still limited. One of the key motivation to develop the optoelectronic memory device comes from the natural merits of light. For example, it can be controlled to travel through a path with long distance. It also has high availability. Such advantages makes the optoelectronic memory devices highly applicable in information storage. Here in this chapter, the latest studies in optically switchable memory device will be introduced. The motivation for this study will be discussed thereafter. More importantly, the experimental design will be introduced and the results will be discussed in detail. Finally, as an important prospective of real world application. The self-destructive memory device function will be demonstrated. The rationale of how it can be used to temporarily storage information, and at the meantime, demonstrate the function of information protection, will be presented.
4.1 Introduction

Nowadays, memory device is a fundamental element in integrated circuits and a core component in data storage. Typically, in a resistive switching memory, the resistance can be switched between High Resistance State (HRS) and Low Resistance State (LRS) when applying a voltage on the electrodes. Although light illumination has some unique advantages compared to electric inputs, currently the investigations in optically switchable memory device is limited. Two reasons cause that the development of optically controllable memory device still challenge and they will be discussed in detail.

First, to successfully engineer an optoelectronic memory device, the photocurrent must be kept after the external stimulation disappeared. However, compare to the matured switching mechanism in electrically activated memory device, such as filament\([1-4]\), the strategy to keep photocurrent after remove the external illumination, is still under exploration. People got inspired from the persistent photocurrent (PPC) phenomena, which means that the current of semiconductor increases upon light illumination, but after light off the current does not return back to the original dark current in a relative long period. This phenomena was observed in 1979 in GaAs\([5]\), after that several semiconductors or heterogeneous interfaces, such as GaN nanowires\([6]\), silicon nanomembranes\([7]\), AlGaAs/GaN\([8]\) as well as SrTiO\(_3\)/LaAlO\(_3\)\([9]\) were reported to demonstrate the PPC properties. Two main mechanisms are responsible for the PPC phenomenon: (1) the electron/hole pairs are separated by the macroscopic potential barrier generated by junctions, surface barriers or doping inhomogeneities\([5]\). (2) There are potential barrier at the center with large lattice relaxation, so the empty defect level lies above conduction band while the occupied defect level lies between the band gap\([10]\). A typical damping curve of SrTiO\(_3\)/LaAlO\(_3\) is shown in Figure 4.1, it can be observed that more than 50% of the initial current can be kept 24 h after light off. In theory, the materials with PPC phenomenon are perfect candidates to fabricate optically written resistive memory device.
However, unfortunately the current naturally existing PPC materials are not quite responsive to light illumination. Upon illumination they cannot provide a desired ON/OFF ratio to ensure the memory device have sufficient resolution. Compare to the electrically switchable memory device, in which plenty of materials, such as metal oxide\cite{11-13}, polymer\cite{14}, amorphous silicon\cite{15,16}, carbon\cite{17}, bio-materials\cite{18-21} etc, was proved to be suitable materials in device fabrication. The selectivity of high sensitive photo-responsive materials is quite limited. Therefore, it is a challenge to make the device switch to a different state that can be distinguished from original state, this is the second reason that limited the optically switchable memory device fabrication. Based on current available studies, people demonstrated the phenomena of “photocurrent storage” in ZnO nanorod arrays with Au outer shell\cite{22,23}, ITO/CeO$_2$–x/AlOy/Al junction structure\cite{24} and ZnO/SrTiO$_3$\cite{25} nanorod array heterogeneous interface. In the above mentioned studies, the challenges were at least partially solved. Figure 4.2 is a summary of these studies.

**Figure 4.1** The decay curve of photoconductivity after light off in SrTiO$_3$/LaAlO$_3$ heterogeneous interface\cite{9}.
Figure 4.2 (a) ZnO/SrTiO$_3$ nanorod based optically switchable memory device, after light removal, the photocurrent can be kept for a long time. (b) ZnO nanorod arrays based memory device, without light irradiation, the device performs typical semiconductor characteristics. Under light illumination, it demonstrates memory behavior. (c) ITO/CeO$_{2-x}$/AlO$_y$/Al based memory. The device can be optically written and information can be erased by applying a reverse voltage bias. However, the ON/OFF ratio is not desired.

Figure 4.2 (a) shows the case performed on ZnO nanorods/SrTiO3 heterostructure. The I-T characteristics shows that unlike the sharp increase and quick damping of photocurrent in a typical photo-sensitive semiconductor, the heterostructure demonstrate a persistent photocurrent when the light turns off. The mechanism was ascribed to that upon illumination the holes and trapped electrons in oxygen
vacancies move toward the interface under the driving force of electrical field and presence of macroscopic potential barrier\textsuperscript{[26]}. Both the captured holes and the ionized oxygen vacancies have long lifetimes because of their large effective mass and low mobility, and their slow drifting back to the original states leads to the occurrence of PPC.

The second example is demonstrated on the ZnO nanorod arrays coated with Au shell. The memory characteristics forms upon light illumination and with the external voltage bias provided on the electrodes. It is explained that the illumination induced desorption of the O$^{-x}$ ads from the ZnO NR surfaces. The O$^{-x}$ ads ions can be attracted or repulsed with positive or negative voltage applied to the top electrode, result in the formation and breaking of conductive filament layer\textsuperscript{[2,27]}. As a result, upon illumination the typical memory characteristics was presented.

The last example was realized in ITO/CeO$_{2-x}$/AlOy/Al junction structure. The device shows “set” operation with illumination, while a negative voltage bias could result in the “reset” of device. When the device being exposed to optical illumination, trapped electrons can be excited and swept away by the build-in electric field, leaving the oxygen vacancies to intensify the band bending at the interfacial region and at the same time facilitate the charge transport across the junction with a thinner Schottky barrier. On the contrary, when a negative electrical-field applied to the device, electrons will be injected into the interfacial region again and support the recovery of initial energy band, result in the current drop back to initial state\textsuperscript{[24,28]}.

Inspired by the available studies and in order to further develop such device, here our objectives include: 1) Demonstrate the SPR enhanced photocurrent: a high ON/OFF ratio is quite important because it could extend the effective working time of memory device. The current available optically switchable memory devices are all fabricated based on the photoconductivity of semiconductors. Although incorporating SPR metal into semiconductors the photocurrent and enhance
photocurrent have been reported in a lot of publications\textsuperscript{[29-31]}, there is no one reported the use of SPR as a tool to optimize the memory performance. Thus, here in this chapter one of the innovations is to utilize SPR effect to enhance the photosensitivity, and in turn, improve the device performance. 2) Exploring multi-addressable memory device function: traditional information storage is based on the binary system of “0” and “1”. In such system the information storage capacity is $2^n$. Suppose multi-level conductance in memory device is developed, the information storage capacity can be enhanced to $m^n$, where $m$ is the number of achievable resistance states. Obviously, there will be a huge increase in the information storage capacity. Currently the optically written memory device can only achieve 2 different states (although there is publication to report multi-level conductance, the actual resolution of is weak). In the current project the multi-addressable characteristics will be illustrated as one of the key innovations. 3) Demonstrating the “self-destructive” function: in a typical memory device, the information can be erased by applying a reverse voltage bias or UV light. The merit of such erase method is obvious, that is, the information removal can be controlled. People can erase information whenever it is needed. However, in some other cases such erase methodology is not the best choice. For example, when there is a confidential document and the information is expected to be compulsively removed by the provider, self-destructive function will be a more effective solution. The self-destructive function is particularly attractive with people’s increasing attentions to privacy, which can be supported by the fast development of Snapchat\textsuperscript{[32]}. As a proof of concept for confidential information protection, the “self-destructive” memory concept, in which the information erase is a spontaneous and compulsory process, will be demonstrated.

This chapter will start from the materials and methods to introduce the device fabrication procedure. Followed by the detailed experimental results discussion. Finally, the potential application of “self-destructive” memory device will be demonstrated.
4.2 Materials and Methods

4.2.1 Electrochemical Deposition of Nanorods

The studied devices were fabricated by electrochemical deposition using an anodic aluminum oxide (AAO) as a template. The detailed fabrication process has been introduced in Chapter 3. The nanorod diameter, component composition, length as well as the sequence can be precisely controlled using this strategy. After electrochemical deposition the backing Ag layer was removed by methanol: hydrogen peroxide: ammonium hydrogen solution=4:1:1 solution, and the template was solved by 3 M NaOH solution. A subsequent drop casting step ensures the spread single nanorods distributed on the silicon wafer with photolithography prepared micro-electrode. Afterwards e-beam lithography will be taken to connect the single nanorod to the micro-electrode, then the devices are ready to undertake electric measurement. Figure 4.3 shows the schematic of device fabrication.

![Fabrication strategy of multi-segmented nanorod devices by electrochemical deposition and the subsequent e-beam lithography.](image)

Figure 4.3. Fabrication strategy of multi-segmented nanorod devices by electrochemical deposition and the subsequent e-beam lithography.
4.2.2 Nanorod Device Characterization

In the electrochemical deposition step, 9 segments Au-Ni-Au-Ni/NiO-CdS-Ni/NiO-Au-Ni-Au nanorods were fabricated. The outer Au segments were deposited for the purpose of connecting to the micro-electrode (circuit formation), while the intermediate Ni segment was used to separate the two Au segments as well as to isolate the SPR effect from the long Au segment. Hence, the effective segments of the device in the current study are the 5 segments Au-Ni/NiO-CdS-Ni/NiO-Au. The Au segment was made for employing the SPR effect and enhance the photocurrent. The Ni/NiO/CdS interface was engineered to control the migration of photogenerated carriers at the interfaces, the electrons/holes movement and mechanism for photocurrent maintaining will be discussed later.

The diameter of nanorod is 300 nm. The length of Au and CdS segments are both 200 nm, the rationale for selecting the size of Au and CdS segments was based on the publication by Wang and co-workers[^35], in which numerical study suggested that the electric fields around the CdS could gain the strongest enhancement when both the lengths of Au and CdS segments were 200 nm. The length of Ni/NiO segment is 100 nm. The length of specific segments was determined based on the linear relationship between the charge quantity applied during electrochemical deposition and the length of deposited materials[^33]. For the current AAO template (Whatman Inc. 0.02μm, 47-mm outer membrane diameter), depositing 1μm Au, Ni(Ni/NiO) and CdS requires 3000 mC, 10000 mC and 6000 mC charge quantity, respectively. For the control experiment, the Au-CdS-Au and pure CdS nanorods were also prepared, in order to compare the photocurrent achievable with and without SPR effect. The SEM image of Au-Ni-Au-Ni/NiO-CdS-Ni/NiO-Au-Ni-Au, Au-Ni-Au-CdS-Au-Ni-Au and Au-Ni-CdS-Ni-Au nanorods are shown in Figure 4.4.
Figure 4.4. SEM images of (a), (b) Au-Ni-Au-Ni/NiO-CdS-Ni/NiO-Au-Ni-Au, (c), (d) Au-Ni-Au-CdS-Au-Ni-Au and (e), (f) Au-Ni-CdS-Ni-Au nanorod devices prepared by electrochemical deposition followed by electron-beam lithography (EBL). (a), (c), (e) are the images for devices connected to microelectrodes while (b), (d), (f) are the magnified images for the inner, effective segments.

4.2.3 Controlling the Formation of Interface

Importantly, it is worthy to note that the NiO/CdS interface should be formed for the purpose of control the migration of photo-generated carriers. The normal Ni...
electrochemical deposition process is based on the bath composition of NiSO$_4$·6H$_2$O, NiCl$_2$·6H$_2$O and H$_3$BO, and Ni segment is the reduced from Ni$^{2+}$. In order to form NiO, in the deposition process, 1 mM KOH and 0.1 M KCl were added to the Ni plating solution. The mechanism of forming NiO in the Cl$^-$ and OH$^-$ concentrated plating solution should be ascribed to: 1) the corrosion of Ni surface in the OH$^-$ and Cl$^-$[36] and 2) the Ni composition undergoes the following chemical reacting under surplus OH$^-$ and at a potential lower than 0.7 V$^{[37-40]}$

\[ \text{Ni(OH)}_2 \rightarrow \text{NiO} + \text{H}_2\text{O} \]

Or \[ \text{Ni(OH)}_2 \rightarrow \text{NiOOH} + \text{H}^+ + \text{e}^-, \text{NiO} + \text{OH}^- \rightleftharpoons \text{NiOOH} + \text{e}^- \]

The X-ray photoelectron spectroscopic (XPS) measurements were performed to investigate chemical compositions of prepared samples. The Ni 2p and O 1s spectrums of electrochemically deposited thin film before adding KOH/KCl are shown in Figure 4.5 (a), (b), while that of samples deposited with KCl and KOH are shown in Figure 4.5 (c) and (d). In the sample that deposited without Cl$^-$ and OH$^-$, Ni is chiefly presented in the form of Ni(0) and Ni$^{2+}$[41,42]. In the film deposited with Cl$^-$ and OH$^-$, it is clearly observed that the Ni$^{2+}$ peak was significantly intensified. Moreover, the Ni 2p peaks shifted toward higher binding energy for about 0.5 eV. Indicating more serious oxidation of the thin film$^{[43]}$. It is worthy to note that in the O 1s spectrum of deposited thin films, after adding Cl$^-$ and OH$^-$ to the plating solution, a new peak presented at around 529.5 eV, which is corresponding to the Ni-O bonding$^{[44]}$, which indicates the formation of NiO in the electrochemical deposition process.
4.3 Principle Outcomes

4.3.1 Surface Plasmon Resonance Enhanced Photocurrent

There are two key motivations for employing SPR active Au segments and thus enhance photocurrent of CdS based nanorods. Firstly, with higher photocurrent, the device can achieve better ON/OFF ratio and improve the device performance. Secondly, with higher ON/OFF ratio, it contributes to better demonstrate the multi-addressable characteristics since more conductance levels are achievable. As a result, the information storage capacity can be improved accordingly.
Figure 4.6a shows a typically current-voltage characteristics of Au-CdS-Au and pure CdS nanorod, both with and without white light illumination (1000 mW/cm²). With similar dark current, it is obvious that the Au-CdS-Au nanorod has much higher photocurrent than pure CdS nanorod. In Figure 4.6b the statistical analysis of photocurrent shows that with Au segments, the photocurrent can be enhanced for 1-2 orders, indicating that significant photocurrent enhancement can be achieved with SPR effect.

![Figure 4.6](image)

Figure 4.6. (a) The current-voltage characteristics of Au-CdS-Au and pure CdS nanorod measures at dark and under light illumination. The incident white light intensity is 1000 mW/cm². (b) the statistical study of photocurrent of Au-CdS-Au and pure CdS nanorod with a fixed voltage bias of 0.5 V, with 1000 mW/cm² white light irradiation.

The mechanism of SPR enhanced photocurrent can be ascribed to three aspects. First, SPR metal can extend the absorption of whole system to longer wavelength. Second, SPR metal can increase the light scattering. Third, exciting electron/hole pairs in the semiconductor by transferring the plasmonic energy from the metal to the semiconductor\cite{45}. Among these mechanisms, the energy transfer theory is closely related to the material selection and nanostructure design. Thus, it will be discussed in detailed.
Figure 4.7. Schematics of the three energy transfer mechanisms from SPR metal to the nearby semiconductor (a) Direct Electrons Transfer (DET). (b) Local Electromagnetic Field Enhance (LEMF). (c) Resonant Energy Transfer (RET).

Based on the study by Wu et al.\textsuperscript{[46]}, energy transfer from SPR metal to semiconductors follow three models, which are illustrated in Figure 4.7. The first energy transfer mechanism is Direct Electrons Transfer (DET) (Figure 4.7a). In this model, the electrons can be directly transferred from SPR metal to the conduction band of semiconductor. The first evidence of DET was reported by Yang et al.\textsuperscript{[47]}. They doped Au and Ag nanoparticles on the TiO\textsubscript{2} nano-porous and found the systems was responsive to visible light. The potential change and IPCE versus wavelength curves are in accordance with the absorption of Au and Ag. It is worthy to note that only when the SPR metal and semiconductor are in direct contact can the electrons be transferred from metal to semiconductor by DET model.

DET is not the only mechanism for energy transfer. Some publications reported that the photocatalysis efficiency still can be improved when there is an isolating layer between SPR metal and TiO\textsubscript{2}. Thus, it is believed that the Local Electromagnetic Field Enhance (LEMF) is the main mechanism for such phenomenon\textsuperscript{[48-51]} (Figure 4.7b). The enhanced electromagnetic field caused by SPR effect can better separate the electron/hole pairs and prevent their recombination. But there are two points worthy to be noted. Firstly, this model is effective only when the energy of incident
light is higher than the band gap. Second, the efficiency of LEMF decays exponentially with the distance between metal and semiconductor\[49\].

On top of DET and LEMF, Resonant Energy Transfer (RET) is the third existing energy transfer mechanism\[52,53\] (Figure 4.7c). Based on this model, the energy can be transferred from the dipoles of SPR metal to the electron/hole pairs in semiconductor. The perquisite of RET is that the metal and semiconductor have overlapped absorption spectrum.

In the current study, the pure CdS achieved ON/OFF ratio of $10^3$-$10^4$, while with SPR effect, it can be enhanced to $10^5$-$10^6$. This is a pronounced result among the photo-sensitive materials. In Table 4.1 the ON/OFF ratio of different photo-sensitive materials is summarized. It can be seen that the ON/OFF ratio varies significantly, depending on the material and designed structure. Generally, CdS is an attractive candidate to drive huge photocurrent due to its good absorption to incident visible light. Meanwhile, the 1-D nanorod structure usually has good performance regarding to the ON/OFF ratio due to the large specific surface area\[54\]. Additionally, in the current study, the structure of single nanorod device ensures the DET (Au and CdS are in direct contact), LEMF (the incident light is white light which is able to separate electrons and holes in CdS) and RET (Au and CdS have overlapped absorption spectrum) effects to work together and enhance the photocurrent, result in the largest ON/OFF ratio among the studies for optically switchable memory device. Larger ON/OFF ratio will benefit the performance of memory device as discussed above.
Table 4.1. Performance summary of nano-photodetectors and memory devices.

<table>
<thead>
<tr>
<th>Material</th>
<th>Structures</th>
<th>ON/OFF Ratio</th>
<th>Memory Behavior</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZnS</td>
<td>Single Nanobelt</td>
<td>$\sim 10^7$</td>
<td>N</td>
<td>[55]</td>
</tr>
<tr>
<td>ZnO</td>
<td>Single Nanowire</td>
<td>$\sim 6$</td>
<td>N</td>
<td>[56]</td>
</tr>
<tr>
<td>CdSe</td>
<td>Single Nanowire</td>
<td>$\sim 10^2$</td>
<td>N</td>
<td>[57]</td>
</tr>
<tr>
<td>CdSe</td>
<td>Single Nanorod</td>
<td>$\sim 3 \times 10^4$</td>
<td>N</td>
<td>[58]</td>
</tr>
<tr>
<td>CdS</td>
<td>Single Nanobelt</td>
<td>$\sim 6$</td>
<td>N</td>
<td>[59]</td>
</tr>
<tr>
<td>CdS</td>
<td>Single Nanowire</td>
<td>$\sim 5 \times 10^4$</td>
<td>N</td>
<td>[60]</td>
</tr>
<tr>
<td>CdS</td>
<td>Aligned Nanowire</td>
<td>$\sim 2 \times 10^2$</td>
<td>N</td>
<td>[61]</td>
</tr>
<tr>
<td>ZnO</td>
<td>Nanowire Network</td>
<td>$\sim 7.5$</td>
<td>N</td>
<td>[62]</td>
</tr>
<tr>
<td>Ge</td>
<td>Nanowire Network</td>
<td>$\sim 5$</td>
<td>N</td>
<td>[63]</td>
</tr>
<tr>
<td>Cu$_2$O</td>
<td>Nanowire Network</td>
<td>$\sim 0.5$</td>
<td>N</td>
<td>[64]</td>
</tr>
<tr>
<td>Bi$_2$S$_3$</td>
<td>Nanowire Network</td>
<td>$\sim 24$</td>
<td>N</td>
<td>[65]</td>
</tr>
<tr>
<td>Zn$_2$GeO$_4$</td>
<td>Nanowire Network</td>
<td>$\sim 4$</td>
<td>N</td>
<td>[66]</td>
</tr>
<tr>
<td>CeO</td>
<td>Sandwiched Structure</td>
<td>$\sim 10-10^2$</td>
<td>Y</td>
<td>[24]</td>
</tr>
<tr>
<td>ZnO</td>
<td>Nanorod Array</td>
<td>$\sim 10^4-10^5$</td>
<td>N</td>
<td>[25]</td>
</tr>
<tr>
<td>ZnO/SrTiO$_3$</td>
<td>Nanorod Array</td>
<td>$\sim 10^3-10^4$</td>
<td>Y</td>
<td>[25]</td>
</tr>
<tr>
<td>CdS</td>
<td>Single Nanorod</td>
<td>$\sim 10^3-10^4$</td>
<td>N</td>
<td>Current Work</td>
</tr>
<tr>
<td>Au-Cds-Au</td>
<td>Single Nanorod</td>
<td>$\sim 10^5-10^6$</td>
<td>N</td>
<td>Current Work</td>
</tr>
<tr>
<td>Au-Ni/NiO-Cds-Ni/NiO-Au</td>
<td>Single Nanorod</td>
<td>$\sim 10^5-10^6$</td>
<td>Y</td>
<td>Current Work</td>
</tr>
</tbody>
</table>

Admittedly, it is noted that in the current study, the intermediate Ni/NiO segment separated the Au and CdS segments, which can weaken the SPR effect that generated from LEMF and RET models. To study the weakening effect, the statistical investigation was taken, and the results are shown in Figure 4.8. With the same incident light intensity and applied bias, the geometric mean of
photocurrent achieved in Au-CdS-Au (4.43*10^7 A) is 2.4 times as the one in Au-Ni/NiO-CdS-Ni/NiO-Au (1.86*10^7 A). The Au-Ni/NiO-CdS-Ni/NiO-Au can also achieve 10^5-10^6 current magnification by shining white light, result in good performance of memory device.

Figure 4.8. Statistical study of the photocurrent distribution of 20 nano-devices with the structure of Au-CdS-Au and Au-Ni/NiO-CdS-Ni/NiO-Au, respectively. The incident light intensity is 1000 mW/cm^2 and the applied voltage bias is 0.5 V.

4.3.2 Controllable Persistent Photocurrent for Optoelectronic Memory Device

In order to verify the hypothesis that by engineering NiO/CdS interface in the 1-D nanorod heterogeneous structure, the photocurrent can be maintained even after remove illumination, the electric measurement was performed on Au-Ni-Au-Ni/NiO-CdS-Ni/NiO-Au-Ni-Au, Au-Ni-Au-Ni-CdS-Ni-Au-Ni-Au, Au-Ni-Au-CdS-Au-Ni-Ni-Au as well as Au-Ni-CdS-Ni-Ni-Au nanorods. Figure 4.9 shows the testing results. Firstly the nanorod devices were exposed to white light, after the photocurrent gradually get saturated (100 s in this case) the light was turned off. The dynamic cyclic performance was measured. It can be observed in Figure 4.9a that upon light illumination, the photocurrent enhanced sharply in all nanorod devices. Especially, as a result of the SPR effect, the Au-CdS-Au, Au-Ni/NiO-CdS-
Ni/NiO-Au and Au-Ni-CdS-Ni-Au nanorod devices achieved ON/OFF ratio higher than $10^5$, while the ON/OFF ratio of pure CdS nanorod was around $10^3$. After remove the light irradiation, the current of Au-CdS-Au, Au-Ni-CdS-Ni-Au and pure CdS quickly drop back to the dark current. However, in the Au-Ni/NiO-CdS-Ni/NiO-Au nanorod, although the device responded to light off, unlike the quick decay observed in the other devices, the photocurrent only dropped less than 2 orders within the same time, indicating the photocurrent was maintained without continuous stimulation. Figure 4.9b is the current-voltage characteristics of Au-Ni/NiO-CdS-Ni/NiO-Au nanorod device initially, after illumination and after light off for different times. The current decreased with time past, but becoming slower with time gone. After 2h the photocurrent is still about 2 orders higher than the initially state, indicating that the information is distinguishable with the original state.

Figure 4.9. (a) Transient photocurrent measurement for Au-CdS-Au, Au-Ni/NiO-CdS-Ni/NiO-Au, Au-Ni-CdS-Ni-Au and pure CdS single nanorod devices under the applied voltage bias of 0.5 V. (b) Typical I-V characteristics of Au-Ni/NiO-CdS-Ni/NiO-Au measured in the dark, after illuminated for 300 s and after turn off light for different times.

To thoroughly study the persistent photocurrent in the current nanodevice, its whole photocurrent damping curve and the repeatability of photo-sensitivity was recorded. Figure 4.10a shows a typical damping characteristics of Au-Ni/NiO-CdS-Ni/NiO-Au nanorod device. The devices took over $5 \times 10^4$ s to return back to the dark current.
After $10^4$ s the current is still perfectly distinguishable with the initial state, indicating the good retention of resistive switching memory properties. The cycling performance is shown in Figure 4.10b, in which the external light illumination was repeatedly turned on and off. The photocurrent variation is stable among different cycles responding to the light on and off operation.

![Graph](image)

**Figure 4.10.** (a) A typical whole photocurrent damping curve for Au-Ni/NiO-Cds-Ni/NiO-Au nanorod after remove light illumination. (b) Repeating photocurrent change by periodically turn on and turn off light illumination in 30 cycles.

The persistent photocurrent phenomena in ZnO was explained to be related to the desorption and subsequent re-absorption of surface oxygen species,[67] and oxygen species induced forming and breaking of filament layer.[22] Here the oxygen species induced PPC can be ruled out since the PPC phenomenon both present in air and in vacuum. A more convincing explanation comes from the migration of photo-generated carrier with the influence of electrical field.[25] Based on this theory here the mechanism is proposed by the schematic in Figure 4.11. Figure 4.11a shows the positions of conduction band and valence band for the CdS and NiO. The positions of conduction band and valence band of NiO are -4 eV and -7.5 eV,[68] while that for CdS are -4.1 eV and -6.5 eV,[69] respectively. The positions of Fermi level for NiO and CdS are -6.5 eV and -4.3 eV, respectively. After contacting NiO with CdS, there will be an internal electrical field formed as a result of the realignment of Fermi level (see Figure 4.11b). Upon light illumination, the
electron/hole pairs will be separated. The electrons will move toward anode, while the holes will move toward the interface to seek for the recombination with the trapped electrons in space charge region (Figure 4.11c). Due to the large mass and low mobility of holes, they have a long lifetime. The photocurrent damps with their slow drifting back, result in the persistent photocurrent.

**Figure 4.11.** The model to explain persistent photocurrent in Au-Ni/NiO-CdS-Ni/NiO-Au nanorod device: (a) Energy level diagram for NiO and CdS before they contact. (b) Fermi level re-alignment and internal electric field formation after contact. (c) movement of holes and electrons upon light illumination.

### 4.3.3 Controllable Multi-addressable Characteristics

Traditionally, the information storage is performed by a typical resistive memory device with binary systems of “0” and “1” states. The information storage capability is \(2^n\), where \(n\) is the number of unit. With the rapid development of information technology, high-density data storage is required. Multi-level conductance is a desirable solution toward this objective because creating a new state can significantly increase the information storage capacity\[^{70,71}\]. By developing a “2”
state the capacity can be increased to $3^n$. With more different states to be created, the capacity can be even larger ($m^n$).

Here the demonstration of resistive memory device with multi-level conductance, driven by different incident light intensity, is presented. First it is assumed that CdS, as a classical photo-sensitive material, has good absorption to photons so that the photocurrent will not be saturated in a specific range. Thus, the relationship between incident light intensity and peak photocurrent was measured. In **Figure 4.12** it can be observed that the log10 of photocurrent of nanodevices is roughly linear correlated to the log10 of incident light intensity, leading to several distinguishable peak photocurrent.

![Graph](image)

**Figure 4.12.** The peak photocurrent-incident light intensity relationship in the Au-Ni/NiO-CdS-Ni/NiO-Au single nanorod devices. The applied voltage bias is 0.5 V.

In **Figure 4.13** it can be clearly observed that by applying a high incident light intensity (3000 mW/cm$^2$, which is the highest intensity that is able to be generated in our current equipment), the device reached a peak photocurrent of 5 µA. After turn of the light source the dynamic current damping curve was measured. It can be found that the remaining current is about 10 nA after turn off light illumination for
1 hour, which is approximately equal to the peak current when applying an intermediate light intensity (10 mW/cm²). Thus, three perfectly distinguishable resistive states can be demonstrated in 1 hour. The developed “2” state would contribute to the information storage capacity increase from original 2^n to 3^n.

**Figure 4.13.** Demonstration of the “0”, “1” and “2” states in the optically switchable memory device by applying different incident light intensity of 3000 mW/cm² and 10 mW/cm². The former one drove the peak current to 5 µA while the latter one lead to a peak current of 10 nA.

To further explore the possibility of improve the information storage capacity, different initial photocurrents (1 nA, 10 nA, 100 nA, 1 µA and 5 µA) were obtained by control the light intensity, as shown in **Figure 4.14.** After turning off the external light source, it can be observed that the resistances in different curves are perfectly distinguishable. The phenomenon indicates that the single nanorod device can demonstrate multi-addressable characteristics, which is the fundamental to improve data storage capacity.

**Figure 4.15** illustrate the mechanism for multi-level storage in the Au-Ni/NiO-CdS-Ni/NiO-Au nanorod based optoelectronic memory device. The information
storage level was determined by binary factors: the peak photocurrent (which is determined by the incident light intensity) and damping time. For a given peak photocurrent, the information will be automatically stored to a different position in specific range of time. Similarly, within a given time horizon, the information storage position varies with different peak photocurrent as well. For example, the information will be stored to the level of 10 nA-100 nA after 10 min if the peak current is 1 µA. However, if the peak photocurrent is 100 nA, at the same time the information will be stored to the level of 1 nA-10 nA. The multi-addressable characteristics could provide flexibility in real world application. At the same time, it can be observed that at least 6 different and distinguishable conductance level was created, indicating the information storage capacity improved significantly compare to the traditional binary storage system.

Figure 4.14. The damping curves of Au-Ni/NiO-CdS-Ni/NiO-Au single nanorod device which was illuminated to generate different photocurrent by control the incident light intensities. It demonstrates the ability for current memory device to show the multi-addressable characteristics.
Figure 4.15. The demonstration of binary information storage system by utilizing the driving factors of peak photocurrent and damping time.

To further investigate the mechanism for photocurrent damping, in Figure 4.16 the photocurrent of damping curve was fitted by numerical function, it is found that the photocurrent decay curves can be well fitted using the exponential model\textsuperscript{[72]}

\[
I(t) = y_0 + A_1 \exp\left(-t/\tau\right)
\] (4.1)

where \(\tau\) is the decay time constant. In the current case, the \(\tau\) value increases with time past, indicating slower photocurrent damping. Interestingly, within a specific time horizon (\(10^0\) s-\(10^2\) s, \(10^2\) s-\(10^3\) s, \(>10^3\) s etc.), the extracted \(\tau\) value in different groups stays constant with tiny deviation, which improved the controllability of information destructing process.
Figure 4.16. Experimental and exponential fitted time dependent photocurrent decay curves within (a) $10^0$ s-$10^2$ s. (b) $10^2$ s-$10^3$ s. (c) $>10^3$ s, the solid and dash lines represent the experimental and fitted curves, respectively. (d) The extracted $\tau$ values for different groups of samples within various time horizons. Group 1, 2, 3, 4 and 5 represents samples with peak photocurrent of 1 nA, 10 nA, 100 nA, 1 $\mu$A and 5 $\mu$A, respectively.

4.3.4 Demonstration of Self-Destructive Memory Behavior for Information Protection

Finally, it can be observed that the function of current optoelectronic memory device is different from the traditional resistive memory device, in which the conductance state maintained relative stable with time past. In the current study, the above mentioned high photo-induced ON/OFF ratio is corresponding to the “write” step in the operation of memory device. Due to the persistent photocurrent phenomenon, the information can be retained and is readable in a long time.
However, it is also observed that with the continuously decrease of photocurrent, eventually the remaining current will be undistinguishable with dark current, corresponding to the “erase” process. Since the erase step appears spontaneously, it can be defined as a self-destructive process. The “self-destructive” characteristics indicates that the Au-Ni/NiO-CdS-Ni/NiO-Au single nanorod not only has the information storage capability, but also has an important advantage of information protection. As a proof of concept to demonstrate the application of our device, a demodulating process was performed on a chip with 3*8 single units, which are 3 mm*3 mm silicon wafers with photo-lithography prepared micro-electrodes, as shown in Figure 4.17. The single units was covered by a designed shadow mask, for some units it is transparent so that the light can pass through while for the rest units the incident light will be blocked. In each single unit one of the target Au-Ni/NiO-CdS-Ni/NiO-Au nanorod device was prepared, by the above mentioned e-beam lithography approach. Upon light irradiation, the units which is uncovered will be exposed to light, and the photocurrent of device will increase accordingly. As a result, the device will be set to “1” state. For the other units, since the incident light is blocked by the shadow mask, the current of device will be kept at initial dark current, and the state will be “0”. This illumination process is corresponding to the “write” step in a typical memory device operation.

Interestingly, since the shape of shadow mask can be tuned, one can decide which unit will be exposed to light illumination. According to ASCII code, the written information can be designed by properly select mask.
Figure 4.17. Schematic diagram to demonstrate the experimental process of optically write the information of “NTU” by eight-bit codes of the American Standard Code for Information Interchange, the inset shows a typical single nanorod device in one single unit.

The word “NTU”, which is abbreviation of Nanyang Technological University, was optically written according to the ASCII code. The ASCII of letter “N”, “T” and “U” are 01001110, 01010100, and 01010101, respectively. Upon light illumination, the single units exposed to light illumination will be set to the state “1”, while the rest units are still “0”. After turn off the light illumination, the remaining current was read at 5 min, 10 min, 20 min as well as 30 min. Figure 4.18 shows the demodulating process. It can be observed that although the current decreased continuously with time past, corresponding to the cell becoming darker, after 5 min, 10 min and 20 min, the remaining current of all devices exposed to light illumination are still distinct to the original state, indicates the information “NTU” can be correctly demodulated. However, after 30 min the remaining current of some devices is no longer distinguishable with the initial state. At this moment, the original information cannot be correctly demodulated. With a false demodulating result of “FTT”, the original information is hidden, which indicates that the information was self-destructed.
Figure 4.18. The demodulating process of the word “NTU” according to the ASCII codes before illumination, after shined light illumination, and after 5 min, 10 min, 20 min and 30 min from light off.

Till now, all the investigations of Au-Ni/NiO-CdS-Ni/NiO-Au single nanorod based optoelectronic memory devices were performed on the rigid silicon wafer. In order to investigate the potential application for the single multi-segments nanorod toward flexible electronics, the typical “write-read-erase” operation was performed on the transparent and mechanically flexible Polyethylene terephthalate (PET) substrate. The bendable microelectrodes were patterned on PET substrate via photolithography, while the subsequent nano-device fabrication was done by e-beam lithography. Figure 4.19 demonstrates the typical “write-read-erase” process as well as the flexible substrate based memory performance. Upon light illumination, the device got sharp current increase, which is corresponding to the “write” operation. Unlike traditional memory device, in which the writing process was done by applying voltage bias, the current device can be written by optical stimulation. The remaining current was read continuously and a long-time persistent photocurrent can be clearly observed after removal of incident light (see in Figure 4.19a). After 1 h the current was still around 2 orders higher than the
pristine state, indicating the memory function. Meanwhile, the erase process happens at the same time without external stimulations, which is corresponding to the information protection function. Figure 4.19b shows the current-time relationship before and after the substrate bended for 100 cycles. The negligible performance change indicates the electric stability of the single nanorod based device.

Figure 4.19. (a) The current-time curves illustrating the original state and the write, read and erase process of the Au-Ni/NiO-CdS-Ni/NiO-Au nanorod device on flexible substrate. (b) the cycling performance of Au-Ni/NiO-CdS-Ni/NiO-Au nanorod device on flexible substrate before and after bending for 100 cycles.
4.4 Conclusion

To summarize, for the first time the optically switchable and time-controllable self-destructive memory devices were developed based on multi-segmented nanorods. As a result of the controllable migration of photo-generated carriers at the NiO/CdS interface, a persistent photocurrent was observed. Based on the durable photoconductivity, the multi-addressable self-destructive memory device have been prepared on rigid and flexible substrates. Combining the photo modulability, time controllability and self-destructive characteristics, the memory device demonstrates a promising application toward the confidential and private information protection.

Reference


Chapter 5

Optically and Electrically Configurable Memory for Programmable Logic Gate with Orthogonal Inputs

Developing memristor based logic gate could contribute to solve the problem of continuous power reliance. Based on the design of circuit different kinds of logic functions can be realized, as discussed in Chapter 2. However, the main studies in this area focus on the integrated circuit design and set up, and electrical stimulation is the only type of input for the circuit. The investigations on employing new stimulus for the circuit is quite limited. In Chapter 4 the design, fabrication, characterization and measurement of the optically switchable memory device have been introduced. Here the study aims to combine the two different types of memory devices into one electric circuit, so that the system can be responsive to different (orthogonal) inputs. Since the optoelectronic memory device demonstrate some unique characteristics compare to the traditional memory devices, some unique logic functions are also expect to be developed. This chapter will start from the hypothesis, followed by introduce the design and set up for the experiment. After that the experimental output under different combinations of inputs will be discussed. Finally, the potential application and the innovation of this kind of logic gate will be discussed.
5.1 Introduction

The conventional logic gate mainly focus on the logic input, output and operation process of circuit. Usually it does not address the problem of logic value storage. This means a typical logic gate need to be supported by continuous power supply. The memristor-based nonvolatile logic circuits was developed to solve the data storage issue and to maintain the logical operation functions when there is power loss\(^1\). Two typical types of memristor-based logic circuits, the IMPLY\(^2-7\) and MAGIC\(^8\), have been introduced in Chapter 2.

However, till now most of the reported memristor-based logic gate are purely operated with the external stimulation of voltage\(^9,10\). This means other naturally existed powers (light, magnetic field, chemical stimulation etc.) cannot contribute to the operation and output of the gate. In Chapter 4, a detailed discussion on the optically switchable memory device has been presented. The single multi-segmented nanorod based memory device can be switched to LRS with light illumination. After the stimulation removed, the information can be stored in a persistent time horizon. More importantly, it was also found that eventually the photocurrent will be non-distinguishable from the original state, based on such characteristics the “self-destructive” memory concept has been raised.

In order to make the logic system responsive to multiple stimulations, here the proposal is to integrate the two types of memory devices into one circuit. Logically, the circuit should be responsive to orthogonal inputs. In Figure 5.1 the hypothesis is summarized. Fundamentally, the circuit is constructed by parallelly connect the single nanorod based memory device to an electrically switchable memory device, as shown in Figure 1.3. It is expected that the designed circuit should perform three functions. Firstly, the logic circuit should be set to LRS with electrical stimulation, optical stimulation or both. Thus, the system should demonstrate a typical “OR” logic gate function. Secondly, unlike traditionally logic gate, which relies on continuous input (power supply) to generate output (signal), in this logic circuit,
once the input is provided, the output can be maintained persistently (theoretically the shorter duration of optoelectronic memory and electrical memory). Thus, the output can be read out continuously with one-time input provided, regardless whether the input is kept. Third, as shown in Chapter 4, the information erase mechanism for current optoelectronic memory is different from traditional electrical memory device, in which the “erase” operation can be finished immediately after the reverse voltage bias is provided. The information erase happens spontaneously. Thus, unlike the typical electrical memory device, in which the information can be reset to “0” whenever needed, the circuit demonstrates a “self-locking” characteristics. Once the input for both electrical side and optical side are “1”. The logic circuit cannot be reset in the “blocking stage” (equal to the persistent photocurrent duration), and the output is compulsively “1”. The logic value reset is possible only when the circuit is unblocked.

![Figure 5.1. Schematic diagram illustrate the operation and purposed functions of the memristor-based logic circuit.](image)

The circuit was established by parallelly connect the optoelectronic memory device to the electric memory device. The logic circuit was proposed to demonstrate three levels of functions: the basic “OR” gate function, the memorable logic gate function (one time input, continuous output) and self-locking logic gate function (output compulsive to be “1” within blocking stage under “1, 1” input).
This chapter will start from the materials and methods to introduce the basic circuit components fabrication procedure and the construction of circuit. After that the individual device performance will be briefly summarized. The output of logic gate under different combinations of inputs will also be discussed. Finally, the logic function and potential application will be discussed.

5.2 Materials and Methods

5.2.1 Setup of Electronic Logic Gate with Orthogonal Inputs

The studied logic circuit was constructed using two fundamental components: the single nanorod based optoelectronic memory device and the electrically switchable memory device based on the sandwich structure. The optoelectronic memory device was prepared by electrochemical deposition, after that the single nanorods can be distributed on the surface of silicon wafer by drop casting. The wafer was patterned micro-electrodes by photolithography in advance. The e-beam lithography will be taken in order to connect the nanorods to the microelectrodes and forming circuit. The electrical memory device was fabricated on a rigid conductive Si wafer. The Si substrates were cleaned in the H2SO4:H2O2=3:1 piranha solution for 45 min, followed by rinsing in DI water and subsequent drying with N2. The wafers undergoes oxygen plasma for 3 min. Afterwards 25 mM of Zn(NO3)2 •6H2O and 50 mM of 2-methylimidazole methanolic stock solutions, which was prepared in advance was used. The silicon wafers were immersed into the mixed solution for half an hour at room temperature for ZIF-8 film growth purpose. After that the samples were rinsed with methanol, dried with N2. Finally, a 150 nm Ag layer was thermally evaporated to the top surface and work as the electrode.

The optoelectronic and electrical memory devices was connected in a circuit. The schematic is shown in Figure 5.2. The external voltage was applied on the circuit.
The output signal was measured on a probe station (Keithley 4200-SCS) with and without light illumination as the current.

**Figure 5.2** Schematic illustrating the logic circuit setup by integrate the single nanorod device based optoelectronic memory and the sandwich structure based Ag-ZIF-8-Si electric memory device.

### 5.2.2 Device characterization

The SEM image of Au-Ni-Au-Ni/NiO-CdS-Ni/NiO-Au-Ni-Au single nanorod based optoelectronic memory device was shown in **Figure 4.4 (a) and (b)**. For the electrical resistive switching memory, a uniform layer of ZIF-8 thin film, which acted as insulator layer, was inserted between the Ag top electrodes and the conductive Si bottom electrode to form the Ag/ZIF-8/Si device\(^\text{[11]}\), which can be observed from **Figure 5.3a**. The thickness of ZIF-8 film and Ag electrode are 60 nm and 150 nm, respectively. The 100μm * 100μm single devices were distributed on the rigid Si substrate, as shown in **Figure 5.3b**.
Figure 5.3 SEM image of Ag-ZIF 8-Si sandwiched memory from (a) cross view and (b) top view of the device arrays.

5.3 Principle Outcomes

5.3.1 Performance for Single Memory Component

The output was measured for the individual optoelectronic and electrically switchable memory devices, respectively. For the optoelectronic memory device, a typical curve is shown in Figure 5.4. Similar to the phenomena observed in Chapter 4, the nanodevice got a sharp current increase upon white light illumination. After turn off the optical stimulation the photocurrent did not quickly return back to the pristine state. In this measured device, the photocurrent increased sharply upon illumination from $10^{-13}$-$10^{-12}$ A to $10^{-7}$-$10^{-6}$ A. And it decreased slowly after light off.
Figure 5.4 A typical current-time characteristics for the individual Au-Ni-Au-Ni/NiO-CdS-Ni/NiO-Au-Ni-Au single nanorod device. The device was firstly exposed to 1000 mW/cm² white light for 2 min to reach the peak current. Then the light was turned off and damping process of photocurrent was recorded. The voltage bias was fixed at 0.5 V during the whole measuring process.

In Figure 5.5 the typical I-V characteristics of ZIF-8 based sandwiched memory device is presented. The device shows a classical non-volatile properties. When a positive voltage bias that reached the threshold was applied, the device can be suddenly switched to LRS. Under a reverse voltage bias it can be reset back to HRS. The resistance switching mechanism was consider to be the combination action of electro-migration and the electron hopping effect\textsuperscript{[12-14]}, which led to the Ag nanoparticles formed in the ZIF-8 insulator layer. After the Ag nanoparticle formed in the switching layer the conductivity of device can be enhanced significantly. Thus, the device can be switched to LRS. The formed Ag nanoparticle can be fractured by applying a reversed voltage bias, which could provide a negative electric field and start the reset process. The conductivity of device drop back and it will be switched back to HRS.
Meanwhile, it is worthy to note that the set voltage of current ZIF-8 based memory device is much higher than a normal working voltage bias for optoelectronic memory device (0.5 V unless mentioned specially). This is important because when an “optical only” is performed, the external voltage bias for the whole circuit can be controlled at 0.5 V. Under such circumstance the optoelectronic memory device can be switched with light illumination while the possibility of electrically switch can be excluded. The ON/OFF ratio as well as the resistance at LRS can be controlled by set the compliance current. In the current case, the device can be set to either \(10^{-3}\) A or \(10^{-4}\) A.

![Figure 5.5](image)

**Figure 5.5** A typical current-voltage characteristics for the Ag/ZIF-8/Si memory device in voltage sweeping mode. The compliance current was set to be (a) \(1 \times 10^{-3}\) A and (b) \(1 \times 10^{-4}\) A for the purpose of prevent device from breakdown and provide a desired ON/OFF ratio.

Notably, the ON/OFF ratio measured as resistance can reach \(10^7\) in the current ZIF-8 based resistive memory device. Such characteristics can provide a low possibility for information misreading. In **Figure 5.6a** it can be seen that the device to device performance difference is not significant. The ON/OFF ratio is large enough for information storage and read out purpose. Among different devices, the set voltage varies from 1.5 V to 2.45 V, significantly higher than the working condition for optoelectronic memory device. The reset voltage ranges from -0.6 V to -3 V.
(Figure 5.6b). The cyclic switching between LRS and HRS can be performed repeatedly, with a relative stable resistance in HRS.

![Graphs](image)

**Figure 5.6** (a) The HRS and LRS distributions of resistance recorded in different devices. The read voltage was set to be 300 mV. (b) the device to device variation of set and reset voltage, which are statistically collected from 25 devices. (c) the HRS and LRS switching operations in 30 cycles, with the read voltage of 300 mV. (d) Statistical result for set and reset voltage in 30 measuring cycles.

Finally, since in the optically switchable memory device, the photocurrent can be maintained in a persistent time horizon, the performance of ZIF-8 based memory device also need to be stable in the same measuring period. In **Figure 5.7** it can be observed that the resistance of device in HRS and LRS has no significant fluctuation in the measuring window for more than $10^3$ s, under a consistent read out voltage of 300 mV. This demonstrate the performance reliability of the ZIF-8 based memory.
Figure 5.7 The characteristics of resistance retention in HRS and LRS at a constant 300 mV read out voltage in $10^3$ s in air, at room temperature. The resistance in different resistance states shows no significant fluctuation.

5.3.2 Demonstration of Logic Function for Different Inputs

The logic circuit can be operations with three groups of inputs: electrical only, optical only and both. Here the output under each specific input(s) will be discussed. Firstly, under the electrical only input. The initial voltage bias was 0.5 V, under which the electric memory cannot be set. The output current kept at $10^{-12}$-$10^{-11}$ A (HRS state). In this stage, the input is “0, 0” and output is “0”. At 20 s, a 3 V voltage, which is high enough to trigger the ZIF-8 based memory switch to LRS, was applied to the circuit. The output suddenly goes to the compliance current ($10^{-4}$ A). At this moment there is no light illumination, thus the input is “1, 0”. The output is “1”. 1 min later the 3 V external voltage stimulation was removed, instead a 0.5 V bias was applied to read the information. It can be observed that although there is no continuous electric input for the circuit, the current read out was still the compliance current and the output kept to be “1”. This illustrates the “memorable logic gate” function. The output does not necessarily depends on the real-time
inputs. When there is one time input, the output generation can be maintained. At 250 s, a -2 V voltage bias was applied, an immediate sharp decrease in the output current can be observed, due to the information erase in ZIF-8 memory device. Afterwards the read out current returned back to the original level.

![Figure 5.8](image)

**Figure 5.8** The logic circuit inputs for “electrical 1, optical 0” and the corresponding output (current) detected.

In **Figure 5.9** the optical only signal is applied on the memory device based logic circuit and the output was detected. In the whole measuring process, a constant voltage bias 0.5 V was applied. Based on the above mentioned study this voltage is not high enough to switch the ZIF-8 based memory device to LRS. Hence, only the optoelectronic memory device could contribute to the output for the whole circuit. Upon light illumination, the separation of electron/hole pairs could significantly enhance the conductivity of CdS\(^{15-17}\), thus the optoelectronic memory device can be switched to LRS. It can be found that when the white light was irradiated on the device at 50 s, the output quickly reached the compliance current (set to be 10\(^{-9}\) A here). Even if the light was switched off 100 s later, the output current was still
higher than the compliance current in the following 1000 s. If the LRS is defined as $10^{-9}$ A and above (Notably, here the LRS is defined as the current of $10^{-9}$ A and above. In real world application there is no strict rule to accurately determining the HRS and LRS. For application purpose the different states need to demonstrate sufficient resolution thus it could decrease the possibility of misreading. Here the point for selection is that on one hand, $10^{-9}$ A is 2-3 orders higher than the initial state, the current difference is sufficient to distinct the LRS and HRS. On the other hand, from the information obtained in Figure 5.4, it roughly takes 1000 s for the device damping from peak photocurrent to $10^{-9}$ A. This is a desired time window for demonstration because it well matches the stable resistance retention time of ZIF-8 based memory.), it means that the optical input can generate persistent, memorable and compulsive “1” output in 1000 s. After 1000 s, the remaining photocurrent dropped below $10^{-9}$ A, and the output switched back to “0”.

![Graph](image.png)

**Figure 5.9** The logic circuit inputs for “electrical 0, optical 1” and the corresponding detected output current.

Finally the scenario in which the logic circuit has both optical and electric input has been measured. As shown in **Figure 5.10,** initially a 0.5 V voltage was applied to the circuit for information read out as well as providing a working power for the
single nanorod based optoelectronic memory device. The read out current was in the range of $10^{-12}$ A to $10^{-11}$ A. Then a 3 V voltage bias was applied to the circuit and a 1000 mW/cm$^2$ of white light was shined to the nanorod device. With the orthogonal inputs applied to the circuit at the same time both the optoelectronic memory device and the electrically switchable ZIF-8 based resistive memory can be switched to their respective LRS. Since the ZIF-8 based memory device can be switched to $10^{-4}$ A (the compliance current) and the LRS for optoelectronic memory was in range of $10^{-7}$ A-$10^{-6}$ A, the read out current was $10^{-4}$ A. After that both the electrical and optical stimulations were removed (voltage bias changed to 0.5 V and light switched off). The read out current was still $10^{-4}$ A due to the memorable characteristics of circuit. 100 s later a reverse voltage bias (-2 V) was applied to the circuit to reset the ZIF-8 based memory device. The electrical memory device was reset and it switched back to the HRS. At this moment the remaining photocurrent in single nanorod based memory is higher than the current of ZIF-8 based memory at HRS. Thus, the output was showed as the current of optoelectronic memory. If the LRS of logic circuit is defined as $10^{-9}$ A and above, it can be found that there is a “blocking stage” within which the output of logic circuit is compulsively “1”, even if the external stimulations are removed and the electrical memory is reset.

The mechanism can be understood as in the parallel circuit:

\[
I_o = I_i + I_e \quad (5.1)
\]

\[
I_i = AI_p \quad (5.2)
\]

Where $I_o$, $I_i$, $I_e$, $I_p$, and $A$ are the output current, the current of optoelectronic memory device, the current of electrical memory, the peak photocurrent of optoelectronic memory and the remaining proportion of peak photocurrent, respectively.

Assume the electrical memory is reset, the output value of circuit should be “1” if $I_i$ is larger than the critical point of LRS. Thus, the output is blocked and is compulsively “1” once illumination is provided. The parameter “A” should decrease with time past, the length of “blocking stage” equals to the time for the device damp from peak photocurrent to the “defined” critical point of LRS, when $AI_p$ equals to the critical point of LRS.
Hence, with the combination of “electrical 1, optical 1” inputs scenario, once the inputs were applied, the logic circuit is self-locked and the output value will be fixed. After the blocking stage, the output value was reset to be “0” since the remaining photocurrent decreased to be lower than $10^{-9}$ A. At that time the output of logic circuit was unblocked. The value can be adjusted between “0” and “1” with the switch of ZIF-8 based electrical memory device, but without the optical side input.

![Diagram](image)

**Figure 5.10** The logic circuit inputs for “electric 1, optical 1”. The optical and electrical inputs and the corresponding output current at different points.

### 5.3.3 Discussion on the Function of Logic Gate

From the discussions on scenarios with different inputs, it can be found that the fundamental function of “OR” logic gate has been successfully realized. With “1, 0”, “0, 1” or “1, 1” inputs, the output current of logic circuit will be detected at LRS and the value is “1”. Besides, the output value “1” does not necessarily relies on the continuous external input, with one time optical and/or electric stimulation applied,
the output can be maintained to “1” even if the stimuli were removed. Thus, the circuit demonstrated memorable logic gate function, which was resulted from the characteristics of its memory components. More importantly, once the circuit was exposed to the orthogonal “1, 1” input, within the blocking stage the output of circuit is compulsively to be “1”, even with the reset of ZIF-8 based electrical memory device. In this scenario the logic circuit demonstrate the self-locking characteristics. The basic functions for the current logic circuit is summarized in Figure 5.11.

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The “OR” logic gate function, the memorable logic gate function and the self-locking logic gate function, were realized in specific scenarios.

Additionally, it is also noted that for the resistive switching behavior, the LRS of electrical memory device is different from that of optoelectronic memory device. Basically, if the compliance current of ZIF-8 based memory is set to be $10^{-4}$ A, it is 2-3 orders higher than the peak photocurrent in optoelectronic memory device. During the damping process, the photocurrent of optoelectronic memory device decreased from $10^{-7}$ A-$10^{-6}$ A to $10^{-10}$ A-$10^{-9}$ A. It is still perfectly distinguishable with the initial state ($10^{-12}$ A-$10^{-11}$ A). Thus, if the multi-level conductance is considered for the information storage capacity improvement, the logic circuit could demonstrate three different levels of outputs: “0”, “1” and “2”. The “1” state was resulted from the case of pure optical input and the “2” state was generated by the case that electrical input was employed. In Figure 5.12 the functions of logic
gate were re-organized. Here the output current of $10^{-7}$ A-$10^{-4}$ A, $10^{-10}$ A-$10^{-7}$ A and $<10^{-10}$ A were defined as state “2”, “1” and “0” respectively. For optical only input, the circuit output is “1” and the value cannot be reset within a specific time horizon. With the electrical only input, the output value of logic gate is “2” and it can be reset to “0” with a subsequent negative voltage bias ($E_2=0$). With both optical and electrical inputs, the output value of circuit was first set to “2” state. Within the blocking stage, the output value can be at most reset to “1” by applying an $E_2=0$ input. The self-locking device function can still be presented.

Figure 5.12 Summary of the logic gate functions with the multi-level conductance taken into consideration. (a) The levels of conductivity were re-defined to “2”, “1” and “0”, corresponding to the output current range of $10^{-7}$ A-$10^{-4}$ A, $10^{-10}$ A-$10^{-7}$ A and $<10^{-10}$ A, respectively. (b) the revised truth table with output “2”, “1” and “0”. The electric inputs $E_1$ and $E_2$ represent the set and reset voltage bias, respectively. The “0” and “1” inputs for $E_2$ is defined as apply and not apply the reset voltage, respectively.

Finally in this chapter, there are two key points need to be noted. Firstly, the current approach is quite productive. For the nanorod device, there are hundreds of separated nanorods on a single piece of silicon wafer. With the following e-beam
lithography, usually 200 nanodevices can be engineered within 2 h experiments. Based on our statistical investigation, the current successful rate for such device is about 34% (76/221). Tens of effective devices can be engineered in a full fabrication procedure. For the electrically switchable memory, the manufacturing technology is matured. With the shadow mask design thousands of devices can be prepared by thermo-evaporation. The successful rate depends on the quality of switching layer and is roughly 25%. Second, consider the device performance. It varies from device to device because: 1) the peak photocurrent of a specific nanorod device is closely related to the nanostructure. The structure is related to the pore size, electrode area, surface roughness etc. In the current stage it is hardly to control all the factors to be consistent. Thus, the photocurrent could vary even under the same condition (see Figure 4.12). 2) the damping characteristics for the optoelectronic memory device also varies from device to device. This is because with similar chemical approach (Cl⁻ and OH⁻ added to the plating solution) the surface oxidation could not be precisely controlled during the electrochemical deposition process. In summary, the approach is productive, with a full set of experimental procedure tens of effective devices can be provided. For a given nanodevice, its cyclical performance and repeatability were also demonstrated. However, due to the nanostructure and surface oxidation difference the performance could vary between devices.

5.4 Conclusion

To conclude, the concept of self-locking memorable logic gate was successfully demonstrated by integrating the optically and electrically switchable memory devices. The following functions have been achieved:

1. The two memory devices can be integrated to demonstrate the function of “OR” logic gate. Illumination and voltage are two separate inputs for such logic gate.
2. The logic gate has memorable function. One time input can lead to continuous output even if the external stimuli are removed. The two inputs have different erase mechanisms. For electrical stimulus, a reversed bias is needed to reset the state while for optical stimulus, the output will automatically change to “0” with time past.

3. Once the optical and electrical stimuli are provided at the same time, after remove the stimuli, the logic gate shows a self-locking characteristics. The “0” state can only be achieved in unblocked stage.

4. By considering the multi-level conductance, the output of logic gate can be re-defined with “0”, “1” and “2” outputs. The “1” state was resulted from the case of pure optical input and the “2” state was generated by the case that electrical input was employed. The truth table can be revised accordingly.

References


Chapter 6

Developing Plasmonic Logic Gate by Orthogonally Modulating Organometallic Molecules

In this chapter the optical logic gate with orthogonal inputs will be developed. One of the optical output is plasmon resonance. A possible approach to tune the SPR characteristics is to change the states of the covered polymers or molecules. However, among all the reported studies, only one external stimulation was applied. To realize the logic function with orthogonal inputs in a single system, the device must be at least responsive to two stimulations. Here the organometallic molecules will be assembled to the plasmonic active Au nanoparticle arrays. In the previous investigations, the molecules are sensitive to both light illumination and electrochemical stimulation. Meanwhile, the molecules were assembled to the nanogap device (see in Chapter 1), and the electronic logic gates were successfully realized. Thus, it is expected that with the molecular state variation, the SPR can be tuned correspondingly and the plasmonic logic gate can be demonstrated under orthogonal stimulations. This chapter will start from the background introduction on the fundamentals of plasmonic logic gate, then the experimental methodologies will be introduced. Finally, the results will be discussed in detail. Especially, the molecular switch in liquid and the SPR shift after assembled the organic/organometallic molecules to the plasmonic active nanoparticle arrays, will be shown.
6.1 Introduction

The traditional information processing is mainly electrical computation. However, due to the rapid development of data intensive information processing, people discovered that the optical computation strategy has several advantages such as highly localized information encoding, smaller scale and cheaper electric to optical or optical to electric transduction\textsuperscript{[1,2]}. Combine with the high availability, board applicability and long distance controllability\textsuperscript{[3,4]} characteristics of optical signal, optical logic gate has significant potential to open a new window for information technology.

Plasmonic spectrum is one of the output for optical signals\textsuperscript{[5]}. Generally it is the extinction spectrum of noble metals (Au, Ag, Cu etc.). In recent years people found that several factors would significantly influence the SPR characteristics. The factors include: (1) the size of particles. According to Mie theory, for spherical particles, with fixed shape and material composition, the LSPR extinction will be dominated by absorption for smallest particles and scattering will take over with the particle size increase. Taken gold nanospheres as an example, the transition appears at round 80 nm\textsuperscript{[6]}. For gold nanospheres, the LSPR peak can shift for 60 nm when the particle size changes between 10 nm and 100 nm\textsuperscript{[7]}. As shown in Figure 6.1a, the obvious color change can be observed with the particle size varies. Generally, with larger gold nanoparticle size, the LSPR will shift toward longer wavelength. (2) Beside size effect, the aspect ratio can also influence the LSPR of gold nanostructures, with the refractive index variation\textsuperscript{[8,9]}. In the study by Huang, X et al.\textsuperscript{[10]}, the LSPR showed red shift with increasing the aspect ratio. (3) Nanostructure shape is also a factor to determine the SPR characteristics. In the work published by Jin. et al.\textsuperscript{[11]}, chemical approach was applied to dynamic tune the shape of sliver nanostructure. As a result, the SPR characteristics varied correspondingly. The results are summarized in Figure 6.1c. (4) On top of the above mentioned size, shape and aspect ratio effects, dielectric environment can also influence the SPR significantly\textsuperscript{[12]}. Generally, changing the dielectric
environment of noble metals, such as coating a layer of materials to tune the dielectric environment from air to the specific material, the refractive index will change accordingly. Thus, the SPR shift is possible to be observed, as seen in Figure 6.1d.

Figure 6.1 The examples illustrating factors that can influence the SPR characteristics: (a) the size effect\cite{13}, (b) the aspect ratio effect\cite{10}, (c) the shape effect\cite{11} and (d) the dielectric environment effect\cite{12}.

When the effect of dielectric environment is considered, one of the methodology is to modify the surface of SPR metals with conductive polymer\cite{14,15} or switchable
molecules\[^{[16,17]}\]. With external stimulation (optical or chemical) induced states variation, the dielectric environment will be changed, leading to the shift of SPR spectrum. However, in these reported methodologies, only single external stimulus was applied. It is expected that multiple stimuli can be accepted by the system. And in turn, generate output signals to realize the logic operation.

Figure 6.2 Schematic diagram illustrating the hypothesis of plasmonic logic gate design: the organometallic molecules were firstly assembled to the plasmonic active substrate. The output extinction signal can be detected. By orthogonally tuning the molecular states (open and close), the configuration will change accordingly, result in the dielectric environment variation. Hence, it is proposed that the LSPR spectrum can be shifted under orthogonal stimulations. The plasmonic logic function concept can be demonstrated with such design.

The previous studies on organometallic molecules, the switching mechanism\[^{[18]}\] and its application toward electronic logic gate\[^{[19]}\], have been introduced. In this chapter, the proposal will be moved one step ahead to the optics. Figure 6.2 shows the hypothesis for the plasmonic logic gate design and operation. Combining the organometallic molecules to the plasmonic active substrate, it is expected that the Au-molecule hybrid structure can be responsive to orthogonal external stimulations. Since the dielectric environment changes due to the difference of molecular conformation in open/close states, the SPR spectrum will shift accordingly. Thus, with the orthogonal inputs to switch molecular states, it is expected that the output
of LSPR peak can be manipulated between \(\lambda_1\) and \(\lambda_2\), and realizing the plasmonic logic operation.

This chapter will start from the materials and methods to introduce the device fabrication and molecular assembly procedure, followed by the experimental results discussion. The operation of molecular switch and the demonstration of plasmonic logic gate will be the key focus of current investigation.

6.2 Materials and Methods

6.2.1 Molecule synthetic procedures

The diethynyl-substituted dithienylethene\[^{20}\], AcS-p-C\(_6\)H\(_4\)-C \(\equiv\) CH\[^{21}\], the ruthenium precursor, \([\text{(dppe)}_2\text{RuCl]}(\text{OTf})\]^\[^{22}\], were prepared as previously reported. To synthesize the \((\text{dppe})_2\text{Ru-C} \equiv \text{C-(C}_{15}\text{S}_{2}\text{F}_{6}\text{H}_{6})\text{-C} \equiv \text{C-Ru(dppe)}_2\text{-S molecule, the experiment was performed in a Schlenk tube}\[^{18}\]. Firstly, the \([\text{S(dppe)}_2\text{Ru]}[\text{OTf}]\) (172 mg, 0.16 mol) and the diethynyl-substituted dithienylethene (33.08 mg, 0.08 mmol) were pumped for 30 min. After that 20 mL of well degassed dichloromethane was transferred to the solids. In the dark environment the mixture was stirred for four days, and then triethylamine (0.2 mL, 3.2 mmol) was added. 30 min later, the reacting solution was evaporated. The dichloromethane solution was rinsed with DI water, dried with Na\(_2\)SO\(_4\), and the residue obtained after evaporation was rinsed with pentane (2 \(\times\) 10 mL). Totally 100 mg of 1o molecule was obtained after drying under vacuum.

6.2.2 Fabrication of Plasmonic Active Substrate

The plasmonic active substrate was engineered on ITO, using the thermo-evaporation approach. During evaporation an ultra-thin AAO membrane was covered on the surface as a shadow mask\[^{23,24}\]. The Au nanoparticles was evaporated and afterwards the membrane was removed by a tape. The nanoparticle arrays are relatively homogenous. From the AFM image (Figure 6.3) it can be
found that the particle diameter is around 80 nm and the height is generally 20 nm-30 nm.

![AFM image of nanoparticle array](image)

**Figure 6.3** The AFM image of nanoparticle array prepared by thermo-evaporation with the ultra-thin AAO membrane as shadow mask.

### 6.2.3 Assembly of Molecules and Controllable Molecular Switch

The Au-S bond is designed to assist the assembly of the organic/organometallic molecules to the gold nanoparticle arrays. First, the ITO glass with gold nanoparticles underwent oxygen plasma to make the surface clean and hydrophilic. Then the substrate was immersed into the THF solution (5 mL), in which the organic/organometallic molecules (1 mg) was dissolved in advance. The assembly process lasted overnight, under the protection of N₂. After rinse the substrate with THF and ethanol, it was placed in the cube and fixed with a tape. The extinction spectrum was taken from the UV-Vis spectrophotometer, after repeatedly tuning the state of molecules. In the switching operation, the solution was irradiated with 360 nm UV light for 30 min to form the close form. To switch it back, 650 nm/700 nm visible light was shined to the solution for 1 h. The electrochemical stimulation was taken in CH₂Cl₂ (0.2 M Bu₄NPF₆), the solution was loaded a positive 650 mV vs Ag/AgCl potential and a subsequent slight negative -100 mV vs Ag/AgCl
potential. Each step of stimulation was applied for 1 min. Figure 6.4 illustrated the experimental procedure.

Figure 6.4 Schematic diagram explaining the whole experimental procedure. The cleaned substrate was immersed into the THF solution in which the organic/organometallic molecules was dissolved. After left in the solution overnight it was rinsed and placed in a cube to apply the light irradiation/electrochemical potential. The extinction spectrum was measured under different molecular states.

6.3 Principle Outcomes

6.3.1 Controlling Plasmon Resonance by Optically Switching the Organic Molecules

The organic molecules can be switched by shining the light with different wavelength. For typical DTE groups, the structure can be changed from the cross-conjugated open molecular state to the $\pi$-conjugated closed state under UV light irradiation$^{[25]}$. The reverse switching operation can be achieve by visible light irradiation. In Figure 6.5 the switching condition and chemical structure of the organic molecules (both open and close state) are summarized.
Figure 6.5 The chemical structures of the DTE based organic molecule in (a) open state and (b) close state. The molecular switch can be achieved by applying incident light with different wavelength. The open to close state switch can be triggered under 360 nm light irradiation while the reverse switch can be done by applying 650 nm visible light.

The UV-Vis extinction spectrum can be used to distinguish the two different molecular states. In Figure 6.6 it can be observed that the photochromic conversion process from the open molecular state to close state could result in significant variation in UV-Vis spectrum. The open state molecule displays the absorption at $\lambda_{\text{max}} = 314$ nm. With UV irradiation for 30 min, the band vanished, accompanied with a broader absorption appeared at $\lambda_{\text{max}} = 604$ nm. This absorption peak can be vanished by applying 650 nm visible light for 1 h. Figure 6.6b shows that the molecular switch also resulted in color change in the solution. By solving the molecular powder in THF solution, the initial liquid was transparent. With UV irradiation, the solution gradually went to the dark blue, corresponding to the red curve in Figure 6.6a. The transition is reversible and the colorless, transparent solution can be obtained after 1 h red light irradiation.
Figure 6.6 (a) the extinction spectrum of THF solution with the DTE based organic molecules dissolved. The black curve represent the open (initial) state molecule while the red curve shows the close state molecule. (b) The appearance difference between the two distinct molecular states. The photo on the left hand side is the open state molecule solved in THF solution while the right hand side photo shows the close state molecule in solution.

Next the illustration will be moved to how such controllable molecular switch could contribute to the plasmon resonance shift in solid state. Since the molecular switch was operated with light illumination, firstly the stability of gold nanoparticle arrays is measured. By applying continuous UV light (360 nm) and visible light (650 nm) irradiation, the plasmon resonance of unmodified Au nanoparticle substrate is same as the one measured in the dark, indicating that the pure Au substrate is stable under light illumination. It should be noted that in the current study, the extinction
characteristics varies device by device. This is because for different samples, the nanoparticle size and homogeneity cannot be perfectly controlled using the shadow mask evaporation methodology. However, since all the measurements were performed on the same device and the substrate position is fixed during the whole testing process, the plasmon resonance shift is comparable.

![Graph showing extinction vs. wavelength for different conditions](image)

**Figure 6.7** The extinction characteristics of unmodified Au nanoparticle substrate that measured in the dark, and with continuous UV/visible light irradiation.

Before measuring the photochromic switching behavior of organic molecule and its influence on the plasmon resonance of the Au-organic molecule hybrid nanostructure, there is still one question need to be answered: is the LSPR peak shift depend on the particle thickness? To answer the question different substrates with particle thickness of 20 nm, 40 nm, 60 nm and 80 nm were prepared. Under the same experimental conditions (molecule concentration, assembly time, substrate size, irradiation power/duration), the $\lambda_{\text{LSPR}}$ shift was recorded by switching the molecule. In **Figure 6.8** it can be learnt that the LSPR shift become more obvious when the substrate is thinner. With the particle thickness increase, the LSPR shift became weaker. Possible explanation for this phenomena is that the LSPR peak position depends on the refractive index, which was determined by the
dielectric environment. The dielectric environment varies with different conformation of molecules. With thinner Au nanoparticle, the contribution from organic molecule conformational change can be higher, result in more obvious LSPR peak shift. On the contrary, larger particle thickness could weaken the contribution from molecule, result in smaller LSPR shift.

Figure 6.8 The relationship between Au nanoparticle array thickness and the range of LSPR peak shift in organic molecule modified Au substrate.

Based on the result, 20 nm thickness particle arrays were used in this investigation. Further lower particle height will make the extinction Au nanoarray not distinct to ITO absorption. The organic molecules were assembled to the Au nanoparticle arrays, in Figure 6.9a it can be observed that the resonance peak shifted from 660 nm (blue curve) to 703 nm (black curve) after the molecules assembled. The significant 43 nm LSPR shift can be explained by the increased medium refractive index. The Discrete Dipole Approximation (DDA) methodology, which is an approximation of Maxwell’s equation, is appropriate to approach the absorption, scattering, and extinction for such particle shape. Based on DDA theory, the extinction intensity can be expressed as

\[ \text{Extinction intensity} \]
\[ E = 24\pi^2 N_A a^3 \varepsilon_m^{3/2} / \lambda \ln(10)[\varepsilon_i / (\varepsilon_r + 2\varepsilon_m)^2 + \varepsilon_i^2] \quad (6.1) \]

Where \( N_A \) is the nanoparticle density, \( a \) is the radius of nanoparticle, \( \varepsilon_i \) and \( \varepsilon_r \) are the imaginary and real part of the dielectric function of SPR metal, respectively. \( \lambda \) is the wavelength of absorbing light, \( \varepsilon_m \) is the dielectric constant of the surrounding medium. From the equation it can be found that the resonance condition is satisfied when

\[ \varepsilon_i = -2\varepsilon_m \quad (6.2) \]

At the mean time it is known that in the bulk metal material the following relationship is satisfied:

\[ \varepsilon_r = 1 - \omega_p^2 / (\omega^2 + \gamma^2) \quad \omega_p >> \gamma \quad (6.3) \]

Where \( \omega_p \) is the plasmon frequency of the bulk metal and \( \gamma \) is the damping frequency of the bulk metal.

So equation 6.3 can be written as:

\[ \varepsilon_r = 1 - \omega_p^2 / \omega^2 \quad (6.4) \]

When equation 6.2 is satisfied, it has

\[ \omega = \omega_p / \sqrt{2\varepsilon_m + 1} \quad (6.5) \]

Meanwhile, the refractive index from surrounding medium, the \( n_{\text{med}} \), is correlated to the dielectric constant, \( \varepsilon_m \), which the relationship in equation 6.6

\[ \varepsilon_m = n_{\text{med}}^2 \quad (6.6) \]
Finally, the relationship between resonance peak position and the refractive index of surrounding medium can be established in equation 6.7:

\[ \lambda_r = \lambda \sqrt{2\varepsilon_m + 1} = \sqrt{2} \lambda n_{med} \quad (6.7) \]

Based on the conclusion in equation 6.7, it can be found that the resonance peak position is linearly correlated to the refractive index in surrounding medium. Thus, when the Au nanoparticle array was modified by the organic molecules, the surrounding medium changed from air to the molecule. As a result, with the increase of \( n_{med} \), the resonance peak will shift toward longer wavelength.
Figure 6.9 (a) The SPR characteristics of unmodified Au nanoparticle array (blue), the array with close state DTE based organic molecules assembled (black), and with open state DTE based organic molecules assembled (red). (b) The magnified resonance curve for Au-open state molecule and Au-close state molecule. (c) The repeated SPR shift realized by light illumination. The resonance peak shift back and forth with the change of incident light wavelength.

After assembly, a 650 nm single wavelength light was illuminated on the Au-organic molecules hybrid structure for 1 h. As shown in Figure 6.6, the molecules can be completely switched back to the open state. Figure 6.9 (a), (b) shows a clear blue shift, indicating the resonance shift is reversible, corresponding to the reversible switching of molecular state. In the first round test, after visible light irradiation, the SPR peak shifted from 704 nm to 688 nm. The measurement was performed for 6 complete cycles, by repeatedly shining UV light and visible light. The LSPR peak shifted back and forth corresponding to the molecular state switch. For open state, the SPR peak position was in range of 688 nm to 691 nm, while after UV illumination, the peak position was 701 nm to 704 nm. Although with minor difference, the two state molecules can generate distinct plasmon resonance as output. The resonance switch can be at least 11 nm. The mechanism for the reversible LSPR shift is still open to discuss and further investigations need to be taken in order to clarify it. However, some possible explanations can be found from related publications. In the work reported by Gayatri K. Joshi and co-workers[17], a 21 nm LSPR shift (red shift for trans and blue shift for cis) was detected with the cis-trans conformational change in the molecules with azobenzene group. The 21 nm LSPR shift was ascribed to: 1) due to the conformational change there is at most 0.6 nm thickness increase in dielectric shell thickness. 2) the enhanced resonance energy transfer between the Au nanoprism substrate and the attached azobenzene, since a better resonance energy transfer takes place when the azobenzenes are in the trans conformation. In our opinion the molecule conformational change is quite similar to the case in the current study. In azobenzene group, the trans conformation is accompanied by 0.6 nm height increase due to the molecule becomes more rigid. In the DTE-based molecule, the open form molecule is less linear and rigid than the
close form molecule$^{[19,27]}$. It is more “similar” to the conformation of cis state. The close state molecule is more linear and rigid compared to the open state, resulting a longer molecule considering the conformational difference. We believe this could at least partially explain the phenomenon observed that the LSPR shows red shift with close form and blue shift with open form.

Admittedly, based on current experimental results some other possibilities which could contribute to explain the observation could not be excluded. Note that the close form molecules has the extinction peak at longer wavelength (604 nm vs. 314 nm for open form). It is possible that the extinction spectrums of both Au nanoarray and the organic molecule overlays, resulting the absorption peak for the Au-close form molecules appears at the longer wavelength than the Au-open form molecules. This hypothesis could also be supported by the fact that lower the thickness of Au nanoarray result in more obvious SPR peak difference. In order to verify the mechanism. Further computational modeling and experiments (i.e AFM to determine the height variation) need to be performed. The work will be take over in the future.

6.3.2 Demonstration of Plasmonic Logic Gate by Orthogonally Tuning the States of Organometallic Molecules

In the DTE based organic molecule, the molecular switch in THF has been observed, supported by the variation of absorption spectrum. The plasmon resonance switch was also found by assemble the molecules to Au nanoparticle arrays and perform the molecular switch operation. In the organometallic molecule, the switching mechanism will be more complex. The switching mechanism and the operation are briefly illustrated in Figure 6.10.
Figure 6.10 The operation and molecular switching mechanism for the organometallic molecule. The molecular switch from open form to close form can be achieved by applying UV light and/or electrochemical oxidization with subsequent reduction voltage bias, while the reverse switch can be achieved by applying 700 nm visible light.

On top of the photochromic switching between the non-conjugated molecular state (open form) and the \(\pi\)-conjugated close form with different wavelength irradiation, the ruthenium complexes can also promote electronic coupling for the metal centre and ligands\(^{[18]}\). Thus, under the external electrochemical positive potential, the molecule can be oxidized, from the open (o state) form to the o\(^{2+}\) state. The o\(^{2+}\) state will underwent the radical coupling process, forming a more stable c\(^{2+}\) (close form) state. Under the reverse scan, the oxidized molecule can be reduced and form the c state. Hence, in the organometallic molecules, there are two ways to complete the open to close form transition: the UV light irradiation and the electrochemical
oxidization with subsequent reduction. The reverse switch can be finished by applying visible light. Additionally, for molecular logic function, the reversible logic “OR” gate can be demonstrated. With UV light and/or electrochemical stimulation the molecular switch can be activated. And the logic value “1”, corresponding to the close form molecule, can also be reset.

![Graph](image)

**Figure 6.11** (a) the extinction spectrum of organometallic molecules in liquid state. The black curve represent the open (initial) state molecule while the red curve shows the close state molecule. (b) The appearance difference between the two distinct molecular states.

The open form and close form of organometallic molecule can be distinguished by their extinction spectrum. They also have significant difference in the color of solution. For the transparent open form molecule, the solution displays the absorption peak at $\lambda_{\text{max}} = 354$ nm. After illuminated with UV light for 30 min, the band vanished, with a new peak appeared at $\lambda_{\text{max}} = 717$ nm. The appearance of solution changed to light green, corresponding to the molecular switch. Consider the absorption difference for the close form of organic and organometallic molecules, here the visible light applied to switch it back to open form was selected.
to be 700 nm. The reverse switch can be realized in 1 h, with 700 nm light illumination.

To manipulate the molecular switch electrochemically, firstly the electrochemical characteristics was measured in high quality CH₂Cl₂ solution with 0.2 M Bu₄NPF₆. Figure 6.12a shows the cyclic voltammograms (CV) of open form and close form molecules. For open form molecule, the wave at E=625 mV vs Ag/AgCl represents the voltage that lead the two metal fragments switched to o²⁺. The o²⁺ state is unstable and thus will automatically undergoes the radical coupling process to form the c²⁺ state, as shown in Figure 6.10. In the reversed cathodic scan, two less positive peaks which can be attributed to the c²⁺/c⁺ and c⁺/c conversion. Thus, logically, the molecule can be switched from open state to close state electrochemically with the pathway of o-o²⁺/c²⁺-c, in which the o-o²⁺ was promoted with a positive voltage bias (650 mV) and the c²⁺-c transition was achieved with a negative bias (-100 mV). Figure 6.12b shows the operation of molecular switch. Notably, the intermediate c⁺ state can only be realized electrochemically, which was reported previously[18]. Since the c⁺ state is unstable it is not included in the current study.
Figure 6.12 (a) CV scanned in CH$_2$Cl$_2$ solution with 0.2 M Bu$_4$NPF$_6$ for the open form molecule (black curve) and close form molecule (red curve). (b) The switching operation to manipulate the molecular state between o/c$^{2+}$/c$^{+}$/c.

Based on the molecular switching mechanism and corresponding operations discussed above, now the molecules will be assembled to the Au nanoparticle array to measure the plasmon resonance shift. Firstly, the optical switch of this molecule is performed. The close form organometallic molecules were assembled to the plasmonic active substrate. In Figure 6.13a it can be observed that the LSPR peak appeared at 669 nm (the blue curve). Note that the resonance peak varies device to device as previously mentioned (compare to Figure 6.9). After 1h light illumination under 700 nm incident light, with the molecular state switched back to open state, a 20 nm blue shift for the LSPR was observed. The new peak position is 649 nm (the red curve), this observation is agree with the finding in organic molecule, but the LSPR shift is slightly higher. In the following cycles the trend can be repeated, but the $\Delta \lambda_{\text{LSPR}}$ slightly lowered to 15 nm, the main reason is that unlike the organic molecule, the organometallic molecule is relative unstable, especially for the open
state. Thus, part of the molecules are possible to be decomposed and result in lowered LSPR shift.

![Graph showing LSPR shifts](image)

**Figure 6.13** (a) The LSPR of nanoparticle array with close state ruthenium based organometallic molecules assembled (blue), and after the molecule switched with visible light (red). (b) The repeated LSPR switch with light illumination. The resonance peak shift back and forth with the change of incident light wavelength.

Finally, the optical and electrochemical stimulations were performed on the same device in order to demonstrate the plasmonic logic gate function. Firstly the organometallic molecules were assembled to the Au nanoparticle array, after which the resonance peak appeared at 627 nm (red curve). Au-organometallic molecule hybrid nanostructure then underwent the 700 nm visible light illumination. Similar to the phenomena observed in previous study, the LSPR peak has a blue shift for about 12 nm. In two cycles the resonance peak shifted according to the variation of molecular state switch. Started from the third cycle the electrochemical stimulation was performed on the system. In the solution the system was firstly applied a 650 mV voltage bias for 1 min, the molecule can be oxidized to $\text{O}^{2+}$. Then a negative -100 mV voltage bias was applied in order to reduce the molecular state back to close form. Similar to the phenomena observed with light illumination, a red shift for LSPR characteristics was detected, indicating that the molecular switch appeared. The plasmon resonance can also be switched back and forth with the molecular switch operation. Thus, the plasmon resonance shifting that controlled by orthogonal inputs, both optically and electrochemically, have been demonstrated.
in the current system. The “OR” logic function is realized with such concept: with the UV light and/or electrochemical stimulation as the inputs, the output, which is $\lambda_{\text{LSPR}}$, can be switched between two different and distinct wavelength. Under such scenario, the $\lambda_{\text{LSPR}}$ in the current device was detected to be 627 nm, corresponding to the combination of Au and close form organometallic molecules. The logic “OR” gate is reversible. Irradiated with 700 nm visible light, the $\lambda_{\text{LSPR}}$ can be switched back to the initial wavelength, which is 615 nm. This plasmonic output is corresponding to the Au-open form organometallic molecules system. Note that due to the device uniqueness such as size, shape and homogeneity, the output wavelength can be different. The key point for this concept is that on the same device, the logic function can be repeatedly demonstrated, and the logic gate is resettable.

In Figure 6.14d the input and corresponding output for liquid phase organometallic molecules as well as the Au-organometallic molecules (solid phase), is summarized. The liquid phase electrochemically operation can be found from reference[18]. Nothing unexpected the liquid phase output is more distinct, with pronounced absorption differentiation and color variation. Considering the output detectability, the molecule level logic operation is more desired. However, in this thesis our main objective is to detect innovative logic operation. For the inputs, orthogonal stimulations were properly selected, both for the electronic and optical logic gates. For output, after the logic gate with electric signals engineered in the last chapter, our purpose is to demonstrate a possibility to realize plasmonic output with orthogonal inputs. Thus, the concept focus on how to engineer a system with distinct output. Compare to the traditional “0” and “1” logic value. Here the logic output is defined as $\lambda_1$ and $\lambda_2$. As stated in Chapter 2, it is somehow difficult to define molecular logic based on the same criteria as that for semiconductor because naturally there are lots of differences on the input and output of them[28,29]. Thus, cautiously here the definition can also be understood as a proof of concept and attempt for possible approach to realize orthogonal stimulations induced “logic operation”.

139
Figure 6.14 (a) The LSPR characteristics detected with open form molecules, and after shined UV light and/or applied electrochemical stimulation to switch the molecule to close state. (b) the repeated LSPR shift with light illumination or electrochemical stimulation. The resonance peak shift back and forth with the change of external inputs. (c) the concept of plasmonic “OR” logic gate, with orthogonal inputs. The output is the LSPR peak position. (d) the output value of plasmonic logic gate in the device tested in above experiment.

6.4 Conclusion

To conclude, the concept of plasmonic “OR” logic gate has been successfully demonstrated with the mechanism of molecular switch at nanoscale. The following conclusions can be draw:

1. The reversible molecular switch in both DTE based organic molecule and organometallic molecule, have been demonstrated. The organic molecule can underwent the reversible state switch with UV/visible light illumination. The organometallic molecule can be switched to close state under UV illumination and/or electrochemical stimulation. It can be switched back with visible light illumination.
2. The fully reversible LSPR peak shift of Au-organic molecule hybrid structure has been successfully demonstrated by control the incident light wavelength. With the combination of Au and close form molecule, the LSPR peak appeared at longer wavelength and it can be switched back with the molecule switched back to open form.

3. The reversible LSPR peak shift of Au-organometallic molecule can be demonstrated by applying light illumination and/or electrochemical stimulation. As a result, a plamonic “OR” logic gate with nanophotonic output has been successfully mimicked.

References


Chapter 7

Discussion and Future Work

In Chapter 7, the general discussion and conclusion will be provided for the whole thesis. In the thesis, under the overall topic of logic function, both electric and optical logic gates with orthogonal inputs were demonstrated at micro or nanoscale. Three achievements were discussed in detail. Firstly, the single nanorod device based optoelectronic memory device has been successfully fabricated. Secondly, integrating the single nanorod based memory device to a ZIF-8 based electrically switchable memory device the memristor based logic gate was demonstrated. Finally, the logic function with optical (plamonic) output was realized by combining the organometallic molecules to the plasmonic active Au nanoparticle array. Additionally, based on the current findings of the research project, the future work that could be conducted will be discussed in this chapter.
7.1 General Discussion

In this thesis, the optical and electronic logic gates with orthogonal inputs have been systematically investigated. Several innovative outcomes were found:

Firstly, for the first time the single nanorod based optoelectronic memory device has been successfully developed. The nanorod device was engineered based on multi-segmented heterostructure. By applying the SPR active Au segments in the nanorod, the photocurrent was significantly enhanced, leading to a desired ON/OFF ratio and thus the performance (duration) of memory device has been improved. Controlling the formation of NiO/CdS interface with chemical approach in order to manipulate the migration of electrons/holes the persistent photocurrent have been detected, in the device prepared on both rigid and flexible substrates. Additionally, the device demonstrated multi-addressable characteristics, by applying various incident light intensity. Thus, the multi-conductance ensured the device could store information at different levels, and improved the information storage capacity significantly. Finally, it was found that in the optically triggered memory device, eventually the information will be automatically erased without external stimulation, this characteristics inspired the demonstration of self-destructive memory device. The concept illustrate that the device have the functions of both information storage and information protection. After specific time horizon the information will be compulsively removed, which could ensure the information security.

Secondly, the single nanorod based optoelectronic memory device was successfully integrated to the circuit with a ZIF-8 based electrically switchable memory device. The ZIF-8 based device, which has similar performance with traditional memory devices, can be switched to LRS under sufficient positive voltage supply. It could be reset back to HRS with reverse voltage bias. Combining the two different types of memory devices into one electric circuit made the system sensitive to multiple
Discussion and Future Work

external stimulations. In the following measurement, the circuit demonstrated three levels of functions:

1) With optical or electric stimulation, or both, the circuit showed an output with LRS, corresponding to the logic value “1”. Thus, the circuit demonstrate the fundamental logic “OR” function.

2) The output does not rely on continuous inputs. With one time optical and/or electric input(s) applied the system has continuous output, indicating it has the memorable behavior. Since the logic circuit was constructed using memory device as component, it demonstrated both logic computation function and memory characteristics.

3) When the system was exposed to both optical and electric stimuli, the logic circuit demonstrated a “self-locking” logic function, which means the output of logic circuit is compulsively “1”. The logic value cannot be erased within the blocking stage, which equals to the time that the optoelectronic memory device took to be self-destructed. Thus, in the “1, 1” input scenario, the circuit demonstrated self-locking memorable logic gate function.

Thirdly, in order to demonstrate the optical logic gate with orthogonal inputs, firstly the organometallic molecules, which were responsive to multiple stimulations, were self-assembled to the plasmonic active Au substrate. The plasmon resonance of the system, was found to the tunable with the switching of molecular state. For the DTE based organic molecule, since it can be switched between the open form and close form with UV/visible light irradiation, the Au-molecule hybrid structure demonstrated the plasmon resonance shifting behavior with changing the molecular state under illumination. For the organometallic molecules, the phenomena can be repeat with multiple stimulations. The system can be switched with optical illumination and/or electrochemical stimulation. Thus, it demonstrated the plasmonic “OR” logic function, with the output of different LSPR peak position.
The logic gate is resettable with visible light irradiation. In this area, the molecular logic functions have been investigated extensively. However, based on our best knowledge this is the first time that the plasmon resonance was controllably shifted in solid state by multiple stimulations, and as a result, the plasmonic logic function was demonstrated.

7.2 Reconnaissance Work for Future Work

In this thesis, the logic functions with electric and optical output and with orthogonal inputs have been successfully demonstrated. The findings could contribute to extend the modulation and function of logic gate. Based on current research, here an outlook for future work will be discussed.

7.2.1 Demonstration of Logic Function in Single Device

In the current thesis, the logic circuit which demonstrated the fundamental “OR” gate function, the memorable logic function and the self-locking logic characteristics has been realized by integrating the single nanorod based optoelectronic memory and the ZIF-8 based electric memory device. However, this approach need to employ two components in one circuit, and the current of electric memory is much higher than the optoelectronic memory. Thus, here one possible approach that could realize the logic function in one device is proposed.

From the discussion in Chapter 2 it can be found that the switching mechanism of sandwich structure memory devices are generally based on the atom migration under electric field. Thus, in metal-insulator (semiconductor)-metal memory structure the switching layer can be selected in a wide range of materials. In fact, CdS nanobelt based floating nanodot gate memory has been successfully developed by Wu and the co-authors\textsuperscript{[1,2]}. The device shows a typical memory performance (Figure 7.1a), and information can be written or erased with positive or negative voltage bias.
Figure 7.1 (a) The structure of floating nanodot gate memory fabricated by CdS FET and Au nanodots. The curves show the $I_{DS}-V_{GS}$ characteristics of device operated under ±1, ±3, ±5 V windows. (b) The read/write/erase operations by applying 5 V and -5 V voltage bias with 200 ms duration$^{[1]}$.

In the preliminary measurement, the resistive switching behavior has been triggered in simple Au-CdS-ITO sandwich structure, as shown in Figure 7.2a. The up layer of Au was evaporated, and the CdS layer was developed electrochemically. The device demonstrated a typical I-V characteristics of memory device. In the future, the sandwiched structure can be improved to the Au-Ni/NiO-CdS-ITO structure. By electrochemically depositing the CdS and Ni/NiO layer with the strategy discussed in Chapter 3 and Chapter 4, the structure may be responsive to light illumination as well. Thus, the logic function may be realized in one single nanodevice.
Figure 7.2 (a) The typical I-V characteristics for an Au-CdS-ITO sandwich structure. The CdS was electrochemically deposited on the ITO substrate, and Au layer was evaporated subsequently. (b) The design of Au-Ni/NiO-CdS-ITO sandwiched structure that is expected to demonstrate the logic function.

7.2.2 Time Dependent Automatic Hierarchical Storage

In Chapter 4 the optoelectronic memory device performance has been discussed in detail. Based on the results showed in Figure 4.9a and Figure 4.15, the photocurrent of optoelectronic memory device continuously damped with time. The proposal is inspired by the design that to integrate photodiode and memory device, by which the photodiode could set a compliance current for the whole circuit, and achieve multi-level data storage (Figure 1.3).

Similar optically driven multi-level conductance was reported by Tim Leydecker et al.\cite{3}, on a photochromic diarylethene based polymer semiconductor. With the stimulation from a 3 ns laser pulses the conductivity of device decreased gradually, and generated 256 (8 bit storage) distinct conductance states. Figure 7.3 is a summary of their design and performance measurement.
Figure 7.3 (a) The chemical structure of DAE, with open form and close form. (b) the $I_{DS}$-$V_{GS}$ characteristics for the open and close form of DAE. (c) the multi-level conductance of device obtained by gradually irradiate the DAE. (d) the $I_{DS}$-time curve for the device measured with 3 ns laser pulse. The current decreased gradually and generated multi-level conductance for 8 bit information storage$^{[3]}$.

Based on the above mentioned multi-level conductance design, the time dependent automatic hierarchical storage is proposed in Figure 7.4. The optoelectronic memory device will be connected in series with the electric memory device. The output of electric circuit will be determined by the current generated from the single nanorod based device. The current generated from the optoelectronic memory can be controlled by binary factors: the incident light intensity and time. Thus, the information storage level can be initially selected by properly decide the incident light intensity. More importantly, the photocurrent of optoelectronic memory damped continuously with time past, result in the compliance current for the circuit drop correspondingly, so the electric memory device can be set to different level. The automatic hierarchical storage can be realized based on time horizon. This concept in agree with the timeliness of information (separately managed based on
their timeliness). In theory, the conductance level that could be generated is infinite, so that provide sufficient space for information storage.

![Circuit Design](image)

**Figure 7.4** (a) The circuit design illustrated the concept realization of automatic hierarchical information storage. The optoelectronic memory device will be integrated with electric memory device by series connection. The initial current can be adjusted with incident light intensity. (b) the hypothesis that information can be stored to different levels at different time, and realize the hierarchical storage based on the timeliness of information.

Admittedly, to realize such idea firstly the current of optoelectronic and electrically switchable memory devices need to be matched. In Chapter 4 it is measured that the peak photocurrent of optoelectronic memory is $10^{-7}$ A-$10^{-6}$ A. Thus, ideally the electric memory could be set to LRS with the compliance current lower than $10^{-9}$
A. Technically the material and fabrication technology need to properly selected. Alternatively, the single nanorod based device can be replaced by the nanorod array. With enhanced photocurrent the current of two components may also be aligned.

7.2.3 Plasmonics in Tunable Gap Structure

In Chapter 6 the plasmonic logic function was realized by assemble the molecules to the Au nanoparticle array and then tuning the molecular state. The Au nanoparticle array substrate was prepared by thermo-evaporation with ultra-thin AAO membrane as template. The idea started with changing the substrate and to tune the plasmonic characteristics as a result. In Chapter 2 it was reviewed that one of the approach is to coat a layer of polymer on the substrate, and with the polymer state change by electrochemical stimulation, the plasmon resonance can be changed as well.

On top of the electrochemically tunable plasmon shift, another approach is to use the thermo-responsive characteristics of hydrogel. The hydrogel can be switched between swollen and collapse state by controlling the temperature. A typical work was report by Wang and the co-workers[4], the design and results are summarized in Figure 7.5. The bowtie nanoantenna arrays was coated with hydrogel and it was found that with increase the temperature the reflection peak showed a red shift gradually.

However, in this study the reflection peak shift was not dramatic. A new design is proposed based on the heterostructure of Au-Ni-Au nanoparticle array. In Figure 7.6a the experimental design schematic is shown. With a layer of hydrogel coated on the Au-Ni-Au array, the structure is fixed after cross-linking the hydrogel. Then the Ni layer can be etched with HCl, after which the nanogap array can be engineered. By controlling the temperature the hydrogel could change between the collapse and swollen state, and the gap size will be tuned correspondingly.
Figure 7.5 (a) The design of bowtie nanoantenna arrays and the process of coating hydrogel. (b) and (c) the SEM images of the Au nanoantenna arrays with and without coating a layer of hydrogel. (d) the reflection measurement under different temperature for the array without hydrogel. (e) the reflection measured by changing temperature on the bowtie nanoantenna arrays with hydrogel coated.

With different gap size in such nanoarray, the coupling peak should vary dramatically. Which could be supported by the simulation result in Figure 7.6b. It can be observed that in the nanoparticle array, assume the period is 460 nm and the diameter is 150 nm, there is a strong coupling peak near 1000 nm when the gap size is 10 nm, and the peak will disappear with the gap size extended to 50 nm. When the hydrogel switch between the collapse and swollen state the thickness could change for 10 times. Hence, if the original gap size is designed to be 10 nm, it can be tuned between 10 nm to 100 nm. The coupling peak can appear and disappear by controlling temperature.
Figure 7.6 (a) The design of tunable gap structure for the purpose of controlling plasmon resonance characteristics. The Au-Ni-Au nanoparticle array structure was fabricated on a glass substrate. The structure was coated with hydrogel and then with the Ni layer etched the gap structure can be tuned with temperature change, which will result in the hydrogel tuned between collapse and swollen state with significant thickness variation. (b) the simulated transmission for the gap size of 10 nm (black) and 50 nm (red). The coupling peak disappears with the gap widening and reappear when it gets narrowed. (c) dimension of the nanostructure for simulation. The period is 460 nm and diameter is 150 nm.

7.3 Conclusion

The optical and electronic logic gates with orthogonal inputs, have been demonstrated at micro and nanoscale. The electronic logic function was realized in memristor based circuit, while the optical logic function was achieved by combining the plasmonic active nanoparticle array with the multi-switchable organometallic molecules.
For future work, the logic function can be realized in one single device. Additionally, the automatic hierarchical storage function is expected to be realized by integrate different memory components. Furthermore, inspired by the plasmonic active nanoparticle array design, a tunable gap structure was proposed to achieve switchable plasmon resonance characteristics.

References