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Circuit Model of Microstrip Patch Antenna on Ceramic Land Grid Array Package for Antenna-Chip Codesign of Highly Integrated RF Transceivers

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Abstract—This paper presents the circuit model of a microstrip patch antenna on a ceramic land grid array (CLGA) package for the antenna-chip codesign of a highly integrated radio-frequency (RF) transceiver. The microstrip patch antenna is fed by packaging interconnect components such as bond wires, signal traces, and vias in a ground-signal-ground (G-S-G) configuration from the carried chip. The circuit model that consists of RLC lumped elements of both microstrip patch antenna and feeding interconnect components has been developed with an emphasis on verifying existing or deriving analytical formulas. The RLC values of the microstrip patch antenna are calculated with our improvements to existing computer-aided design formulas, while the RLC values of the feeding interconnect components are calculated with more efforts. In particular the C values related to the vias and signal traces require to be calculated numerically and they are calculated here with the method of moments and the conformal mapping method, respectively. The circuit model is validated with numerical simulations (High Frequency Structure Simulator) and network analyzer measurements.

Index Terms—Ceramic land grid array package (CLGA), circuit model for antenna-chip codesign, integrated circuit package antenna (ICPA), low temperature co-fired ceramic (LTCC) technology, single-chip radio-frequency (RF) transceivers.

I. INTRODUCTION

HIGHLY integrated radio-frequency (RF) transceivers have been developed in deep submicron complementary metal oxide semiconductor (CMOS) technology for wireless local area network (WLAN) applications recently. Typical RF transceivers designed in 0.18-μm CMOS for WLAN operation at 5.8 GHz have die sizes less than 16 mm² [1]. An antenna is a critical component for any RF transceiver. It is well known that the antenna requires a considerable volume for efficient radiation. The integration of an efficient antenna on the same die with other transceiver circuits is not economically feasible and let alone the lossy nature of CMOS that greatly reduces the antenna radiation efficiency. As a result, the antenna is left external to the chip (or chips) in virtually all solutions of RF transceivers.

To provide RF transceivers with compatible antennas, dielectric chip antennas have been developed in low-temperature co-fired ceramics (LTCC) technology [2]. Dielectric chip antennas are physically small but still discrete. They need to be assembled with RF transceivers on printed circuit boards to realize functional wireless systems. It should be also noted that previous work has involved integrating cavity-backed patch antennas [3], [4] or stacked patch antennas [5] directly on the transceiver modules using LTCC process for system-on-package (SOP) applications. To better match with highly integrated RF transceivers, Zhang has proposed to integrate antennas on or in chip packages in LTCC technology [6]. An antenna implemented in this manner is known as integrated circuit package antenna simply integrated circuit package antenna (ICPA) [7]. An ICPA offers the possibility to combine an antenna and a single-chip RF transceiver die into a standard surface mounted device. Thus, the assembly cost and printed circuit board area of a discrete dielectric chip antenna can be saved. Also, the ICPA offers the possibility of the antenna-chip codesign of a RF transceiver without the constraint of 50-Ω common impedance interface between the antenna and the chip. The 50-Ω standard was optimized for interconnect matching with a coaxial cable. Whereas in chips and packages, signal traces, vias, and bond wires are utilized for interconnect. In addition, MOS transistors are capacitive devices and inductors are employed to match MOS transistors to 50 Ω for acceptable RF performance. Inductors consume larger die area and have poor quality factor. The removal of any on-chip inductor is rather desirable. In the antenna-chip codesign at least two on-chip inductors for matching the low noise amplifier (LNA) to the 50-Ω antenna can be eliminated. We can determine the feed location of the antenna to be inductive (rather than 50 Ω) so as to resonate with the capacitive impedance of the MOS transistors in the low noise amplifier of the receiver [8]. The antenna-chip codesign has to be implemented in a circuit simulator, say, Cadence RF Spectra. All circuit simulators rely on circuit models. Thus, the development of a circuit model for the ICPA is of great importance.

Any printed circuit antenna can be used for the ICPA. A microstrip patch antenna is chosen because in-depth knowledge on the antenna is available and the microstrip patch enhances the ICPA thermal performance. For the microstrip patch antenna, it is usually modeled as a simple parallel resonant RLC circuit. A lot of work has been done to calculate the RLC values in the circuit model [9]–[12]. In this paper, more accurate improvements to the existing calculations have been made. Furthermore, like an inductor added to represent the probe feed of the microstrip antenna, a few RLC subcircuits have been
included to model the feeding interconnect components: bond wires, signal traces, and vias in the G-S-G configuration from the carried chip in the ICPA. The details of the ICPA in ceramic land grid array (CLGA) package format and its equivalent circuit model are described in Section II. The validation of the circuit model with the High Frequency Structure Simulator (HFSS) simulations and measurements is made in Section III. Finally, the conclusions are summarized in Section IV.

II. ICPA IN CLGA PACKAGE AND ITS CIRCUIT MODEL

CLGA packages reduce integrated circuit mounted height by eliminating the solder balls that are used for mounting CBGA packages to printed circuit boards. CLGA packages are designed for enhanced thermal operation, improved RF performance and resistance to mechanical stress failures.

Fig. 1 shows the ICPA in the custom designed cavity-down 48-land thin CLGA package format. The ICPA consists of three co-fired laminated ceramic layers, with a bare chip cavity formed in the middle. There are two buried layers and one top-layer metallization in the construction. The lower buried layer provides the metallization for the signal traces, while the upper buried layer provides the metallization for the ground plane of the ICPA. The microstrip patch antenna of the ICPA is realized with top-layer metallization. The single-chip RF transceiver die is attached facing downwards on the ground plane with conductive adhesive. There are 48 signal traces; the outer ends of 48 signal traces are connected to 48 lands through 48 vias, while the inner ends of 48 signal traces are connected to the single-chip wireless transceiver die through 48 bond wires.

The conventional feeding techniques for microstrip patch antennas are probe-feeding and aperture coupling. They are not suitable to feed the microstrip patch radiating element in the ICPA. It is seen from Fig. 1 that the microstrip patch antenna of the ICPA is fed by packaging interconnect components such as bond wires, signal traces, and vias in a G-S-G configuration from the carried chip. The proposed equivalent circuit model of the ICPA feeding network is shown in Fig. 2.

As can be seen from Fig. 2, the microstrip patch antenna, the feeding via under the ground plane, the G-S-G signal traces, the G-S-G bond wires, the vias to lands and lands are represented with the corresponding equivalent RLC subcircuits.

A. Circuit Model of Microstrip Patch Antenna

The RLC values in the circuit model of the microstrip patch antenna are calculated below. The feeding via above the ground plane is represented by an inductive reactance term [9]

$$XL = \frac{377 f_r H}{\alpha_0} \ln \left( \frac{c_0}{\pi f_r d_{uv} \sqrt{\varepsilon_r}} \right)$$

where $c_0$ is the velocity of light, $d_{uv}$ is the diameter of the feeding via, $H$ is the thickness of the substrate between the microstrip patch and ground plane, $\varepsilon_r$ is the relative permittivity of the substrate, and $f_r$ is the resonant frequency of the microstrip patch antenna. The $L_{XL}$ in Fig. 2 is the equivalent inductance for the feeding via above the ground plane.
The resonant resistance $R_a$ of the parallel RLC circuit is given by [9]:

$$R_a = \frac{Q_{total} H}{\pi f_r \varepsilon_{dyn} \varepsilon_0 W_{eff}} \cos^2 \left( \frac{\pi X_{eff}}{L_{eff}} \right)$$  \hspace{1cm} (2)$$

where we propose an effective length $L_{eff}$ to take into account the influence of the fringing field at the corners and the dielectric inhomogeneity of the ICPA; accordingly, the distance from the feeding point to the patch edge $X$ is replaced by

$$X_{eff} = X + \frac{(L_{eff} - L)}{2}.$$  \hspace{1cm} (3)

In (2) $\varepsilon_{dyn}$ is the dynamic permittivity, which is a function of the dimensions of the ICPA and relative permittivity $\varepsilon_r$ as well as the different modes field distribution [13]. In the calculation of $\varepsilon_{dyn}$, $C_{e1,stat}(\varepsilon)$ represents the edge capacitance on one side of a patch length $L$ and $C_{e2,stat}(\varepsilon)$ represents the edge capacitance on one side of a patch width $W$. $C_{e1,stat}(\varepsilon)$ is given by

$$C_{e1,stat}(\varepsilon) = \frac{1}{2} \left[ C_t(W, H, \varepsilon_r) - \frac{\varepsilon_{\varepsilon_r} W}{H} \right] L$$  \hspace{1cm} (4)$$

where $C_t(W, H, \varepsilon_r)$ is the total capacitance of the microstrip patch of width $W$ [14]. To obtain $C_t(W, H, \varepsilon_r)$, the modulus of the integrals $m$ is first calculated as

$$\frac{W}{2H} = \frac{2}{\pi} K'(m)Z_n \left( \frac{\phi_1}{\alpha} \right)$$  \hspace{1cm} (5)$$

Second, the equation of the curve $\upsilon(u)$, which separates the two dielectrics, is given by

$$\sin \left( \frac{\upsilon}{m_1} \right) = g \left( \frac{u}{m_1} \right)$$

$$= \left\{ \frac{\cosh \left( \frac{u}{m_1} \right) \ln \left( \frac{u}{m_1} \right)}{2 K'(m) - \frac{\pi u}{2K(m)K'(m)} - Z_n \left( \frac{u}{m_1} \right) \cosh^2 \left( \frac{u}{m_1} \right) + \cosh^2 \left( \frac{u}{m_1} \right) \right\}^{-\frac{1}{2}}$$  \hspace{1cm} (6)$$

where $m_1 = 1 - m$

$$\upsilon(u) = \sin^{-1} \left( \frac{u}{m_1} \right) = F \left( \frac{\phi_3}{m_1} \right)$$

here $\phi_3 = \sin^{-1} \left[ g(u/m_1) \right]$.

A number of values of $u$ between 0 and $K(m)$ are selected, and the respective values of $\upsilon$ can be calculated.

Third, once the voltages at all nodes in the column next to a metal plate are known, the total capacitance of the microstrip patch of width $W$ can be obtained through the calculation of total surface charge $Q_s$. The relative effective permittivity $\varepsilon_{eff}$ can be calculated as

$$\varepsilon_{eff}(W) = \sum_{k=1}^{N} \varepsilon_{rk} \Delta V_k$$  \hspace{1cm} (7)$$

where $\varepsilon_{rk}$ is the permittivity at $k$ subsection, $\Delta V_k$ is the voltage difference at $k$ subsection between the node at the conductor plate and the node at the conductor plate, $N$ is the number of subsections.

Finally, the capacitance of the microstrip line with width $W$ will be calculated as

$$C_t(W, H, \varepsilon_r) = \frac{2}{\pi} \varepsilon_{eff}(W) \varepsilon_0 K'(m) \frac{K(m)}{H}$$  \hspace{1cm} (8)$$

Similarly, $C_{e2,stat}(\varepsilon)$ is given by

$$C_{e2,stat}(\varepsilon) = \frac{1}{2} \left[ C_t(L, H, \varepsilon_r) - \frac{\varepsilon_{\varepsilon_r} L}{H} \right] W.$$  \hspace{1cm} (9)$$

The advantage of utilizing the above method is the exact determination of the curve that separates the two dielectrics in the transformed plane, so $C_t(W, H, \varepsilon_r)$ is more accurate than the traditional analytical formula derived in [9].

$Q_{total}$ is the quality factor associated with system losses, which include radiation losses from the walls $Q_r$, losses in the dielectric $Q_d$ and losses in the conductor $Q_c$.

$$\frac{1}{Q_{total}} = \frac{1}{Q_r} + \frac{1}{Q_c} + \frac{1}{Q_d}$$  \hspace{1cm} (10)$$

where $Q_r$, $Q_d$ and $Q_c$ are given by [6]

$$Q_r = \frac{\varepsilon_0 \sqrt{\varepsilon_r}}{4 f_r H}$$  \hspace{1cm} (11)$$

$$Q_d = \frac{1}{T_g}$$  \hspace{1cm} (12)$$

$$Q_c = \frac{7860 \sqrt{f_r} \times Z_{a0}(W) \times H_{ol}}{P_n}$$  \hspace{1cm} (13)$$

where $T_g$ is the dielectric loss tangent; $f_r$ is in GHz, $Z_{a0}(W)$ is the impedance of an air filled microstrip patch of width $W$ and thickness $H$, which is evaluated from $Z_{a0}(W)$ by setting $\varepsilon_r = 1$. 
The impedance of the dielectric filled microstrip patch of width \( W \) is given as

\[
Z_d(W) = \frac{\sqrt{\varepsilon_{\text{eff}}(W)}}{c_0 C_{tu}(W, H, \varepsilon_r)}
\]  

(14)

and

\[
P_d(W) = \frac{2\pi \left[ \frac{W}{H} + \frac{\varepsilon_{\text{eff}}(W)}{\varepsilon_r} \right]}{\left( \frac{W}{H} + \frac{\varepsilon_{\text{eff}}(W)}{\varepsilon_r} \right)^2} \left( 1 + \frac{H}{W} \right).
\]  

(15)

As mentioned before, \( f_r \) is the resonant frequency of the microstrip patch antenna at which the real part of the input impedance reaches the maximum, the additive reactance term \( XL \) does not modify the value of the resonant frequency

\[
f_r = \frac{c_0}{2\sqrt{\varepsilon_{\text{dyn}}}} \left( \frac{m}{W_{\text{eff}}} + \frac{n}{L_{\text{eff}}} \right)^{1/2}.
\]  

(16)

The effective width \( W_{\text{eff}} \) and length \( L_{\text{eff}} \) are calculated from the following relation:

\[
L_{\text{eff}} = L + \left( \frac{W_{\text{eq}} - W}{2} \right) \left( \frac{\varepsilon_{\text{eff}}(W) + 0.3}{\varepsilon_{\text{eff}}(W) - 0.258} \right).
\]  

(17)

where \( W_{\text{eq}} \) is the equivalent width calculated from the planar waveguide model

\[
W_{\text{eq}} = \frac{120\pi H}{\varepsilon_{\text{eff}}(W) c_0}.
\]  

(18)

Similarly, we can calculate \( W_{\text{eff}} \) by replacing \( L_{\text{eff}}, L, W_{\text{eq}}, W \) and \( \varepsilon_{\text{eff}}(W) \) with \( W_{\text{eff}}, W, L_{\text{eq}}, L \) and \( \varepsilon_{\text{eff}}(L) \), respectively.

Finally, the capacitance and inductance of the microstrip patch antenna are calculated by

\[
C_a = \frac{Q_{\text{total}}}{2\pi f_r R_a},
\]  

(19)

\[
L_a = \frac{R_a}{2\pi f_r Q_{\text{total}}}.
\]  

(20)

The dispersion effect of \( \varepsilon_{\text{eff}} \) in frequency domain is considered in this work. An accurate equation for evaluating the dispersion effect in frequency domain is given below [15]

\[
\varepsilon_{\text{eff}}(W, f) = \varepsilon_r - \frac{\varepsilon_r - \varepsilon_{\text{eff}}(W, 0)}{1 + P}
\]  

(21)

where

\[
P = \left( \frac{H}{Z_{\text{tot}}(W)} \right)^{1.23} \left[ 0.43 f^2 - 0.009 f^3 \right]
\]  

(22)

where \( H \) is in millimeters and \( f \) in GHz. Similarly, we can calculate \( \varepsilon_{\text{eff}}(L, f) \) by replacing \( \varepsilon_{\text{eff}}(W, 0) \) and \( \varepsilon_{\text{eff}}(W, f) \) with \( \varepsilon_{\text{eff}}(L, 0) \) and \( \varepsilon_{\text{eff}}(L, f) \), respectively.

B. Circuit Model of Feeding via Under Ground Plane

\( L_{\text{v,lower}} \) and \( R_{\text{v,lower}} \) are the inductance and resistance of the feeding via under ground plane. The inductance is calculated by

\[
L_{\text{v,lower}} = 20 L_{\text{v,lower}} \left[ \ln \left( \frac{2 L_{\text{v,lower}}}{r_{\text{v,lower}}} \right) - 1 \right] \text{nH}
\]  

(23)

where \( L_{\text{v,lower}}, r_{\text{v,lower}} \) are the length and the radius of the feeding via (in millimeters) under the ground plane

\[
R_{\text{v,lower}} = \frac{L_{\text{v,lower}}}{\sigma S_{\text{v,lower}}}
\]  

(24)

where \( L_{\text{v,lower}}, S_{\text{v,lower}}, \) and \( \sigma \) are the length, the cross-section area, and the conductivity of the feeding via under the ground plane.

\( C_{\text{v,lower}} \) is the capacitance between the feeding via under the ground plane and the ground plane as well as the shorting vias. It is calculated by the method of moments.

C. Circuit Model of G-S-G Signal Traces

\( C_{\text{sig}} \) is the capacitance of the signal traces, which is a CPW structure and calculated by the conformal mapping method [16]

\[
C_{\text{sig}} = 2 \varepsilon_0 \varepsilon_{\text{eff}} \left[ \frac{K(k_1)}{K'(k_1')} + \frac{K(k_2)}{K'(k_2')} \right] \times l_s
\]  

(25)

where \( K(k_1) \) is the complete elliptic integrals of the first kind

\[
\varepsilon_{\text{eff}} = 1 + q_1 (\varepsilon_r - 1) + q_2 (\varepsilon_r - 1)
\]  

\[
q_1 = \frac{K(k_1)}{K'(k_1')} \left[ \frac{K(k_1)}{K'(k_1')} \right]^{-1}
\]  

\[
q_2 = \frac{K(k_2)}{K'(k_2')} \left[ \frac{K(k_2)}{K'(k_2')} \right]^{-1}
\]  

\[
k_0 = \frac{s_s}{s_s + g_s}
\]  

\[
k_1 = \frac{\sinh \left[ \frac{\pi (s_s + g_s)}{2 \Delta s_{2}} \right]}{\sinh \left[ \frac{\pi g_s}{2 \Delta s_{2}} \right]}
\]  

(26)

\[
k_2 = \frac{\sinh \left[ \frac{\pi (s_s + g_s)}{2 \Delta s_{2}} \right]}{\sinh \left[ \frac{\pi g_s}{2 \Delta s_{2}} \right]}
\]  

where \( l_s \) is the length of the signal trace, \( h_{s1} \) and \( h_{s2} \) are the height from signal trace to ground plane and from signal trace to land, respectively, \( g_s \) is the signal trace gap, \( s_s \) is half the signal trace width.

The signal trace inductance \( L_{\text{sig}} \) is calculated by the following equation [17]:

\[
L_{\text{sig}} = \frac{u_t l_s}{2\pi} \left\{ \arcsin \left[ \frac{l_s}{u_t} \right] + \frac{l_s}{u_t} \left[ \left\{ 1 + \frac{l_s}{u_t} \right\}^2 - 1 \right] \right\}
\]  

(27)

where \( u_t \) is the width of the signal trace, \( t \) is the thickness of the signal trace, \( l_s \) is the length of the signal trace. In Fig. 2, \( L_{\text{stch}} \) and \( L_{\text{stov}} \) represent the inductances of the signal trace, the lengths of which are the signal trace to the bond wire and the signal trace to the via connecting the land, respectively.
D. Circuit Model of G-S-G Bond Wires

The inductance and capacitance of the bond wire are given as follows [18]:

\[
L_w = 2l_w \ln \left( \frac{4h_w}{d_w} \right) \text{nH} \tag{28}
\]

\[
C_w = \frac{0.5563l_w}{\ln \left( \frac{4h_w}{d_w} \right)} \text{pF} \tag{29}
\]

where \(l_w, d_w,\) and \(h_w\) are in cm, \(l_w, d_w,\) and \(h_w\) are the length of the bond wire, the diameter of the bond wire, and the distance from the bond wire to the ground plane, respectively. Here it should be mentioned that the grounded bond wires slightly reduces the inductance of the signal bond wire as calculated by (28) and the encapsulant slightly increases the capacitance of the signal bond wire as calculated by (29). The resistance of the bond wire also approximates using the same formula as the feeding via under the ground plane.

E. Circuit Model of Lands

\(C_{\text{via}}, R_v,\) and \(L_v\) are the capacitance, resistance and inductance of the vias connecting the lands. \(C_{\text{via}}\) is again obtained using Method of Moments. \(R_v\) and \(L_v\) are calculated as the same equations for the feeding via under ground plane.

\(C_{\text{lg}}\) is the capacitance of the lands. It is again calculated using the conformal mapping method

\[
C_{\text{lg}} = 2 \varepsilon_0 \varepsilon_{\text{eff}} \left[ \frac{K(k_0)}{K(k'_0)} + \frac{K(k_1)}{K(k'_1)} \right] \times h_l \tag{30}
\]

where

\[
\varepsilon_{\text{eff}} = 1 + q_1 (\varepsilon_r - 1)
\]

\[
q_1 = \frac{K(k_1)}{K(k'_1)} \left( \frac{K(k_0)}{K(k'_0)} + \frac{K(k_1)}{K(k'_1)} \right)^{-1}
\]

\[
k_0 = \frac{s_t}{s_t + g_l} \tan(h_l \frac{\pi k_0}{2h_l})
\]

\[
k_1 = \frac{\tanh (\frac{\pi k_1}{2h_l})}{\tanh (\frac{\pi (s_t + g_l)}{2h_l})} \tag{31}
\]

where \(h_l\) is the length of the land, \(h_l\) is the height from land to ground plane, \(g_l\) is the gap between lands, and \(s_t\) is half the land width.

III. VALIDATION OF THE CIRCUIT MODEL

In this section, the modeled results are discussed and validated with HFSS simulations and measurements for a typical ICIA. The ICIA is designed with Ferro-A6 LTCC material system with dielectric constant of 5.9 and loss tangent of 0.002 at 6 GHz. Fig. 3 shows the photo of the fabricated microstrip patch antenna part of the ICIA. The ICIA measures \(17 \times 17 \times 1.6\) mm\(^3\). The thickness of the top, middle, and bottom layers are 0.8, 0.4, and 0.4 mm, respectively. The vias have the same diameter of 100 \(\mu\)m. The signal traces have the same size of \(2 \times 0.4\) mm\(^2\). The lands are squares with a length of 0.34 mm. The feeding via to the microstrip patch is 1.2 mm long, while the other vias to the ground plane and lands are 0.4 mm long. The aperture on the ground plane for the feeding via to pass through is 0.6 mm in diameter. The feeding and grounded bond wires with a diameter of 32.5 \(\mu\)m are 1.22 mm long. Referring to Fig. 1, the dimensions of the microstrip patch antenna are: \(L = 9.9\) mm, \(W = 15\) mm, \(X_0 = 0.9\) mm, \(Y_0 = 1.4\) mm, \(X = 2.35\) mm, and \(Y = 7.5\) mm.

A. Microstrip Patch Antenna Results

Fig. 4 shows the measured, modeled, and simulated return loss for the microstrip patch antenna. The result calculated by the method in [9] is also included for comparison purpose. As can be seen from Fig. 4, the center frequencies of the impedance bandwidth are 5.9, 5.83, 5.84, and 6.24 GHz for the measured, modeled, simulated, and calculated results, respectively. The difference between the measured and our modeled is only 0.07 GHz (0.07/5.9 = 1.19%), while the difference between the measured and calculated from the method in [9] is 0.34 GHz (0.34/5.9 = 5.76%).

Fig. 5 shows the measured, modeled and simulated input impedance, it shows the calculated input impedance from [9] as well. The resonant frequencies are 5.83, 5.7, 5.77, and 6.15 GHz from the measured, modeled, simulated, and calculated results, respectively. The difference between the measured and our modeled is only 0.13 GHz (0.13/5.83 = 2.2%), while the difference between the measured and calculated is 0.32 GHz (0.32/5.83 = 5.5%).

The resonant resistance of the \(RLC\) parallel circuit is 89.3 \(\Omega\), 85.45 \(\Omega\), 87.7 \(\Omega\), and 103.05 \(\Omega\) from the measured, modeled, simulated, and calculated results, respectively. The difference between the measured and our modeled is 3.85 \(\Omega\) (3.85/89.3 =
input impedance is zero, we have 5.822 and 5.745 GHz from the modeled and simulated results, respectively. The difference between our modeled and the simulated is only 0.077 GHz (0.077/5.745 = 1.34%) The modeled and simulated resonant resistance are 26.5 Ω and 25.7 Ω, respectively. The difference is 0.8 Ω (0.8/25.7 = 3.1%).

IV. Conclusion

A circuit model of a microstrip patch antenna on a CLGA package was developed with an emphasis on verifying existing or deriving analytical formulas. The circuit model considered the microstrip patch antenna fed by packaging interconnects such as bond wires, signal traces, and vias in a G-S-G configuration from the carried chip. The model was validated with the HFSS simulations and measurements, it is well suitable for the antenna-chip codesign of a highly integrated RF transceiver.

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REFERENCES

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