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<th>Analysis and design of power efficient class D amplifier output stages (Published version)</th>
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<td><strong>Author(s)</strong></td>
<td>Chang, Joseph Sylvester; Tan, Meng Tong; Cheng, Zhihong; Tong, Yit Chow</td>
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Transactions Briefs

Analysis and Design of Power Efficient Class D Amplifier Output Stages
Joseph S. Chang, Meng-Tong Tan, Zhihong Cheng, and Yit-Chow Tong

Abstract—A Class D amplifier comprises a pulse width modulator and an output stage. In this paper, we analyze the power dissipation mechanisms and derive the overall power efficiency of the output stage realized using the finger and waffle layouts. We compare the relative merits of these layouts. We propose two design methodologies to determine the aspect ratios of the transistors in the output mode for optimum power efficiency (op-

Index Terms—Amplifier, Class D, efficiency, optimization, output stage.

LIST OF PARAMETERS USED

\[ \begin{align*}
\alpha & \quad W_s/W_m, \\
\beta & \quad \text{Gain factor } (\mu A N^2) \text{ of a MOS Transistor (MOST)}. \\
\beta_m & \quad \text{Gain factor of an } n\text{ MOST}. \\
\beta_p & \quad \text{Gain factor of a } p\text{ MOST}. \\
C_{GSD} & \quad \text{Gate-to-source capacitance per unit gate width}. \\
C_{GDSO} & \quad \text{Gate-to-drain capacitance per unit gate width}. \\
C_{GHO} & \quad \text{Gate-to-substrate capacitance per unit gate width}. \\
C_f & \quad \text{Zero-biased } n\text{-junction area capacitance}. \\
C_{JSW} & \quad \text{Zero-biased } p\text{-junction periphery capacitance}. \\
C_l & \quad \text{Output filter capacitance}. \\
C_{ox} & \quad \text{Oxide capacitance per unit gate area}. \\
C_p & \quad \text{Total parasitic capacitance}. \\
C_{pad} & \quad \text{Bond pad capacitance}. \\
D & \quad \text{Modulation index } (V_c/V_s). \\
\varepsilon_{ox} & \quad \text{Permittivity of the gate oxide}. \\
f_c & \quad \text{Triangular signal (carrier) frequency}. \\
f_s & \quad \text{Input signal frequency}. \\
\eta & \quad \text{Efficiency of the amplifier } (\eta = P_{OUT}/P_{IN}). \\
i_{DD} & \quad \text{Supply current}. \\
i_o & \quad \text{Load current}. \\
I_0 & \quad \text{Maximum output current } (V_{DD}/R_L). \\
I_{mean} & \quad \text{Mean value of the short-circuit current}. \\
L & \quad \text{Channel length of a MOST}. \\
L_m & \quad \text{Channel length of an } n\text{ MOST}. \\
L_p & \quad \text{Channel length of a } p\text{ MOST}. \\
L_{DS} & \quad \text{Length of the source or drain area}. \\
L_o & \quad \text{Output filter inductance}. \\
P_E & \quad \text{Total power drawn from the supply}. \\
P_{out} & \quad \text{Output power at the load}. \\
\end{align*} \]

\(R_{ctn}\) \quad n-type contact resistance per contact.
\(R_{ctp}\) \quad p-type contact resistance per contact.
\(r_{on}\) \quad Total on-resistance of a Class D bridge output stage.
\(R_L\) \quad Load resistance.
\(R_n\) \quad Source or drain area resistance per square of an n MOST.
\(R_p\) \quad Source or drain area resistance per square of a p MOST.
\(\tau\) \quad Rise or fall time of a PWM signal.
\(T\) \quad Tapering factor of a string of inverters. [7]
\(t_{ox}\) \quad Gate oxide thickness.
\(\mu_n\) \quad Electron mobility.
\(\mu_p\) \quad Hole mobility.
\(V_{DD}\) \quad Supply voltage.
\(V_{GS}\) \quad Gate-to-source voltage.
\(V_{DS}\) \quad Drain-to-source voltage.
\(V_c\) \quad Peak voltage of the input signal.
\(V_{c}\) \quad Peak voltage of the triangular carrier signal.
\(V_{th}\) \quad Threshold voltage of a MOST.
\(V_{th,n}\) \quad Threshold voltage of an n MOST.
\(V_{th,p}\) \quad Threshold voltage of a p MOST.
\(W_n\) \quad Channel width of the n MOST output stage inverter.
\(W_p\) \quad Channel width of the p MOST output stage inverter.

I. INTRODUCTION

There is a continuing demand including auditory prosthesis [1] and hearing instruments (aids) [2]–[6] for circuits featuring micropower, low voltage and small IC area. The Class D amplifier, depicted in Fig. 1, is often used as the power amplifier in hearing instruments due to its high efficiency (>80%) over a large modulation index range (output signal swing). Despite the recent interest in several low-voltage low-power Class D amplifier designs and architectures [3]–[6], the design and optimization (in terms of power efficiency) of the output stage of the Class D amplifier remain largely empirical: design the aspect ratio of the transistors of the output stage to be as large as tolerable so as to obtain an output stage with a low on-resistance, typically <30\,\Omega.

In this paper, we show that the empirical design methodology does not necessarily yield an optimized design. We analyze the power dissipation mechanisms and derive the overall power efficiency of the Class D output stage for the finger and waffle layouts. We show that there is a tradeoff between the different power dissipation mechanisms when designing the output transistor aspect ratios. We propose two novel design methodologies leading to mathematical expressions that specify the optimized aspect ratios of the output stage transistors, optimized in terms of the power efficiency for a given fabrication process, supply voltage, and load resistance.

II. POWER DISSIPATION MECHANISMS

The Class D amplifier, as depicted in Fig. 1, comprises a pulse width modulator (PWM) and a bridge output stage. The bridge output stage consists of two cascades of CMOS inverters, and the load comprises an LC filter and load resistor \(R_L\). The power dissipation mechanisms are due to 1) parasitic capacitance \(P_T = (1/2)\rho_sC_sV_{DD}^2\); 2) short-circuit current during the transitions, \(P_T = I_{mean}V_{DD}\); and 3) on-resistance \(P_T = (1/T)\int_{0}^{t}i_{out}^2dt\).

We derive the three power dissipation mechanisms for the bridge output stage (comprising two strings of \(N\) inverters) realized using the
Fig. 1. Block diagram of a full-bridge output Class D power amplifier.

Fig. 2. IC layout of a transistor based on (a) the finger layout and (b) the waffle layout.
finger [Fig. 2(a)] and waffle [Fig. 2(b)] layouts and summarize them in Table I. In these derivations, we have assumed that \( L_n = L_p = \text{minimum} \) \( L \) and \( \beta_n = \beta_p = \beta \).

Using these derivations, we shall now describe two design methodologies for designing the transistor widths \( W \) for power efficiency.

### III. Power Efficiency Optimization

We shall assume that the three power dissipation mechanisms are independent and the total power dissipation is a summation of the individual power dissipations.

#### A. Optimization to a Single Modulation Index

The power efficiency can be written as

\[
\eta(W_p) = \frac{1}{1 + \chi(W_p)}
\]

where \( \chi(W_p) = P_r / P_{out} + P_r / P_{out} + P_r / P_{out} \). For maximum power efficiency, we would need to satisfy the condition

\[
\frac{\partial F(\eta, W_p)}{\partial W_p} = 0.
\]

The optimized channel width for the desired single modulation index \( D \)

\[
W_p = D \times \frac{B_1}{B_2 + B_3}
\]

where

\[
B_1 = \left( \frac{K_4 + K_5 + \frac{2K_6}{V_{DD} - V_{th}}}{r_{on}} \right) R_L,
\]

\[
B_2 = D^{-2} R_L \sum_{i=0}^{N-1} T_i^{-i}
\]

and

\[
B_3 = \frac{2D^{-2} R_L (V_{DD} - 2V_{th})^3}{V_{DD}} \sum_{i=0}^{N-1} T_i^{-i}.
\]

We note here that the higher the desired modulation index, the better is the maximum efficiency (the maximum efficiency being \( D = 1 \)) but at the cost of a larger IC area due to the larger transistor \( W \). In summary, to design an optimum power efficient Class D output stage to a given single modulation index \( D \), fabrication process, \( V_{DD} \), and \( R_L \), the \( W_p \) of the \( p \)-MOS transistor in the output inverter is given by \( (1) \). For the \( n \)-MOS transistor, the optimum channel width \( W_n \) is given by \( \alpha \).

The remaining transistor widths of the preceding inverters in the Class D output stage are designed according to the tapering factor \( T \) [7]. The optimized channel width given by \( (1) \) applies to both the finger and waffle layouts.

This optimization to a single modulation index is simplistic because the signal swing in an amplifier usually varies over a range of modulation indexes. Furthermore, this simplistic optimization raises the question of how to choose the appropriate \( D \) and implies that the power efficiency of a design whose transistor width \( W \) is optimized in this manner may not be optimum over a range of modulation indexes. This is depicted in the design examples in Fig. 3.

#### B. Optimization to a Range of Modulation Indexes

We rewrite the power efficiency \( \eta \) as a function of two variables \( W_p \) and \( D \)

\[
\eta(W_p, D) = \frac{P_{out}}{P_{out} + P_r + P_r + P_r} = \frac{x_1 D^2}{x_2 D^2 + x_3}
\]

where

\[
x_1 = (1/2)r_0^2 R_L, \quad x_2 = (1/2)r_0^2 (r_{on} + R_L)
\]

and

\[
x_3 = P_r + P_r.
\]

We can show that the average power efficiency over the range of \( D_1 \) to \( D_2 \) is

\[
\eta_{av}(W_p) = \frac{1}{D_2 - D_1} \int_{D_1}^{D_2} (W_p, D) dD = \frac{1}{D_2 - D_1} \left[ \left[x_4 D_2 - x_4 \sqrt{x_5} \tan^{-1}(D_2/x_5) \right] - \left[x_4 D_1 - x_4 \sqrt{x_5} \tan^{-1}(D_1/x_5) \right] \right]
\]

where

\[
x_4 = \frac{x_1}{x_2}, \quad x_5 = \frac{x_3}{x_2}.
\]
To determine $W_p$ for maximum average power efficiency, we set $d\eta_a(W_p)/dW_p = 0$

$$
\Rightarrow \frac{1}{D_2 - D_1} \left\{ \frac{D_2}{\sqrt{2x_5}} \frac{dx_4}{dW_p} + \frac{D_2 x_4 \frac{dx_4}{dW_p}}{2x_5 \left( 1 + \frac{D_2}{x_5} \right)} - \tan^{-1} \left( \frac{D_2}{\sqrt{2x_5}} \frac{dx_4}{dW_p} \right) \right\} = 0. \quad (4)
$$

The value of $W_p$ in (4) may be obtained by a number of numerical methods, including the secant method [8]. In summary, to design an optimum power efficient Class D output stage for a given range of $D_1$ to $D_2$, fabrication process, $V_{DD}$, and $R_s$, the $W_p$ of the p-MOS transistor in the output inverter is given by (4). The optimum channel width $W_n$ is given by $\alpha$ and the remaining transistor widths of the preceding stages are designed according to $T$.

### IV. DESIGN EXAMPLES, SIMULATION AND EXPERIMENTAL RESULTS

Consider a typical Class D amplifier output stage design for a hearing instrument whose application parameters are $V_{DD} = 2.5$ V, $\tau = 5$ ns, $f_s = 1$ kHz, $R_L = 600$ $\Omega$, $f_c = 40$ kHz, $L_s = 30$ mH, $L_n = L_p = 1.2$ $\mu$m, and $C_t = 0.1$ $\mu$F. For the finger layout, $L_{DS} = 4$ $\mu$m, $l_1 = 1.6$ $\mu$m, $l_2 = 1.2$ $\mu$m, and $l_3 = 1.2$ $\mu$m. For the waffle layout, $m = 4.8$ $\mu$m, $m_1 = 3.2$ $\mu$m. Note that although $V_{DD} = 1.3$ V is typical in hearing instruments, it is unsuitable here due to the fabrication process used. The tapering factor was chosen to be $T = 9$.

This output stage is to be realized using a typical 1.2-$\mu$m bulk CMOS process whose parameters are $V_{DD} = V_{DD} = 0.75$ V, $\mu_n = 533$ cm$^2$/V-s, $\mu_p = 92$ cm$^2$/V-s, $\varepsilon_{ox} = 3.45 \times 10^{-11}$ F/m, $C_{ox} = 1.41 \times 10^{-3}$ F/m$^2$, $C_J = 0.35 \times 10^{-3}$ F/m$^2$, $C_{GSO} = C_{GDO} = 0.3 \times 10^{-3}$ F/m, $C_{GBO} = 0.1 \times 10^{-3}$ F/m, $C_{JSW} = 0.23 \times 10^{-9}$ F/m,

#### TABLE II

<table>
<thead>
<tr>
<th>Layout</th>
<th>Optimized $W_p$ ((\mu)m)</th>
<th>Normalized Area</th>
<th>Average Power Dissipation</th>
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</thead>
<tbody>
<tr>
<td>Finger</td>
<td>11,913</td>
<td>5.8</td>
<td>12.1%</td>
</tr>
<tr>
<td>Waffle</td>
<td>13,972</td>
<td>5</td>
<td>11.7%</td>
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#### Fig. 3

Power efficiency curves of a Class D output stage optimized for maximum efficiency to a single modulation index at different modulation indexes. Design 1: $D = 0.1$; Design 2: $D = 0.25$; and Design 3: $D = 0.9$.

#### Fig. 4

The microphotograph of the two Class D output stages: top—waffle layout and bottom—finger layout.
Using (1), we design the transistor $W$ optimized to a single modulation index $D$ at different modulation indexes ($D = 0.1, 0.2, \ldots, 1$) for the finger and waffle layouts. We can show that although the power efficiency of the output stage realized by the finger and waffle layouts is nearly equal, the IC area in the waffle layout is on average 12% smaller. On this basis, we recommend the waffle layout for the design of a Class D amplifier output stage optimized to a single modulation index.

Consider now a case where we compare a design optimized to a single modulation index at $D = 0.9$ and the other optimized to a range of modulation indexes $D_1 = 0.025$ to $D_2 = 0.8$. This modulation index range is typical in a hearing instrument design. Using (1) and (4), we compute the optimized $W$ and summarize the salient parameters of this comparative study in Table II. We note here that by employing a waffle layout optimized to a range of modulation indexes, we obtain a greatly improved design over the finger layout optimized to a single modulation index. The improvement is a 42% relative reduction in power dissipation and requires only one sixth of the IC area. This improvement is very significant because the output stage dissipates the largest power in the amplifier and typically occupies 50% of the total Class D amplifier IC area. Based on these results, we recommend that the Class D amplifier output stage be designed using the waffle layout and optimized to a range of modulation indexes.

Fig. 4 depicts a microphotograph of an IC comprising two Class D output stages, a finger and waffle layout. The theoretical, simulated and measured power efficiencies for the waffle layout is shown in Fig. 5. We note that the theoretical, simulated, and measured power efficiencies agree well (although not shown, the theoretical, simulated, and measured power efficiencies for the finger layout also agree well), hence, verifying the theoretical derivations.

Fig. 6 depicts the measured waveforms of the PWM signal (top) at one of the Class D output stages and the demodulated output signal (bottom) across the load.
monic distortion. Modulation and can show that it has negligible effect on the total harmonic distortion.

V. CONCLUSION

An analysis of the power dissipation mechanisms which determines the power efficiency of the output stage of a Class D amplifier has been presented. Expressions of these power dissipation mechanisms for the finger and waffle layouts have been derived. Two proposed methodologies to optimize (optimized for a given fabrication process, supply voltage, and load resistance) the aspect ratios of the transistors in the output stage have been presented. For the design of a Class D amplifier output stage, the proposed optimization based on a range of modulation indexes and realized by the waffle structure is recommended.

REFERENCES


An Adaptive Demodulator for the Chaotic Modulation Communication System with RBF Neural Network

Tommy W. S. Chow, Jiu-Chao Feng, and K. T. Ng

Abstract—Chaotic modulation is an important spread spectrum (SS) technique amongst chaotic communications. The logistic chaotic signal acts as the modulation signal in this paper. An adaptive demodulator based on the radial basis function (RBF) neural network is proposed. The demodulator makes use of the good approximate capacity of RBF network for a nonlinear dynamical system. Using the proposed adaptive learning algorithm, the source message can be recovered from the received SS signal. The recovering procedure is on line and adaptive. The simulated examples are included to demonstrate the new method. For the purpose of comparison, the extended-Kalman-filter-based (EKF) demodulator was also performed. The results indicate that the mean square error (MSE) of the recovered source signal by the proposed demodulator is significantly reduced, especially for the SS signal with a higher signal-to-noise ratio (SNR).

Index Terms—Adaptive demodulator, chaos, RBF neural network, spread spectrum.

I. INTRODUCTION

Amongst the different strategies able to guarantee multiple access to a channel, increasing attention has been brought to spread spectrum (SS) and code division multiple access (CDMA) techniques. The main characteristic of SS/CDMA techniques is the spreading of the information signal over a bandwidth much larger than the original [1], [2]. With the recent progress in the theory of nonlinear dynamics and chaos, there has been increasing interest in applying chaos into an SS/CDMA communication system [3]–[6]. Of the different approaches to realize chaotic SS/CDMA communications, chaotic modulation is an important technology which employs a chaotic dynamical system to modulate the transmitted source signal to achieve the purpose of SS/CDMA communication [7]–[9]. More precisely, the transmitted signal is stored in a bifurcation parameter of the chaotic dynamical system. By keeping this bifurcation parameter in the chaotic regime, the modulated broadband signal may be used for the transmitted signal. At a receiver, the source information can be recovered by a special demodulation technology. The main advantage of the chaotic modulation technique is that it does not require any code synchronization. The crucial factor to realize this approach in a noise channel is, however, the evaluation of the bifurcation parameter for the chaotic dynamical system. Several demodulators with a simple inversion procedure for the logistic map transmitter have been proposed in [10] and [11]. These approaches operate very well when the environment is completely noise free. There is no doubt that the effectiveness of the inversion approaches degrade when channel noise exists. A different approach was developed to estimate the parameters of a chaotic dynamical system in the noise case [12]. The method was developed for off-line processing and usually requires a very long data sequence for a reliable noise reduction. All of these methods were designed for a constant parameter chaotic system and do not possess the ability to track a time-varying parameter, as...