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Effective Channel Length and External Series Resistance Models of Scaled LDD pMOSFETs Operating in a Bi-MOS Hybrid-Mode Environment

Siuang Hing Lionel Seah, Kiat Seng Yeo, Jian Guo Ma, and Manh Anh Do

Abstract—The effective channel length $L_{\text{eff}}$ and total external series resistance $R_{\text{EXTTOT}}$ of deep submicron lightly doped drain (LDD) pMOSFETs, operating in a Bi-MOS hybrid-mode environment, have been modeled as functions of bias and temperature. The accuracy of the device threshold voltage used in the $L_{\text{eff}}$ and $R_{\text{EXTTOT}}$ extraction routine is discussed. The proposed models have been verified for temperature ranging from 223 K to 398 K and source-to-body voltage $V_{SB} \geq 0$ V conditions.

Index Terms—Deep submicron, effective channel length, external series resistance, hybrid-mode, lightly doped drain (LDD), temperature-dependent.

I. INTRODUCTION

The $L_{\text{eff}}$ and $R_{\text{EXTTOT}}$ are important parameters needed to accurately model the $I$–$V$ characteristics of short-channel LDD MOSFETs [1]. Most analyses in the literature (e.g., [2]–[12]) either ignore the body terminal of the devices, assume the body and source terminals having the same potential, or consider the source-body junction in reverse biased mode. Recently, hybrid-mode devices employing lateral p-n-p BJT in a pMOS structure have been brought into attention due to their high current gain and simple technology [13]–[15]. For a device operating in a Bi-MOS hybrid-mode environment, its gate and body terminals may be biased independently such that potential across the source-body junction becomes greater than 0 V, while maintaining the MOSFET in active mode. This requirement has prompted the question of whether or not $L_{\text{eff}}$ and $R_{\text{EXTTOT}}$ commonly extracted from the experimental data remain valid for $V_{SB} \geq 0$ V. The knowledge of such dependency on the body bias is important to ensure proper prediction of the device performance in hybrid-mode operation.

II. DEVICE STRUCTURES AND MEASURING EQUIPMENT

The device structure used in the measurement consists of a series of silicon p-channel LDD MOSFETs fabricated with a gate oxide thickness $t_o$ of 5 nm. The channel width $W$ for all devices is 20 $\mu$m, whereas the gate length $L$ varies from 1 $\mu$m down to 0.25 $\mu$m. N-well implantation was formed using phosphorus of $2 \times 10^{13}$ $\text{cm}^{-2}$ dosage and an energy level of 600 keV. The drain/source implantation was carried out using boron with a dose of $3 \times 10^{15}$ $\text{cm}^{-2}$ and an energy level of 30 keV. The p$^+$ LDD implants were established with a dose of $2 \times 10^{14}$ $\text{cm}^{-2}$ and an energy level of 20 keV. The p$^+$ junction depth $X_j$ and the p-LDD junction depth $R_j$ are approximately 0.15 $\mu$m and 0.075 $\mu$m, respectively. A channel implant dose of $3 \times 10^{12}$ $\text{cm}^{-2}$ and an energy level of 70 keV is added for threshold voltage adjustment. Device measurements were performed using a semiconductor parameter analyzer and a TEMPTRONIC system which controls the temperature of the wafer.

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to an accuracy of ± 0.5 K. Measurements were done and repeated on a vibration-free table with the CASCADE MICROTECH probing station enclosed in a light-shield box.

III. \( R_{TOT_{ex}} \) AND L\(_{eff} \) EXTRACTION AND MODELING

Assuming symmetrical device and applying very low source-to-drain voltage \( V_{SD} \), the total source-to-drain resistance across the extrinsic pMOSFET can be derived from the linear region drain current expression as in [16], expressed as

\[
R_{TOT_{ex}} = R_{TOT_{ex}}(V_{SG}, V_{SB}, T) + \frac{L}{\mu_{p_{eff}}} \frac{L}{C_{ox}} \left( V_{SG} - V_{SD} - 0.5 V_{SD} \right)
\]

(1)

where

- \( R_{TOT_{ex}} \) sum of resistances of the contact, wiring, \( p^+ \) diffusion region, and \( p^+ \) lightly doped regions of the source and drain side;
- \( \Delta L \) channel length reduction;
- \( C_{ox} \) gate oxide capacitance per unit area;
- \( \mu_{p_{eff}} \) temperature-dependent hole mobility adapted from [17].

Expressions similar to (1) have been reported in [1]–[8], [18]. However, they have generally made use of a device threshold voltage obtained at room temperature and \( V_{SB} = 0 \) V. As widely known, the threshold voltage of short-channel devices is related to the drain/body bias, channel length and temperature. Hence, using a bias/temperature-independent threshold voltage in the extraction routine would be inadequate for \( V_{SB} \geq 0 \) V and/or when the temperature differs from the room temperature. To overcome this problem, an effective threshold voltage suitable for Bi-MOS hybrid-mode operating condition is used here. The effective threshold voltage, considering drain-induced barrier lowering (DIBL), body-induced-barrier-lowering (BIBL), and temperature effects, is expressed as

\[
V_{T_{eff}} = V_{TO} - \eta V_{SD} - \gamma V_{SB} - (T C_1 + T C_2 V_{SB}) \left( \frac{T}{300 \text{ K}} - 1 \right)
\]

(2)

where \( V_{TO} \) is the zero-bias threshold voltage extracted at \( T = 300 \) K using the “Transconductance Peak” method [19]. For \( V_{SD} = 0.05 \) V considered here, the DIBL effect contributed by the term \( \eta V_{SD} \) can be ignored. The BIBL factor \( \gamma \) accounts for the reduction in the threshold voltage when \( V_{SB} \) increases [13]. The parameter \( T C_1 \) is defined as the temperature compensation factor extracted at \( V_{SB} = V_{SD} = 0 \) V, whereas \( T C_2 \) is the temperature compensation factor for \( V_{SB} > 0 \) V. The composite effect of \( V_{SB} \) and temperature on \( V_{T_{eff}} \) is illustrated in Fig. 1. At \( V_{SB} = 0 \) V, \( V_{T_{eff}} \) reduces about 23% when the temperature increases from 223 K to 398 K. However, for \( V_{SB} > 0 \) V, the reduction rate of \( V_{T_{eff}} \) with temperature increases. The use of (2) in the extraction procedure implies that for a specific source-to-gate bias \( V_{SG} \), the gate drive \( V_{G_{eff}} = (V_{SG} - V_{T_{eff}} - 0.5 V_{SD}) \) varies with \( L \), \( T \), and \( V_{SB} \) through \( V_{T_{eff}} \). Therefore, any extraction errors contributed by using a bias/temperature-independent threshold voltage are avoided.

As widely known, the carrier density modulation effect in the overlapping regions between the lightly doped regions and the gate in the LDD structure, and the fringing field conductivity modulation effect cause \( R_{TOT_{ex}} \) to be gate-bias-dependent. On the other hand, the increase in gate control over the mobile charge at the two ends of the channel leads to the expansion of the effective channel toward the source and drain regions. Fig. 2 shows \( R_{TOT_{ex}} \) and \( \Delta L \) at various temperatures exhibiting similar declining trends with increasing \( V_{G_{eff}} \). For \( V_{SB} = 0 \) V and \( T = 300 \) K, \( R_{TOT_{ex}} \) and \( \Delta L \) decrease by 28.75% and 18.02%, respectively, as the gate drive \( V_{G_{eff}} \) increases from 0.55 V to 1.95 V. Reductions in \( R_{TOT_{ex}} \) and \( \Delta L \) result in higher \( V_{SD_{eff}} \) appearing across a “longer” intrinsic pMOSFET channel. This phenomenon is critical in deep submicron devices because of the associated scaling of supply voltage (i.e., \( V_{SD} \)) applied to the extrinsic pMOSFET. If gate-bias-independent \( R_{TOT_{ex}} \) and \( \Delta L \) values, extrapolated at a low gate bias, are used in modeling the \( I-V \) characteristics of the device, underestimation of source-to-drain current \( I_{SD} \) would be resulted at high \( V_{SG} \) biases. Therefore, the determination of \( R_{TOT_{ex}} \) and \( \Delta L \) is important to ensure accurate prediction of the device characteristics for a wide range of gate biases.

To investigate the effect of \( V_{SB} \) and temperature independently, the extracted \( R_{TOT_{ex}} \) and \( \Delta L \) are averaged over the entire \( V_{G_{eff}} \) range considered earlier. This is accomplished by extending the method proposed in [18] to various \( V_{SB} \) biasing and temperature conditions. This technique allows the isolation of the gate modulation effect and yet does not require a fixed gate bias to be defined. In retrospect
[4], a very slight increment in $R_{T_{TOTtest}}$ and $\Delta L$ with temperature has been observed, as depicted in Fig. 3 (inset). Although applying $V_{SB} > 0$ V reduces the charge sharing effect [5], [7], narrowing of the depletion width at the source-body and drain-body junctions lengthens the effective channel region, justified by the reduction in $\Delta L$ with increasing $V_{SB}$ as indicated in Fig. 3. It is interesting to note that this channel lengthening effect appears to increase the numerator of the second term in (1), and hence the channel resistance. However, applying $V_{SB}$ also causes the physical broadening of the channel formation under the gate. In contrast, this phenomenon reduces the intrinsic channel resistance. As mentioned earlier, increasing $V_{SB}$ reduces $V_{off}$. This effect reduces the channel resistance per unit length and is well represented by utilizing $I_{SD}$ in the second term in (1). As compared to $V_{SB} = 0$ V condition, $I_{SD}$ increases when the device is biased with $V_{SB} > 0$ V. For a fixed $V_{SD}$, $I_{DS} = I_{SD}/V_{SD}$ reduces as a result. From the experimental results, the drop in $R_{tot}$ resulted from the increase in channel carriers collected at the drain region is also reflected in the trend of $R_{T_{TOTtest}}$, as shown in Fig. 3. Therefore, the results have proven that one important contributing factor to $I_{SD}$ increment for $V_{SB} > 0$ V is the composite effect between the resultant $R_{T_{TOTtest}}$, $\Delta L$, and $V_{off}$.

Fig. 3. Dependence of $R_{T_{TOTtest}}$ and $\Delta L$ on source-body voltage $V_{SB}$ and temperature (inset).

Fig. 4. Prediction of the drive current (solid lines) for different temperatures, gate lengths and body/gate terminal biases. The markers $\bigcirc$, $\bigtriangleup$, and $\triangle$ represent the measurement data for $V_{SB} = 0$ V, 0.4 V, and 0.6 V, respectively.

$V_{SD} = 0.05$ V

$V_{SD} = 3$ V $T = 300$ K

$V_{SD} = 2$ V $T = 398$ K

$V_{SD} = 1$ V $T = 223$ K

Combining the gate bias modulation, temperature and body bias effects, the $R_{T_{TOTtest}} (\Omega)$ and $L_{off} (\mu m)$ are modeled as

$$R_{T_{TOTtest}}(V_{SCH}, V_{SBH}, T) = aT + b - c(V_{SCH} - V_{off}) - dV_{SBH}$$

$$L_{off}(V_{SCH}, V_{SBH}, T) = L(\mu m) - \Delta L(V_{SCH}, V_{SBH}, T)$$

$$\Delta L(V_{SCH}, V_{SBH}, T) = eT + f - g(V_{SCH} - V_{off}) - hV_{SBH}$$

where $a$, $b$, $c$, $d$, $e$, $f$, $g$, and $h$ are coefficients extracted experimentally, given in Table I. The validity of the proposed $R_{T_{TOTtest}}$, $L_{off}$ and $V_{off}$ models are verified by applying the modeled values into conventional drain current model expression as in [16]. Fig. 4 demonstrates good agreements between the experimental and modeled drain current characteristics for a wide range of biases and temperatures.

IV. CONCLUSIONS

The $R_{T_{TOTtest}}$ and $L_{off}$ of scaled hybrid-mode devices have been investigated. Together with a novel $V_{off}$ expression, analytical $L_{off}$ and $R_{T_{TOTtest}}$ models useful for devices operating in a Bi-MOS hybrid-mode environment have been presented. By including the effect of body bias and temperature in the $R_{T_{TOTtest}}$, $L_{off}$, and $V_{off}$ models, the drain current characteristics of scaled devices operating in a Bi-MOS hybrid-mode environment can be predicted accurately using conventional drain current expression.

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Patterning Sub-30-nm MOSFET Gate with I-Line Lithography

Kazuya Asano, Yang-Kyu Choi, Tsu-Jae King, and Chenming Hu

Abstract—We have investigated two process techniques: resist ashing and oxide hard mask trimming. A combination of ashing and trimming produces sub-30-nm MOSFET gate. These techniques require neither specific equipment nor materials. These can be used to fabricate experimental devices with line width beyond the limit of optical lithography or high-throughput e-beam lithography. They provide 25-nm gate pattern with z-line lithography and sub-20-nm pattern with e-beam lithography. A 40-nm gate channel length nMOSFET is demonstrated.

I. INTRODUCTION

Currently, MOSFET gate length for advanced research is below 50 nm. Making such a small feature is not an easy task, in general. Although e-beam lithography employing some positive resists such as PMMA has high resolution, its throughput is too low even for research.

We will discuss two techniques that provide sub-30-nm line width without using any special equipment or materials. The first technique is resist ashing. This technique was developed for making submicron devices from g-line lithography about ten years ago [1]. Since then, it has been rather widely used to produce smaller features than the resolution limit of optical lithography [2]–[4]. The second technique is an oxide hard mask trimming. Oxide hard mask trimming is relatively straightforward, but we have found no reports that describe it, let alone report on its use in the sub-30-nm regime. A combination of these two techniques makes it possible to fabricate 25 nm line width using i-line lithography.

II. EXPERIMENTS AND RESULTS

A. Ashing i-Line Resist

Sample wafers were exposed with an i-line stepper. The thickness of the positive i-line resist was 1.1 μm and baked at 90 °C for 1 min before exposure and 120 °C for 1 min after exposure, respectively. The resist patterns after a development were ashed in an oxygen-plasma asher, Technics PE II. Oxygen pressure was 260 mTorr with a flow rate of 51.1 sccm. The ashing rate of the i-line resist without hard baking (120 °C) is shown in Fig. 1. The vertical ashing rate is the rate of reduction of the resist thickness, while the horizontal ashing rate is the rate of reduction of the line width. Both ashing rates change linearly with the ashing power and are independent of the initial line width.

The ratio of the horizontal ashing rate to the vertical ashing rate is about 1:2:1, which produces isotropic profile. Ashing does not change the edge roughness of the resist as shown in Fig. 2(a). The smoothness of the initial lines is very important for good ashing results. In the case of i-line lithography, line smoothness depends strongly on the mask quality. The taper angle of the narrow resist profile at the top corner increases slightly after ashing. The top of the resist may be rounded in the end. This can happen earlier in narrow lines than in wide patterns. Even if the top of the resist is rounded off, etching does not present a problem as long as the resist is thick enough.

B. Ashing e-Beam Resist

Two chemically amplified resists, SNR-2000 and SAL601, were evaluated. Ashing of the e-beam resists was done in the same asher, Technics PE II.

In the case of e-beam resist patterns, only a small amount of ashing compared to i-line patterns is needed because the initial line width is 100 nm or less. We fixed the ashing power at 5 W, which was the lowest power to sustain stable plasma. The ashing rates of the e-beam resists are 22–30 nm/min at 5 W power. For SAL and SNR, the ashing rates were almost the same.

One interesting phenomenon is resist hardening caused by SEM. Since SAL and SNR are negative resists, they are hardened by the exposure to e-beam (energy is less than 1 KeV) during SEM. After SEM, ashing rate of the resist patterns exposed to the e-beam decreased to two-thirds of those not exposed.

In Fig. 3(a), the SEM picture of a 17-nm ashed SNR-2000 resist line is shown. This line was originally 80-nm wide after e-beam lithography.

C. Oxide Hard Mask Trimming

The concept of oxide hard mask trimming is similar to the resist ashing. After the ashing-down of the gate resist patterns, an oxide hard mask pattern is anisotropically etched. A Lam research model