A Micropower-Compatible Time-Multiplexed SC Speech Spectrum Analyzer Design

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Abstract— **A micropower-compatible time-multiplexed SC speech spectrum analyzer embodying several new design methodologies is described. In the bandpass filter (BPF) section, the dc offset differences between channels are reduced by a careful biquadratic filter design, and a capacitor sharing technique is employed to reduce chip area. A new time-multiplexed full-wave rectifier (FWR) is also proposed. Expressions for the errors that limit the accuracy of the running spectrum due to nonidealities are formulated. An experimental four-channel spectrum analyzer has been fabricated and measurements from prototypes showed that the proposed design methodologies are satisfactory in achieving the design specifications.**

I. Introduction

SPEECH spectrum analyzers are used as front-end processors in a vast number of speech applications including auditory prostheses and sensory aids for the hearing impaired [1], automatic speech recognition [2]–[6], vocoders [6], and the like to perform short-time spectrum analysis. In battery-operated biomedical speech processing applications [1] where chip area and power dissipation are critical design requirements, a micropower analog switched-capacitor (SC) implementation is attractive.

This paper describes a time-multiplexed SC speech spectrum analyzer design based on the classical filter bank approach [1]–[6] comprising three functional blocks as depicted in Fig. 1: bandpass filter (BPF), full-wave rectifier (FWR), and low-pass filter (LPF) sections. Tables I and II summarize the specifications of a spectrum analyzer [1], which include frequency (passband bandwidth of BPF's) and temporal resolutions (weighting functions or impulse responses of the BPF's and LPF's) [1], [6, p. 142]. The accuracy of the running spectrum output of the spectrum analyzer is limited by its nonidealities, in particular, the dc offset of these blocks and FWR threshold voltage. The FWR threshold voltage is the input signal level (relative to analog ground) at which the FWR inverts the signal to perform full-wave rectification, and is ideally zero. These nonidealities are important considerations as they would inadvertently be measured as energy in the band-limited signal. In this paper, expressions describing these errors are derived that provide insight into where these nonidealities are least tolerated. Acceptable upper limits on these nonidealities for a practical system can therefore be determined.

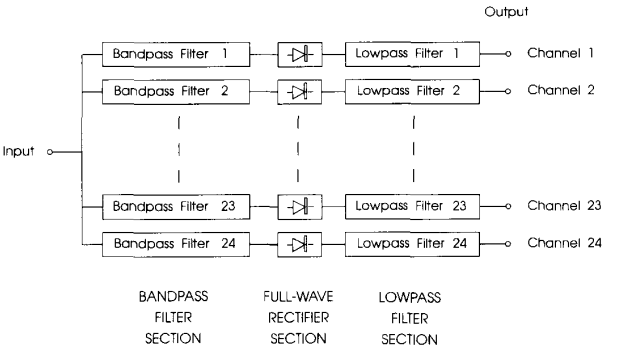

Fig. 1. Block diagram of a filter bank spectrum analyzer.

The time-multiplexed SC spectrum analyzer described in this paper embodies several novel design methodologies with the objective of attaining small chip area and low power dissipation. DC offset differences between different time-multiplexed BPF's (see Section II) are reduced by a careful biquadratic filter (biquad) design. A capacitor (cap) sharing technique is proposed that achieves substantial chip area savings and a new SC FWR is presented. In addition, the complete spectrum analyzer is micropower compatible, i.e., all its subcircuits are strictly comprised of uncoupled and coupled-in-cascade amplifier structures [10].

This paper is arranged in the following manner. Sections II, III, and IV describe the time-multiplexed BPF, FWR, and LPF sections, respectively. Section V discusses other considerations pertinent to the application of time- multiplexing. Measurements on the prototypes of a four-channel speech spectrum analyzer fabricated using a CMOS process are described in Section VI.

II. Time-Multiplexed Bandpass Filter Design

The transitional Butterworth and Bessel filter approximations [11] and the generic BP01 transformation [12] are used in the BPF synthesis. Two problems in the BPF section realization, namely the difference dc offsets and required chip area, are now addressed. Consider first the dc offsets problem. DC offsets arise in SC circuits due to op-amp input-referred

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TABLE I
SPEECH SPECTRUM ANALYZER SPECIFICATIONS FOR A BIOMEDICAL APPLICATION[1]

Parameter	BPF Section	FWR Section	LPF Section
No. Channels	24	24	24
Function	4th Order Filter	Full-Wave Rectification	3rd Order Filter
Spacing	Passbands spaced in Bark Scale ([1], Table 1)	-	Uniform 35 Hz Cut Off
Adjacent Filter Passband Overlap	-3 dB	-	-
Analysis Range	200 Hz - 4 kHz	-	-
Temporal Resolution	< 20 ms	-	< 20 ms
Dynamic Range	> 60 dB	> 60 dB	> 60 dB
Relative Spectrum Error+	< 1 %	< 1 %	< 1 %
Crosstalk	< -40 dB	-	-
Clocking Frequency (per Channel)	10.42 kHz	10.42 kHz	Multirate 10.42 kHz and 1.3 kHz

Total Power Dissipation < 10 mW with ±2.5V voltage supply

\+ due to DC offset differences in the BPF, FWR and LPF sections, and threshold voltage differences in the FWR section (see text for further explanation)

TABLE II
BPF SECTION SPECIFICATIONS

BPF	Centre Frequency	-3 dB Passband	Comments
1	250	100	
2	350	100	
3	450	100	
.	.	.	
11	1150	100	
12	1365	130	
13	1502	143	
.	.	.	
22	3541	337	
23	3894	370	
24	1365	130	zero input filter

offset, clock feedthrough, charge pumping, etc. [13]. The dc offsets can be categorized into "common" and "difference" offsets. The common offset resulting in "common error" is the same for all time-multiplexed BPF's, for example, the input-referred dc offset of the time-multiplexed op amps, and can be obtained from the output of a zero-input BPF [2], [3]. This offset is usually of little consequence, as it is the same for all filter channels and is easily accounted for. The difference offsets, on the other hand, are the dc offset differences between different time-multiplexed BPF's resulting in unequal "difference errors" at the output of the spectrum analyzer, and are therefore difficult to account for.

One obvious method to reduce the difference offsets between BPF channels involves cascading high-pass filters to the preceding BPF's [2]. This method, however, is not only uneconomical in hardware terms but also undesirable because the high-pass filters may introduce further unequal dc offsets. Another reported technique [3] involves the use of resistor strings to provide voltage division so that cap ratios of all BPF's are identical resulting in identical dc transfer functions. Resistor strings are, however, undesirable in a monolithic realization because they require large chip area (polysilicon resistors are used for precision), dissipate considerable power, and result in prohibitively long time constants which in turn limit high-speed operation. Resistor strings are therefore unacceptable in a micropower realization, in particular in a time-multiplexed application where high speed is imperative.

The solution proposed here is to design the biquads such that dc transfer functions from the input of each biquad op amp to the output of the biquad are *independent* of cap ratios. Hence, for a fixed input offset voltage, the dc offset at the output of the time-multiplexed biquad is theoretically uniform for all channels, resulting in common offsets only. To put it differently, the objective here is to match the dc transfer functions of the time-multiplexed biquad for all channels so that the same input offsets result in common output offsets. Fig. 2(a) and (b) depicts such a biquad and its signal-flowgraph, respectively. The transfer function of the biquad is

$$\frac{V_{\text{out}}(z)}{V_{\text{in}}(z)} = \frac{Jz^{-1}(1-z^{-1})}{(1+F)+z^{-1}(AU-F-2)+z^{-2}}. \tag{1a}$$

The offset voltage sources at the input node, V_{off0}, and output terminals of the two op amps of the biquad, V_{off1} and V_{off2}, are also shown. Fig. 2(c) depicts the feedforward paths from these sources to the biquad output. The feedforward path for V_{off0} is the same as that for the input signal and $V_{\text{out}}(z)/V_{\text{off0}}(z)$ is as expressed in (1a). Using Fig. 2(c), it can be shown that

$$\frac{V_{\text{out}}(z)}{V_{\text{off1}}(z)} = \frac{A(1-z^{-1})}{(1+F)+z^{-1}(AU-F-2)+z^{-2}} \tag{1b}$$

$$\frac{V_{\text{out}}(z)}{V_{\text{off2}}(z)} = \frac{-AU-F(1-z^{-1})}{(1+F)+z^{-1}(AU-F-2)+z^{-2}}. \tag{1c}$$

At dc

$$\left.\frac{V_{\text{out}}(z)}{V_{\text{off0}}(z)}\right|_{z=1} = \left.\frac{V\text{out}(z)}{V_{\text{off1}}(z)}\right|_{z=1} = 0 \tag{2a}$$

$$\left.\frac{V_{\text{out}}(z)}{V_{\text{off2}}(z)}\right|_{z=1} = -1. \tag{2b}$$

From (2a) and (2b) it can be seen that these dc transfer functions are independent of capacitor ratios. The simple solution proposed here for time-multiplexed circuits is significant because the resultant BPF section design is not only micropower compatible but also hardware efficient, and no additional hardware is required to reduce the difference offsets. However, some difference dc offsets between the time-multiplexed BPF's are still likely due to other factors described earlier, but they are expected to be in the millivolts range rather

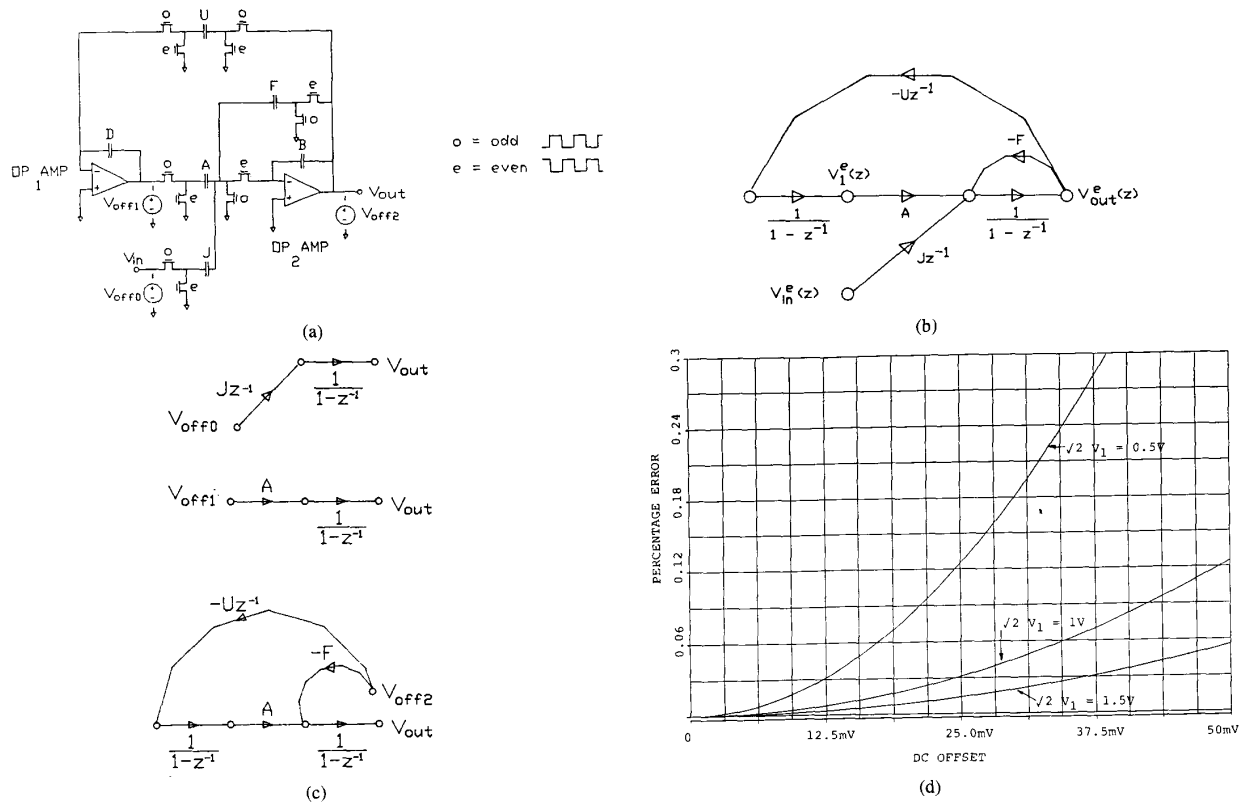


Fig. 2. (a) BPF biquad and dc offset sources at three nodes (all switches are CMOS). (b) Signal-flow graph and transfer functions. (c) Feedthrough paths from dc offset sources to the output of the biquad. (d) Effect of BPF dc offset to percentage error for peak input voltages, $\sqrt{2}V_1$, of 0.5, 1, and 1.5 V.

than 10's or 100's of millivolts (see Section VI for values measured from prototype devices). In addition, if the dc offsets of the BPF's are predominantly due to the input-referred op-amp offsets (typically 10–30 mV), the time-multiplexing approach is, in this respect, advantageous over conventional unmultiplexed methods since the same op amps are used for all channels.

At this juncture, it is of interest to derive expressions to quantify the error due to the residual difference dc offsets. This error is quantified for signals after full-wave rectification because the running spectrum output of the spectrum analyzer is the slow-varying average output of the individual BPF's obtained after rectification and low-pass filtering. The error is

$$\text{Error} = \frac{|\text{Average (offset sinusoid) - Average (zero offset sinusoid)}|}{\text{Average (zero offset sinusoid)}} \times 100\% \quad (3)$$

where offset sinusoid refers to the full-wave rectified output of a BPF with dc offset, and zero offset sinusoid refers to the full-wave rectified output of a BPF without offset. The average of the waveforms in (3) is derived as follows:

$$\text{Area under sinusoid waveform (fully rectified with offset over } 2\pi \text{ radians)} = \left(\int_0^{\pi} \sqrt{2}V_1 \sin\theta d\theta\right) + \left(\int_0^{\pi} \sqrt{2}V_1 \sin\theta d\theta - 2\int_0^{\varphi} \sqrt{2}V_1 \sin\theta d\theta - V_{\text{off}}\pi + 2V_{\text{off}}\varphi\right) + 2\left(V_{\text{off}}\varphi - \int_0^{\varphi} \sqrt{2}V_1 \sin\theta d\theta\right) + (V_{\text{off}}\pi) \quad (4)$$

where $\sqrt{2}V_1$ is the peak value of the sinusoid, $\sqrt{2}V_1 \sin\theta$ is the sinusoid waveform without offset, V_{off} is the dc offset, and $\varphi = \sin^{-1}(V_{\text{off}}/\sqrt{2}V_1)$. From (4), the average value of a fully rectified waveform with dc offset, V_{off}, is

$$\text{Average} = \frac{2}{\pi}\left\{V_{\text{off}} \sin^{-1}\frac{V_{\text{off}}}{\sqrt{2}V_1} + \sqrt{2}V_1\sqrt{\left[1 - \left(\frac{V_{\text{off}}}{\sqrt{2}V_1}\right)^2\right]}\right\}. \quad (5)$$

Expressions (4) and (5) may be used for a sinusoid without offset by setting V_{off} to zero. Using (3) and (5), the theoretical percentage error at the output of a spectrum channel, assuming

ideal rectification, was computed as a function of dc offset of the BPF and is plotted in Fig. 2(d) for different levels of input sinusoidal peak voltages, $\sqrt{2}V_1 = 0.5$, 1, and 1.5 V. It can be seen that the percentage error is smaller for larger values of $\sqrt{2}V_1$. It is further noted that the effect of dc offset on error is small, for example, a 50-mV dc offset would only result in an error of 0.13% for $\sqrt{2}V_1$ of 1 V. This desirable effect is because an increased average value of the first half of the sinusoid with dc offset is accompanied by a corresponding reduced average value of the second half of the sinusoid, a direct consequence of full-wave rectification. In Section VI, these errors will be evaluated on the basis of measured dc offsets from prototype integrated circuits.

Consider now the large chip area requirement for the BPF section. A time-multiplexed approach is adopted as it is an area-efficient method of realizing filter banks [1], [3]–[5], [14], [15] (especially if the number of clock signals are small). Fig. 3(a) depicts the time-multiplexed BPF biquad previously shown in Fig. 2(a). The multiplexing sequence is defined according to the clock signals given in Fig. 3(b) where one fourth-order filter (two biquads in cascade) of the BPF section is serviced during a local clock period. It can be seen that by appropriate switch phasings and local clock definitions, caps A, F, J, and U do not carry any charge information from one local clock period to the next. As the value of J remains invariant (Table IIIa), it is conveniently shared among all BPF's.

Despite time-multiplexing, the required chip area for the BPF section is still large because the BPF channels have disparate passband specifications leading to a large capacitance spread. Furthermore, if a modular layout with equal allocated areas for each channel is preferred, the area allocated to each channel would need to be set to the area of the channel with the largest capacitance. Thus, if the capacitance area for this channel is reduced, substantial area savings can be accomplished. This is achieved by sharing the A array caps in two ways. First, it can be seen from Table IIIa that all A caps are larger than two units. A common 1 unit cap $A0$ can therefore be shared by all channels as shown in Table IIIb and Fig. 3(c). In this manner, an A cap is made up by connecting $A0$ in parallel to a residual A_x cap, i.e., $A = A0 + A_x$ (x being the BPF channel in question). Second, filter channels with large A values (channels 9–24) can share a further common cap AA of 11 unit caps, also depicted in Table IIIb and Fig. 3(c). In these cases, the A cap is realized by a parallel combination of $A0 + AA + A_x$; for example, in channel 9, this corresponds to $A = 1 + 11 + 1.34$ unit caps, respectively. An additional clock signal $Pd9$–$Pd24$, a signal that goes high at the commencement of local clock period $Pd9$ and low at the end of $Pd24$, is used to connect AA into the circuit during the appropriate times, or alternatively, a bank of switches may be used. As a result of the cap sharing, the area allocated for the channel with the largest capacitance is eight unit caps less, yielding a total area savings of approximately 15% (taking into account area for clock bus, interconnections, op amps, and caps).

The proposed cap sharing is also advantageously applied to cap array U. Consider the application of a cap array comprising $U0$ and UU in Fig. 3(d) in place of the 24-cap array in Fig. 3(a). For channels 1–8, a common 1 unit cap $U0$ is

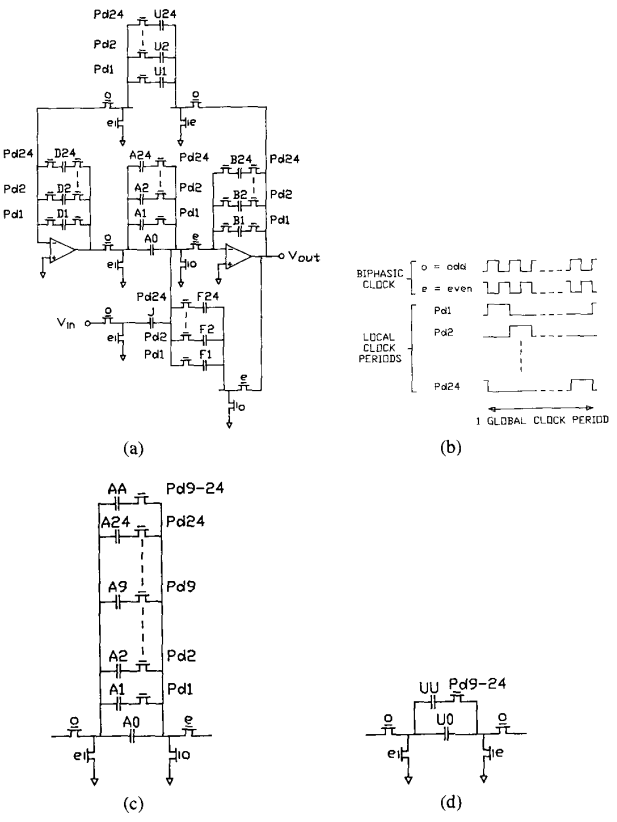


Fig. 3. (a) Time-multiplexed BPF biquadratic filter. (b) Clock signals. (c) Capacitor array A employing the capacitor sharing technique. (d) Capacitor array U employing the capacitor sharing technique.

TABLE IIIa
CAP VALUES FOR ONE BPF BIQUAD

	UNIT cap in subgroup (A,J,F,B) = 0.4pF ; subgroup (D,U) = 1.2 pF					
BPF	A	B	D	F	J	U
1	2.92	21.07	7.62	1.00	1.00	1.00
9	13.34	19.17	1.60	1.04	shared	1.00
20	16.46	9.97	1.00	1.38	shared	1.55

TABLE IIIb
CAP VALUES FOR ONE BPF BIQUAD EMPLOYING CAP SHARING TECHNIQUE

Common Capacitor A0 = 1 unit, Common Capacitor AA = 11 units
Common Capacitor U0 = 1 unit, Common Capacitor UU = 1 unit
UNIT cap in subgroup (A,J,F,B) = 0.4pF ; subgroup (D,U) = 1.2 pF

BPF	A	B	D	F	J	U
1	1.92	21.07	7.62	1.00	1.00	1.00
9	1.34	19.17	3.19	1.04	shared	2.00
20	4.46	9.97	1.29	1.38	shared	shared

shared. In subsequent channels 9–24, a further common 1 unit cap UU is connected in parallel to $U0$; the D caps are adjusted accordingly to preserve the same D/U cap ratios (Table IIIb). As in the previous case, the same clock signal $Pd9$–$Pd24$ or a bank of switches is used to connect UU into the circuit during the appropriate times. By noting that the smallest integrating cap is at least 1 pF for clock feedthrough and power supply coupling noise considerations, the resulting area saving is of the order of 5%. With reference to Table IIIa and IIIb, it can be seen that as a result of cap sharing, the smallest integrating D cap is slightly increased (from 1.0 to 1.2); this improves the worst-case noise performance of the time-multiplexed biquad. In summary, the cap sharing methodology proposed in this paper achieved a total area savings of approximately 20%.

III. Full-Wave Rectifier (FWR)

The proposed parasitic insensitive biphasic SC FWR is presented in Fig. 4(a). During the even phase, op amp 1 becomes a voltage follower where its input-referred dc offset is sampled by $C1$ and $C2$, and the dc offset of the comparator (op amp 2) is sampled by $C3$. The op amps are autozeroed [16] during this phase. In the following odd phase, op amp 1 acts as a delay-free unity gain ($C1 = C2$) inverting amplifier. The comparator, on the other hand, compares the output of this inverting amplifier with the input signal and determines if the input signal is positive or negative relative to analog ground. If the input is positive, the output of the FWR is simply the input signal shown as "path +" in Fig. 4(a). On the other hand, if the input signal is negative, the output of the FWR is the output of the inverting amplifier depicted as "path−." The circuit thus performs the full-wave rectification function: $V_{\text{out}}(nT) = V_{\text{in}}(nT) \cdot \text{sign}\,[V_{\text{in}}(nT)]$.

As a result of autozeroing during the even phase, all caps do not retain any charge information pertaining to the input signal of the FWR. The FWR can therefore be time-multiplexed where *all* its circuit elements are shared by all channels, hence achieving substantial chip area savings. Note that by appropriate switch phasings, the time-multiplexed FWR uses the biphasic clock signals only, resulting in a simple compact interconnection layout. It is further evident from Fig. 4(a) that the FWR is jitter-free as its output is available during the same instant the input is sampled, making a sample-and-hold input unnecessary. The comparator of the FWR is designed to sense the differential input signal, that is, the difference between the input signal and its inverted equivalent obtained from the unity-gain inverting amplifier. In this manner, the required threshold voltage of the FWR at which the input signal is inverted is reduced, and is therefore better than those described in [7]–[9]. However, the threshold is not expected to be zero (ideally zero) due to the charge injection of the switch across the input and inverting input terminals of the comparator. Power dissipation is slightly reduced in this design by sampling the comparator output during the odd phase only.

As a matter of interest, further power savings may be obtained by compromising the FWR threshold voltage. By grounding the bottom plate (drawn as top plate in Fig. 4(a)) of $C3$, the difference voltage for the comparator to sense is

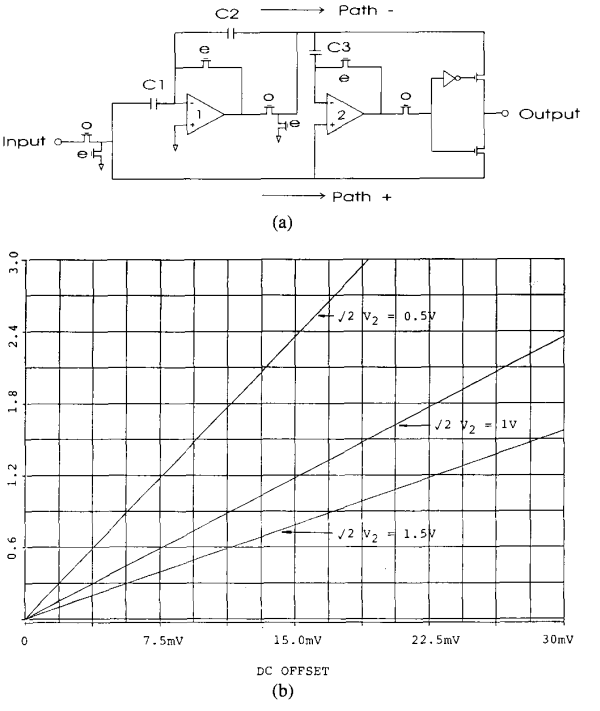


Fig. 4. (a) Time-multiplexed FWR. (b) Effect of FWR dc offset (fixed threshold voltage of 2 mV) to percentage error for peak input voltages, $\sqrt{2}V_2$, of 0.5, 1, and 1.5 V.

effectively halved. However, the output of the comparator during the odd phase can now be used to power down the biasing current of the inverting amplifier when the input to the FWR is above analog ground. In this manner, power dissipation is reduced since the inverting amplifier is only active when it is required to invert the input signal. This technique has, however, not been used in this design. It is worthwhile noting that the dc offset compensation feature of the FWR is still retained with this modification.

The nonidealities of the FWR that affect the accuracy of the running spectrum are the dc offset, V_{off}, and threshold voltage, V_s. Using the error definition in (3), the average value of a sinusoid taking V_{off} and V_s into account is given in (6).

$$\text{Average} = \frac{1}{2\pi}\left\{2(V_{\text{off}} - V_s)\sin^{-1}\frac{V_s}{\sqrt{2}V_2} + 4\sqrt{2}V_2 + V_{\text{off}}\pi\right\} \tag{6}$$

where $\sqrt{2}V_2$ is the peak sinusoid voltage. The percentage error of the FWR against V_{off} for a fixed V_s of 2 mW (a typical value for prototype devices described in Section VI) for input sinusoid peak voltages $\sqrt{2}V_2$, of 0.5, 1, and 1.5 V is shown in Fig. 4(b). As in the BPF section, the effect of the nonidealities to error is small due to full-wave rectification. The computed errors using (3) and (6) correspond to common errors as they are the same for all spectrum channels (serviced by the same time-multiplexed FWR).

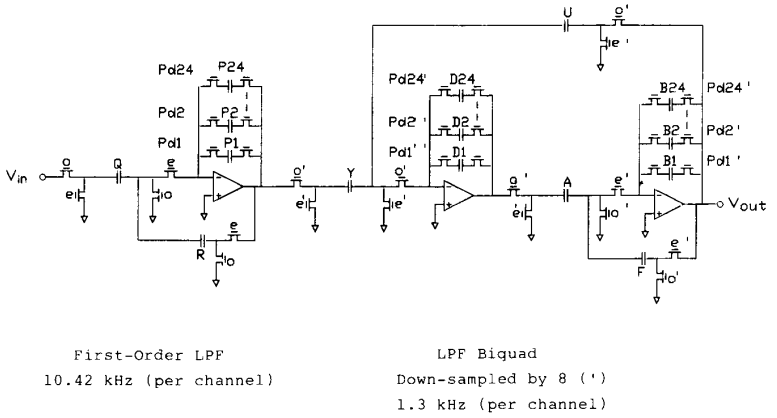


Fig. 5. Time-multiplexed third-order LPF.

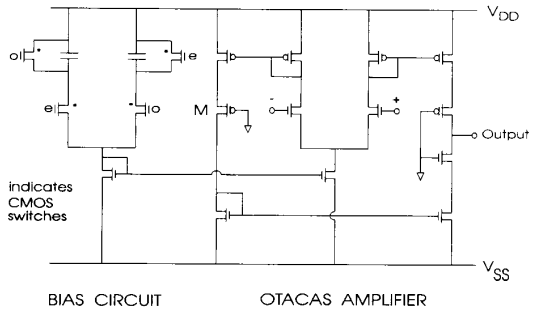
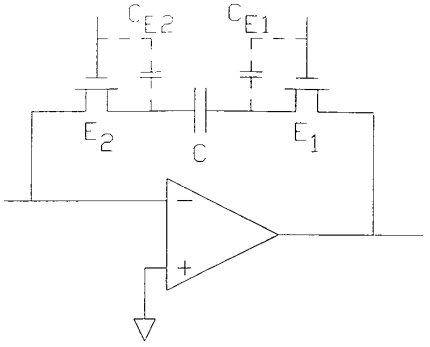


Fig. 6. Schematic of op amp and bias circuit.



Parasitic Capacitance	Switch Timing	Input Offset Voltage
C_{E2}	E_1 closes before E_2	$V_E \cdot C_{E2} / (C_{E2} + C)$
	E_2 closes before E_1	$V_E \cdot C_{E2} / C$
C_{E1}	E_1 opens before E_2	$-V_E \cdot C_{E1} / (C_{E1} + C_{E1})$
	E_2 opens before E_1	0

Note : V_E is clock switching voltage; C_{E1} and C_{E2} are parasitics associated with switches E_1 and E_2 respectively

Fig. 7. Clock feedthrough and clock phasing using modified switchings.

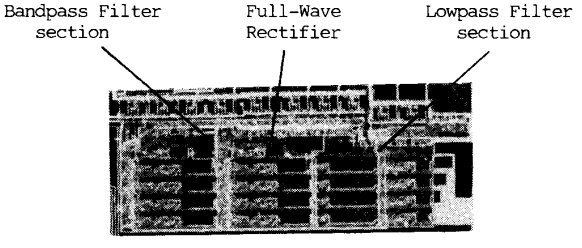


Fig. 8. Microphotograph of a prototype four-channel SC speech spectrum analyzer.

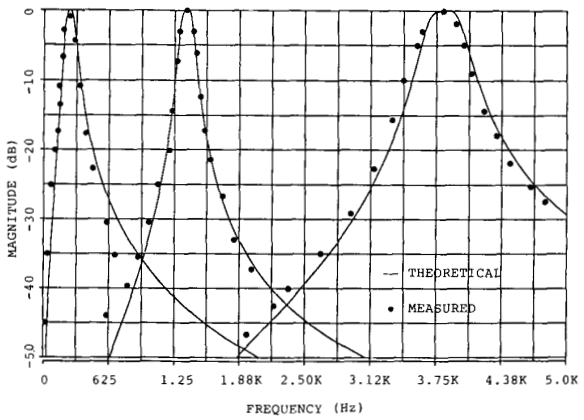
IV. Time-Multiplexed Low-Pass-Filter Section Design

The LPF synthesis utilizes the Bessel filter approximation and the LP01 [12] transformation. The LPF is sampled at the same rate as the preceding FWR for aliasing considerations, resulting in a high sampling rate to cutoff frequency ratio (approximately 300). As this high ratio yields a large cap spread, a multirate sampling technique is adopted, as depicted in Fig. 5, for the third-order LPF. The first-order LPF clocked at 10.42 kHz (per channel) shown on the left serves as an antialiasing filter to the following biquad which is down sampled by a factor of 8 (1.3 kHz per channel). All nonintegrating caps in Fig. 5 are designed so that they do not carry charge information from one local clock period to the next, and as these caps are identically valued for all spectrum channels, they are shared.

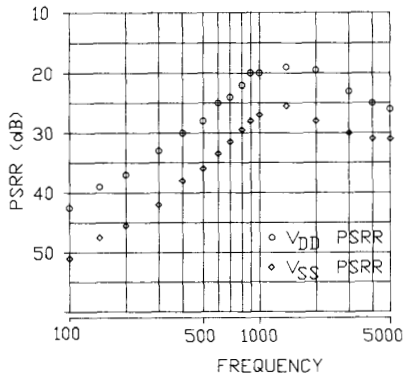
The dc offset differences between the time-multiplexed LPF's are not theoretically a problem as all LPF's (Table I) have identically valued caps. Thus, in view of errors due to dc offset differences, a time-multiplexed approach is advantageous over an unmultiplexed realization since the same time-multiplexed op amps are used. In a practical implementation, however, some small dc offset variations between LPF's are expected due to variations in LPF capacitances across spectrum channels as a result of manufacturing process, nonidentical clock signals for switches, etc. The percentage error using (3) can be computed simply by dividing the dc offset voltage by the average value of the output of the LPF. In other words, the error due to dc offset is inversely proportional to the average voltage level.

V. Design of Op Amp and Clocking

The amplifier employed shown in Fig. 6 is based on a one-stage architecture with a differential input and single output [17] and is known as an OTACAS. The symmetry of this



(a)



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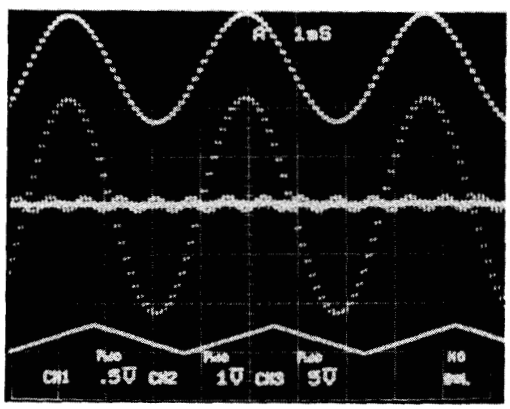
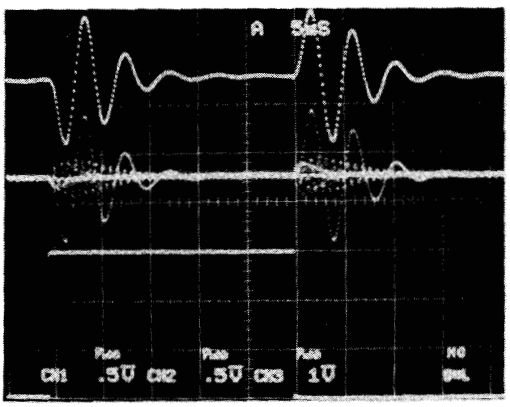


(c)



(d)

Fig. 9. (a) Theoretical and measured frequency responses of the BPF section. (b) PSRR variation plotted against positive rail, V_{DD}, and negative rail, V_{SS} (channel 12). (c) Bottom trace shows sawtooth input (270 Hz); middle trace depicts time-multiplexed output of three active and one zero-input channels; and top trace is the demultiplexed output of channel 1. (d) As (c) but depicting step responses.

op amp has, however, been improved in this design by the addition of a cascode transistor (denoted as M in Fig. 6) at one of the current mirror branches. The enhanced symmetry improves the offset performance and makes the op amp less sensitive to positive supply variations [18]. This amplifier is synchronously dynamic biased [17] where the current is swept from a high initial value (large bandwidth and high slew) down to a low value (maximum voltage gain and low power) during each biphasic clock phase. The biasing circuit is shown in Fig. 6.

In a time-multiplexed application where integrating caps are periodically connected and disconnected, there exists an open-loop condition experienced by the op amps. During this nonoverlap period when all clock signals are low, the op amps may undesirably drift to the supply rails. Several techniques to overcome this problem have been reported, requiring critical clocking circuitry or additional hardware. In the present design, the use of synchronous dynamic biasing is advantageous because the op-amp bias currents are effectively turned off during these nonoverlap intervals, resulting in insufficient slew for the op amps to drift to the supply rails.

A clocking scheme has been described in [20] to reduce clock feedthrough, and hence dc offset. This scheme can be extended to include the integrating capacitor switches clocked by local clock periods in a time-multiplexed application as shown in Fig. 7. Of particular interest from Fig. 7, it can be seen that theoretically no feedthrough occurs when the switch at the inverting input node opens before the switch at the output of the op amp at the end of a local clock period. This scheme is, however, not considered in the present design as it would significantly increase the complexity of the clock generators and the corresponding interconnections.

VI. Experimental Results

An experimental four-channel (three active channels: channels 1, 12, and 23 in Table I, and one zero-input channel) speech spectrum analyzer was fabricated using a 5-μm double-poly CMOS process. The integrated circuit layout was very regular as shown in Fig. 8 where the area allocated for each channel was equal. The active analog area was approximately 1.1×2.8 mm^2.

Fig. 9(a) depicts the close agreement between the theoretical (using SWITCAP [21]) and measured frequency responses of the BPF section. The largest dc offset difference between the

TABLE IV
SUMMARY OF MEASURED BPF CHARACTERISTICS
Temperature = 25°C, frequency response = channel 12, clocking frequency per channel = 10.42 kHz, filtering = four poles, supply = ±2.5 V, clocking = ±2.5 V

Parameter	Condition	Value
Difference DC Offset	1V peak input	8 mV
Difference Error	1V peak input	0.003 %
Integrated Noise	20 Hz - 5 kHz	239 μV_{rms}
Signal Swing	1 % THD	3 V_{p-p}
Dynamic Range		73 dB
PSRR	1 kHz, V_{DD}	-27 dB
	1 kHz, V_{SS}	-20 dB
Crosstalk	see text	-43 dB
Current Drain BPF section (4 channels : 16 poles)		496 μA
Chip Area BPF section (4 channels : 16 poles)		1.8 mm^2

BPF's in a given chip was typically 8 mV (for five chips) corresponding to 0.003% difference error (Fig. 2(d)) of the spectrum level measurement for a 1-V peak input signal. These measurements therefore show that by careful biquad design, the error due to difference dc offsets between time-multiplexed BPF's is negligible. The zero-input BPF typically observed 15 mV (0.01% common error for 1-V peak input). The current drain of the BPF section was 496 μA for a ±2.5-V supply. The total integrated noise from 20 Hz to 5 kHz was 239 μV_{rms} and the signal swing at 1% total harmonic distortion (THD) was 3 V_{p-p} (peak-to-peak) or 1.06 V_{rms}, resulting in a dynamic range of 73 dB. The performance of the BPF (channel 12) is summarized in Table IV. When a ±1.5-V power supply and ±2.5-V clocking signals were used, the current drain and dynamic range were 275 μA and 64 dB, respectively. When filters with far apart passbands were addressed successively, the crosstalk was −43 dB, meeting design specifications (< −40 dB). The variation of PSRR (V_{DD} and V_{SS}) with frequency is depicted in Fig. 9(b). Fig. 9(c) and (d) shows the responses of the BPF's to sawtooth and step inputs, satisfying the specifications in Table I.

The theoretical and measured transfer functions of the FWR are depicted in Fig. 10. The threshold voltage V_s was typically 2 mV while the dc offset V_{off} of the unity-gain inverting amplifier was typically 4 mV for all spectrum channels. The combined V_s and V_{off} represents a small common error of 0.3% for a peak signal of 1 V (Fig. 4(b)). The difference error was zero and the PSRR at 1 kHz was −25 dB. The LPF frequency response is shown in Fig. 11 where the measured response agreed well with the theoretical response. The dc offset between different LPF's was typically 3 mV within a given chip (for five chips), a difference error of 0.9% for a peak input signal of 1 V. The dc offset of the LPF's was typically 15 mV (4.7% common error) and the dc PSRR

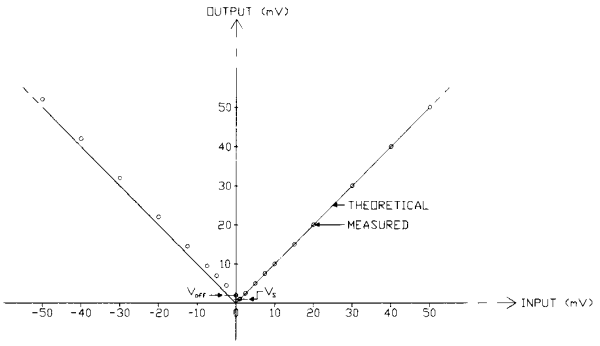


Fig. 10. Theoretical and measured frequency responses of the FWR.

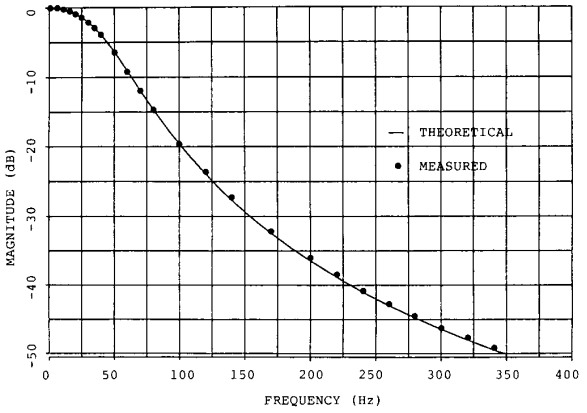


Fig. 11. Theoretical and measured frequency responses of the LPF.

was −35 dB. These measurements are summarized in Table V.

The predominant difference error between channels that limited the accuracy of the measurement of the running spectrum was from the LPF section (see second row, Tables IV and V). However, the difference errors of the BPF, FWR, and LPF sections derived on the basis of measured dc offsets and threshold voltage were small and met the design specifications. In the authors' view, these errors are satisfactory for most speech applications. The current drains of the prototype integrated circuit were 900 and 500 μA for ±2.5- and ±1.5-V supplies, respectively (the op amps were deliberately overdesigned). The final design comprising 24 channels using a 5-μm CMOS process is expected to dissipate approximately 1 mA (including clocking circuitry) with a ±1.5-V supply, and would meet the power specification for biomedical applications.

VII. CONCLUSIONS

A time-multiplexed micropower-compatible SC speech spectrum analyzer embodying several new design methodologies has been described. In the BPF section, the difference dc offset was small due to a careful biquad design, and a cap sharing technique has been used. A time-multiplexed FWR has also been proposed. Error expressions have been formulated to quantify the accuracy of the running spectrum

TABLE V
SUMMARY OF MEASURED FWR AND LPF CHARACTERISTICS
Temperature = 25°C, frequency response = channel 12, clocking frequency per channel: FWR = 10.42 kHz, and LPF = 1042 kHz (one pole) and 1.3 kHz (two poles), filtering = three poles for LPF, supply = ±2.5 V, clocking = ±2.5 V

Parameter	Condition	Value	
		FWR	LPF
Difference DC Offset	1V peak input	0 V	3 mV
Difference Error	1V peak input	0 %	0.9 %
PSRR	FWR : 1 kHz LPF : DC	-25 dB	-35'dB
Current Drain FWR section (4 Channels) LPF section (4 Channels : 12 poles)		248μA	155 μA
Chip Area (FWR and LPF sections)		0.18 mm^2	1.1mm^2

due to the nonidealities of the BPF, FWR, and LPF sections. Measurements from prototypes have verified the proposed methodologies, showed that the errors due to nonidealities meet design specifications, and were sufficiently small for most speech applications.

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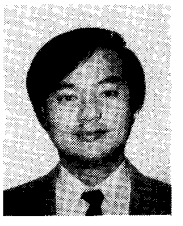

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