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Scalable Model of On-Wafer Interconnects for High-Speed CMOS ICs

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Abstract—This paper describes the development of an equivalent circuit model of on-wafer interconnects for high-speed CMOS integrated circuits. By strategically cascading two-π blocks together, the lumped model can characterize the distributed effects. Besides, the elaborately proposed model characterizes the frequency-variant characteristics with frequency-independent components. Thus, the model can be easily plugged into commercial computer-aided design tools. By adopting a newly invented optimization algorithm, namely, particle swarm optimization (PSO), the model parameters are extracted and formulated as empirical expressions. Therein, with each set of the geometrical parameters, the interconnect behaviors can be accurately predicted. The accuracy of the model is validated by comparisons with the on-wafer measurements up to 30 GHz. Moreover, the scalability of the proposed model is also discussed.

Index Terms—CMOS interconnects, empirical formulas, lumped equivalent circuit model, particle swarm optimization, scalable, scattering parameter measurements.

I. INTRODUCTION

A FIRST-TIME working wafer is the ultimate target of every integrated circuit (IC) design. However, this goal is more and more difficult to achieve as the operating frequency keeps on increasing drastically. Thus, reliable device model becomes a prerequisite. Any poorly characterized element may cause a disaster to the circuit and even the entire system [1].

Due to the ever-increasing circuit complexities and the operating frequencies, circuit performances become more and more subjected to the interconnect behaviors [2]. The lack of adequate high-speed interconnect models which are compatible with the commercial computer-aided design (CAD) tools is one of the most crucial problems facing the industry. In most available CAD tools, the interconnects are insufficiently modeled as RC components [3]. To improve the accuracy, RLC models have been proposed. Unfortunately, drawbacks still exist in those RLC models. The frequency-variant characteristics, which are substantial at high frequencies are not included in those RLC models [4]. As an improvement, some models employ frequency-variant components to characterize the frequency-variant behaviors [5]. However, up to now the simulations of this kind of components are not supported by commercial circuit simulators. Thus, there is growing interest in the field of high-speed interconnect modeling [5]–[7]. Compared with other modeling approaches, the measurement-based modeling approach has more silicon-verified accuracy and more computational efficiency [8]. This is the main reason that we adopt it as our methodology. However, the cost for the on-wafer fabrication is very high. Therefore, up to now there are very limited reports on this approach for high-speed interconnect modeling.

The extraction of model parameters is another crucial task of the model development. Both the accuracy and the efficiency have to be concerned. The performance of the extraction is strongly dependent on the chosen algorithm. The application of genetic algorithms (GAs) [8], Levenberg–Marquardt (LM), steepest descent, Gauss–Newton method [9], etc., have been reported in the literature. Very recently, a new concept named particle swarm optimization (PSO) was proposed [10]. It simulates the simplified movement of the society composed by individuals. The most distinguished point of PSO is that the members of the group share information among them. Therefore, the efficiency is increased. It is computationally inexpensive in terms of memory and time. Moreover, PSO requires only very primitive mathematical operations. It can be implemented within a few lines of computer codes [11].

In this paper, an elaborately proposed frequency-independent lumped equivalent circuit model is introduced to characterize the frequency-variant behaviors of the high-speed interconnects. Several test structures are designed and fabricated using a 0.18-μm RF CMOS process by Chartered Semiconductor Manufacture, Ltd. (CHRT). PSO is employed for the parameter extraction. Through a thorough literature search, it is the first time for PSO to be applied for model parameter extraction. After parameter extractions, empirical formulas have been generated for the model components. Thus, just like the parameterized transistor models used in SPICE, our proposed model will free the designers from having to define the detailed device characteristics. The validity of the proposed model is demonstrated by on-chip measurements over a wide frequency range from 50 MHz to 30 GHz. Besides, the scalability of the model is also discussed. Furthermore, the paper can also be used for the establishment of accurate experimental database for on-wafer high-speed interconnects.

The organization of this paper is as follows. Section II describes the designed test structures. In Section III, the proposed model construction is introduced. Section IV presents the methodology of parameter extraction using PSO and the
II. Test Structure Design and Measurement

Since the top metal layer is commonly allocated for routing critical high-frequency paths, our test structures are designed and fabricated on the top metal layer employing a CHRT 0.18-μm RF CMOS technology. The physical dimensions of the test structures are carefully selected. The lengths are various from 100 to 800 μm, while the widths are in the range of 1.5 to 20 μm. The criteria for selecting the minimum width is derived from the foundry design rules, which state that the minimum top-metal width is 1.5 μm. The reason for selecting 20 μm as the maximum width is that the widths of the devices used in typical circuits are usually less than 20 μm. The selection of the minimum length is based on the concern of the measurement precision. 800 μm is selected since the maximum length as the total die size of typical circuit subblocks is around 800 by 800 μm. Fig. 1 illustrates the top view of the fabricated test structures. Due to the space limitation of the figure, only six sets of the test structures are shown.

After fabrication, a Cascade Microtech Probe Station and an HP 8510C Vector Network Analyzer are employed for on-wafer measurement. In order to exclude the imperfections of the testing equipment, a short-load-open-through (SLOT) [12] calibration technique is performed. Then, S-parameter measurements are performed on the test structures from 50 MHz to 30 GHz. After that, the de-embedding is carried out using a Y-parameter-based technique [13].

III. Modeling Scheme

The function of the interconnects is to connect different devices or blocks together. In the low-frequency ranges, the interconnects can be characterized by frequency-independent resistors and capacitors. However, this RC model is not applicable at high frequencies, since the interconnect characteristics are much different. With the increases of the operating frequency, the inductive effect, skin effect, substrate effect, and distributed effect begin to impact [14]. All these effects are dependent on the frequency. Consequently, the characteristics of high-speed interconnects are frequency-variant as well.

Ideally, frequency-variant models should be used in the simulations. However, simulations of the frequency-variant parameters are currently not supported by the conventional circuit simulators such as SPICE, which is the essential tool for IC designers. Thus, we proposed an equivalent circuit model to characterize these frequency-variant effects with frequency-independent components.

A. Schematic Model Diagram

According to Edwards and Steer in [15], when the length of the interconnect is less than λ/20, where λ is the wave length, a lumped one-π model is adequate. When the length is longer than λ/10, the transmission line model should be used. As stated in Section II, the lengths of our test structures are various from 100 to 800 μm. In the interested frequency range, i.e., 50 MHz to 30 GHz, neither the lumped one-π model nor the transmission line model is appropriate. Therefore, the choice of the model topology should be carefully concerned.

Considering the model simplicity and the implementation facility in both time and frequency domain, we proposed a two-π lumped equivalent circuit model. By strategically cascading two-π lumped blocks together, as illustrated in Fig. 2, the distributed effects can be introduced into a compact model. In order to simplify the model construction and parameter extraction, the series blocks of each π are forced to be identical and so are the shunt blocks. This optimization is physically acceptable due to the symmetrical structure of the interconnect.

B. Equivalent Circuit Model

Based on the schematic diagram, a two-π equivalent circuit model is proposed from a physics point of view, as shown in Fig. 3.

Traditionally, on-chip interconnect was modeled as a coupled RC network [16]. The impact of the magnetic field was generally neglected. However, with the recent significant increase of the operating frequency, the impact of magnetic field and magnetic coupling cannot be neglected [17]. Hence, an inductor should be introduced in the equivalent circuit model to characterize the effects of the magnetic field. In our proposed model, the inductance is characterized by \( L_s \), which represents the ideal series inductance.
At dc, the resistance of a conductor is frequency independent. It is the function of the length, the width, the thickness, and the resistivity of the interconnect material. The component $R_s$ represents the ideal series resistance of the interconnects.

In high-speed ICs, as the operating frequency approaches multigigahertz, the skin effect becomes very significant [18]. As the skin depth decreases with the frequency increasing, the resistance of the conductor becomes frequency-variant. It increases along with the frequency. Therefore, the behavior of the interconnect becomes more resistive than inductive at high frequencies. However, as mentioned in Section I, the frequency-variant components are not supported by conventional circuit simulators. Therefore, the frequency-variant skin effect has to be characterized by carefully proposed frequency-independent components. In Fig. 3, the series components $R_{sk}$ and $L_{sk}$ connected in parallel in our proposed model are introduced to characterize the skin effect. In the paralleled branch, at low frequencies, the currents mostly pass through $L_{sk}$. When the operating frequency rises, more currents shift to the path of $R_{sk}$.

Besides the skin effect, the substrate losses are also substantial at gigahertz frequencies. In current CMOS RF technologies, unmanageable high-frequency losses are caused by the low-resistivity substrate [19]. Based on the understandings of the physical structure, the shunt block is proposed. As illustrated in Fig. 3, $C_{ox}$ represents the oxide layer capacitance. $R_{sub}$ symbolizes the substrate resistance while $C_{sub}$ represents the capacitance of the substrate.

IV. PARAMETER EXTRACTION USING PSO

A. Problem Formulation

The parameter extraction of this work can be formulated as an objective function.

First, the admittance of each subblock, as shown in Fig. 2, $Y_1$ and $Y_2$, are derived as functions of the equivalent circuit components as illustrated in Fig. 3

$$Y_1 = \frac{1}{j\omega L_{sk} + R_s + \frac{j\omega L_{sk} R_s}{j\omega L_{sk} + R_{sk}}}$$

$$Y_2 = \frac{1}{\frac{1}{j\omega C_{ox}} + \frac{R_{sub}}{j\omega C_{ox} R_{sub} + 1}}.$$  

$Y$-parameters can be presented as functions of $Y_1$ and $Y_2$, as presented in [20]. On the other hand, the measured $S$-parameters can be converted into $Y$-parameters, based on the conversion equations given in [20]. Therefore, $Y_1$ and $Y_2$ can be presented as functions of $S$-parameter. Thus, the values of $Y_1$ and $Y_2$ can be obtained from the measurement results. Therefore, the equivalent circuit components can also be obtained.

The proposed objective function $F_{0k}(X)$ is described in (3). There are two parts in $F_{0k}(X)$ connected by the plus sign. The first part is the average error between the derived admittances and those obtained from the measurements. The second part is the variance of the error

$$F_{0k}(X) = \sum_{i=1}^{m} \left( f_i(X)^2 + [f_i(X) - F_{mean}]^2 \right).$$  

In (3), the vector $X = (X_1, X_2, ..., X_n)$ represents the component values to be extracted ($L_s$, $R_s$, $L_{sk}$, and $R_{sk}$ of block $Y_1$ and $C_{ox}$, $C_{sub}$, and $R_{sub}$ of block $Y_2$). As for the parameter $k$, when it equals 1, it denotes that the objective function works for block $Y_1$. While when it equals 2, the objective function is for block $Y_2$. $n$ is the total number of parameters in each block. $m$ is the total number of frequency points under consideration. $f_i(x)$ is the error between the simulated admittance and the ones obtained from the measurement results at each frequency point under interest. The definition of $f_i(x)$ is given in (4). $F_{mean}$ is the mean error within the whole concerned frequency range, which is defined in (5).

$$f_i(X) = \frac{Y_{simulated(i)} - Y_{measured(i)}}{Y_{measured(i)}}$$  

$$F_{mean} = \frac{\sum_{i=1}^{m} f_i(X)}{m}.$$  

B. Application of PSO for Parameter Extraction

PSO [10] is employed to search for the optimal model parameters, i.e., $L_s$, $R_s$, $L_{sk}$, and $R_{sk}$ of block $Y_1$ and $C_{ox}$, $C_{sub}$, and $R_{sub}$ of block $Y_2$, which can minimize the objective function $F_{0k}(X)$. The returned component values are the optimized set that can make the simulation results fit the measurement data best. The procedure is summarized as follows.

1) Initialize a population pool of particles with random positions and velocities in the problem space. The population size is set to be 20 in this work.
2) Evaluate the fitness values according to the objective function as described in (3).
3) Compare each particle’s fitness value with the record of $pbest$ [10] of its own. If the current value is smaller than
the $p_{best}$, then the value of $p_{best}$ is changed to the current value, and the $p_{best}$ location is replaced with the current location vector.

4) Compare $p_{best}$ of each particle with $g_{best}$ [10]. If the current value is smaller than $g_{best}$, then change $g_{best}$ into the current value, and keep track of the location.

5) Change the velocity and position [10]. In this paper, $w \in [0.4, 0.9]$, $c_1 = 1$, $c_2 = 3$.

6) Repeat steps (2)–(5) until the terminating condition is satisfied, i.e., the $g_{best}$ does not change for 30 generations.

### C. Performance Analysis of PSO

The extraction performance of the PSO is compared with the GA. In order to make the comparison, the population size, initialization, terminating condition, and fitness function of the GA are set the same as the PSO. The comparison results are given in Table I.

It is clear from Table II that PSO locates near the optima significantly faster than GA. The test result implies that PSO is a more efficient tool for parameter extraction. As much as 37.3% is saved in computation time.

### V. Results, Verification, and Scalability

#### A. Results

The extracted parameters are summarized as functions of the design parameters. Therein, with every set of the length and width, the model parameters can be calculated. Then, $S$-parameters of the interconnect are also available. The summarized expressions are presented below. The coefficients of each formula are listed in Table II

\begin{equation}
L_s = a_1 + b_1l + c_1 \log W + d_1(\log W)^2 + e_1l\log W
\end{equation}

\begin{equation}
L_{sk} = a_2 + b_2l + c_2 \frac{l}{W} + d_2 \frac{d}{W^2}
\end{equation}

\begin{equation}
R_s = a_3 + b_3l + c_3 \frac{l}{W} + d_3 \frac{d}{W^2}
\end{equation}

\begin{equation}
R_{sk} = a_4 + b_4l + c_4 \frac{l}{W} + d_4 \frac{d}{W^2} + e_3l \frac{W}{d}
\end{equation}

\begin{equation}
C_{ox} = a_5 + b_5l + c_5W + d_5W^2 + e_5lW
\end{equation}

\begin{equation}
C_{sub} = a_6b_6lW^{c_6}
\end{equation}

\begin{equation}
R_{sub} = a_7b_7lW^{c_7}
\end{equation}
B. Verification

With the aid of Matlab, simulations of the proposed two-π model are performed based on the parameter values derived from the empirical formulas. The simulated S-parameters are compared with the corresponding measured ones. The plots are presented in Figs. 4–7. Considering the symmetry of the interconnect test structure, it is known that \( S_{ij} = S_{ji} \) and \( S_{ii} = S_{jj} \) [21]. Therefore, only \( S_{11} \) and \( S_{21} \) are compared here. The magnitudes and phases are plotted separately. In order to demonstrate the necessity of using the two-π model, simulation results of using a one-π model are also plotted in Figs. 4–7. One of the proposed two-π branches is adopted as the structure of the one-π model. The parameter extraction of the one-π model follows the same procedure as for the two-π model.

From these four figures of comparisons, satisfactory agreements between the simulated S-parameters employing the two-π model and the measurement results over the whole frequency range have been achieved. It demonstrates that the proposed two-π equivalent circuit model and the formulated empirical parameter expressions are capable of accurately characterizing the behaviors of the on-wafer straight-line interconnects over a large range of frequencies up to 30 GHz. It is also observed that the one-π model works well for the interconnect with the length of 100 μm. However, when the length increases, the inadequacy becomes apparent. This phenomenon can be explained by the \( \lambda/20 \) rule as stated in Section III-A.

C. Discussions of Model Scalability

It is important to note that the given formulas of the model parameters are fit to our specific test chip and process. Moreover, these formulas are only valid within a geometrical range, which is within the coverage of our test structures. For the length, the valid range is from 100 to 800 μm, while for the width, it is only applicable between 1.5 and 20 μm. However, as stated in Section II, most of the on-wafer interconnects used in high-
speed ICs are within this range. Namely, the provided geometrical extent is sufficient for most cases. For those rare cases, in which the lengths of the interconnects are longer than 800 μm, a cascading methodology can be applied. Thus, the severe distributed effect can be characterized. First, the long connection is split into smaller segments with lengths less than 800 μm. Then, two-π models are developed for each segment. After that, those two-π blocks are cascaded together to form the complete model for the entire connection. This method has been employed to form a 1600-μm interconnect with two 800-μm segments, an 800-μm interconnect with two 400-μm segments, as well as to a 400-μm interconnect with two 200-μm segments. Referring to Figs. 8–11, the simulated results agree well with the measurement data (due to the lack of the measurements of 1600 μm, an electromagnetic (EM) simulator IE3D is employed to generate the reference curve). These experiments also prove the scalability of our proposed model.

VI. CONCLUSION

A two-π lumped equivalent circuit model has been developed for on-wafer high-speed interconnects. Complicated frequency-variant effects have been characterized by frequency-independent components. The scalability of the proposed model has also been discussed and proved.

It is the first time that the newly proposed PSO is applied to the parameter extraction of an equivalent circuit model. The performance of PSO is compared with GA, which is widely used for optimization. The comparison result implies that PSO is a more efficient tool for parameter extraction. The computation time saved is as much as 37.3%.

The extracted parameters are summarized as empirical expressions. Therefore, it only requires the acknowledgement of geometrical dimensions of the interconnect to obtain the accurate performance prediction. Since the equivalent circuit model consists only ideal SPICE compatible elements, namely, frequency independent resistors, inductors, and capacitors, the model can be directly incorporated into commercial circuit simulators as subcircuit prototype.

REFERENCES

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