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<th><strong>Title</strong></th>
<th>0.058 mm² 13 Gbit/s inductorless analogue equaliser with low-frequency equalisation compensating 15 dB channel loss</th>
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<td><strong>Author(s)</strong></td>
<td>Balachandran, Arya; Chen, Yong; Choi, Pilsoon; Boon, Chirn Chye</td>
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This letter presents an inductorless 13 Gb/s analog equalizer with an additional low frequency equalization (LFEQ) to counter the low frequency channel losses. An active feedback topology for the proposed equalizer together with negative capacitance circuit is used to extend the bandwidth to compensate a 15 dB channel loss at Nyquist. The LFEQ improves the measured data jitter of the conventional equalizer from 0.41 UI to 0.12 UI for a pseudorandom binary sequence (PRBS) of $2^{31}-1$. The proposed prototype was implemented in 65 nm CMOS, occupying active area of merely 0.058 mm$^2$. It exhibits a power efficiency of 1.07 mW/Gb/s under a supply voltage of 1.2 V and a BER < 10$^{-12}$.

Introduction: Due to the demand for wide bandwidth at data rate of tens of Gb/s, inductive peaking [1] for the analog equalizers is commonly used in the wireline receivers. However, the passive inductors result in large area, thus making the overall solution not suitable for compact on-chip wireline solutions. Conventional linear equalizers [2-5] also tend to overlook the low frequency losses from the cable, owing to smooth slope of the low frequency losses compared to the sharp slope of high frequency losses. However, as the eye measurement extends over several UL, the long-term inter-symbol interferences (ISIs) caused by the low frequency losses result in increased data jitter.

The proposed analog equalizer implements an intermediate to high frequency equalization, while providing an additional LFEQ to counter the long-term ISIs. Bandwidth improvement in the absence of inductive peaking is achieved by an active feedback [6] topology as well as through capacitance reduction at the output, via a negative capacitance (NC) circuit [7]. The fixed LFEQ in the active feedback creates a zero-pole pair at low frequencies and thus, counts the low frequency channel losses resulting in an improved transient performance over long measurement samples.

Analog Equalizer Cell: The proposed equalizing cell (Fig. 1) consists of a continuous time linear equalizer (CTLE), a fixed LFEQ and a NC circuit. The CTLE comprises of a conductance stage which is source degenerated with a resistor ($R_{SD}$) and a varactor ($C_I$), which are tuned by two voltage controls, $V_{C_{BS}}$ and $V_{C_{CS}}$ respectively. The second stage of the equalizing cell uses an active feedback for bandwidth extension in the absence of inductive loading as well as provides a fixed equalization in the lower and wider frequency range with minimal peaking.

![Fig. 1. Schematic of the proposed equalizing cell](image_url)

The variable RC-degeneration in the first stage (Fig. 1) provides the dc gain and high frequency peaking, without an inductive load. The variable gain boosting is realized by varying the resistive degeneration. As $V_{C_{BS}}$ increases, the source node of $M_1$ gets increasingly degenerated with a reduced $R_{SD}$, leading to an overall increase in the dc gain. The zero and the poles of the CTLE are given in (1). $\omega_{z1}$ is decided by the degeneration elements, $R_{SD}$ and $C_I$. $C_{CS}$ primarily decides the location of $\omega_{z2}$, for a given bias current of the differential stage, $I_{bc}$ and the effective load capacitance, $C_{LS}$ as seen by the CTLE output, decide $\omega_{p2}$.

$$\omega_{z1} \approx \frac{1}{R_{SD}C_I}, \quad \omega_{z2} \approx \frac{g_{m1}}{C_S}, \quad \omega_{p2} \approx \frac{1}{R_{L1}C_{LS}} \quad (1)$$

The proposed inductorless 13 Gb/s LN-CTLE has been successfully implemented in 65 nm CMOS technology. The performance of the proposed CTLE is depicted in Fig. 2. The simulated frequency response of the overall equalizer is shown in Fig. 2(b), which shows a loss of ~15 dB at 6.5 GHz. The measured frequency responses are provided in Fig. 2(c). The LFEQ stage in each of the equalizing filter provides a gain of 2.8 dB. The improvement in the simulated frequency response of the overall equalizer, for the lower frequencies starting at ~250 MHz in the presence of the channel with LFEQ is demonstrated in Fig. 2b.

The frequency responses of the overall linear equalizer were simulated to verify the tunability of $V_{C_{BS}}$ (Fig. 3a) and $V_{C_{CS}}$ (Fig. 3b). When $V_{C_{CS}} = 1.0$ V, the overall gain variation is up to 15 dB. The zeros shift towards higher frequency as $V_{C_{BS}}$ decreases under the fixed $V_{C_{CS}}$. For the time-domain response, the effect of LFEQ is seen as an improved jitter performance. The parasitic annotated simulations of the overall equalizer show that the peak-to-peak data jitter improved from 25 ps of that of a conventional equalizer to 6.5 ps with the proposed equalizer.
The proposed prototype was fabricated in 65 nm CMOS with a compact active area of 0.058 mm$^2$, as shown in the die photograph with zoomed-in layout (Fig. 4). The measurement setup for the prototype consists of the probe station, the serial J-BERT (N4903B) and oscilloscope (Agilent 86100A).

Fig. 4. Die photo with zoomed-in layout

The eye diagrams at the output of the conventional CTLE without LFEQ (Fig. 5a) and at the output of the proposed equalizer with LFEQ (Fig. 5b) at 13 Gb/s are shown for a 2$^{31}$-1 PRBS input pattern, with >1.3k input samples. The pk-to-pk data jitter shows a marked improvement from 32 ps (0.41 UI) in the conventional CTLE to 9.34 ps (0.12 UI) in the proposed equalizer with an eye height of 185 mVpp. The design achieves a measured horizontal eye opening of 0.66 UI at BER < 10$^{-12}$. The total active power consumption is 14 mW under a supply voltage of 1.2 V, resulting in a figure of merit (FOM) of 0.071 pJ/bit/dB. Table 1 summarizes the die performance and the comparison with the prior art.

Fig. 5. Measured 13 Gb/s eye diagrams
a Conventional CTLE without LFEQ
b Proposed equalizer with LFEQ

Measurement Results: The proposed prototype was fabricated in 65 nm CMOS with a compact active area of 0.058 mm$^2$, as shown in the die photograph with zoomed-in layout (Fig. 4). The measurement setup for the prototype consists of the probe station, the serial J-BERT (N4903B) and oscilloscope (Agilent 86100A).

Table 1: Die summary and benchmark with prior art.

<table>
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<tr>
<th>Data rate (Gb/s)</th>
<th>Technology (CMOS)</th>
<th>Supply (V)</th>
<th>Channel loss @ Nyquist (dB)</th>
<th>Inductor load</th>
<th>Area(mm$^2$)</th>
<th>Horizontal Eye$^2$ (UI) / BER</th>
<th>Power Efficiency (mW/Gb/s)</th>
<th>FOM (pJ/bit/dB)</th>
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<tbody>
<tr>
<td>10</td>
<td>130 nm</td>
<td>1.2</td>
<td>12</td>
<td>Yes</td>
<td>0.35</td>
<td>- / 0.68 / 0.62 / 10$^{-12}$</td>
<td>0.41 / 1.43 / 3.8</td>
<td>0.034 / 0.095 / 0.108 / 0.071</td>
</tr>
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Concluded: This letter has reported an inductorless analog equalizer with the LFEQ. Fabricated in 65 nm CMOS, the prototype exhibits a FOM of 0.071 pJ/bit/dB at 13 Gb/s and an ultra-compact active area of 0.058 mm$^2$. The proposed equalizer reduces the equalized data jitter from 0.41 UI to 0.12 UI for 15 dB channel loss against a conventional linear equalizer.

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Arya Balachandran and Chirm Chye Boon (VIRTUS, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore)

E-mail: arya001@e.ntu.edu.sg

Yong Chen (State Key Laboratory of Analog and Mixed-Signal, University of Macau, Macao, People’s Republic of China)

Pilsoon Choi (Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA, USA)

References