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Author(s)	Lin, Yiding; Anantha, P.; Lee, Kwang Hong; Chua, Shen Lin; Shang, Lingru; Tan, Chuan Seng
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Geometry and Thermal Stress Analysis of In-plane Outgassing Channels in Al_2O_3-Intermediated InP (Die)-to-Si (Wafer) Bonding

Yiding Lin,[a,b] P. Anantha,[a] Kwang Hong Lee,[b] Shen Lin Chua,[c] Lingru Shang,[a] and Chuan Seng Tan[a,b,c,z]

[a]*School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798*
[b]*Low Energy Electronic Systems (LEES), Singapore-MIT Alliance for Research and Technology (SMART), Singapore 138602*
[c]*Temasek Laboratories@ NTU, Research Techno Plaza, Singapore 637553*

Thermal-mechanical characteristics and outgassing efficiency of integrated in-plane outgassing channels (IPOCs) at Al_2O_3-intermediated InP (die)-to-Si (wafer) bonding interface is investigated. The IPOCs are introduced and investigated via both multi-physics simulation and experimental demonstration. Thermal stress simulation indicates that Al_2O_3 bonding layer efficiently mitigates the stress as observed at top InP surface, compared to that of conventional SiO_2 intermediate layer. By introducing IPOCs, the thermal stress decreases with increasing IPOC spacing-to-width (*S*/*W*) ratio. Experimentally, high quality InP/Al_2O_3/Si direct bonding is firstly demonstrated. Seamless bonding interface is observed, along with reasonable bond shear strength of 2.57 MPa and minimal residual stress in the transferred InP layer. Efficiency of the IPOCs is then evaluated by comparing interfacial void densities of InP bonded on dimension-varied-IPOC-patterned Si. A significant void density reduction up to two orders of magnitude is observed, with a decreasing *S*/*W* ratio. An optimal *S*/*W* ratio of 2.5 is therefore proposed to compromise between the thermal stress degradation (∼10%) and outgassing efficiency improvement (∼90% void density suppression). This work is thus significant as it could provide guidelines to establish high quality hybrid-integrated optoelectronic devices for Si photonic applications.
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Silicon Photonics[1,2] has attracted prominent interest with its promising applications for optical interconnects in CMOS electronics[3] with advantages of high speed, cost effectiveness and low power consumption over conventional Cu interconnects. However, the inherent challenge for Si to lase due to its indirect bandgap nature has made realizing monolithic silicon photonic integrated circuits difficult. Therefore, hybrid-integrated platforms of III-V based materials on Si[4,5] has been developed, making use of their direct bandgap advantage for substantial numbers of active optoelectronic device applications.[6]

In realizing such hybrid platforms, direct wafer bonding method is widely utilized. Recently, Fan et al.[7] and Anantha et al.[8] reported successful InP (die)-on-Si (wafer) direct bonding utilizing thin high-*k* Al_2O_3 as the intermediate bonding layer. Both studies indicate that Al_2O_3 exhibits superior thermal dissipation and inter-diffusion barrier properties than that of SiO_2-intermediated InP/Si bonding.[9] However, the bonding quality is still limited by interfacial voids which may cause optical coupling scattering or loss.[10] These voids are formed by the accumulation of gas by-products (mainly consisting of H_2 and H_2O molecules), generated from interfacial polymerization reactions,[11] at residual bonding interfacial hydrocarbon sites.[12] Several approaches have been investigated to suppress the interfacial void density.[10,13–17] Liang et al.[10] used vertical outgassing channels (VOCs) in InP-on-SOI bonding to absorb and out-diffuse the gas by-products into porous buried SiO_2 layer. Although void-free bonding has been achieved, these absorbed gases were found to cause serious film delamination at high temperature post-bonding processes.[13] Zhang et al.[14] and Matsumoto et al.[15] adopted long post-bonding annealing and temperature ramp time, respectively, to achieve minimized void size and density. However, long annealing time inhibits the fabrication throughput and therefore may not be an optimal solution.

On the other hand, in-plane outgassing channel (IPOC) can be an efficient outgassing approach. Earlier work by Kissinger et al.[16] and Ram et al.[17] reported the advantages and application of IPOCs, respectively, for successful demonstration of bonding interfacial void suppression. Recently, Zhang et al.[13] also employed IPOCs at InP/Si bonding interface in combination with VOCs for successful InP regrowth on bonded InP films. However, detailed analysis of IPOC outgassing efficiency has not been investigated yet. Meanwhile, low thermal conductivity of air (∼0.026 WK^{-1} m^{-1} at 20°C[18]) occupied in the IPOCs might cause degraded heat dissipation of the bonding structure. The hindered thermal dissipation may further induce stress-correlated issues. Several reports[19,20] have shown thermal stress-induced device reliability deteriorations.

Therefore, in this work, influence of bonding-interfacial IPOC design parameters on thermally-induced stress and outgassing efficiency characteristics of InP/Al_2O_3/Si homogeneous bonding is studied. The thermally-induced stress is investigated by finite element multi-physics simulation. The thermal stress between Al_2O_3 and SiO_2 intermediate layers is compared. To investigate the IPOC parameter effect, width- and spacing-varied IPOCs are inserted and fabricated in the simulation model and at the bonding interface, respectively. Thermal stress and interfacial void densities are compared accordingly and an improved IPOC spacing-to-width (*S*/*W*) ratio is ultimately proposed to optimize between thermal stress degradation and outgassing efficiency improvement.

Thermal Stress Analysis

Finite element simulator - COMSOL Multiphysics was used to study thermal stress characteristics of InP-on-Si bonded structures. Only a quarter of the structure was simulated, utilizing structure symmetrical property. The models without IPOCs were firstly constructed with its geometry as shown in Figures 1a and 1b. The models consist of InP and Si layers with thickness of 1 μm and 15 μm, respectively, to represent the real bonded structure without compromising the simulation accuracy. An intermediate oxide (Al_2O_3 or SiO_2) bonding layer was inserted in between. To link the thermal stress analysis to prior studies,[7–9] the oxide layer thickness is varied from 10 to 200 nm. Based on the estimation in Ref. 7, a heat flux of 1×10^8 W/m^2 was applied on the top InP surface. All the material parameters used are listed in Table I, which are also identical to prior work.[7] All the materials are assumed to be linear elastic and the strain-free temperature was set at room temperature (25°C). The thermal stress induced on top of InP from the models are compared to a direct bonding model (without intermediate layer) for analysis.

Figure 2 shows the thermal stress induced on top InP layer as a function of intermediate layer thickness. The reference line corresponds to the stress from a direct-bonded InP-on-Si structure, without any intermediate layer. It is observed that the thermal stress of InP/Al_2O_3/Si structure reveals negligible variation with respect to Al_2O_3 thickness, as well as that of InP-on-Si structure. While the thermal stress of InP/SiO_2/Si structure increases significantly with increasing intermediate layer thickness. The large thermal stress

[z]E-mail: tancs@ntu.edu.sg

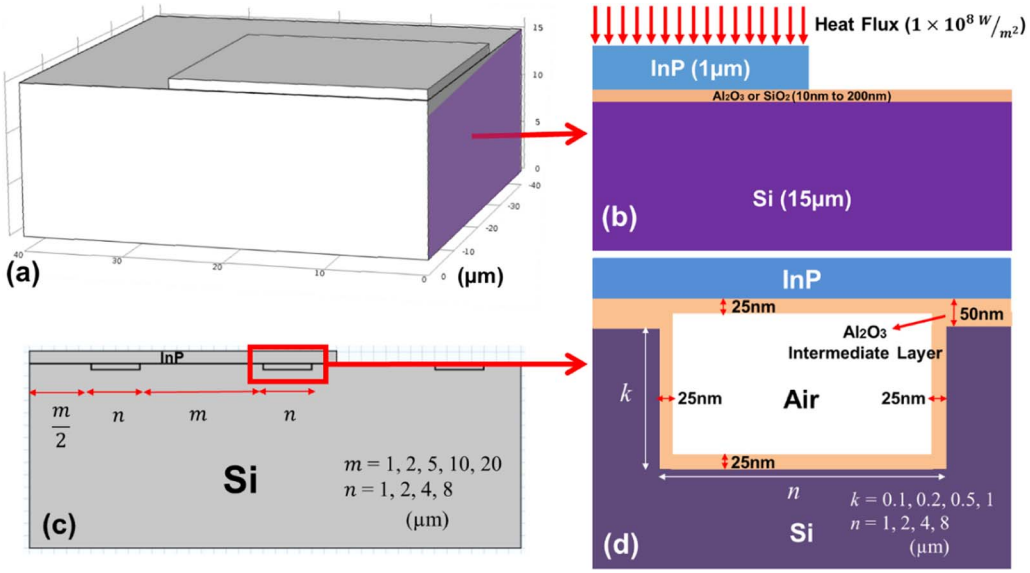

Figure 1. The COMSOL model geometry top view (a) and side view (b); Cross-sectional view of the model geometry with IPOCs inserted (c), with the highlighted close-up view shown in (d).

difference between InP/Al_2O_3/Si and InP/SiO_2/Si structures is due to lower thermal conductivity of SiO_2 than that of Al_2O_3, as discussed in Ref. 7. In general, the thermally-induced strain, ε, between the two adjacent layers is linearly proportional to the temperature deviation ΔT, as shown below:[21]

$$\varepsilon = \Delta T \times (\alpha_A - \alpha_B) \quad [1]$$

where α_A and α_B refer to the coefficients of thermal expansion (CTE) of Si and InP, respectively. Therefore, the thermally-induced stress follows the corresponding temperature profile. The lower thermal conductivity of SiO_2 increases InP/SiO_2/Si temperature, and the thermal stress as a consequence. More careful inspection of the plot further reveals that the thermal stress of InP/Al_2O_3/Si structure slightly decreases with increasing intermediate layer thickness. This might be attributed to the larger CTE of Al_2O_3 ($8.0 \times 10^{-6}K^{-1}$) than that of both InP ($4.8 \times 10^{-6}K^{-1}$) and Si ($2.6 \times 10^{-6}K^{-1}$). This would result in larger thermal expansion of Al_2O_3 to mitigate the compressive strain on top InP layer induced by InP and Si thermal mismatch. On the contrary, the lower CTE of SiO_2 ($0.56 \times 10^{-6}K^{-1}$) would aggravate the top InP compressive thermal strain. Therefore, compared to SiO_2, Al_2O_3 intermediate layer provides superior thermal stress mitigation, to prominently release the top InP thermal stress.

IPOCs are then inserted into the model with 50 nm Al_2O_3 intermediate layer to study their impact on thermal stress characteristics. The cross-sectional views of the IPOC are shown in Figures 1c and 1d. The IPOCs are designed on Si wafer due to ease of process and only unidirectional IPOCs are considered for the sake of efficient outgassing. Channel width, n, channel spacing, m, and channel depth, k, are varied as listed in Table I. Al_2O_3 deposited is assumed to be conformal with the sidewalls of the channels and the space in channels is filled with air. All other simulation settings remain identical. Figure 3a shows the thermal stress characteristics of InP/Al_2O_3/Si with 0.5 μm IPOC depth as a function of channel width at different channel spacing. The thermal stress is found to increase with increasing channel width regardless of channel spacing variations. Furthermore, the gradient of thermal stress increment decreases with widening of channel spacing. The thermal stress at 8 μm channel width increases by 297% at 1 μm spacing while only a 6% increase is observed at 20 μm spacing. The intensified thermal stress is explained by the equivalent thermal resistance increase at InP/Al_2O_3/Si bonding interface caused by stagnant air of low thermal conductivity occupied in the channels. With channel width widening or channel spacing shrinkage, the equivalent thermal resistance at the bonding interface increases further and thus drags up the thermal stress. Figure 3b shows the thermal stress characteristics of InP/Al_2O_3/Si with 10 μm channel spacing as a function of channel width at different channel depths. Similar trend in thermal stress increment with respect to channel width is observed. It is specifically found that, the thermal stress at 8 μm width increases only by 11% from 100 nm to 1 μm channel depth. Therefore, compared to channel width and spacing, channel depth is relatively an insignificant factor to influence InP/Al_2O_3/Si thermal stress. It is the area

Table I. Material parameters used in thermal stress analysis.

Material Parameters	Si	InP	SiO_2	Al_2O_3
Coefficient of Thermal Expansion ($\times 10^{-6}$ K^{-1})	2.6	4.8	0.56	8.0
Poisson's Ratio	0.28	0.36	0.17	0.22
Young's Modulus (GPa)	165	61	75	400
Thermal Conductivity (W/m•K)	131	68	1.4	30

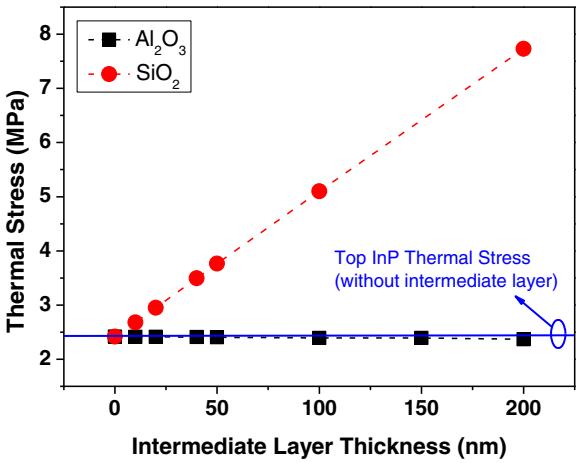

Figure 2. Thermal stress induced on InP as a function of intermediate layer thickness. The reference line indicates the top InP thermal stress from InP/Si bonding without intermediate layer.

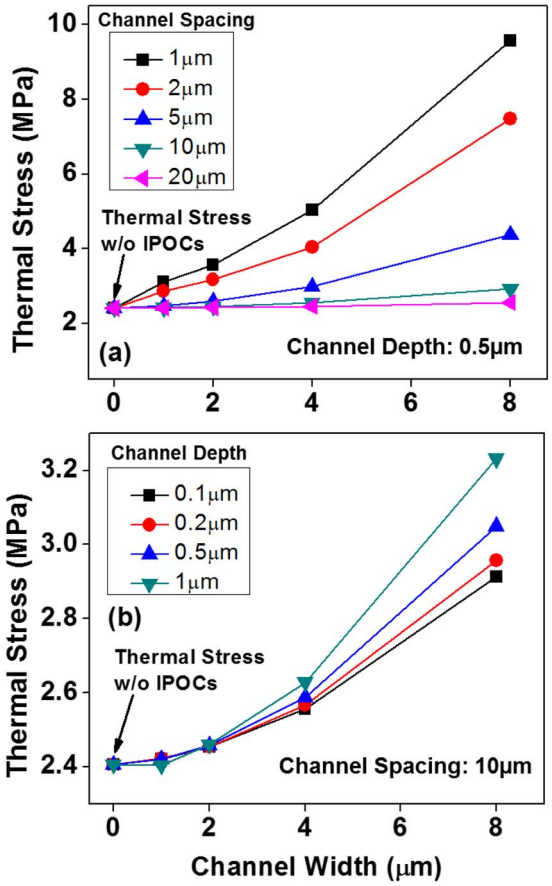

Figure 3. Thermal stress induced on InP as a function of (a) IPOC width and spacing, with depth of 0.5 μm and (b) IPOC width and depth, with spacing of 10 μm.

occupied by IPOCs at the bonding interface that significantly intensifies the thermal stress. Channel width and spacing as a consequence, should be designed narrower and wider respectively. This minimizes the influence of thermal stress toward the bonded structure.

To better understand the influence of channel width and spacing on InP/Al_2O_3/Si thermal stress characteristics, IPOC Spacing-to-width (*S*/*W*) ratio is introduced. *S*/*W* ratio is defined as the ratio between the channel spacing and channel width. Figure 4 shows the thermal stress of InP/Al_2O_3/Si as a function of *S*/*W* ratio. The thermal stress decreases sharply with increasing *S*/*W* ratio below ~2.5, above which the decrement becomes gradual. To investigate the extent of InP/Al_2O_3/Si thermal stress deterioration with IPOC insertion, the simulated thermal stress of InP/50nm-SiO_2/Si without IPOCs was added into the plot (lower reference line). It is found that InP/Al_2O_3/Si could maintain its thermal stress superiority over InP/SiO_2/Si for *S*/*W* ratio above 1. In addition, the simulated thermal stress of InP/Al_2O_3/Si (without IPOCs) at 300°C (post-bonding annealing temperature) is inserted to predict the risk of film de-bonding due to IPOC-induced thermal stress. As crack-free InP/Al_2O_3/Si bonding has been achieved experimentally,[22] in which 300°C annealing was experienced, it is inferred that the thermal stress induced by IPOCs might not cause the bonded layer to crack/de-bond because it is still far less than that at 300°C annealing (upper reference line).

Experimental

InP (Die)/Al_2O_3/Si (Wafer) direct bonding.— InP direct bonding on plain Si was firstly investigated using Al_2O_3 as the intermediate layer. Here n-type 6-inch silicon wafers with 625 μm thickness, (100) in orientation, 25 Ω•cm in resistivity and less than 10 μm in total

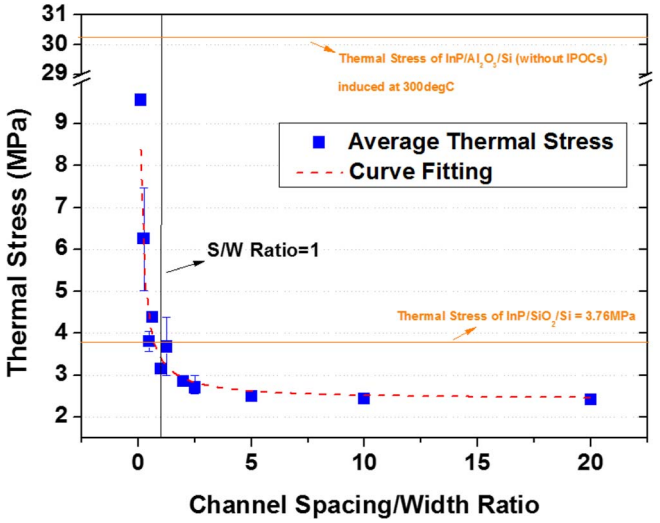

Figure 4. Thermal stress induced on InP as a function of IPOC spacing-to-width ratio. The right tick label indicates the normalized thermal stress with respect to that of InP/Al_2O_3/Si direct bonding (without IPOCs).

thickness variation (TTV) were utilized. As-purchased InP wafer was used with epi-layers of 100 nm $In_{0.53}Ga_{0.47}As$ and 50 nm InP grown sequentially on semi-insulating SI (100) InP substrate (2-inch, n-type, S-doped and thickness of 350 ± 50 μm). The InGaAs layer acts as an etch-stop layer to protect the epi-InP layer from being removed in post-bonding InP substrate wet etching process. The Si wafers were cleaned using standard Piranha solution to eliminate surface organic contaminants. The InP wafers were firstly rinsed in acetone followed by isopropyl alcohol (IPA) to remove surface particles. 30% NH_4OH solution cleaning was then carried out to remove the native oxide. Cleaned Si and InP wafers were deposited with 10 nm Al_2O_3 high-*k* dielectric deposition at 250°C using ALD (atomic layer deposition). The deposition thickness and temperature are based on literature reports.[8] As single or arrays of optoelectronic devices are generally required in photonic integrated circuits, InP-die-to-Si-wafer bonding approach is adopted for convenient placement and economic advantages. Therefore, after Al_2O_3 deposition, the InP wafers were diced into 1 cm × 1 cm dies. Prior to bonding, both InP dies and Si wafer are treated with 15 s O_2 plasma surface activation, followed by deionized (DI) water rinsing. The purpose of O_2 plasma activation is to remove surface hydrocarbon contaminants[14] and improve surface hydrophilicity.[23] The subsequent DI water rinsing step is to passivate the bonding surface with high density of hydroxyl (-OH) groups. Both these steps aid in improving the bond strength. The rinsed Si wafer and InP dies were spin-dried and N_2 blow-dried, respectively. Finally, epi-layer-side of the InP dies were manually placed on Si in cleanroom ambient to initiate bonding. Post-bonding treatment (applying 3 MPa external pressure for 2 hours followed by 300°C annealing for 3 hours) was followed to further enhance the bond strength.

IPOCs design and fabrication.—IPOCs design on Si wafer.— IPOC dimension parameters are designed based on prior relevant work[10,13,17] to pair up with above thermal stress study, as tabulated in Table II. As it is learnt that IPOC depth does not significantly alter

Table II. IPOC parameter design for thermal stress analysis.

	IPOC Width, *n*	IPOC Spacing, *m*	IPOC Depth, *k*
Variables (μm)	1	1	0.1
	2	2	0.2
	4	5	0.5
	8	10	1
		20	

Table III. IPOC parameter design for outgassing efficiency study.

	IPOC Width, n	IPOC Spacing, m	IPOC Depth, k
Variables (μm)	2	2.5	0.15
	4	5	
	8	10	
	16	20	

InP thermal stress, it is fixed at 150 nm. The reasoning behind is that 150 nm is sufficient to diffuse out the bonding gas by-products since these gas molecules are normally of sub-nanometer size.

As discussed before, IPOCs are patterned on Si wafers. Figure 5a shows the schematic of a novel IPOC distribution design for all width and spacing parameter combinations. 100 μm-wide IPOC-free areas were introduced between adjacent IPOC regions consisting of 10 channels, for the purpose of sustaining adequate bonding area. This also enables one to conveniently observe void density contrast between IPOC and IPOC-free areas.

IPOCs fabrication.—The fabrication process flow of patterning IPOCs on Si wafers is illustrated in Figure 6a. The piranha-solution-cleaned Si wafer was firstly spin-coated with photoresist (PR). After soft-baking, UV exposure and PR development, reactive-ion etching (RIE) was carried out using Cl_2 plasma to form the IPOCs. After RIE, the residual PR was removed by O_2 plasma ashing. Figure 6b shows the scanning electron microscope (SEM) image of patterned IPOCs. The inset depicts the corresponding cross-sectional SEM image. Surface profiler measurement confirms the trench depth as 147.9 nm, which is within design expectation. The IPOC-patterned Si wafer was then deposited with Al_2O_3 and the bonding process was carried out identically to InP/Al_2O_3/Si direct bonding.

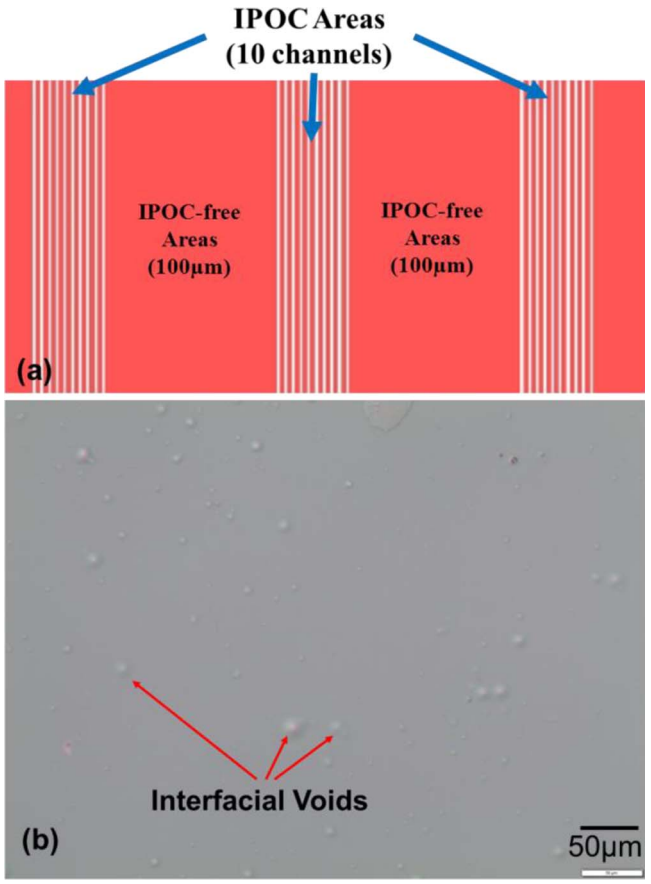

Figure 5. (a) IPOC distribution design for all width and spacing parameter combinations; (b) Optical microscope image of non-IPOC-patterned InP/Al_2O_3/Si bonded sample after InP substrate removal, with high density of interfacial voids seen (~3.6 ×10^4 cm^{-2}).

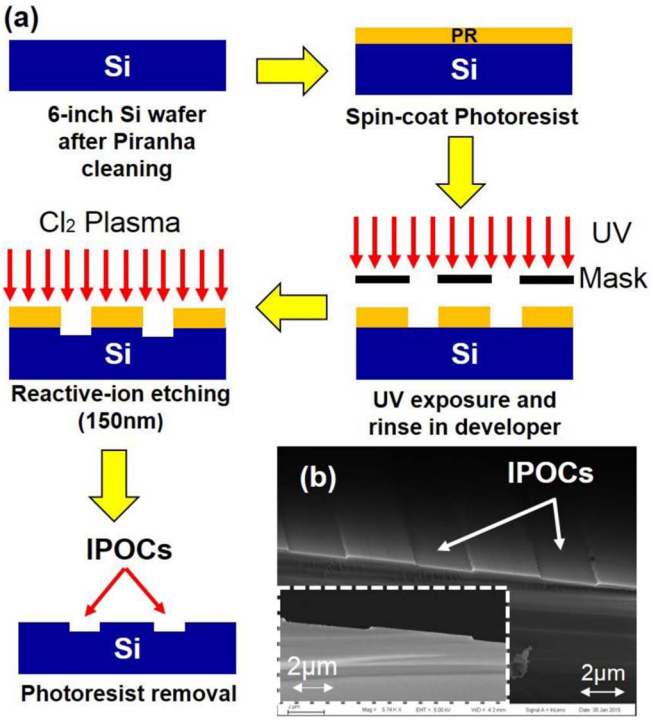

Figure 6. (a) Schematics of IPOC fabrication process flow on Si wafers; (b) SEM image of fabricated IPOCs, with the cross-sectional image shown in the inset.

Wet chemical etching.—Post bonding, the bonded InP dies were immersed into HCl: H_3PO_4: H_2O (3:2:1) mixed solution to remove the InP substrate. Due to its high etching selectivity of InP from InGaAs,[24] the wet etching automatically stops at the InGaAs layer to protect the epi-InP underneath for further characterization.

Results and Discussion

InP/Al_2O_3/Si direct bonding (without IPOC patterning).—InP/Al_2O_3/Si direct bonding without IPOC patterning was firstly performed. Figure 7a shows the 5 μm × 5 μm atomic force microscopy (AFM) 3D surface profile of InP die after O_2 plasma activation. Its corresponding surface contact angle is shown in the inset to evaluate surface hydrophilicity. The InP surface observed is smooth and contaminants free, with a 0.27 nm RMS roughness well below ~0.5 nm requirement for successful bonding.[25] The measured contact angle of 8.4° is also sufficient to form a hydrophilic InP surface for strong bonding.[22] The IR image of the InP die-bonded wafer is shown in Figure 7b. Majority of the dies are well bonded, only presenting un-bonded regions at the edge of the dies seen as darker fringes. The reason for the appearance of un-bonded regions could be due to contaminants introduced at the bonding surface during pre-bonding process as well as chipped/scratched surface caused during the InP dicing process.

After chemical etching of the InP substrate, the samples were cleaved from back side Si to reveal the cross-sectional bonding interface. Figure 7c shows the SEM image of the bonding interface. The InP layer is found to be seamlessly adhered to Si substrate, without any voids seen at bonding interface. This verifies strong interfacial bonding energy as it can withstand the highly destructive mechanical cleaving process. Die shear test further confirms reasonably strong bonding energy by obtaining maximum shear strength of 2.57 MPa, which is higher than reported values.[26,27]

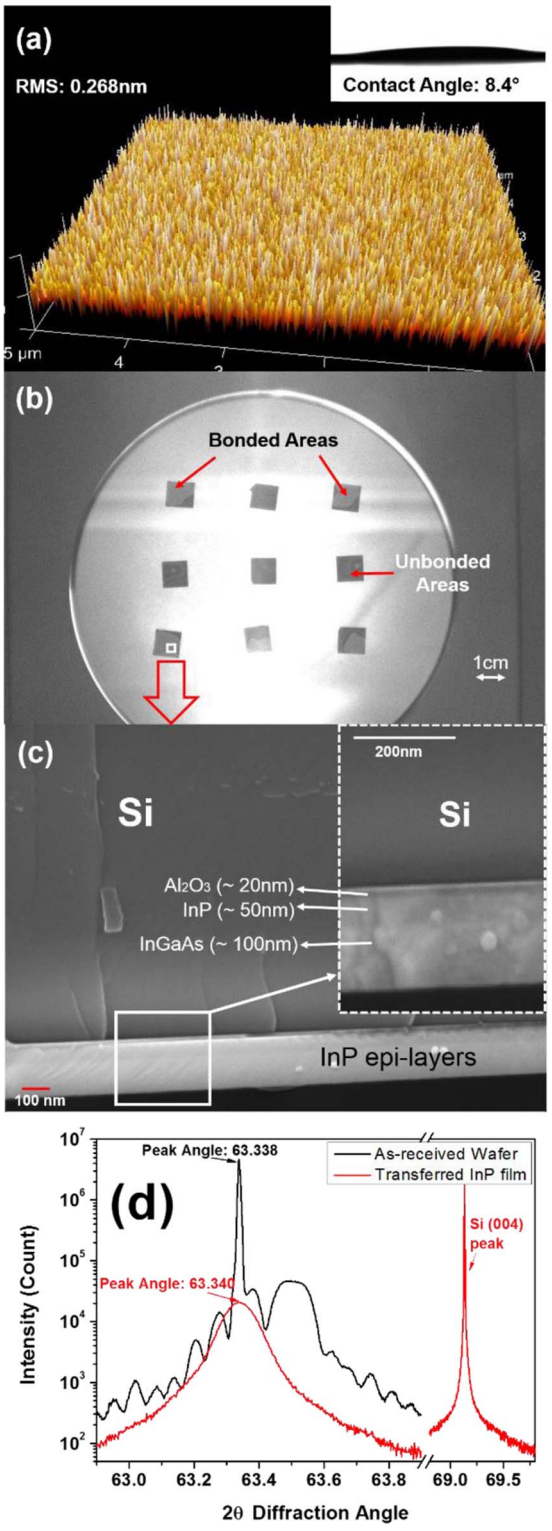

Figure 7. (a) AFM scan of 10 nm Al_2O_3-deposited InP die after 15 s O_2 plasma activation, with the corresponding contact angle shown in the inset; (b) IR image of InP dies bonded onto Si, with 20 nm Al_2O_3 employed as intermediate layer; (c) Cross-sectional SEM image of the bonded InP die on Si (highlighted in (b)); Inset shows the magnified image of the bonding interface; (d) XRD ω-2θ characterization of the InP/Al_2O_3/Si bonded sample, with (004) rocking curve of as-received InP epi-wafer as reference.

Further, XRD ω-2θ scan of the bonded sample is performed to evaluate material quality (Figure 7d). The as-received InP epi-wafer is used as reference. Bonded InP film (004) peak is found to be

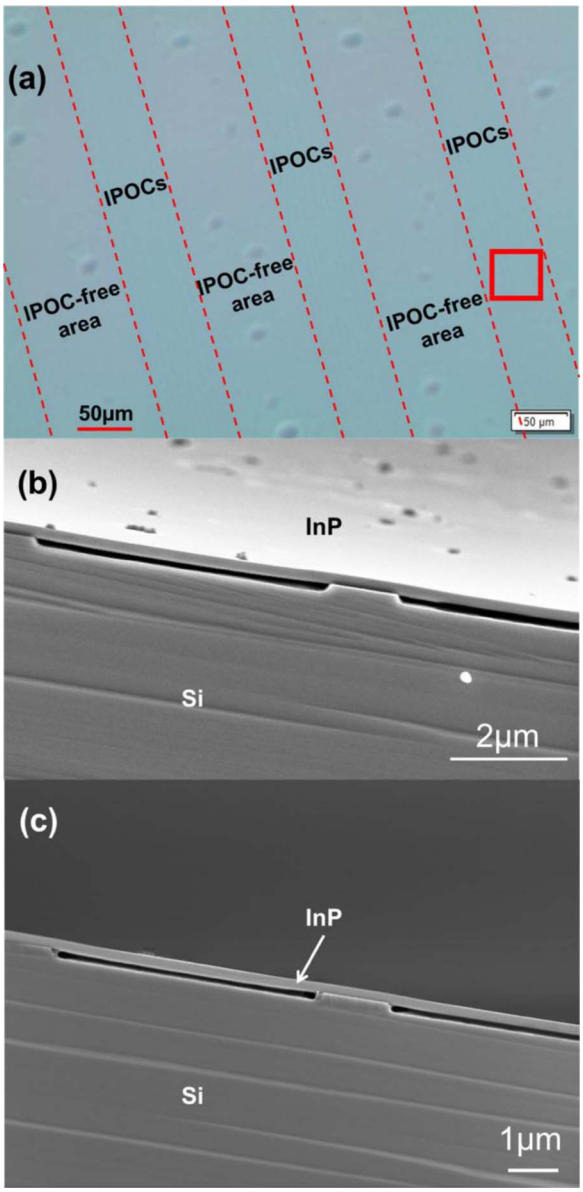

Figure 8. (a) Optical microscope image of the InP die bonded on Si patterned with 4 μm IPOC width and 2.5 μm spacing; The corresponding tilted planar and cross-sectional SEM images from the highlighted box area in (a) are shown in (b) and (c), respectively.

well aligned with that of the as-received wafer, indicating minimal InP residual strain shift throughout bonding and chemical etching processes. The broadening of bonded InP (004) peak is attributed to the inferior crystal quality of InP epi-grown film, post removal of the single crystalline InP substrate.

Outgassing efficiency study by InP/Al_2O_3/IPOC-patterned-Si direct bonding.— Although strong bond strength has been achieved for InP/Al_2O_3/Si homogeneous direct bonding, the bonding quality is still constrained by high density of interfacial voids, as shown in Figure 5b. The optical microscope image (10X) shows InP/Al_2O_3/plain-Si bonded structure post removal of the bulk InP. Interfacial void density is calculated as the ratio between void count in the image and the area of the image. The void density is approximately $\sim 3.6 \times 10^4$ cm^{-2}.

Figure 8a shows the optical microscope image of InP/Al_2O_3/IPOC-patterned-Si with IPOC width of 4 μm and spacing of 2.5 μm. Significant interfacial void distribution contrast can be identified between IPOC-patterned and IPOC-free regions. Most of the voids appear at

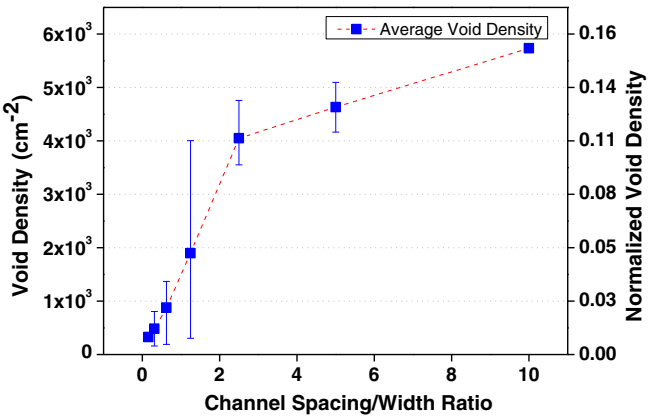

Figure 9. Void density as a function of IPOC *S/W* ratio. The right tick label indicates the normalized void density with respect to that of InP/Al_2O_3/plain-Si.

IPOC-free regions whereas the InP bonded on IPOC-patterned Si is nearly void-free. Therefore IPOCs are found useful to diffuse out the gas by-products generated during bonding process. The gas accumulation in IPOC-free regions is probably attributed to their larger distance toward the nearest IPOC than their maximum out-diffusion length, hence forming the interfacial voids.

An identical sample was cleaved perpendicular to the IPOC direction. Figures 8b and 8c show the corresponding 30°-tilted (the planar bonding interface is defined as 0°-tilted) and cross-sectional SEM images, respectively. From 8b, the bonded InP film surface is revealed to be smooth and uniform, without any rupture or delamination observed. The tiny particles and black spots on the surface are the contaminants introduced during dicing and the etch residue resulting from HCl: H_3PO_4: H_2O etching, respectively. Furthermore, the bonded InP film is observed (Figure 8c) to be solidly suspended above IPOCs, without any sagging and collapse. These two SEM images also verify the high interfacial bonding energy that could withstand the destructive cleaving process, although the bonded area has been shrunk significantly.

The interfacial void density was calculated from all IPOC-dimension-varied bonded samples. Only IPOC-patterned areas are included into calculation. To correlate with thermal stress study, averaged void densities were presented as a function of IPOC S/W ratio (Figure 9). Significant void density suppression up to two orders of magnitude is observed, compared to the sample without IPOCs (as in Figure 5b). It is also found that the void density decreases with decreasing IPOC *S/W* ratio. As the decreasing *S/W* ratio corresponds to shrinkage of IPOC spacing or widening of IPOC width, the average distance for a gas by-product molecule to reach IPOC tends to decrease. Therefore these interfacial bonding gas by-products and volatile hydrocarbon contaminants are more prone to be channeled out. As it has also been studied that interfacial hydrocarbons may serve as nucleation sites for interfacial voids,[28] the reduced hydrocarbon and gas by-products might jointly contribute to void density suppression. Furthermore, the reduced bonded area due to shrinkage of *S/W* ratio might also lead to suppressed void density since the amount of surface hydroxyl group for gas by-products generation is reduced.

Combining the thermal stress analysis and outgassing efficiency study, an optimal IPOC *S/W* ratio of 2.5 is proposed to compromise between thermally-induced stress degradation and outgassing efficiency improvement. At this *S/W* ratio, ~90% of void density suppression is achieved with only ~10% thermal stress increment. Recently, Srinivasan et al.[29] reported competitive reliability performance of III-V distributed feedback lasers fabricated on hybrid-integrated III-V/Si platform, which is formed by 60 nm-SiO_2-intermediated InP-on-SOI bonding.[9] By extrapolating InP/60 nm-SiO_2/Si thermal stress from Figure 2 and comparing it with the ~10%-increased thermal stress of InP/Al_2O_3/Si (at *S/W* = 2.5) in Figure 4, it could be found that

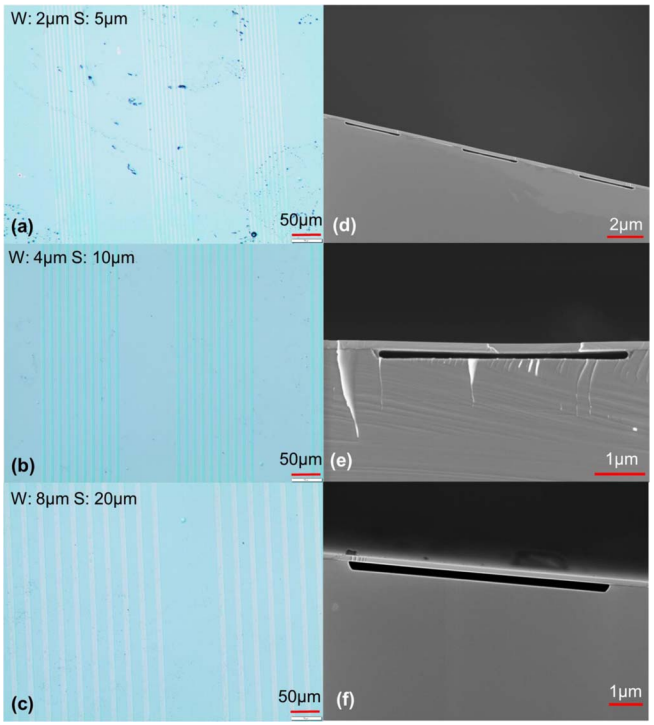

Figure 10. Optical microscope images of InP/Al_2O_3/Si bonded samples with *S/W* ratio of 2.5: (a) IPOC width of 2 μm and spacing of 5 μm; (b) IPOC width of 4 μm and spacing of 10 μm; (c) IPOC width of 8 μm and spacing of 20 μm. (d), (e) and (f) show the corresponding cross-sectional SEM images of the samples in (a), (b) and (c), respectively.

the ~10% thermal stress increment of InP/Al_2O_3/Si (~2.7 MPa) is still ~33% lower than that of InP/60 nm-SiO_2/Si (~4 MPa). Therefore, it could be inferred that, ~10% thermal stress increment might not be detrimental for the reliability of similar devices fabricated on InP/Al_2O_3/Si platforms. The study gives us some benchmark to propose 2.5 as the optimal *S/W* ratio. However, experimental verification for ultimate device thermal stress and reliability performance has to be proposed for future work.

Figures 10a, 10b and 10c show optical microscope pictures of InP/Al_2O_3/Si bonded sample with optimal *S/W* ratio of 2.5 in our experiments. All the images are nearly void-free, with few voids found only in IPOC-free areas. The black spots in (a) are the etching residuals on the sample surface and could be eliminated by chemical etching optimization. Figures 10d, 10e and 10f indicate the corresponding SEM cross-sectional images of the transferred InP films from the samples in (a), (b) and (c), respectively. The transferred films in all images are flat and uniformly suspended above the channels. All the results support good quality of InP/Al_2O_3/Si bonding with 2.5 IPOC *S/W* ratio.

An additional merit for applying IPOCs at InP/Al_2O_3/Si bonding interface is to take advantage of the spacing part of IPOC as some innate Si rib waveguide structure with air cladding. By properly adjusting the waveguide design parameters[30] to align with that of IPOCs, both low-loss optical transmission and coupling could be expected to maximize the optical efficiency and meanwhile reduce the process cost.

Conclusions

In this work, thermally-induced stress characteristics and outgassing efficiency of in-plane outgassing channels (IPOCs) have been studied simultaneously for InP/Al_2O_3/Si die-to-wafer bonding. It is found from the simulations that, compared to SiO_2, Al_2O_3-intermediated InP-on-Si bonding owns the advantage of mitigating the thermal stress on bonded InP. The thermal stress is shown to be even

lower than that of InP/Si direct bonding. It is also found that designing IPOC *S*/*W* ratio above 1 maintains the thermal stress relief superiority of InP/Al_2O_3/Si over InP/SiO_2/Si bonding. In experimental investigations, successful InP/Al_2O_3/plain-Si bonding is demonstrated. A reasonably strong bonding shear strength (2.57 MPa) is revealed. XRD and cross-sectional SEM analysis verifies stress-free and seamless InP film transfer onto Si. IPOC outgassing efficiency is then studied by fabricating dimension-varied IPOCs on Si followed by InP/Al_2O_3/Si bonding. The interfacial void density is observed to decrease with decreasing *S*/*W* ratio, where up to two orders of magnitude suppression is achieved. Bonding quality is not degraded with uniform and flat film suspension observed above IPOCs. An optimal IPOC *S*/*W* ratio of 2.5 is therefore proposed to compromise between the thermally-induced degradation and outgassing efficiency improvement. This work paves the way for future high quality hybrid-integrated optoelectronic device fabrication for silicon photonics integrated circuit applications.

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