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Methods for Resolving the Challenges of Degradation Diagnosis for SiC Power MOSFET

YANG HUI-CHEN

School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University in partial fulfilment of the requirement for the degree of Doctor of Philosophy

2019
Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

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Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

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Authorship Attribution Statement

This thesis contains material from 4 papers published in the following peer-reviewed journals and conference proceedings in which I was the first author.


The contributions of the co-authors are as follows:
- Dr. Simanajorang provided the initial project direction and supervised the project.
- I designed and implemented the monitoring unit, as well as carried out the measurements.
- I prepared the manuscript drafts. The drafts were revised by A/Prof See. All authors contributed to the final version of the manuscript.


The contributions of the co-authors are as follows:
- A/Prof See initiated the idea of this study, provided critical feedback and revised the manuscript drafts.
- Dr. Li provided technical support during experiments.
- I prepared the manuscript drafts. Both Dr. Simanajorang and Dr. Li helped review the manuscript.
- The development of the on-state circuit model of power MOSFET, experimental design, sample preparation, measurements and data analyses were conducted by me.

The contributions of the co-authors are as follows:

- Dr. Simanjorang provided helpful advice on shaping the manuscript.
- I prepared the manuscript drafts. A/Prof See helped revising the manuscript.
- I conceived the idea, designed and carried out the experiments.

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ABSTRACT

Methods for Resolving the Challenges of Degradation Diagnosis
for SiC Power MOSFET

by

Hui-Chen Yang

Modern society is in quest of more electric power in various sectors. The rising power demand has driven the development trend of power electronic converters toward higher power density. Power electronic converters, however, are subject to continuous electrical and thermal strains that threaten their reliability. Any unexpected failure can incur unnecessary economic loss or even worse, safety hazards. Semiconductor power devices are the backbones in a power electronic converter, and yet, they are recognized as one of the most failure-prone components. Therefore, early detection of a power device’s incipient abnormality due to either aging, electrical stress or defect is crucial.

Degradation diagnosis is a process of identifying an evolving damage before it develops into destructive failure. A variety of degradation diagnosis techniques have been proposed in earlier works. Among them, the time-domain on-state characteristics and thermal path integrity are the most frequently chosen properties as indications of device wear-out. As the measurable electrical variations associated with degradation are typically subtle, the measurements are susceptible to system’s noise and loading conditions. Besides, as power applications are pursuing higher switching frequency to gain power density, the measurement system is demanding for higher bandwidth, which
could reach its data rate bottleneck. For reliable and accurate prediction of developing faults, these challenges must be addressed.

In this thesis, silicon carbide (SiC) MOSFET is chosen as the device for degradation diagnosis study, as it has shown great promise for high power density converter (HPDC) design owing to the excellent material property for high-frequency and high-temperature operation. The practical reliability issues responsible for power device degradation and challenges in degradation diagnosis are investigated. Special solutions are proposed to counter these challenges. Firstly, a voltage monitoring circuit with built-in isolation is proposed and experimentally verified up to 100 kHz. The embedded isolation eliminates EMI influence on the measured data, allows direct processing of the measured voltage information, and relaxes the data rate bottleneck of the data transmission interface of a measurement system. Secondly, a non-intrusive measurement method that measures the on-state impedance of a power device in frequency domain for offline degradation diagnosis is proposed. The method overcomes the shortcomings of the conventional time-domain methods, which are easily affected by system’s noise and may have difficulties on detecting subtle electrical changes associated with reliability issues. Finally, a temperature sensor-less method is proposed to estimate power MOSFET’s junction temperature. It has experimentally demonstrated that by means of device saturation current ($I_{d,sat}$) measurement, junction temperature can be estimated either by $I_{d,sat}$, $\sqrt{I_{d,sat}}$, or the extracted threshold voltage.
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Chapter 1

INTRODUCTION AND MOTIVATION

1.1 A More Electric Society and Key Technology Trends

With the continuous demands for portable consumer electronics, information and communication technology (ICT) infrastructures and the increasing usage of renewable energy sources, the use of more electric power has become a megatrend in modern society. It is estimated that the world net electricity generation will increase 45% between 2015 and 2040 [1]. Not only industrial and commercial sectors are electric power hungry, the transportation sector is demanding more electric power as well. The concerns of fast depleting fuel resources and global warming have catalysed the development of more electric transportation. The idea is to reduce fuel consumption by introducing electric energy into propulsion. In addition, by replacing the conventional mechanically driven subsystems with electrical loads, better system integration and reliability performance can be achieved. More electric aircraft (MEA) [2] and hybrid electric vehicle (HEV) [3] are two representative examples.

The intensifying needs for electric power urges energy-efficient solutions to support a sea of applications, ranging from milliwatts portable equipment, tens and hundreds of watts power supplies for home and office appliances, kilowatts data centres, kilowatts to megawatts motor drives, to thousands of megawatts ac utility power systems. Power electronic converters are the key technology for the efficient use of electric energy. High efficiency and low loss are the basic requirements for a power converter to ensure the good utilization of energy sources. The development of power electronic converters
have shown a trend toward higher power density, as shown in Figure 1.1 [4]–[13]. This trend is driven by the limited deployment space, rising power demand and the advancement of semiconductor technology. A high power density design means less conduction loss per unit area, higher integration freedom, and therefore, lowers the installation cost. The compact size and lightweight requirements drive the power conversion design toward higher switching frequency.

Figure 1.1. Power density trend of various applications. (Figure information is compiled based on [4]–[13].)

Semiconductor power devices are the key enablers for keeping up with the development trend. Today, the market of semiconductor power devices is dominated by silicon technology. It has been steadily improved towards smaller feature size, higher cell density and, thanks to the launch of new device structures [14]–[15], a better trade-off between on-state resistance and breakdown voltage. However, silicon-based devices will reach their limitations due to the fundamental material properties. Besides, although smaller chip volume enables higher switching speed, it comes with the penalty of larger
heat dissipation per unit area, which means a better thermal management is needed. Compared to silicon (Si), wide-bandgap (WBG) materials offer higher breakdown voltage and faster switching capability. With the same breakdown voltage, WBG materials can achieve smaller resistance per unit area. Owing to the higher melting points compared to Si, WBG materials are suitable for high temperature operation. Silicon carbide (SiC) and gallium nitride (GaN) are by far the most promising WBG materials that have been under extensive research. Figure 1.2 compares the key material properties between Si, SiC and GaN [16]–[17]. Although GaN theoretically provides better high frequency performance than SiC, the lower thermal conductivity suggests less efficient heat dissipation and hence, lower power density. Besides, the cost is high to fabricate good quality GaN bulk substrate for high-voltage GaN vertical devices. As such, SiC devices have the full potential to become the key player of next-generation high power density converters. And yet, without a reliable design, none of the benefits matter.

Figure 1.2. Material properties of Si, SiC and GaN. (Figure information is compiled based on [16]–[17].)
1.2 Reliability Issues of Semiconductor Power Devices

As the backbones in a power electronic converter, semiconductor power devices are suffering from continuous electrical and environmental stresses during operation. Studies have shown that power devices are one of the most vulnerable components in a power converter, and they are at the top rank in a 2011 industrial-based survey, as shown in Figure 1.3 [18].

![Figure 1.3. Fragile components in power converters.](image)

The survey also pointed out that electrical overload, system transients and environmental stresses constitute most of the failure causes; while component design and manufacturing have relatively minor contributions to the failure of power converters. Modern power converters are typically well protected from overstress damage through over-voltage, over-current and over-temperature sensing and protection circuits. Damages induced by power and thermal cycles are gradual. It can lead to drastic failure once the damage accumulation reaches the critical level, resulting in unexpected system downtime and unnecessary economic loss. Even worse, it can lead to fatal consequences for those systems that cannot afford unexpected failures, such as aerospace applications. This kind of long-term wear-out can be prevented by tracking the changes of measurable deterioration indicators, and then scheduling necessary maintenance in the most cost-
effective way. This requires the knowledge of the correlation between reliability issues and measurable deterioration indicators.

Deterioration of a power device can either happen in the package structure or in the die itself.

1. Package-related deterioration

A robust power device package is expected to provide high thermal conductivity, low parasitics, necessary insulation, and good power cycling capability for standing a long lifetime. Figure 1.4 (a) illustrates package-related deterioration with the cross-sectional views of generic discrete-type and module-type packages, which are designed for low and high-power applications, respectively. Due to the wide variation of the coefficients of thermal expansion (CTEs) of the layered structure, as shown in Figure 1.4 (b) [19]–[21], a power device package is prone to repetitive temperature swings and Joule heating. Over time, repetitive thermal stresses create voids and cracks, which usually start to form from edges, in solder layers. The growing delamination between layers reduce the attached area, which impedes the heat flow and degrades the thermal conduction performance. The thermal conduction performance of a package can be characterized by thermal impedance, which describes the amount of power dissipated per one-degree Celsius change between two locations.

Another commonly seen failure appears at bond wires. General observations including bond wire lift-off and heel cracking. Bond wire resistance is typically assumed to be negligible compared to the overall on-state resistance, where the resistance change due to damage is hardly noticeable. However, it might be observable through the measurement of on-state resistance if the die self-heating introduces detectable change at a particular operating condition.
Die-related deterioration

Figure 1.5 illustrates the die-related deterioration with a planar SiC DMOSFET structure. There are two major issues that degrade the device performance. The first is charge effects, including charge trapping within gate oxide and SiC–oxide interface, as well as mobile ion contamination; the second is body diode degradation.

Charge trapping occurs when charge carriers gain sufficient kinetic energy from electrical and thermal energies. The trapped charges alter the interfacial charge
amounts, resulting in threshold voltage change. A positive shift in threshold voltage leads to an increase in on-state resistance; while a negative shift in threshold voltage gives rise to off-state leakage current and the risk of false turn-on. Both introduce excess power losses that jeopardize the life span of a device.

The gate-bias-induced threshold voltage shift in SiC MOSFETs has been received particular attention as it suffers more severe variations compared to Si-based devices. It has been observed that a positive gate bias results in positive threshold voltage shift, and vice versa. The shift amount is higher at high temperature condition and can vary widely between different manufacturers. Studies have shown that the phenomenon is insignificant at switching condition, as the effects of on-state and off-state biases are countering each other [22]–[23].

Mobile ions usually come from the environmental radiation and manufacturing process. Due to their high mobility, a high quantity of mobile ions might develop into conducting channels that give rise to leakage current. Also, the mobile ionic charges can alter the threshold voltage. Since the contamination sources are external, other than ensuring a clean fabrication process, it can be prevented by applying a protection

Figure 1.5. Die-related deterioration of a SiC MOSFET.
layer on top of the die surface. Aerospace applications may require special cares as they are exposed to heavier radiation than field applications.

For applications utilizing body diode as free-wheeling diode, the forward conduction stress can induce stacking faults in SiC crystal structure that yield an increase in forward bias voltage and, consequently, higher loss [24]. This reliability issue can be prevented by bypassing the body diode with an anti-parallel Schottky diode.

Owing to the continuing advancement of semiconductor technology in device structure, oxide quality, and high temperature tolerance, package design has become the major bottleneck that restrict the achievable performance and reliability of a power device. Therefore, package-related deterioration is more commonly observed in real applications. In the future, the development of new package design with better matched CTEs is the key for realizing high power density and long lifetime.

1.3 Challenges of Deterioration Diagnosis

Although there has been attempted to embed subcircuits in a power module for package wear-out detection [25], the approach requires modification of the assembly and the direct copper bonding (DCB) layout, which increase the complexity and cost of a power module. It is more favourable to diagnose deterioration with measurable electrical signals. On-state resistance and thermal impedance are the most frequently chosen parameters for deterioration diagnosis, as they provide the most direct evidence for device wear-out. However, several challenges remain in actual implementation:

1. **Data rate bottleneck of a measurement system**

As power applications are pursuing higher switching frequency, the measurement system is demanding for higher data rate to ensure the data is captured
successfully at on-state periods during fast switching operation. The data transmission interface can reach its data rate bottleneck.

2. *Measurement are susceptible to loading conditions and system’s noise*

Identifying the subtle changes associated with deterioration remains a challenging task as they are hidden in relatively large signals during switching operation. A small amount of measurement error can lead to considerable bias in the chosen aging indicator. For more advanced high-power devices with only a few milliohm on-state resistance, high-resolution data acquisition system is required, which implies a more stringent data rate bottleneck.

3. *Accurate and timely junction temperature estimation*

Junction temperature is the key information for thermal impedance computation. The major challenge lies in how to accurately estimate the junction temperature at a particular operating point under fast-changing operating condition. There has been intensive research on junction temperature estimation using measurable temperature-sensitive electrical parameters. However, a widely accepted solution suitable for practical applications has not yet been found.

4. *Cost*

Cost is often the major concern in terms of practicality. Since it is hard to judge a true degradation from a single electrical parameter, a number of sensing circuits are expected in a deterioration diagnosis system. How to achieve a significantly lower cost of a diagnosis system compared to the power converter cost is one of the future concerns.

**1.4 Thesis Organization**

This thesis investigates the causes behind power device wear-out, and the challenges in diagnosing gradual faults before drastic failure. Unique solutions are proposed to
counter these challenges. SiC power MOSFET is adopted as the device-under-test (DUT) throughout this research for its promising potential in the future high power density converter design. Chapter 2 provides a comprehensive review on current solutions and techniques for deterioration diagnosis, including on-state resistance monitoring, aging-related switching characteristics monitoring and thermal impedance measurement. To address the data rate bottleneck of a deterioration monitoring system, an isolated voltage monitor is proposed in Chapter 3. The functionality of the proposed circuit is analysed and experimentally validated on an in-service H-bridge inverter to demonstrate its on-line monitoring capability. Chapter 4 proposes a nonintrusive, inductively coupled approach for offline deterioration diagnosis that measures the on-state impedance of a DUT in frequency domain. The proposed method aims to overcome the shortcomings of the conventional time-domain-based methods, as they are easily affected by loading conditions and system’s noise. In Chapter 5, a junction temperature estimation method is proposed to solve the drawbacks of existing methods, such as slow response time and measurement difficulties. Finally, Chapter 6 concludes the thesis with the main contributions listed, and discusses future works that are worth exploring.
Chapter 2

LITERATURE REVIEW OF DIAGNOSIS OF POWER DEVICES DEGRADATIONS

Degradation diagnosis is a process of identifying an evolving damage before it develops into destructive and irreversible failure. It involves the measurement of pre-defined electrical degradation indicators under a specific operating condition and the analyses of their deviations from the norm. The measurement of degradation indicators can be carried out either under online or offline conditions. An online measurement takes data continuously from an in-service system with embedded sensing circuits [26]; while an offline measurement retrieves data periodically with a specific test sequence [27] from a system temporarily halt operation.

Online diagnosis needs to deal with varying operating and thermal conditions, which are determined by actual load profiles. This complicates the analyses of degradation indicators as most of them have temperature dependency. A true degradation can be masked by thermal effects and failed to detect in time. To simplify the problem, some laboratory studies performed online deterioration diagnosis under controlled repetitive operating condition so as to create a periodically varying thermal condition [28]–[29]. Since a degraded device introduces more power loss, degradation can be identified by monitoring the increment of the on-state electrical parameters at a particular operating current. In short, diagnosis involving actual mission profile is not possible without the device’s junction temperature information. Mission-profile-based online diagnosis remains a great challenge. Studies have linked mission-profile with life consumption
through thermomechanical or electrothermal models [30]–[31]. Thermomechanical models are physical-based models developed for estimating the package lifetime subject to bond wire liftoff and solder fatigue [32]. They require detailed and specific information such as material properties and physical dimensions, which are typically lacking for designers. Electrothermal models are the basis for thermal impedance calculation. They can be constructed analytically by finite element method (FEM), or experimentally through temperature and power loss measurement [33]. Measurement-based electrothermal model is more popular as the analytical-based model cannot reflect the influence of degradation. Accurate measurement of junction temperature is considered to be the most critical challenge for online diagnosis, which necessitate the need for timely and precise junction temperature estimation methods.

Offline diagnosis aims to simplify the measurement efforts required for online manner by applying specially designed test routine on an idle or halted system [34]. As the operating and thermal conditions are well-controlled, deterioration can be detected through a single indicator.

In this chapter, existing degradation diagnosis techniques for power device are reviewed. Since die-related deterioration is relatively rare compared to package-related deterioration under high-temperature power cycling, the main focus will be on techniques developed for the latter. Three kinds of techniques will be reviewed in this chapter. The first one is the classic method that monitors the static characteristics at on-state; the second one utilizes switching behaviours that are correlated with degradation, and finally the third one evaluates the thermal path integrity with electrothermal model.

### 2.1 Static Characteristics Method

Static characteristics involve parameters that reflect the resistance deviation of the turn-on path of a power device, i.e. on-state voltage and on-state resistance. The former
is typically adopted for insulated gate bipolar transistor (IGBT); while the latter is chosen for power MOSFET due to its resistive on-state behaviour. Since the individual resistance variation caused by solder degradation, delamination, metallization and bond wire damage are generally subtle, the change in on-state resistance can only be detected under high current operation, or when the overall effect is noticeable [35]–[36]. It implies that a single cause of deterioration is hardly measured.

A resistive loss model has been proposed in [37] for indirect on-state resistance monitoring via readily available signals. However, it is not a universal solution as the model is specifically designed for forward converter. The most popular implementation relies on specifically designed circuits for direct measurement, where precise on-state voltage and device current measurement techniques must be developed.

### I. On-state Voltage Measurement Techniques

There lie several challenges for the development of on-state voltage measurement technique, including:

(a) It should not affect a power conversion system under its usual operating condition;
(b) Accuracy demand for detecting weak signal change from a large signal;
(c) Capable of capture data from a fast-switching operation when implemented online;
(d) It should not occupy significant area to the power conversion system; and
(e) The voltage monitoring design should be robust.
Reed relay

Reed relay is the simplest measurement technique, as shown in Figure 2.1 (a). The relay simply enabled whenever the measurement is performed [38]. The major drawback of reed relay is the slow response time, which is typically much longer than the switching period and therefore, prevents it from real-time online implementation.

Limiting-diode-based

As shown in Figure 2.1 (b), Zener diode is the main component of this technique to protect the output $V_{sense}$ from high off-state voltage [39].

Resistor $R$ is used to limit the current flowing through both diodes to protect them from burn-out. It also limits the power loss when a high voltage, typically hundreds of volts, appears during the power MOSFET turn-off. The regular diode added in series with Zener diode is to reduce the total capacitance looking into the output node to improve the $RC$ time delay. The diode voltage ($V_Z + V_D$) should be designed to be higher than the on-stage voltage range desired to be detected. The sensed output is given by

$$V_{sense} = \begin{cases}  
V_{DS} - I_R R, & \text{power device } ON \\
V_Z + V_D, & \text{power device } OFF 
\end{cases}$$

(2.1)
where $I_R$ is the reverse leakage current of the Zener diode. The current $I_R$ should be limited within $P_Z/V_Z$ by the resistor $R$, where $P_Z$ is the maximum power rating of the Zener diode. The presence of $R$ introduces an $IR$-drop error in this circuit. To gain higher accuracy, one has to trade with smaller power loss. The sensed output error is given as follows

$$|\Delta V_{VM}| = I_R R \quad (2.2)$$

**Blocking-diode-based**

![Blocking-diode-based on-state voltage measurement technique.](image)

**Figure 2.2.** Blocking-diode-based on-state voltage measurement technique.

This technique utilizes a high-voltage diode to block the high-voltage from the circuit to be measured when the power MOSFET is turn-off. The on-state voltage is passed to the measurement circuit together with a diode offset during the on-state period. Hence, the diode offset has to be removed through circuit techniques for accurate measurement. Figure 2.2 shows an implementation of blocking-diode-based technique with diode offset cancellation [40]. The two high-voltage diodes $D1$ and $D2$ are biased with the same current as the input current of the op-amp is negligible. The output error of this topology consists of the diode offset introduced by process and temperature variations, op-amp input offset ($V_{os}$) and the error due to resistor mismatch. With negligible input
current of the op-amp, when the power MOSFET turns on, the current $I$ through $R1$ and $R2$ is $(V_{D2} - V_{os})/R1$. Since $V_{sense} = V_{DS} + V_{D1} + V_{D2} - I(R1 + R2)$, the sensed output voltage is summarized as follows:

$$V_{sense} = \begin{cases} V_{DS} + V_{D1} + V_{os} - \frac{R2}{R1}(V_{D2} - V_{os}), & \text{power device ON} \\ V_{DD} + V_{D4} - \left(1 + \frac{R2}{R1}\right)(V_{D2} - V_{os}), & \text{power device OFF} \end{cases} \quad (2.3)$$

By observing (2.3), at the condition of power device is ON, if $V_{os} << V_{D1}$ and $V_{D2}$, by designing $R1 = R2$, we can have $V_{sense} \approx V_{DS}$ if the high-voltage diodes are well-matched. To account for the resistance variations, taking $R1 = (1 \pm p\%)R$ and $R2 = (1 \pm q\%)R$, the resultant output error will be

$$|\Delta V_{VM}| = V_{D1} + V_{os} - \frac{(1 \pm q\%)}{(1 \pm p\%)}(V_{D2} - V_{os}) \quad (2.4)$$

Gating-transistor-based

Instead of diode, gating-transistor-based technique utilizes a transistor to avoid high voltage affecting the measurement circuit, as shown in Figure 2.3 [29]. Compared to the current-limiting resistor used in the limiting-diode-based technique, the resistance of $R1$ in this topology can be much smaller, as it does not require to handle high current flow.

Figure 2.3. Gating-transistor-based on-state voltage measurement technique.
The transistor \( M_{sw} \) is biased with a constant voltage source \( V_{G,sw} \). The non-toggling operation eliminates charge injection interference. The sensed output is quasi-isolated from the switching device by an op-amp and a common-gate amplifier (\( MN \)).

The error of this topology is contributed by the on-state resistance of \( M_{sw} (R_{sw}) \), op-amp input offset (\( V_{os} \)) and mismatched resistors. When the power MOSFET turns on, \( V_{R2} \) is determined by the voltage divider formed by \( RI \) and \( R_{sw} \). When the power MOSFET turns off, \( V_{R2} \) is clamped at \((V_{G,sw} - V_{th,sw} + V_{os})\), where \( V_{th,sw} \) is the threshold voltage of \( M_{sw} \). The sensed output voltage is summarized as follows:

\[
V_{sense} = \begin{cases} 
\frac{R3}{R2} \left( \frac{R1}{R1 + R_{sw}} V_{DS} + V_{os} \right), & \text{power device ON} \\
\frac{R3}{R2} (V_{G,sw} - V_{th,sw} + V_{os}), & \text{power device OFF}
\end{cases}
\] (2.5)

The ratio of \( R2 \) and \( R3 \) can be adjusted to provide the necessary sensed output range. By choosing \( RI \) to be relatively larger than \( R_{sw} \) and \( R2 = R3 \), \( V_{sense} \approx V_{DS} \) is obtained. To account for the variations of resistors, taking \( R2 = (1 \pm q\%)aR \) and \( R3 = (1 \pm r\%)bR \), the resultant output error will be

\[
|\Delta V_{VM}| = (k - 1)V_{DS} + kV_{os}
\] (2.6)

where \( k = \frac{(1\pm r\%)b}{(1\pm q\%)a} \).

The isolation function in this topology is limited due to the lack of physical isolation barrier. The major disadvantage of this technique is the need for an extra active device with the same breakdown capacity as the power MOSFET to be measured.
II. Device Current Measurement Techniques

Shunt Resistor

This is a method with simplicity and high-bandwidth. The device current is obtained by measuring the voltage drop across the current sense resistor in series with the power MOSFET, as shown in Figure 2.4 (a). Due to the linear Ohmic behaviour, the voltage drop can exceed the operating range of the following measurement circuits when large device currents are measured. The current sense resistor requires low temperature coefficient of resistance (TCR) for accurate sensing. To minimize the interference to the switching circuit, as well as to have less power dissipation, the shunt resistance has to be as small as possible.

Multi-finger Device

As shown in Figure 2.4 (b), the multi-finger device structure duplicates the device current with the designed ratio. Therefore, the fractional current can be measured without interfering the switching circuit. It can also ease the operating range design of the following measurement circuits. To have a precise current duplication, the power MOSFET fingers must have identical structure within the same package. This requires extra manufacturing cost.

Stray Inductance

In this technique, the stray inductance at the power source terminal is serving as an inherent current sensor, as shown in Figure 2.4 (c) [41], where \( S \) is the main source terminal (power source) and \( S' \) is an additional source connection (Kelvin source connection) that used as the reference potential for the gate driver. \( L_S \) and \( L_{S'} \) are the parasitic inductances of the power source and the Kelvin source connection, respectively.
By assuming the gate current to be negligible compared to the device current \( I_d \), the voltage between the two source connections (\( V_{ss'} \)) is given by

\[
V_{ss'} \approx -L_s \frac{dI_d}{dt}
\]  

(2.7)

Through signal integration, the device current can be recovered as follows

\[
I_d \approx \frac{RC}{L_s} V_{id}
\]  

(2.8)

This method is prone to noise as the stray inductances are generally small. Besides, bond wire damage can change the stray inductances, further affecting the measurement accuracy.

**Non-intrusive Current Sensors**

Current sensors are the most favourable methods owing to their non-intrusive nature, such as current transformer, Hall-effect sensor and Rogowski coil. Among them, Rogowski coil has the advantage of high bandwidth and linearity, for it has no magnetic core to saturate. Figure 2.4 (d) illustrates the operating principle of Rogowski coil, which is similar to the stray inductance technique. A voltage proportional to the rate of device current change is induced across the air-cored coil, as given by equation (2.9), where \( M \) stands for the mutual inductance between the source conductor and the Rogowski coil. The current is then recovered through signal integration as derived in equation (2.10).

\[
V_{coil} = M \frac{dI_d}{dt}
\]  

(2.9)

\[
I_d = \frac{RC}{M} V_{id}
\]  

(2.10)
2.2 Switching Characteristics Method

Bond wire damage is one of the most concerned reliability issues, as bond wires are suffering from large temperature fluctuations with small contact areas. The resulting change in on-state resistance and junction temperature may not be easily detected. In [43], the overall resistance and inductance of the power devices with partial bond wire liftoff have been compared with a fault-free device. It shows that the parasitic inductance becomes larger as the number of lifted bond wires increases; while the resistance is hardly change. To counter the difficulty, some researches have turned to switching characteristics method.

Figure 2.4. Overview of device current measurement techniques. (a) Shunt resistor. (b) Multi-finger device. (c) Stray inductance [41]. (d) Rogowski coil [42].
Device Voltage during Turn-on/Turn-off Process

Bond wire damage can alter the gate turn-on waveform [43]. This is due to the change of the input capacitance of a power device. As illustrated in Figure 2.5, where a planar power MOSFET with interelectrode capacitors and parasitic inductors shown, the input capacitance is defined by totalling the gate-to-source ($C_{GS}$) and gate-to-drain capacitances ($C_{GD}$).

$$C_{iss} = C_{GS} + C_{GD} \quad (2.11)$$

where $C_{GS}$ is constituted by the parallel capacitors $C_{oxm}$, $C_{oxn}$ and $C_{oxp}$, which are defined by the overlap area between poly-Si gate and source metallization, $n^+$ region and p-base, respectively; $C_{GD}$ is comprised of the series connection of the gate-oxide capacitance $C_{ox}$ and the capacitance of depletion area $C_{dep}$. Hence, equation (2.11) can be rewritten into

$$C_{iss} = (C_{oxm} + C_{oxn} + C_{oxp}) + \left( \frac{C_{ox}C_{dep}}{C_{ox} + C_{dep}} \right) \quad (2.12)$$

Figure 2.5. Interelectrode capacitors and parasitic inductors of a power MOSFET.
For a power module with multiple paralleled dies, the bond wire liftoff can lead to complete disconnection of a die, resulting in the reduction of active areas of $C_{oxm}$, $C_{oxn}$ and $C_{oxp}$; also, the depletion area is no longer existed. The input capacitance is reduced and, consequently, the gate will have a faster turn-on compared to the fault-free condition. The observation, however, is based upon the assumption that all the bond wires of one die is completely disconnected, which is very rare.

Bond wire damage can alter the turn-off overshoot of drain-to-source (or collector-to-emitter) voltage as well due to the variation of parasitic inductance. A more severe damage to the bond wire results in higher parasitic inductance, as a result, larger overshoot can be observed [43]. As the rate of change of drain-to-source (or collector-to-emitter) voltage, $dV_{DS}/dt$ (or $dV_{CE}/dt$), is current and temperature dependent [44], degradation has to be justified under the same device current and junction temperature conditions.

**Turn-off Time**

A package’s thermal path deterioration results in temperature rise of a power device. As $dV_{DS}/dt$ (or $dV_{CE}/dt$) is temperature dependent, turn-off time can serve as an indirect package deterioration indicator [45].

**Gate Current**

As aforementioned, the complete die disconnection leads to input capacitance reduction. This not only influences the gate turn-on voltage waveform, but also affects the gate current. A deteriorated device is expected to have a lower peak gate current compared to a fresh device, as smaller input capacitance is being charged. It has been demonstrated in [46] that the variation of gate current is detectable only when all the
bond wires of one of the paralleled chips in a power module were lift-off. The gate current of the partial bond wire lift-off condition showed no visible difference compared to the fault-free condition.

Switching characteristics method is appealing for the capability of detecting deterioration when a device is in operation. The main drawback is that the switching waveforms can be strongly influenced by additional inductance of external routing conductors, making it difficult to judge whether there is a true defect in a power device. Besides, the sensitivity of some parameters to degradation can be small. For examples, the change in turn-off time have shown less than 0.1 microsecond in [45], and the peak gate current change during turn-off is less than 200 mA in [46]. These indicate the need for high-precision analog-to-digital converters where cost concern emerges.

2.3 Thermal Impedance Measurement Method

Thermal Impedance defines the thermal dissipation performance of a package. It can reflect the deterioration of heat flow path. Most studies attribute the rise of thermal impedance to the degradation of die attach layer [47]–[49], as it has large contact area to the heat source and suffers the worst thermomechanical stress in the package structure. It has been identified in [49] that the size of solder voids has a greater impact on the thermal dissipation performance than the total area of voids, as larger voids create more concentrated hot spot and result in poor heat transfer.

Theoretical thermal impedance is determined by the dimension and the thermal characteristics of individual layers. As shown in Figure 2.6 (a), a single layer can be modeled with a thermal resistor $R_{th}$ (the resistance of heat flow) and a thermal capacitor $C_{th}$ (the heat capacity of a material), as defined by
where $d$ is the thickness of the layer; $A$ is the effective cross-sectional area perpendicular to the heat flow; $\lambda$, $\rho$ and $C_T$ are the thermal conductivity, density and specific heat of the material, respectively [50]. The thermal impedance model of a package can be obtained by stacking all layers together, as the ladder-network shown in Figure 2.6 (b).

Although the ladder-network allows access to the temperature information of individual layers, the lack of package parameters, however, restricts the practical usage. In practical applications, the thermal impedance is often modeled in a simplified mathematical form, as given by [51]

$$Z_{th} = \sum_{i=1}^{n} R_{th,i} \left( 1 - e^{-t R_{th,i} C_{th,i}} \right)$$  

Figure 2.7 shows the corresponding pi-model, where the model parameters can be extracted from the transient thermal impedance curve that typically provided in device datasheet. Alternatively, $Z_{th}$ can be treated as a black box and obtained experimentally by the following definition.
where $T_j$ is the junction temperature, $T_{ref}$ is the temperature of the reference plane and $P_{loss}$ is the power dissipated by the die.

\[ Z_{th}(t) = \frac{T_j(t) - T_{ref}(t)}{P_{loss}(t)} \]  

(2.15)

**Figure 2.7.** Mathematically simplified thermal model: pi-model, also known as Foster-model.

It is known difficult to measure the switching power loss of a power device accurately [52]. Offline thermal impedance measurement avoids the difficulty by operating a power device at on-state under controlled case temperature, i.e. $T_{ref}$ in equation (2.15) is fixed. Typical test sequence is a train of repetitive pulses, where each pulse consists of a heating phase and a short junction temperature estimation phase. Figure 2.8 shows the measurement concept. The power device is heating up to a certain temperature during the heating phase either by applying a constant power [48] or constant current [53]. The heating process is then interrupted by applying a relatively much smaller power/current for junction temperature estimation. The thermal impedance can be calculated every cycle from equation (2.15). A closed-loop control is required for constant power method to maintain the desired power level. Since the conduction loss of a power device increases with rising temperature, instantons power loss calculation is necessary for constant current method.
Some studies have proposed indirect methods to evade power loss measurement, junction temperature estimation, or both. A method for monitoring the health condition of IGBT based on junction temperature variation is proposed in [54]. In [55], solder layer degradation is diagnosed by case-above-ambient temperature rise at a pre-defined electrical operating point. In most cases, however, electrical operating point is changing faster than the thermal transient of a heat sink, meaning that thermal impedance calculation is necessary where power loss measurement is inevitable. In [56], solder fatigue is identified through case temperature measurement only. This is based on the assumption that the damage in solder layer modifies the heat spreading path, resulting in different case temperature distribution. Although case temperature is easily accessible, the results depend greatly on the measurement location. Also, the measurement is sensitive to ambient temperature fluctuations.

**Figure 2.8.** Offline thermal impedance measurement methods. (a) Constant power method. The device current is adjusted by $V_{GS}$ control to achieve the desired power level. (b) Constant current method. The device current is switching between high ($I_{d, high}$) and low ($I_{d, low}$) current levels for heating and junction temperature estimation, respectively. (c) The typical test sequence.
2.4 Summary

Thermomechanical fatigue of bond wire and solder layer are the dominate reliability concerns. Since all degradation indicators are temperature dependent, offline diagnosis and online implementation with controlled operating condition are the most widely used practice. The most developed methods for degradation diagnosis are based on the measurement of on-state parameters. Better solutions for bond wire lift-off detection are still in need as bond wire lift-off may not develop detectable on-state parameter changes due to the negligible resistance compared to the overall resistance along the turn-on path. The measurement circuits have to be protected from large voltage and switching transients in practical implementations, thus, electrical isolation is necessary. Methods based on switching characteristics have appealing potential for embedding in operating converters, but they are easily influenced by routing connections. Thus, more explorations are needed. Thermal impedance measurement relies on accurate power loss and junction temperature information, which are both challenging to obtain under switching condition. In whichever method, junction temperature is critical and difficult to measure directly. Methods for obtaining junction temperature information will be reviewed in Chapter 5.
Chapter 3

**ISOLATED VOLTAGE MONITOR FOR ONLINE MONITORING SYSTEMS**

Power conversion systems are facing more stringent reliability requirements in industrial applications not only for the purpose of reducing the maintenance cost subject to non-scheduled system inspection, but also for avoiding drastic failures particularly for those applications that cannot afford any unexpected power shutdown such as aerospace applications. For a switching power device, the on-state voltage is commonly chosen as the key health status indicator, as it directly reflects the resistance deviation of the turn-on path under a specific loading and thermal condition, which serves as a useful input for degradation due to defect or aging. Various voltage monitoring methods have been proposed in recent years in response to the emerging needs of degradation diagnosis. The most popular implementation relies on circuits specifically designed for direct voltage measurement. However, they are vulnerable to data corruption due to electromagnetic interference (EMI), meaning that proper electrical isolation is needed.

In this Chapter, a voltage monitor with embedded isolation is proposed and demonstrated. The on-state voltage measured by the isolated voltage monitor can be processed directly by signal processing unit. This chapter begins with a system overview, describing the need of embedded isolation. The operating principle and design considerations are detailed. A comprehensive analysis on performance metrics with reference to prior arts is given, which can be applied to the design for targeted applications to overcome specific design challenges.
3.1 The Need for Embedded Isolation

Direct on-state voltage measurement requires physical contact to the switching node with wide voltage swing. It is necessary to isolate the measurement points from data acquisition system not only to protect measurement circuits against electrical damage, but also to avoid noise coupling from common ground loop. Conventional on-state voltage measurement circuits, as reviewed in Chapter 2.1, are lack of galvanic isolation and hence, an isolation interface has to be implemented in system side.

Isolation interface can be achieved either by analog or digital manner [57]–[59]. Analog isolator transfers continuous signals across isolation barrier and requires one for each measurement point; while digital isolator has relatively higher noise immunity as it digitizes signal before transmission. It requires the same amount of isolated lines as the bit number of the digitized data. If the digitized data is transmitted in serial form, only one isolated line is needed. Figure 3.1 shows the conventional on-state voltage measurement system. The measured on-state voltage is sampled by a \( n \)-bits high precision analog-to-digital converter (ADC), and then transmitted to the microcontroller through an isolated serial data interface. The implementation has been demonstrated at 2.5 kHz in [28].

![Conventional on-state voltage measurement system](image)

**Figure 3.1.** Conventional on-state voltage measurement system.

The conventional on-state voltage measurement system requires a digital isolator for
data transmission. However, as power conversion systems are moving toward higher switching rate, the digital isolator can reach its data rate overhead, which is determined by the number of points desired during the on-state period, and the measurement resolution. The measurement resolution is determined by the bit number and the supply voltage of the ADC. As the on-state voltage change due to incipient degradation is usually a result of junction temperature rise, the temperature sensitivity of the on-state voltage is a measure for determine the required measurement resolution. For example, the on-state voltage of the power device adopted in [28] has a temperature sensitivity of 2 to 3 mV/°C for high current. To detect the on-state voltage variation subject to a degree C change, the measurement resolution has to be lower than 2 mV. In [28], a 14-bits ADC with +/- 5 V supply is chosen to achieve a resolution of 0.61 mV.

According to the same references in Figure 1.1, a large part of mid- to high-power applications are operating at a switching frequency below 100 kHz. Since higher switching frequency is a future pursuit, here we consider an example with 100 kHz switching frequency: to retrieve one data point from 50 % duty cycle and encoded with 10-bits ADC, at least 2 Mbps data rate is required for the digital isolator. In reality, more data points are often desirable to average out the measurement error. Also, the requirement can become more stringent due to varying duty cycle. Taking the same example again but with 100 data points to retrieve, the minimum data rate requirement for the digital isolator now becomes 200 Mbps, which has exceeded the capacity of most commercially available isolators [60]–[61]. The bit number required for ADC is generally higher than the one used in the example, which indicates a more stringent data rate requirement.

To overcome the hurdle, the isolation interface can be brought to the analog front end as shown in Figure 3.2. In this case, the requirement for the isolation interface is limited
by the switching rate of power device only. The measured on-state voltage can be processed by micro-controller directly. As data sampling and signal processing are completed in chip level, better signal integrity can be achieved.

![Diagram](image_url)

**Figure 3.2.** On-state voltage measurement system with isolation interface embedded in the analog front end.

### 3.2 Proposed Isolated Voltage Monitor

There are two questions to ask before designing an isolated voltage monitor (IVM): What type of signal isolation technique is suitable for integration into the analog front end; and how to protect the IVM from high-voltage damage when the power device to be measured is at off-state.

Signal isolation is achieved by transferring information across a physical isolation barrier, such as air gap or dielectric material. An information can be transmitted across the isolation barrier in the form of light (optical coupling), electric field (capacitive coupling) or magnetic field (inductive coupling). As steady-state signal cannot be transmitted through capacitive coupling or inductive coupling, both capacitive coupling and inductive coupling techniques are not suitable for embedding in the analog front end. LED-photodiode combination is an optical coupling method that provides the design freedom to allow either digital or analog signal to transmit. Besides, it has the advantage of electromagnetic interference immunity. Hence, LED-photodiode
combination is chosen for the design of the proposed IVM.

Next, to protect the IVM from high-voltage damage, the IVM can be disconnected from the power device to be measured by inserting a switch or a high-voltage diode between the input of the IVM and the drain of the power device, or by limiting the input voltage with a Zener diode. Some applications can be found in Chapter 2.1. Compared to switch-based and Zener-diode-based methods, high-voltage-diode-based method has the advantage of faster response time and reasonable area occupation. Thus, high-voltage diode will be incorporated into the proposed IVM design.

Before analysing the detailed operation, the minimum detectable voltage range is defined. The minimum detectable voltage range depends on the device characteristics, aging variation and the operating condition of the targeted application. Considerations are slightly different for IGBT and power MOSFET. For IGBT, a general rule for device failure claim is that when the device has $\Delta V_{CE}\%$ increments in $V_{CE}$ at a defined operating condition at a thermal steady state [62], as given by

$$
\Delta V_{CE}[\%] = \frac{1500}{I_{rated}}
$$

(3.1)

where $I_{rated}$ is the rated current for a specific power module. The rise in $V_{CE}$ is a result of the lumped effect of higher resistance along the turn-on path, and device self-heating. Taking a commercial 1.2kV IGBT module (SKM150GB12T4G, Semikron) with the rated nominal current of 150 A as an example, the device is claimed to be failed when it has 10% increments in $V_{CE}$. Considering the worst case, where the junction temperature is 150 °C, according to the device datasheet [63], a fresh device has $V_{CE}$ of 2.3 V when the device is driving with the nominal gate bias and 150 A device current. The device failure is claimed when $V_{CE}$ has approximately 230 mV increments. Thus, the detectable voltage range for this power device has to cover at least up to 2.53 V.
For power MOSFET, the minimum detectable range is determined by the on-state resistance \( R_{\text{ds(on)}} \) and the operating current. For a commercially available 1.2 kV, all-SiC power module (CAS120M12BM2, Cree Inc.) with \( R_{\text{ds(on)}} \) of 13 mΩ, the maximum rating of the drain current is 100A if 120 °C worst case temperature is assumed [64], resulting in 1.3 V on-state voltage before wear-out developed. Actual detectable range should be higher to cover \( R_{\text{ds(on)}} \) variation due to temperature effect and aging. Current trend for failure judgement relies on experimental data-driven method [65]–[66].

### 3.2.1 Basic Operation Principle and Analysis

**A. Basic Principle**

Figure 3.3 shows the proposed IVM. Two high-voltage diodes \( D_H \) and \( D_L \) are used to block the high off-state voltage across the drain and source nodes. During the on-state period of the power device, both diodes are forward biased and the current flow through \( R_1 \) is as follows:

\[
I_{R1} = \frac{V_{DS} + V_{DH} - V_{DL}}{R_1}
\]  

(3.2)

![Figure 3.3. Proposed isolated voltage monitor.](image-url)
Assuming 1) the gate current of both op-amps are much smaller than $I_{R1}$; 2) The op-amp input offsets are negligible; 3) photodiodes PD1 and PD2 are identical with the same current transfer ratio with respect to LED; and 4) high-voltage diodes $D_H$ and $D_L$ are identical with the same forward current, we can have zero diode offset error, i.e. $V_{DH} - V_{DL} = 0$. Then, the output voltage of the IVM can be calculated as follows:

$$V_{sense} = V_{DS} \left( \frac{R_2}{R_1} \right)$$  \hspace{1cm} (3.3)

In reality, the diode offset error has to be taken into consideration as the current flow through $R_H$ and $R_L$ are uneven. Other error sources are relatively minor such as negligible op-amp input current. By well-organizing the geometric position of the two photodiodes and LED, the mismatch of current transfer ratio can be ignored. Resistor mismatch can be suppressed by choosing high precision resistors. Overall, the high-voltage diode offset is the major error source of this structure.

The diode offset is a result of intrinsic device mismatch and asymmetric forward current. Process variation is the root cause of device mismatch, leading to different intrinsic parameters such as reverse saturation current and therefore, non-identical current-voltage characteristics. Compared to asymmetric forward current, intrinsic device mismatch is negligible by assuming the high-voltage diodes are from the same manufacturing batch. According to Figure 3.3, the diode forward current difference is given by

$$I_{DL} - I_{DH} = (I_{RL} - I_{RH}) + 2I_{R1} = \frac{V_{DS} - \Delta V}{R} + \frac{2(V_{DS} - \Delta V)}{R_1}$$  \hspace{1cm} (3.4)

where $\Delta V$ is the diode offset voltage as defined by $\Delta V = V_{DL} - V_{DH}$ and $R_L = R_H = R$. Equation (3.4) gives a quick insight that the higher the $V_{DS}$, the greater the offset as the
forward current difference becomes larger. By designing the forward current to be higher, $\Delta V$ will become less sensitive to forward current change.

Taking a three phase 50 kW high power density converter (HPDC) for aerospace application with rated AC side line-to-neutral voltage ($V_{ac}$) of 230 V as a target application [67], the peak current flow through a power switch is calculated to be 102.5 A. If the HPDC is implemented with the all-SiC power module CAS120M12BM2 with $R_{ds} \text{on}$ of 13 mΩ, the measurable voltage ranges of the IVM has to be at least up to 1.33 V. Figure 3.4 shows the error between input ($V_{DS}$) and output ($V_{sense}$) of the proposed IVM with supply voltage $V_{DD}$ of 5 V for $V_{DS}$ up to 1.8 V. By designing $R_L = R_H = 5k$, the errors are smaller than 3%. Error can be suppressed by choosing smaller resistance, which corresponds to previous analyses that $\Delta V$ is less sensitive to diode forward current change at higher forward current. When replacing both resistors with identical current sources much greater than $I_{R1}$, errors are below 0.3%. In real applications, $V_{DS}$ is switching with high voltage swing. Figure 3.5 shows the simulated operation of IVM with $V_{DS}$ switching at 100 kHz between 750 V and 1 V to emulate the actual behaviour. It shows that IVM tracks on-state voltage well during sensing periods.

**Figure 3.4.** Output error of the proposed IVM with different $R_H$ and $R_L$ settings: $R_H = R_L = 20\, \text{k}\Omega$, 5 \text{k}\Omega and 2.5 \text{k}\Omega, respectively. The output error of both $R_H$ and $R_L$ are replaced by ideal current sources is shown as well.
B. IVM for Higher-accuracy-demand Applications

For applications that require higher monitoring accuracy, slight modifications can be made as shown in Figure 3.6. The two current paths $I_{RH}$ and $I_{RL}$ in Figure 3.3 are now provided by cascode current mirrors that served as two identical current sources $I_H$ and $I_L$. By accounting op-amp offsets, the current of photodiode $PD1$ is given by

$$I_{PD1} = I_H - I_L$$

Figure 3.5. Simulated operation of IVM with $V_{DS}$ switching at 100 kHz between 750 V and 1 V. The sensing periods of IVM are labeled with double-arrows.

Figure 3.6. Isolated voltage monitor for higher-accuracy-demand applications with op-amp input offsets ($V_{os1}$, $V_{os2}$) shown.
\[ I_{R1} = \begin{cases} \frac{V_{DS} + V_{DH} - V_{DL} - V_{os1}}{R1}, & \text{power device ON} \\ \frac{V_{DD} - |V_{BE}| - V_{DL} - V_{os1}}{R1}, & \text{power device OFF} \end{cases} \] (3.5)

By designing \( PD1 \) and \( PD2 \) to have the same current transfer ratio with respect to \( LED \), the sensed output voltage is summarized as follows:

\[ V_{\text{sense}} = \begin{cases} \frac{R2}{R1} (V_{DS} + \Delta V_d - V_{os1}) + V_{os2}, & \text{power device ON} \\ \frac{R2}{R1} (V_{DD} - |V_{BE}| - V_{DL} - V_{os1}) + V_{os2}, & \text{power device OFF} \end{cases} \] (3.6)

where \( \Delta V_d \) is the diode offset defined by \( \Delta V_d = V_{DH} - V_{DL} \). Note that the equations for power device \( OFF \) in equations (3.5) and (3.6) are valid only when the op-amps’ virtual short conditions are established. Equation (3.6) indicates that by designing \( R1 = R2 \), we can have \( V_{\text{sense}} \approx V_{DS} \) when a power device is at on-state under the condition that both the diode offset and op-amp input offset are negligible.

Since \( I_H \approx I_L \), the diode forward current difference given in equation (3.4) becomes \( 2I_{R1} \). With negligible op-amp input current, by choosing \( I_H \) and \( I_L \) to be much larger than \( I_{R1} \), the currents of \( D_H \) and \( D_L \) will be equal to \( I_H \) and \( I_L \), respectively. Again, the output error between \( V_{DS} \) and \( V_{\text{sense}} \) is simulated with different current settings of \( I_H \) and \( I_L \), where \( I_H = I_L \). The results are shown in Figure 3.7. The output error is suppressed to below 0.43% at the current setting larger than 1.85 mA.

It is worth to explore how thermal gradient influences the sensed output voltage, as the monitoring circuit might exposed to harsh environments. According to equation (3.6), where power device is \( ON \), the sensed output voltage correlates with the resistance ratio \( R2/R1 \), diode offset and the input offsets of op-amps. Typical SMD type resistors have a wide range of temperature coefficients, ranging from a few to hundreds of ppm/°C. By choosing resistors with large resistance and low temperature coefficient,
thermal gradient effect on the resistance ratio $R_2/R_1$ can be neglected. For general purpose precision op-amps, the input offset drift due to temperature variation is typically $< 10 \mu V/^\circ C$, which is negligible as well. Therefore, thermal gradient has the major effect on diode offset. A detailed diode offset analysis accounting for thermal gradient effect is given here. By assuming $I_L = I_H + \Delta I$ and the temperatures of $D_L$ and $D_H$ are $T + \Delta T$ and $T$, respectively, the diode offset $\Delta V_d$ is derived as follows:

\[
\Delta V_d \approx \frac{n k T}{q} \ln \left( \frac{I_H}{I_{s,H}} \right) - \frac{n k (T + \Delta T)}{q} \ln \left( \frac{I_L}{I_{s,L}} \right) = \frac{n k T}{q} \left[ \ln I_H - \ln I_{s,H} \right] - \left( 1 + \frac{\Delta T}{T} \right) \left( \ln I_L - \ln I_{s,L} \right) = \frac{n k T}{q} \left[ \ln \left( \frac{I_H}{I_L} \right) - \ln \left( \frac{I_{s,H}}{I_{s,L}} \right) \right] - \frac{\Delta T}{T} V_{DL} \tag{3.7}
\]

where $I_{s,L}$ and $I_{s,H}$ are the reverse saturation currents at the respective temperatures.

The reverse saturation current is proportional to the square of intrinsic carrier density $n_i^2$, which is both material and temperature dependent as described by

\[
\text{Figure 3.7.} \text{ Output error of the isolated voltage monitor for higher-accuracy-demand applications under different current settings of } I_H \text{ and } I_L, \text{ where } I_H = I_L.
\]
\[ n_i^2 = BT^3 e^{-\frac{E_G}{kT}} \] (3.8)

where \( B \) is a material-dependent constant, \( T \) is the absolute temperature, \( k \) is the Boltzmann’s constant and \( E_G \) is the bandgap energy of semiconductor in eV [68].

By using the same type of diodes, we can have:

\[
\ln \left( \frac{I_{s,H}}{I_{s,L}} \right) = 3 \ln \left( \frac{T}{T + \Delta T} \right) - \frac{E_G}{kT} \left( \frac{\Delta T}{T + \Delta T} \right)
\] (3.9)

By combining equations (3.7) and (3.9), we can get:

\[
\Delta V_d = \frac{nkT}{q} \left\{ \ln \left( \frac{I_H}{I_L} \right) - \left[ 3 \ln \left( \frac{T}{T + \Delta T} \right) - \frac{E_G}{kT} \left( \frac{\Delta T}{T + \Delta T} \right) \right] \right\} \frac{\Delta T}{T} V_{DL}
\] (3.10)

If both high-voltage diodes are operating at the same temperature, i.e. \( \Delta T = 0 \), then:

\[
\Delta V_d \approx -\frac{nkT}{q} \left( \frac{\Delta I}{I_L} \right) \quad \text{when} \quad \Delta I \rightarrow 0
\] (3.11)

For a design with \( T = 300 \text{ K} \), \( I_L = 10 \text{ mA} \), \( I_H = 9 \text{ mA} \), emission coefficient \( n = 1 \), \( V_{DL} = 0.7 \text{ V} \) and \( E_G = 1.2 \text{ eV} \), the diode offset for one degree and ten degrees K changes are \(-0.812 \text{ mV} \) and \(15.218 \text{ mV} \), respectively. It indicates the importance of maintaining both diodes under similar thermal conditions. This can be achieved by placing the two diodes close to each other, or by choosing diodes within the same package. Equation (3.11) can be rewritten into equation (3.12).

\[
\Delta V_d = -\frac{nkT}{q} \left[ \frac{(V_{DD} - 2|V_{BE}|) (R_H - R_L)}{V_{DD} - 2|V_{BE}|} \right] R_L
\] (3.12)

\[
= \frac{nkT}{q} \left( \frac{R_L - R_H}{R_H} \right)
\]

It shows that with well-matched \( R_H \) and \( R_L \), diode offset can be eliminated. Finally,
based on equation (3.6), to account for resistor variation and photodiodes’ current mismatch, taking $R_1 = (1 \pm p\%)R$, $R_2 = (1 \pm q\%)R$ and photodiodes with $\pm r\%$ current mismatch, then the output error can be computed as follows:

$$|\Delta V_{VM}| = (k - 1)V_{DS} + k\Delta V_d - kV_{os1} + V_{os2}$$  \hspace{1cm} (3.13)

where $k = \frac{(1\pm r\%)(1\pm q\%)}{(1\pm p\%)}$.

It reveals that $V_{DS}$ is always scaled by a factor $k$ regardless of how well the diode offset can be controlled. As a result, it is critical to choose high-precision resistors and optocoupler with small transfer gain (current ratio of $PD1$ and $PD2$) variation for achieving good accuracy.

C. Influence of Resistor Matching

To have a further insight into the influence of resistor matching, the output error $|\Delta V_{VM}|$ of the proposed IVM with cascode current mirror structure is simulated and compared with prior arts. The blocking-diode-based and gating-transistor-based topologies shown in Figure 2.2 and 2.3 are chosen for comparison for their popularity. Figure 3.8 shows the $|\Delta V_{VM}|$ of the proposed IVM and prior arts, where those resistor pairs that required to be highly matched are having $\pm 1\%$ and $\pm 0.1\%$ mismatch, respectively. All general design conditions are kept as similar as possible, including 1) identical component parts are adopted for high-voltage diodes and op-amps; 2) all op-amps are biased with $\pm 10$ V power supply; 3) all high-voltage diodes are biased with 10 mA; and 4) 1 mV input offset is added to every op-amp. Thermal-gradient-induced-error is not considered in this simulation.

The SPICE model of a commercially available SiC power MOSFET (C2M0080120D, Cree Inc.) is adopted as the device under monitor in the simulation. $V_{DS}$ is monitored with the device current swept from 0.5 A to 36 A, which creates an on-state voltage
range with maximum value around 3 V. The output errors have shown great improvement for every topology when resistor pairs are having smaller mismatches. The blocking-diode-based prior art shows less sensitive to $V_{DS}$ variation among all the topologies. In conclusion, by choosing high-precision resistors, the proposed IVM can have comparable output error performance when benchmarked with prior-art topologies and outstands with embedded isolation feature.

3.2.2 Experimental Verification

A. DC Characteristics

Both the basic and improved IVM are implemented. The DC performance are compared in Figure 3.9 together with the ideal case, i.e. the ratio of $V_{sense}$ to $V_{DS}$ is unity. Measurement results show that the IVM for higher-accuracy-demand applications follows the ideal case better. It improves the error from smaller than 7.1% to 1.9% within the designed range compared to the basic IVM.

Figure 3.8. Simulated output error comparison of the proposed IVM and prior arts. For blocking-diode-based prior-art topology shown in Figure 2.2, $R1 = 50k + n\%$ and $R2 = 50k - n\%$; for gating-transistor-based topology shown in Figure 2.3, $R2 = 1k + n\%$ and $R3 = 1k - n\%$; for the proposed IVM, $R1 = 50k + n\%$, $R2 = 50k - n\%$, $R_H = 860 + n\%$ and $R_L = 860 - n\%$. (a) With 1% resistor mismatch ($n=1$). (b) With 0.1% resistor mismatch ($n=0.1$).
B. Clamped Inductive Load Testing

A clamped inductive load testing with all-SiC half-bridge power module (CAS120M12BM2, Cree Inc.) is conducted to emulate the actual switching operation. Figure 3.10 shows the schematic and test setup for measuring the on-state voltage, where the device current of the low-side MOSFET (\(I_d\)) is measured by a current transformer with a scaling factor of 1/5. The results are shown in Figure 3.11. \(I_d\) increases gradually as the turn-on time increases, as well as the on-state voltage. Results show that the proposed IVM tracks on-state voltage well.

C. Functional Validation on a H-bridge Inverter

The functionality of the proposed IVM for online on-state voltage monitoring is validated on a SPWM controlled H-bridge inverter. Figure 3.12 shows the schematic and test setup. Key operating parameters are listed in Table 3.1. Both the high- and low-side devices of Leg A are monitored, and the results are shown in Figure 3.13 and 3.14, respectively. The results show that the proposed IVM is functioned properly on an in-service system, where the on-state voltage of the high- and low-side power devices are monitored at positive and negative half cycles of the AC output current, respectively.
Figure 3.10. (a) Schematic of the clamped inductive load testing. (b) Test setup. (①: Load inductor; ②: half-bridge power module; ③: IVM prototype.)

Figure 3.11. Measurement results of clamped inductive load testing. Left: Switching behaviour. From top to bottom: $V_{GS}$, $V_{DS}$, scaled $I_d$. Right: Stacked view of on-state voltage ($V_{DS}$) and IVM output ($V_{sense}$).

Figure 3.12. (a) Schematic of H-bridge inverter. (b) Test setup of on-state voltage monitoring of H-bridge inverter.
Table 3.1 Operating Parameters of the H-bridge Inverter

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Carrier Wave Switching Frequency ($f_{sw}$)</td>
<td>20k-Hz</td>
</tr>
<tr>
<td>Output AC Frequency</td>
<td>400-Hz</td>
</tr>
<tr>
<td>Load Inductance</td>
<td>246-μH</td>
</tr>
<tr>
<td>DC Power Supply ($V_{dc}$)</td>
<td>100-V</td>
</tr>
<tr>
<td>Switching Power Device</td>
<td>C2M0080120D</td>
</tr>
</tbody>
</table>

Figure 3.13. On-state voltage monitoring of the high-side power device of Leg A. (a) Current of load inductor ($I_L$) and output of IVM ($V_{sense}$). IVM tracks on-state voltage at positive half cycle of $I_L$. (b) Enlarged view of (a).

Figure 3.14. On-state voltage monitoring of the low-side power device of Leg A. (a) Current of load inductor ($I_L$) and output of IVM ($V_{sense}$). IVM tracks on-state voltage at negative half cycle of $I_L$. (b) Enlarged view of (a).
3.3 Online Monitoring of SiC Power MOSFET

To demonstrate the online monitoring capability of the proposed circuit, a SPWM-controlled H-bridge inverter constructed by discrete SiC power MOSFETs (C2M0080120D, Cree Inc.) with an inductive load is designed. A degraded sample is prepared and included in the H-bridge inverter to validate the online diagnosis method.

3.3.1 High-temperature Performance of IVM

For the ease of integration with the half-bridge structure of the H-bridge inverter, two identical IVMs based on Figure 3.6 are designed and integrated on a printed circuit board (PCB). For the ease of discussion, they will be referred as high-side voltage monitor (HSVM) and low-side voltage monitor (LSVM). A high temperature environment is emulated to verify the thermal gradient effects on the fabricated prototype, the DC characteristics of the LSVM is measured at both room temperature and high temperature environments. As shown in Figure 3.15 (a) and (b), the fabricated PCB is placed on top of a heatsink, which is attached to a hotplate (UC150, Stuart) with 125 °C temperature setting, at a 0.5 cm distance to emulate the high temperature environment. Figure 3.15 (c) shows the thermal image of the prototype when both HSVM and LSVM are powered up. It is observed that the temperature surrounds both HSVM and LSVM is higher than 80 °C, which is a good emulation of harsh thermal environment for both voltage monitor circuits. The measured DC characteristics are shown in Figure 3.16 together with the ideal case. It shows that the performance at both room temperature and the said high temperature environment are closely matched to the ideal case, which proves the well-functionality of the proposed IVM even at high temperature. The results show that the output errors are slightly lower at high temperature environment compared to room temperature condition, which suggest that the two high-voltage diodes might have closer
matched temperature under the emulated ambient condition.

Figure 3.15. (a) Test setup for high-temperature performance evaluation. (HSVM: high-side voltage monitor; LSVM: low-side voltage monitor) (b) Side view. The implemented PCB is situated 0.5 cm away from the top of a heatsink. (c) Thermal image of the operating IVMs with 125 °C hotplate setting.

Figure 3.16. Measurement results of LSVM. (a) Output DC characteristics. (b) Output error.
3.3.2 Preparation of Degraded Sample

A power cycling test is performed to degrade a C2M0080120D sample. The device is controlled at an always-turn-on state, and then heated up and cooled down repetitively with a constant current of 24 A and 0.5 A, respectively. Case temperature is adopted as the control parameter here. When the case temperature has 10 °C increments compared to the initial value, the cooling process began; after the case temperature has reached the initial value, the heating process starts until another 10 °C increments in case temperature. The device is stressed by the resulting junction temperature excursions. Figure 3.17 shows the case temperature and the resulting $V_{DS}$ during the early cycles of the power cycling test, where device aging is not evolved yet. The increasing $V_{DS}$ during every heating phase indicates the positive temperature dependence of $R_{dson}$. $R_{dson}$ is calculated every 10 cycles at the beginning of the heating phase so that the same case temperature can be assumed for each calculation. The results are plotted in Figure 3.18. It is found that $R_{dson}$ has a sudden increase when the cycle count approaches 20,000 and the increment is close to 30% after 20,000 power cycles. It can be observed that $R_{dson}$ has a gradual rise before the sharp change.

The resulting degradation is more likely to be package-related, as the power cycling test introduced repeated temperature swings, which is the major stressor for a device package. Bond wire damage is often developed prior to solder layer fatigue, as a bond wire bears a more severe local heating than a solder layer. Cracks often grow slowly from the edge of a bond wire heel, resulting in non-uniform current distribution and higher device temperature. Such degradation reflects on moderate increase in $R_{dson}$. Once the cracks further grow, or bond wire lift-off occurred, a great change in $R_{dson}$ can be observed, as a drastic current redistribution took place.
3.3.3 Online Monitoring Demonstration

Figure 3.19 (a) shows the SPWM-controlled H-bridge inverter constructed for demonstration. The proposed IVM is deployed to monitor leg B of the inverter, as shown in Figure 3.19 (b).

Figure 3.20 shows the load inductor current ($I_L$) and the monitored $V_{DS}$ waveforms for both high-side ($V_{sense,H}$) and low-side ($V_{sense,L}$) power MOSFETs with 20 kHz switching frequency. The on-state voltage is monitored when the device current has the same polarity as the load inductor current. This is due to the unipolar operation of the proposed IVM.
The H-bridge inverter is firstly constructed with non-degraded devices. Then, the low-side MOSFET of leg B is replaced with the degraded sample stressed by 20,000 power cycles. The output of the LSVM and the device current of both the non-degraded and degraded devices that measured by a Rogowski coil (CWTMini HF06B, PEM) are captured and then processed. In order to capture meaningful data, $V_{\text{sense},L}$ and device current are captured at the middle of each on-state period when $V_{\text{sense},L}$ is larger than 0.5 V and when the duty time of one switching cycle is greater than 10%. The sampled
data and calculated $R_{dson}$ during half of the fundamental cycle of the load inductor current are shown in Figure 3.21. The slightly increasing tendency of $R_{dson}$ implies that the device junction temperature is rising. Due to the inductive load and stable ambient environment, the online demonstration has a repetitive operating condition. Since the on-state electrical parameters observed during online monitoring exhibit an effect of electro-thermal positive feedback, the degraded device can be identified by observing a higher on-state voltage at the same device current level as the healthy device, as labelled by points A and B in Figure 3.21. This is because the degraded device has higher power loss.

![Sampled data of both non-degraded and degraded devices. Top to bottom: device current of low-side MOSFET, LSVM output voltage ($V_{sense,L}$), calculated $R_{dson}$.](image)

**Figure 3.21.** Sampled data of both non-degraded and degraded devices. Top to bottom: device current of low-side MOSFET, LSVM output voltage ($V_{sense,L}$), calculated $R_{dson}$.

Table 3.2 summarizes the measured $R_{dson}$ for both non-degraded and degraded devices. The offline measurement is taken during the power cycling test, as shown in Figure 3.18, where the initial $R_{dson}$ and the $R_{dson}$ after 20,000 cycles’ degradation are recorded in the table. The online measurement refers to the one performed on an
operating H-bridge inverter as described, the corresponding $R_{dson}$ at points A and B plotted in Figure 3.21 are recorded in the table. It shows that the $R_{dson}$ of both non-degraded and degraded devices measured with on-line manner are higher than those measured with off-line manner. This is because the latter are captured at the same thermal condition at the beginning of the device heating phase, while the former are captured from an operating power conversion system with higher device temperature. As the degraded device dissipated more heat, it will have a steeper increase in $R_{dson}$ compared to the non-degraded device from point A to B. It can be observed by identifying a larger $\Delta R_{dson}$ at point B than point A.

<table>
<thead>
<tr>
<th>Measurement Manners</th>
<th>Non-degraded (mΩ)</th>
<th>Degraded Sample (mΩ)</th>
<th>$\Delta R_{dson}$ (mΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offline</td>
<td>80.42</td>
<td>104.46</td>
<td>24.04</td>
</tr>
<tr>
<td>Online (Point A)</td>
<td>90.69</td>
<td>115.00</td>
<td>24.31</td>
</tr>
<tr>
<td>Online (Point B)</td>
<td>100.00</td>
<td>132.50</td>
<td>32.5</td>
</tr>
</tbody>
</table>

### 3.3.4 Further Investigation on IVM Switching Behaviour

Figure 3.22 (a) shows a closer view of the IVM output waveform at 20 kHz together with the load current $I_L$. It shows sufficient timing period for data sampling. The functionality of IVM at higher switching frequency at 100 kHz is verified as well. As shown in Figure 3.22 (b), the on-state voltage can be monitored as long as the duty time of a switching period is greater than 30%, which is common for high frequency applications.
3.4 Summary

A voltage monitoring circuit with inherent isolation has been designed, developed and experimentally verified. It can be tailored to fit different power converters with different rated specifications by selecting appropriate design parameters of each component. The tailoring depends on the on-state voltage range specified by the targeted application and the corresponding semiconductor power switch.

Table 3.3 compares the simulated output error, advantages and disadvantages
between the proposed IVM and the existing prior arts. With high-precision resistors, the proposed IVM can achieve comparable or better output error performance as compared to the method with embedded isolation feature.

The electrical isolation eliminates EMI influence on the measured data and allows direct processing of the monitored voltage information, which greatly simplified the system integration effort. With the electrical isolation feature, it is highly desirable for online health monitoring of power switching devices in an in-service power conversion system. By using the on-state voltage of a new and healthy device as a benchmark, the sensed output voltage has the ability to distinguish a deteriorated device from a healthy one under the same operating condition. The on-state voltage allows the on-state resistance to be calculated for further failure analysis purpose. Based on a comprehensive analysis of the output error, the error of the proposed topology has shown to be unaffected by high environmental temperature and it can be further optimized through careful selection of circuit components.

| Topology                          | Output Error $|\Delta V_{vd}|$ (mV) | Advantages/Disadvantages                                      |
|-----------------------------------|---------------|------------------------------------------------------------|
|                                   | 1% $R^{\dagger\dagger}$ Mismatch | 0.1% $R^{\dagger\dagger}$ Mismatch |                                                        |
| Blocking-diode-based Prior Art    | < 25          | < 12                                                       |
| (Figure 2.2)                      |               |                                                             |
| Gating-transistor-based Prior Art | < 65          | < 8                                                        |
| (Figure 2.3)                      |               |                                                             |
| The Proposed IVM                  | < 65          | < 8                                                        |

$^{\dagger}$ The data shown are simulated results that summarized form Figure 3.8.

$^{\dagger\dagger}$ Resistor mismatch.

The electrical isolation eliminates EMI influence on the measured data and allows direct processing of the monitored voltage information, which greatly simplified the system integration effort. With the electrical isolation feature, it is highly desirable for online health monitoring of power switching devices in an in-service power conversion system. By using the on-state voltage of a new and healthy device as a benchmark, the sensed output voltage has the ability to distinguish a deteriorated device from a healthy one under the same operating condition. The on-state voltage allows the on-state resistance to be calculated for further failure analysis purpose. Based on a comprehensive analysis of the output error, the error of the proposed topology has shown to be unaffected by high environmental temperature and it can be further optimized through careful selection of circuit components.
Chapter 4

**Offline Deterioration Diagnosis in Frequency Domain**

Inductive coupling method is a nonintrusive method that has been applied for various in-circuit impedance measurement applications since early 70s, including line impedance extraction [71], output impedance extraction of clock driver [72], and interelectrode capacitances characterization of power devices [73]. It has been further improved for better measurement accuracy with two-port network model in [74]. In this chapter, an offline deterioration diagnosis method for power devices based on the inductive coupling method is proposed. The on-state impedance of a power device in frequency domain can be measured as a deterioration indicator. The proposed method eliminates direct electrical contact with the power device to be measured. With careful setup and calibration, the proposed approach has the ability to detect the deviation of on-state impedance from its norm for deterioration diagnosis purpose. For demonstration purpose, a commercially available SiC power MOSFET (P/N: C2M0080120D, Cree Inc.) is adopted throughout this chapter.

**4.1 Limitations of Time-domain Diagnosis**

Conventional time-domain voltage or current waveforms measurement methods require direct electrical contacts to the power device to be measured to diagnose its health status. The intrusive nature requires special design considerations to minimize the impact imposed on the power conversion system. Among them, on-state voltage and
on-state resistance are the most frequently chosen parameters for health diagnosis purpose. As the on-state resistance change is rather small as compared to the overall on-state impedance of the power device to be measured, the change in these two parameters may not be easily noticeable, especially for power device with low operating current. Major reliability issues may not be identified in time such as bond wire damage.

Alternatively, switching characteristics have been used as indirect indicators of a power device’s defects as reviewed in chapter 2.2. Although they have shown attractive online implementation potential since the degradation information is hidden in operating waveforms, the robustness of degradation diagnosis is hard to guarantee as switching characteristics are sensitive to routing conditions and parasitic elements. Also, the fluctuation behaviour can be very different depends on how a device being degraded. For examples, increase in parasitic inductance due to damaged bonding wires results in higher voltage spike during turn-off transition [43] and reduction in gate capacitance due to long-term thermos-electrical stress results in lower turn-off ringing [69]. Before acceptable diagnosis capabilities are demonstrated, more studies are needed to investigate the correlation between the variation of switching properties and the true mechanism behind.

In view of the limitations faced by the time-domain measurement methods, this chapter proposes an alternative non-intrusive method based on a fully inductively coupled approach to measure the on-state impedance variation in frequency domain. Unlike conventional intrusive time-domain methods that monitor the variation of DC characteristics of a power device, the proposed method is by itself electrically isolated from the electrical system to be measured, which allows direct measurement of the on-state impedance of a power device without disturbing its usual operating condition. It can be shown later that the measured on-state impedance of a power device in
frequency-domain provides more visible changes and insights for deterioration
diagnosis purpose.

4.2 On-state Frequency Response of SiC Power MOSFET

The on-state frequency response of a SiC power MOSFET is analysed with the on-
state equivalent circuit model shown in Figure 4.1 (a). $L_g$, $L_d$ and $L_s$ are the bond wire
inductance of the gate, drain and source, respectively; $R_g'$ is the total resistance of the
internal and external gate resistances in series; $C_{gd}$ and $C_{gs}$ are the gate-to-drain and gate-
to-source capacitances, respectively; and $R_{dson}$ is the on-state resistance. The drain-to-
source on-state impedance is defined as the impedance looking into drain node, as
indicated as $Z_{SiC}$. By applying $\Delta$-Y transformation, $C_{gd}$, $C_{gs}$ and $R_{dson}$ can be converted
to $Z_g$, $Z_d$ and $Z_s$, as shown in Figure 4.1 (b).

![On-state equivalent circuit model of a SiC power MOSFET](image)

**Figure 4.1.** (a) On-state equivalent circuit model of a SiC power MOSFET. (b) Equivalent on-state model of a SiC power MOSFET by converting $C_{gd}$, $C_{gs}$ and $R_{dson}$ to $Z_g$, $Z_d$ and $Z_s$ through $\Delta$-Y transformation.

For a sinusoidal steady-state signal of angular frequency $\omega$, the on-state impedance
can be expressed as
\[ Z_{\text{SiC}} = (j\omega L_d + Z_d) + \left( R'_g + j\omega L_g + Z_g \right) \parallel (j\omega L_s + Z_s) \]  

(4.1)

\( Z_g, Z_d \) and \( Z_s \) are determined by \( \Delta - Y \) transformation as follows

\[ Z_g = \frac{Z_{gd}Z_{gs}}{Z_{\text{total}}} \quad Z_d = \frac{Z_{gd}Z_{ds}}{Z_{\text{total}}} \quad Z_s = \frac{Z_{gs}Z_{ds}}{Z_{\text{total}}} \]  

(4.2)

where \( Z_{gd} = \frac{1}{j\omega C_{gd}} \), \( Z_{gs} = \frac{1}{j\omega C_{gs}} \), \( Z_{ds} = R_{\text{ds}o} \) and \( Z_{\text{total}} = Z_{gd} + Z_{gs} + Z_{ds} \).

For a power MOSFET operating at on-state, \( V_{DS} \approx 0 \) V. \( Z_g \) is usually \( \gg Z_s \) within the frequency range of interest, which can be judged by taking the ratio of \( Z_g \) to \( Z_s \), where

\[ \frac{Z_g}{Z_s} = R_{\text{ds}o} \]  

From the datasheet of the targeted SiC power MOSFET C2M0080120D [70], where \( C_{gd} \approx 412 \) pF and \( R_{\text{ds}o} = 80 \) mΩ at 20 A rated current, we can have \( \left| \frac{Z_g}{Z_s} \right| \approx 2.41 \times 10^2 \) at 20 MHz. Thus, equation (4.1) can be simplified to

\[ Z_{\text{SiC}} \approx Z_d + Z_s + j\omega (L_d + L_s) \]  

(4.3)

Substituting \( Z_d \) and \( Z_s \) from equation (4.2) into (4.3) gives

\[ Z_{\text{SiC}} = \frac{R_{\text{ds}o}}{1 + j\omega R_{\text{ds}o} (C_{gd} \parallel C_{gs})} + j\omega (L_d + L_s) \]  

(4.4)

Equation (4.4) shows that \( R_{\text{ds}o} \) dominates in \( Z_{\text{SiC}} \) at low frequency. As frequency increases, the inductive effect of bond wires starts to surface and the inductive reactance dominates in \( Z_{\text{SiC}} \) at high frequency.

The on-state frequency response of a SiC power MOSFET is simulated by using the generic packaged SPICE model of C2M0080120D provided by the manufacturer. Figure 4.2 shows the schematic of the frequency response simulation.

The power MOSFET \( M_{\text{SiC}} \) is fully turned on with nominal \( V_{GS} \). The DC voltage source together with a biasing resistor \( R_b \) provide a device current of 1 A for \( M_{\text{SiC}} \). A
10 μF coupling capacitor \( C_C \) is inserted to provide a small signal path for the sinusoidal steady-state signal \( V_{ac} \). Figure 4.3 (a) shows the simulated frequency response of \( |Z_{SiC}| \) up to 20 MHz. As expected, resistive and inductive behaviours are observed at low and high frequency, respectively. From the simulated frequency response, \( Z_{SiC} \) can be modeled as a series \( RL \) circuit with \( R = 69.2 \) mΩ and \( L = 15.5 \) nH, where the impedance is plotted together with the simulated response in Figure 4.3 (a). In the frequency range of interest, the capacitive effects of \( C_{gd} \) and \( C_{gs} \) are insignificant. For more advanced power MOSFET with lower \( R_{ds(on)} \) and higher \( C_{gd} \), the upper frequency limit for the above simplification to be valid is expected to be lower. In other words, a device with higher

![Figure 4.2](image_url)

**Figure 4.2.** Schematic of the frequency response simulation of a SiC power MOSFET.

![Figure 4.3](image_url)

**Figure 4.3.** (a) Simulated frequency responses of the on-state impedance of the SiC power MOSFET, C2M0080120D, and its equivalent series \( RL \) model. (b) Equivalent circuit model of \( Z_{SiC} \).
$C_{gd}$ reduces the maximum measurable frequency. A device with a higher measurable frequency range is preferred for experimental validation across a wide frequency band. However, the device selection is unlikely to affect the measurement of $R_{dson}$ at low frequency, which is dominated by resistive behaviour.

4.3 Proposed Inductive Coupling Approach for Deterioration Diagnosis

4.3.1 Theoretical Background

The concept of measuring an unknown impedance $Z_x$ using inductive coupling method is illustrated with the basic setup shown in Figure 4.4.

It involves two current probes and a vector network analyzer (VNA). A coupling capacitor $C_c$ with an ESR of $R_c$ and ESL of $L_c$ is inserted to provide the small signal path for a sinusoidal test signal injected from port 1 of the VNA. The sinusoidal test signal is injected into the designed small signal path, which consists of the unknown impedance,
wiring parasitics and coupling capacitor, through the injecting probe. The same signal is picked up by port 2 of the VNA through the receiving probe. The resultant impedance measured by the VNA is the sum of $Z_x$, the impedance of wiring parasitics $Z_w$ and the impedance of coupling capacitor $Z_c$. If $Z_w$ and $Z_c$ are known, $Z_x$ can be extracted. By adopting current probe with high permeability magnetic core, the current probe and the wire being clamped are considered to be well-coupled, where the leakage inductance and the core loss are usually negligible. Hence, the current probe and the circuit wiring being clamped are equivalent to a transformer with a turn ratio of $n$:1, which can be represented by a two-port network with $ABCD$ matrix representation. Before moving further, it is worth to revisit the basics of $ABCD$ matrix.

The $ABCD$ matrix, also known as transmission, cascade or chain matrix, is a form of two-port network representation that allows individual two-port networks to be combined in a cascading configuration. Figure 4.5 shows a two-port network with $ABCD$ matrix representation.

![Figure 4.5. Two-port network with $ABCD$ matrix representation.](image)

The $ABCD$ matrix relates the output voltage and current to the input ones with the following format:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix}$$

(4.5)

where each parameter is defined as follows:
\[ A = \frac{V_1}{V_2} \bigg|_{t_2 = 0} \quad B = \frac{V_1}{I_2} \bigg|_{V_2 = 0} \quad C = \frac{I_1}{V_2} \bigg|_{t_2 = 0} \quad D = \frac{I_1}{I_2} \bigg|_{V_2 = 0} \]  

(4.6)

For a two-port network with both ports are matched to a 50 Ω system, the \( ABCD \)-parameters can be obtained by converting the \( S \)-parameters measured by a VNA as follows [75]:

\[
\begin{align*}
A &= \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{2S_{21}} \\
B &= \frac{25[(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}]}{S_{21}} \\
C &= \frac{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}{100S_{21}} \\
D &= \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{2S_{21}}
\end{align*}
\]

(4.7)

Based on the theory of \( ABCD \) matrix, the basic setup shown in Figure 4.4 can be partitioned into three cascaded two-port networks, as shown in Figure 4.6 (a), where the currents and voltages of the respective ports are labelled. The first two-port network \( M_{\text{inj}} \) is the injecting probe clamped onto the circuit wiring, the second two-port network \( M_{\text{circuit}} \) is the circuit itself and the last two-port network \( M_{\text{rec}} \) is the receiving probe clamped onto the circuit wiring. \( M_{\text{system}} \) represents the overall two-port network seen by ports 1 and 2 of the VNA. \( V_{\text{inj}} \) is the sinusoidal voltage source injected from port 1 of the VNA. \( V \) is the impedance measured by the VNA, where \( Z = Z_x + Z_w + Z_c \). The overall two-port network and the corresponding cascading partitions represented by \( ABCD \) matrices are shown in Figure 4.6 (b) and (c), respectively, where \( M_{\text{system}} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{system}}, M_{\text{inj}} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{inj}}, M_{\text{circuit}} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{circuit}} \) and \( M_{\text{rec}} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{rec}} \).

According to the definition of \( ABCD \) matrix shown in equation (4.5), we have that
\[
\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{system}} \begin{bmatrix} V_4 \\ I_4 \end{bmatrix}
\]
\[
= \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{inj}} \cdot \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{circuit}} \cdot \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\text{rec}} \begin{bmatrix} V_4 \\ I_4 \end{bmatrix}
\] (4.8)

In another word, the overall two-port network seen by the VNA is the product of the individual two-port networks, as given by

**Figure 4.6.** (a) Equivalent two-port network of the basic setup of inductive coupling method for unknown impedance measurement. (b) The overall two-port network seen by ports 1 and 2 of the VNA, and (c) the corresponding cascading partitions represented by \(ABCD\) matrices.
\[
\begin{bmatrix}
A & B \\
C & D
\end{bmatrix}_{\text{system}} = \begin{bmatrix}
A & B \\
C & D
\end{bmatrix}_{\text{inj}} \cdot \begin{bmatrix}
A & B \\
C & D
\end{bmatrix}_{\text{circuit}} \cdot \begin{bmatrix}
A & B \\
C & D
\end{bmatrix}_{\text{rec}}
\tag{4.9}
\]

By observing Figure 4.6 (a), we have the overall impedance of the setup (Z) as follows:

\[
Z = \frac{V_2}{I_3}
\tag{4.10}
\]

which is the \(B\) parameter of \(M_{\text{circuit}}\). Once \(M_{\text{system}}, M_{\text{inj}}\) and \(M_{\text{rec}}\) are known, the \(B\) parameter of \(M_{\text{circuit}}\) can be obtained by solving equation (4.11).

\[
\begin{bmatrix}
A & B \\
C & D
\end{bmatrix}_{\text{circuit}} = \begin{bmatrix}
A & B \\
C & D
\end{bmatrix}_{\text{inj}}^{-1} \cdot \begin{bmatrix}
A & B \\
C & D
\end{bmatrix}_{\text{system}} \cdot \begin{bmatrix}
A & B \\
C & D
\end{bmatrix}_{\text{rec}}^{-1}
\tag{4.11}
\]

Again, the unknown impedance \(Z_x\) can be extracted from \(Z\) by removing the impedance of wiring parasitics and coupling capacitor (\(Z_u\) and \(Z_c\)) from \(Z\). The procedure will be covered in detail in the following section, Chapter 4.3.2.

Based on equation (4.7), the generic form of the \(ABCD\) parameters of each two-port network is given as follows:

\[
\begin{bmatrix}
A & B \\
C & D
\end{bmatrix} = \begin{bmatrix}
1 + S_{ii} - S_{jj} - S' & 25 \cdot (1 + S_{ii} + S_{jj} + S') \\
\frac{2 \cdot S_{ji}}{1 - S_{ii} - S_{jj} + S'} & \frac{S_{ji}}{100 \cdot S_{ji}} & \frac{S_{ji}}{2 \cdot S_{ji}}
\end{bmatrix}
\tag{4.12}
\]

where the subscripts \(i\) and \(j\) represent the input and output ports of each two-port network, respectively; and \(S' = S_{ii}S_{jj} - S_{ij}S_{ji}\).

In equation (4.11), \(M_{\text{system}}\) is obtained by measuring the overall two-port network, where \(M_{\text{inj}}\) and \(M_{\text{rec}}\) can be obtained by characterizing each inductive coupling probe through measurement. To characterize \(M_{\text{inj}}\), the \(S\) parameters are measured by injecting a sinusoidal test signal from port 1 of the VNA into the injecting probe, which is clamped onto a wire with two ends connected to port 2 of the VNA, as illustrated by Figure 4.7.
To characterize $M_{rec}$, the receiving probe is connected to port 2 of the VNA. Then, the $S$-parameters are measured by injecting a sinusoidal test signal from port 1 of the VNA into a wire that being clamped by the receiving probe, as illustrated by Figure 4.8. The measured $S$-parameters are then converted to $ABCD$-parameters by equation (4.12). The wire being clamped has to be as short as possible to minimize the influence of parasitics. To achieve accurate characterization, it is best to fix the current probes on an evaluation printed circuit board (PCB) [74].

![Figure 4.7](image1.png)  
**Figure 4.7.** Characterization of $M_{inj}$. (a) Measurement setup. (b) Equivalent two-port network.

![Figure 4.8](image2.png)  
**Figure 4.8.** Characterization of $M_{rec}$. (a) Measurement setup. (b) Equivalent two-port network.

### 4.3.2 Measurement Setup and Validation

Based on the concept shown in Figure 4.4, a measurement setup is designed for measuring an unknown impedance under specific operating condition. Figure 4.9 shows the measurement setup to measure an unknown impedance $Z_x$ powered by a DC voltage.
$Z_s$ is the impedance of the power supply loop formed by the power supply $V_{DC}$, the biasing resistor $R_b$ and the routing connections. $Z_c$ is the resultant impedance of $C_c$ and interconnections between nodes A and B. Two inductive probes, one for signal injection and another for reception, are clamped onto the circuit wiring with a coupling capacitor $C_c$. Port 1 of the VNA injects a sinusoidal signal into the circuit through the injecting probe. The injected signal flows into two paths, one into DC power supply and another into the unknown impedance. The same signal returns to the injecting point and is measured by port 2 of the VNA through the receiving probe. The overall impedance measured by the VNA is $Z = Z_c + Z_s \parallel Z_x$. By designing $|Z_s| \gg |Z_x|$, $Z_x$ can be extracted by subtracting $Z_c$ from $Z$.

![Figure 4.9. Unknown impedance measurement setup under operating condition based on inductive coupling method.](image)

Two identical inductive coupling probes (Tektronix CT6) and a VNA (Rohde & Schwarz ZNB20 VNA, frequency range: 100 kHz to 20 GHz) are selected for the experimental validation. Since the final goal is to measure a SiC power MOSFET under its on-state operation, where the unknown impedance is expected to be relatively small at the frequency range of interest, $R_b$ is chosen to be 11.2 $\Omega$ such that $|Z_s| \gg |Z_x|$ and 1 A biasing current is provided. The relatively low biasing current is chosen such that it avoids large variation in on-state resistance due to junction temperature change caused
by self-heating, as well as to have low power dissipation in the biasing resistor. Although $Z_c$ can be de-embedded from the impedance measured by the VNA, it is a good practice to minimize $Z_c$ as much as possible so that the unknown impedance dominates in the measurement. Prior to the impedance measurement of a power device, the measurement setup is validated with several precision passive components that are treated as unknown impedance to be measured. All these passive components are surface-mounted device (SMD) type with negligible parasitics.

Before the measurement of the unknown impedance, the inductive coupling probes are characterized based on the setup shown in Figure 4.7 and 4.8 to obtain $M_{inj}$ and $M_{rec}$. In order not to deviate from the focus of the thesis, the measured $ABCD$-parameters of $M_{inj}$ and $M_{rec}$ are included in the Appendix section. The overall impedance $Z$ is measured first. Then, the unknown impedance is replaced with a short circuit to measure $Z_c$. Since the parasitics of the wiring connections contributed by the path “node A $\rightarrow$ unknown impedance $\rightarrow$ node B” is much smaller than that contributed by the path “node A $\rightarrow$ $C_c$ $\rightarrow$ node B”, the later dominates $Z_c$. Figure 4.10 shows that $|Z_c|$ is well below 200 mΩ in the frequency range of interest. Finally, the unknown impedance $Z_c$ can be obtained by subtracting $Z_c$ from $Z$ under the condition that $|Z_s| \gg |Z_x|$. For further investigation, $Z_s$ can be determined by replacing the unknown impedance with an open circuit. Although this also includes the impedance contributed by the path “node A $\rightarrow$ $C_c$ $\rightarrow$ node B”, the impedance of power supply and biasing resistor dominate the measurement due to the much smaller $Z_c$. Figure 4.11 shows the measurement results of SMD passive resistors. The standard precision resistors of 1 Ω with ±1% tolerance are chosen. Firstly, one 1 Ω resistor is measured and then, two 1 Ω resistors in parallel (0.5 Ω) and finally three 1 Ω resistors in parallel (0.33 Ω). The measured resistances with the proposed method have agreed well with the actual resistances.
Next, the behaviour of $RC$, $RL$ and $RLC$ combinations are measured and validated. Figure 4.12 shows the measured frequency response of 0.5 $\Omega$ resistor, 47 nF capacitor, as well as both in parallel. It is observed that the frequency response of 47 nF capacitor is flattened at low frequency. This is because the low frequency impedance of 47 nF $\text{capacitor}$ is lower than the resistance of the circuit. The frequency response of small-resistance resistors is also shown in Figure 4.11. The impedance magnitude decreases as the frequency increases, which is typical for capacitors in parallel with resistors.
capacitor and $Z_s$ are comparatively large, the assumption $|Z_s| \gg |Z_x|$ is no longer hold. This observation indicates the significance of designing $|Z_s| \gg |Z_x|$. When $RC$ is in parallel, the impedance is dominated by resistor at low frequency and capacitor at high frequency. The result shows expected behaviour, with the transition frequency of $\frac{1}{2\pi RC}$, which is 6.77 MHz in this case.

![Graph](image)

**Figure 4.12.** Measured frequency response of 0.5 $\Omega$ resistor, 47 nF capacitor, resistor-capacitor in parallel and $|Z_s|$.

Figure 4.13 is the measurement results of 0.5 $\Omega$ resistor, 210 nH inductor, as well as both in series. When $RL$ is in series, the resistor dominates the overall impedance at low frequency and the inductor governs at high frequency. The transition frequency can be computed by $\frac{R}{2\pi L}$, which is around 379 kHz.

To emulate the typical on-state impedance of a SiC power MOSFET, where resistive behaviour dominates at low frequency and inductive behaviour governs at high frequency, a combination of 0.5 $\Omega$ resistor, 210 nH inductor and 200 pF capacitor, as shown in Figure 4.14 (a), is measured. The result is plotted together with the simulated frequency response and $|Z_s|$ in Figure 4.14 (b). It shows that both measured and
simulated results are consistent.

Figure 4.13. Measured frequency response of 0.5 Ω resistor, 210 nH inductor, resistor-inductor in series and $|Z_s|$.

Figure 4.14. (a) $RLC$ combination to be measured. (b) Measured, simulated impedance frequency response of a parallel $RC$ circuit in series with $L$ and $|Z_s|$.
4.4 Deterioration Diagnosis of SiC Power MOSFET

4.4.1 Preparation of Deteriorated Samples

Samples with two kinds of deteriorations are prepared for diagnosis in this section. The first kind is device with long-term thermal-stress aging; the second kind is device with bond wire damage only. For comparison, two fault-free samples are prepared as well. Figure 4.15 shows the four samples to be measured from the same manufacturing batch (P/N: C2M0080120D). Sample-A and Sample-B are prepared for long-term aging diagnosis, where the former is a non-degraded, fault-free device; and the latter is degraded by 20,000 power cycles, as described in Chapter 3.3.2. Both have pin length of 2 cm. The impedance frequency responses of Sample-A and Sample-B are compared to evaluate the degradation of the power MOSFET after the accelerated thermal stress. Sample-C and sample-D are arranged for bond wire damage evaluation. Sample-C is a non-degraded, de-capsulated power MOSFET with two of the bond wires connected to the source terminal cut to emulate the defect. Since the pin leads of Sample-C have been cut short to 1.1 cm during the de-capsulation process, its impedance frequency response will be compared with that of Sample-D, which is a fresh device with the same pin length as Sample-C, for bond wire damage diagnosis. Figure 4.16 shows the images of Sample-C before and after the cutting of bond wires, where source and drain terminals have three bond wires, respectively, before the damage.
4.4.2 Offline Diagnosis

A test fixture based on Figure 4.9 is designed and fabricated for measuring the on-state impedance \( Z_{\text{SiC}} \) frequency response of the prepared samples, as shown in Figure 4.17. The terminal blocks are fix-mounted on the PCB for ease of test sample replacement between measurements so as to maintain similar environmental condition. Two CT6 current probes are fixed positioned to minimize the impact of stray capacitance associated with the current probes. The wires through the current probes should be kept as short as possible to minimize the effect of inductive reactance.

![SiC power MOSFETs to be measured. Sample-A: non-degraded, with pin length of 2 cm; Sample-B: degraded by 20,000 power cycles; Sample-C: non-degraded, de-capsulated with bond wire damage; Sample-D: non-degraded, with pin length of 1.1 cm.](image)

![Images of Sample-C before (left) and after (right) the cutting of bond wires.](image)
A. Long-term Aging

Both Sample-A and Sample-B are fully turned on with a nominal gate bias voltage of 20 V. Figure 4.18 shows the on-state impedance $Z_{SiC}$ characterized by the proposed method at 1 A operating current, where the impedance behaviours are in close agreement with simulation shown in Figure 4.3. The results show that low-frequency $|Z_{SiC}|$ of the degraded device is higher than that of the non-degraded device, while no difference in inductive reactance is observed, which implies no significant damage on bond wires. To verify the measurement, $|Z_{SiC}|$ at 100 kHz, which is the lowest measurement frequency of the VNA, is chosen for comparison with the $R_{dson}$ at DC that measured by an $I-V$ curve tracer (Tektronix 371A), as $|Z_{SiC}|$ is dominated by $R_{dson}$ at low frequency due to the insignificant inductive effect. Figure 4.19 shows the $I-V$ characteristics of Sample-A and Sample-B measured by the $I-V$ curve tracer. It shows that $R_{dson}$ of the degraded
Sample-B deviates from its initial value by 25% and 29.1% at 1A and 10 A operating current, respectively. The comparison of measured $R_{dson}$ at DC and 100 kHz at 1 A operating current are summarized in Table 4.1. The proposed method shows 23% $R_{dson}$
increment of the degraded sample, which agrees well with the measured $R_{dson}$ from $I$-$V$ curve tracer.

\begin{table}[h]
\centering
\begin{tabular}{|c|c|c|}
\hline
\textbf{Measurement Method} & \textbf{$R_{dson}$ (mΩ) @ 1A, Room Temperature} \\
\hline
I-$V$ Curve Tracer & 64.0 & 80.0 \\
The Proposed Method & 68.8 & 84.4 \\
\hline
\end{tabular}
\caption{Comparison of $R_{dson}$ by Different Methods}
\end{table}

\textit{B. Bond Wire Damage}

Bond wires contribute a significant part of the parasitic inductance within a package. Since the inductive reactance dominates $Z_{SiC}$ at higher frequency, a power MOSEFT with damaged bond wires is expected to exhibit higher inductive reactance at higher frequency. Figure 4.20 shows the measurement results with and without damaged bond wires, where both samples are fully turned on with $V_{GS} = 20$ V. As expected, Sample-C has higher impedance than Sample-D at higher frequency, with the extracted inductances of 15.3 nH and 12.7 nH, respectively. The extracted inductance of Sample-D is smaller than Sample-A that measured previously, which is reasonable since the pin length is shorter than Sample-A. It also indicates that device pins do contribute additional inductances. There is no visible $|Z_{SiC}|$ changes observed at low frequency, which supports the general finding that bond wires contribute insignificant parts of on-state resistance. The results indicate that time-domain diagnosis methods may have difficulty to detect such damage, as the measurement is at DC. Hence, the merit of frequency-domain impedance measurement becomes apparent.
Proper gate biasing voltage for a power MOSFET is essential for efficiency optimization of a power conversion system. Larger gate biasing voltage reduces both a power MOSFET’s conduction loss and switching loss due to lower $R_{ds_{on}}$ and faster switching transient. Although larger gate biasing voltage introduces higher gate driver loss, it is typically insignificant compared to the total loss of a power conversion system.

Gate drivers are the core of proper gate driving, and yet one of the fragile parts in a power conversion system. It is considered to be the third most fragile parts in the 2011 industrial-based survey [18], as shown in Figure 1.3. Gate driver failure can be caused by routing disconnections or electromagnetic interferences [76]. It can lead to insufficient gate biasing voltage and higher $R_{ds_{on}}$, resulting higher power dissipation and might consequently cause thermal runaway [77]. To demonstrate the capability of the proposed method to detect insufficient gate bias, the non-degraded Sample-A is

![Graph showing impedance frequency response with and without damaged bond wires.](image)

**Figure 4.20.** On-state impedance frequency response with and without damaged bond wires.

*C. Loss of Gate Control*

Proper gate biasing voltage for a power MOSFET is essential for efficiency optimization of a power conversion system. Larger gate biasing voltage reduces both a power MOSFET’s conduction loss and switching loss due to lower $R_{ds_{on}}$ and faster switching transient. Although larger gate biasing voltage introduces higher gate driver loss, it is typically insignificant compared to the total loss of a power conversion system.

Gate drivers are the core of proper gate driving, and yet one of the fragile parts in a power conversion system. It is considered to be the third most fragile parts in the 2011 industrial-based survey [18], as shown in Figure 1.3. Gate driver failure can be caused by routing disconnections or electromagnetic interferences [76]. It can lead to insufficient gate biasing voltage and higher $R_{ds_{on}}$, resulting higher power dissipation and might consequently cause thermal runaway [77]. To demonstrate the capability of the proposed method to detect insufficient gate bias, the non-degraded Sample-A is

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measured with different gate biasing voltages. Higher $R_{\text{ds(on)}}$ is observed as $V_{GS}$ decreases, as shown in Figure 4.21. The measured $|Z_{\text{SiC}}|$ at 100 kHz, which is dominated by $R_{\text{ds(on)}}$, are compared with the calculated $R_{\text{ds(on)}}$ based on measured $V_{DS}$ and $I_d$ at DC. The results are summarized in Table 4.2, which shows a good agreement between DC measurement and the proposed method.

![On-state impedance frequency response of the non-degraded Sample-A with different gate biasing voltages.](image)

**Figure 4.21.** On-state impedance frequency response of the non-degraded Sample-A with different gate biasing voltages.

<table>
<thead>
<tr>
<th>$V_{GS}$ (V)</th>
<th>$R_{\text{ds(on)}}$ (mΩ) @ 1A, Room Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Calculated from DC Measurement</td>
</tr>
<tr>
<td>20</td>
<td>67.3</td>
</tr>
<tr>
<td>17.5</td>
<td>72.9</td>
</tr>
<tr>
<td>15</td>
<td>80.2</td>
</tr>
<tr>
<td>12.5</td>
<td>92.4</td>
</tr>
<tr>
<td>10</td>
<td>120.5</td>
</tr>
<tr>
<td>7.5</td>
<td>225.3</td>
</tr>
</tbody>
</table>
4.5 Summary

Based on inductive coupling approach, a nonintrusive measurement method for the diagnosis of a SiC power MOSFET’s health status under its on-state operating condition has been described and validated. Unlike time-domain based methods, where the measured waveforms can be influenced by system noise, the proposed method allow us to ensure sufficient signal-to-noise ratio (SNR) in each test signal frequency by adjusting the injecting signal’s amplitude. Also, the inductive effects of routing connections can be de-embedded in the proposed method. The proposed method has the ability to detect degradation that is not easily noticeable from the changes in time-domain waveforms, such as bond wire damage. The proposed method does not require direct electrical contact with the power device to be measured and therefore eliminates the safety hazards if the power device operates at very high voltage. The highly compact inductive probes with very small aperture size make the proposed method easily implementable with very little space. Using a selected power MOSFET as the test sample, it has demonstrated that by observing the impedance frequency response at both low and high frequencies, it is able to identify causes of on-state impedance variation, such as aging, damaged bond wires, etc., which have direct impact on the reliability of a power conversion system. Hence, the proposed method can be a useful mean for reliability and failure analyses.
Chapter 5

JUNCTION TEMPERATURE ESTIMATION METHOD

Keeping the operating junction temperature of a SiC MOSFET within safe and tolerable range is vital not only for safety reasons, but also for extending the device’s life span as thermal transient has a direct impact on device aging. Conventional methods use thermal sensors for temperature monitoring, but these sensors require extra space. Response time and fabrication effort are both concerns when choosing a thermal sensor. In this chapter, a temperature sensor-less method for junction temperature estimation that based on device’s saturation current measurement is proposed. The proposed method is demonstrated with the discrete SiC power MOSFET, P/N: C2M0080120D, Cree Inc., on both clamped inductive load configuration and a boost converter.

5.1 Importance and Challenges of Junction Temperature Estimation

Junction temperature information is essential in two aspects: 1) device overheating prevention, and 2) calculation and interpretation of aging indicators for degradation diagnosis purpose.

Device overheating prevention  Power conversion systems are often exposed to severe ambient conditions where the intensive thermal stresses threaten the reliability of power devices. The operating environment temperature may exceed 150 °C in some high reliability demand applications, such as aerospace systems, electric vehicles and traction systems. To ensure a reliable operation, junction temperature must be considered during the design stage and well-controlled while in operation. Overheating prevention protects power devices from prolonged temperature condition that exceeds
safe limit, which leads to device destruction and consequently, system failure.

Degradation diagnosis purpose The variations of classical on-state aging indicators and switching characteristics are results of the collective effects of different operating conditions, device degradation and junction temperature change. Junction temperature information helps to better identify failures from aging indicators. Besides, junction temperature is essential for the calculation of thermal impedance, which is one of the most important thermal performance metrics.

It is difficult to measure junction temperature through direct access to the die in practical operation. Although it is possible to fabricate PN diode on-chip as an embedded temperature sensor, such sensor occupies the chip’s active area and compromises the device’s current carrying capability. To prevent over-temperature failure, power modules often have thermal sensors mounted on base plate near to the die for junction temperature measurement such as negative temperature coefficient (NTC) thermistor [78]. The monitored temperature is an averaged result over the attached surface, and the measurement accuracy depends greatly on the sensors’ position. Such sensors, however, exhibit relatively slow response time and are inadequate for degradation diagnosis purpose as aging indicators are correlated with operating conditions, i.e., transient temperature is of interest rather than steady-state temperature. Temperature-sensing diode that fabricated on chip surface [79] provides fast response time, however, it requires extra fabrication efforts. Given these shortcomings of thermal sensors, there are numerous studies utilizing analytical electrothermal models and measurable temperature sensitive electrical parameters for junction temperature estimation, as they are theoretically capable of estimating instantaneous junction temperature. Since most of these parameters are varied with degradation, the estimates
are not valid throughout the life span of a power device. In short, a universal approach for junction temperature estimation at operating condition is still lacking and remaining as one of the most challenging tasks of degradation diagnosis.

5.2 Current Status of Junction Temperature Estimation

Electrothermal models, i.e. $R_{th}C_{th}$ networks as reviewed in Chapter 2.3, are widely used for real-time junction temperature calculation in industrial applications. This is attributed to the accessible loss and thermal data given in semiconductor datasheet. Today, several semiconductor manufacturers have provided software tools for power loss and junction temperature simulation, such as Infineon’s IPOSIM [80], Semikron’s SemiSel [81] and Mitsubishi’s MELCOSIM [82]. As the data presented in datasheet are generic, where worst case is often considered, the calculated temperatures are typically higher than actual ones.

Reference [83] evaluates the accuracy of electrothermal-model-based method for junction temperature estimation. It shows that even with precise power loss measurement, the estimated junction temperature still has error close to ±20%. The accuracy of $R_{th}C_{th}$ network can be improved by constructing Cauer-model with detailed geometries and properties of the constituent materials. However, the calculation is affected by temperature as the key material properties – thermal conductivity and specific heat, are temperature sensitive [84]. Another common practice is to build Foster-model for individual devices by offline characterization where temperature and power dissipation are well-controlled. Further improvement can be made by accounting aging effects through dynamic update of thermal models [31], [85]–[86].

The efforts required for accurate electrothermal model development, as well as the difficulty of precise operating power loss measurement facilitate the study of alternative methods. There are a great number of published works dedicated on junction
temperature estimation via electrical temperature sensitive parameters. As additional measurement circuits and control strategies are usually involved, this kind of methods are still limited to laboratory-level demonstration and phenomena description.

Both static and switching electrical parameters have been studied for junction temperature estimation. Reference [87] presents a broad overview of real-time junction temperature estimation methods, including on-state voltage, threshold voltage, short-circuit current, turn-on/turn-off delay and device current slope during turn-on. On-state voltage is widely accepted for IGBTs’ junction temperature estimation. It has been demonstrated as a robust junction temperature estimator in [88]. However, the study has not considered aging effects. Due to the load dependency of on-state voltage, device current information is required in online implementation. The influence of interconnection parasitics can be magnified if the on-state voltage is measured at high current condition. Reference [89] describes solutions to cancel out the effects of parasitics by subtracting two on-state voltages that measured at different gate biasing voltages or device currents. However, the newly defined parameters exhibit only a few mV sensitivities, which are challenging for online measurement.

Similar to on-state voltage, on-state resistance is a classic junction temperature estimator for power MOSFETs, which is load dependent [90]. As SiC MOSFETs are less temperature sensitive compared to Si devices [91] due to the wide-bandgap nature, measurement of SiC MOSFETs’ on-state resistance is a more challenging task. For example, the temperature sensitivity of the on-state resistance of a commercially available 1.2 kV/36 A SiC MOSFET from Cree Inc. is around 0.5 mΩ/°C [90]. Such low sensitivity implies that any slight measurement error can lead to misleading information.

Adopting switching characteristics for junction temperature estimation is attractive
due to the potential of integrating the measurement circuits with gate driver. Switching characteristics, however, are easily affected by operating variables and interconnection conditions. Besides, these parameters present low temperature sensitivities. In [92], the gate turn-off delay time of a 1.2 kV/300 A power module has 3.35 ns/°C sensitivity; and for a 3.3 kV/1.5 kA power module, only 0.8 ns/°C is observed. Reference [93] shows that the normalized device current switching rate during turn-on is less than 0.0015/°C for a 42 A SiC MOSFET. The results have shown poor linearity. Besides, the sensitivity is reduced for devices with smaller current rating and lower gate resistance. The turn-on delay evaluated in [94] have shown ≈ 2 ns/°C sensitivity. These results indicate that measurement circuits with high resolution and large bandwidth are musts.

Recently, internal gate resistance has been reported as a junction temperature estimator, which can be extracted through the measurement of the peak voltage across the external gate resistor [95]. The results show good linearity and load independence, with sensitivity below 3 mΩ/°C. The temperature sensitivity is uncertain for different devices, as gate resistance is affected by doping profile during the fabrication process.

One of the general concerns of using electrical temperature sensitive parameters is the need for calibration, where the variation of the selected parameter over temperature is determined prior to temperature estimation. Due to process variation, calibration for individual devices in the system under monitor is required for accurate estimation. The complexity of calibration procedure and additional measurement circuits, together with the robustness of the selected temperature sensitive parameter subject to device degradation, will be the decisive factors for the possible realization in practical implementations.

5.3 Intrinsic Temperature Dependences in SiC Power MOSFET

Temperature has a direct impact on semiconductor’s fundamental properties. This
section provides information of intrinsic temperature dependences of semiconductor that affect static and switching characteristics of a power MOSFET. Since threshold voltage is potentially useful for junction temperature estimation for it is independent of load variation and is free from package degradation, an overview of prior works on threshold voltage monitoring will be given in this section.

5.3.1 Fundamental Properties

The temperature dependences of the on-state resistance and the threshold voltage of a power MOSFET arise majorly from the temperature effects on bandgap energy, carrier mobility and intrinsic carrier concentration of the material. The measured on-state resistance is the total of the channel resistance \( R_{ch} \), the drift region resistance \( R_{drift} \) and the minor resistances from accumulation region, JFET region and contacts \( R_m \). The temperature effect is dominated by the channel and drift region carrier mobilities \( \mu_{ch} \) and \( \mu_{drift} \) as described by:

\[
R_{dson} = R_{ch} + R_{drift} + R_m = \frac{1}{\mu_{ch}C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{th})} + \frac{W_D}{\mu_{drift}qAN_D} + R_m
\]  

(5.1)

where \( C_{ox} \) is the unit gate oxide capacitance, \( W \) and \( L \) are the channel width and length, respectively, \( W_D \) is the drift region width, \( q \) is the elementary charge, \( A \) is the device active area and \( N_D \) is the doping concentration of the drift region [96]. As temperature elevates, \( \mu_{drift} \) reduces due to scattering effects; while \( \mu_{ch} \) can be improved in SiC MOSFET because of the reduced interface traps [97]. The opposite interaction leads to possible nonlinear temperature dependence of the \( R_{dson} \). The temperature sensitivity of the \( R_{dson} \) is associated with how dominant the channel and drift region resistances are. Generally speaking, the drift region resistance becomes more significant for devices
with a breakdown voltage higher than 100 V [98]. For high-voltage devices where the drift region resistance dominates the overall $R_{ds}$, a more positive temperature sensitivity can be observed compared to low-voltage devices, where the channel resistance has a greater share of the total $R_{ds}$. Device structure has an influence on the temperature sensitivity of the $R_{ds}$ as well. It has been shown in [99] that with the same high breakdown voltage, the $R_{ds}$ of the device with trench structure has a lower temperature sensitivity compared to the device with planar structure. This could be due to the proportion of the channel resistance in the overall $R_{ds}$ increases, because of the device with trench structure has a lower $R_{ds}$ compared to the device with planar structure owing to the absence of the JFET region.

Threshold voltage is the gate-to-source voltage required to induce strong inversion in the channel. It has to against 1) the voltage potential for sustaining the no charge condition between oxide–semiconductor interface (flat band voltage), 2) bulk potential, 3) the depletion layer charges, and 4) voltage due to oxide charges. Its temperature dependence is dominated by 2) and 3), as described as follows:

$$V_{th} = V_{FB} + \frac{\sqrt{4\varepsilon_{SiC}kTN_A\ln\left(\frac{N_A}{n_i}\right)}}{C_{ox}} + \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) - \frac{Q_{ox}}{C_{ox}}$$  \hspace{1cm} (5.2)

where $V_{FB}$ is the flat band voltage, $\varepsilon_{SiC}$ is the dielectric constant of SiC, $k$ is Boltzmann’s constant, $T$ is the absolute temperature, $Q_{ox}$ is the effective oxide charge, $C_{ox}$ is the gate oxide capacitance, $N_A$ is the doping concentration of p-well and $n_i$ is the intrinsic carrier concentration, which has a strong positive temperature dependency [98]. An approximately linear negative temperature dependence of threshold voltage has been well acknowledged in past studies.

The temperature dependences of a power MOSFET’s switching characteristics are results of the interaction between the threshold voltage, the carrier mobility, as well as
the internal capacitances, which are influenced by depletion region capacitance. Depletion capacitance is inversely proportional to the width of the depletion region, which is related to the doping concentration. For the depletion capacitance between the n-type drift layer and the p-base region, the depletion width is related to the built-in junction potential as well, which is a function of the temperature dependent parameter – intrinsic carrier concentration of the semiconductor. The temperature dependences of the parasitic capacitances are typically neglected in actual practice, however, it has been considered in some studies. For examples, in [96], the temperature dependence of the built-in junction potential is included in the parasitic capacitance model to characterize the transient behaviour of a power MOSFET; in [92], the positive temperature dependence of the gate turn-off delay time is attributed to the increasing depletion capacitance due to the temperature effect on carrier concentration. Past studies have proven the positive temperature dependence of the drain current switching rate $dI_d/dt$ [100] and the negative temperature dependence of the voltage switching rate $dV_{CE}/dt$ [44]. In general, measuring the switching characteristics of SiC power MOSFETs are challenging due to the faster switching nature compared to Si-based devices.

5.3.2 Prior Works on Threshold Voltage Monitoring

The most common practice for measuring threshold voltage is the constant current method. A small constant current, typically a few mA, is applied to a power device in diode-connected configuration, where drain and gate terminals are connected. The resulting gate-to-source voltage is defined as the threshold voltage. This is the simplest method that generally adopted for datasheet characterization, yet the usage is limited to offline implementation.

Past studies have put efforts into making threshold voltage measurement online by capturing gate-to-source voltage when device current is zero during turn-on transition.
This method, however, requires continuous sampling and high-speed measurement circuits [101]. Otherwise, the switching time has to be extended with large external gate resistor [86]. Since the exact point of current rise from zero is desired, the measurement is susceptible to noise.

To reduce the effort needed in finding zero current, some studies utilized the voltage across the stray inductance of source terminal as a flag of the onset of current flow [102]– [104]. This concept is similar to the device current measurement method described in Figure 2.4 (c), where a voltage proportional to the rate of current change \( \frac{dI}{dt} \) is generated across the stray inductance between the power source and Kelvin source terminals \( (V_{SS}) \). When a pre-set voltage level is detected, the corresponding gate-to-source voltage is sampled as threshold voltage. The method requires the availability of auxiliary Kelvin source contact. Also, the measurement can be affected by wiring degradation, as it gives rise to higher stray inductance, which induces larger \( V_{SS'} \) and therefore, the time instance of the onset of device current flow can be detected earlier and the corresponding threshold voltage is expected to be lower compared to wiring-degradation-free condition.

5.4 Proposed Method for Junction Temperature Monitoring

In view of the measurement difficulties involved in existing methods, a new solution to mitigate the aforementioned measurement error and the measurement circuits’ bandwidth requirement is proposed and validated in this chapter. With device current measurement only, the saturation current can be obtained with ease and by itself a temperature estimator. The temperature dependence of the square root of the saturation current is identified to have high linearity. Furthermore, the threshold voltage can be extracted for junction temperature estimation.
5.4.1 Principle

During the turn-on process of a SiC power MOSFET, it always goes through saturation region before fully turn-on, where resistive behaviour is observed. The clamped inductive load configuration shown in Figure 3.10 (a) is a good way to investigate the turn-on process of a power device. Since most of the real-world applications contained mainly inductive load, the load inductor is simplified to a constant current source. Thus, the full load current is drawn as constant in Figure 5.1. Figure 5.1 shows the typical turn-on waveforms of a SiC power MOSFET with gate-to-source voltage \( V_{GS}(t) \), device current \( I_d(t) \) and drain-to-source voltage \( V_{DS}(t) \) shown. The turn-on process comprises of four phases:

*Phase A:* The gate-to-source capacitor is charged, and \( V_{GS}(t) \) increases gradually from the nominal turn-off voltage (\( V_{GS,off} \)) to the threshold voltage (\( V_{th} \)). The power device is at off-state. No current flows through the device, while \( V_{DS}(t) \) remains at off-state voltage \( V_{DC} \).

*Phase B:* The power device starts to turn on as \( V_{GS}(t) > V_{th} \). The device current begins to flow and rises from zero to the full load current. The freewheeling body diode of the high-side power MOSFET forces \( V_{DS}(t) \) to remain unchanged until the power device carries the full load current. \( V_{GS}(t) \) continues to increase to the so-called Miller plateau voltage \( V_p \) at the end of this phase.

*Phase C:* This phase is commonly known as Miller plateau period. During this phase, \( V_{DS}(t) \) starts to decrease all the way to the on-state voltage (\( V_{DS,on} \)) of the power device. The drastic drain voltage change leads to the charge change in the gate-to-drain capacitor from negative to positive, which has to be accommodated by the gate drive current. A plateau-like region is therefore
created. If all the gate driving current is diverted to charge the gate-to-drain capacitor, a flat waveform of \( V_{GS}(t) \) will be observed.

**Phase D:** The gate drive current continues to charge the gate-to-source capacitor to the nominal fully turn-on voltage \( (V_{GS, on}) \). \( V_{DS}(t) \) reaches the minimum on-state voltage, where \( V_{DS}(t) = I_{load}R_{ds(on)} \).

The saturation region is the portion where \( V_{th} < V_{GS}(t) < (V_{DS}(t) + V_{th}) \), which incorporates phase B and part of phase C, as the shaded area marked in Figure 5.1. Since the SiC MOSFET is operating at full load current during phase C, the proposed method will utilize the device current during phase B to avoid excessive switching loss.

![Diagram](image)

**Figure 5.1.** Turn-on timing of SiC MOSFET. As \( V_{GS}(t) \) increases from the nominal turn-off voltage \( (V_{GS, off}) \) to the turn-on voltage \( (V_{GS, on}) \), \( I_{d}(t) \) changes from zero to the full load current \( (I_{load}) \). At the same time, \( V_{DS}(t) \) drops from \( V_{DC} \) to the on-state voltage \( (V_{DS, on}) \) of the SiC MOSFET.

The device current during saturation region is temperature dependent, which can be expressed by equation (5.3) [105]:

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\[ I_{d,sat}(T) = \frac{\mu(T)C_{ox}Z}{2L} \left[ V_{GS} - V_{th}(T) \right]^2 \left( \frac{L}{L - \Delta L} \right) \] (5.3)

where constants \( \mu, Z, C_{ox}, L, \Delta L, \) and \( T \) are the carrier mobility, the length of active area in vertical dimension defined for device with vertical structure, unit gate oxide capacitance, channel length, the channel length reduction due to depletion, which is subject to increasing drain-to-source voltage, and temperature, respectively. The channel length reduction phenomenon is known as channel length modulation. It is worth noting that channel length modulation has a stronger impact on submicron and deep-submicron lateral MOSFETs than vertical power MOSFETs. However, the effect has been considered in literatures, especially those involved in device modeling [98, 106]. Channel length modulation effect may be attenuated when a large drain-to-source voltage is applied to a vertical power MOSFET. This is due to a large portion of the voltage is sustained by the drift region and only a fraction of the voltage is across the device channel. To have a generic expression of the device saturation current, \( \Delta L \) term is included in equation (5.3).

The quadratic term in equation (5.3) implies that the temperature dependence of \( I_{d,sat} \) exhibits some non-linearity. A linear temperature dependence can be found by taking the square root of the saturation current \( \sqrt{I_{d,sat}(T)} \), as given by

\[ \sqrt{I_{d,sat}(T)} = k\sqrt{\mu(T)}[V_{GS} - V_{th}(T)] \] (5.4)

where \( k = \sqrt{\frac{C_{ox}Z}{2L} \left( \frac{L}{L - \Delta L} \right)} \).

Since the device is not fully turned on, the temperature effect on carrier mobility can be neglected, as compared to the temperature effect on threshold voltage [93]. Thus, the temperature dependence of \( \sqrt{I_{d,sat}(T)} \) is dominated by \( [V_{GS} - V_{th}(T)] \), and is expected
to have linear increments as temperature rises due to the approximately linear negative temperature dependence of threshold voltage.

Threshold voltage can be extracted with two sets of saturation current $I_{d1}$ and $I_{d2}$ that biasing with known gate-to-source voltage $V_{GS1}$ and $V_{GS2}$, respectively. Under the same temperature condition, the terms $\frac{\mu(T)C_{ox}Z}{2L}$ and $\frac{L}{L-\Delta L}$ in equation (5.3) can be eliminated by dividing $I_{d2}$ by $I_{d1}$:

$$\frac{I_{d2}(T)}{I_{d1}(T)} = \frac{[V_{GS2} - V_{th}(T)]^2}{[V_{GS1} - V_{th}(T)]}$$

(5.5)

By solving equation (5.5), the threshold voltage at a specific temperature can be obtained as follows, where $a = \sqrt{\frac{I_{d2}}{I_{d1}}}$.

$$V_{th}(T) = \frac{aV_{GS1} - V_{GS2}}{a - 1}$$

(5.6)

### 5.4.2 Multi-level Gate Control Method

Device saturation current can be obtained by the multi-level gate control method illustrated in Figure 5.2, where $V_{GS}$ is controlled by a test mode enable/disable signal $test_en$. When test mode is enabled ($test_en$ is high), two test voltages ($V_{GS1}$, $V_{GS2}$) will be generated during the saturation region and the corresponding saturation currents can

![Figure 5.2](image_url)

**Figure 5.2.** Multi-level gate control method for saturation current measurement. The Miller plateau period is not drawn here for the ease of illustration.
be obtained \((I_{d1}, I_{d2})\).

Multi-level gate control is achieved by adding a multi-level output (MLO) generation block to the conventional isolated gate driver, as illustrated with the typical clamped inductive load configuration shown in Figure 5.3. The MLO generation block is inserted between nodes A and G of the turn-on gate resistor path so that the minimum change is made on the traditional driving scheme. Three switches, \(S1\) to \(S3\), are controlled by \(test\_ctrl\), \(V_{test\_ctrl}\) and \(V_{adj\_ctrl}\), respectively. Test mode is enabled/disabled by switching \(S1\) off/on. During normal operation where junction temperature monitoring is disabled, \(V_{GS}\) is supplied by the conventional gate driver by turning \(S1\) on. When \(V_{th}\) monitoring is desired, test mode is enabled by turning \(S1\) off so that \(V_{GS}\) is supplied by the MLO generation block. \(S2\) is inserted to prevent current shoot-through between the transitions.

**Figure 5.3.** Proposed multi-level gate control circuit for driving a power MOSFET with clamped inductive load configuration.
of \( V_{GS} \) supply. When test mode is enabled, two \( V_{GS} \) levels can be supplied by turning \( S3 \) on and off, as given by

\[
\begin{align*}
V_{GS1} &= V_{ref} - V_s & S3 \text{ OFF} \\
V_{GS2} &= \left(1 + \frac{R1}{R2}\right)V_{ref} - V_s & S3 \text{ ON}
\end{align*}
\] (5.7)

Detailed operation is illustrated in Figure 5.4, where \( PWM \) is a double pulse for gate control in a clamped inductive load testing. The SiC MOSFET is switched normally between nominal \( V_{GS,\text{on}} \) and \( V_{GS,\text{off}} \) when test mode is disabled (\( test\_ctrl \) is low). When test mode is enabled (\( test\_ctrl \) is high) while \( S2 \) is not turned on yet (\( V_{test\_ctrl} \) is low), \( V_{GS} \) is slowly pulled to \( AVSS \) through resistor \( R_{GS} \). Then, \( V_{GS} \) is set to \( V_{GS1} \) by turning \( S2 \) on (\( V_{test\_ctrl} \) is high) while \( S3 \) remains off (\( V_{adj\_ctrl} \) is low), and the corresponding device current \( I_{d1} \) is recorded. Finally, \( V_{GS} \) is set to \( V_{GS2} \) by turning \( S3 \) on (\( V_{adj\_ctrl} \) is high) to capture another saturation current \( I_{d2} \). The normal operation can be resumed once the settled current information is captured. All the switches in the MLO generation block should not switch at the same time to avoid current shoot-through.

![Figure 5.4](image)

**Figure 5.4.** Timing diagram of the multi-level gate control method. Test mode is enabled when \( test\_ctrl \) is high. Switches \( S2 \) and \( S3 \) in Figure 5.3 are turned on when the corresponding control signals are high.
With the measured saturation current, the $V_{th}$ at a preset temperature can be obtained by equation (5.6) with the two sets of $V_{GS}$ described in equation (5.7). For timing-critical applications, the two-step gate control can be reduced to one-step, either $I_{d,sat}$ or $\sqrt{I_{d,sat}}$ can be adopted as temperature estimator.

5.4.3 Experimental Validation

The multi-level gate control method is validated by clamped inductive load testing, which emulates the switching operation of a SiC MOSFET. Figure 5.5 shows the measurement setup based on the schematic shown in Figure 5.3. A discrete SiC power MOSFET $M_{SiC}$ (C2M0080120D, Cree Inc.) is fixed on top of a heatsink and the temperature is controlled by placing it on a hotplate (UC150, Stuart). The preset temperature is read by an analog temperature sensor (LMT86, Texas Instruments), which is placed adjacent to $M_{SiC}$. A 246 μH inductor is chosen as the inductive load ($L_{load}$), and a SiC Schottky diode (C4D20120A, Cree Inc.) is used as the freewheeling diode ($D_H$). The MLO generation block and conventional gate driver are designed on separated printed circuit boards (PCBs) for flexibility.

![Figure 5.5. Measurement setup for the validation of the multi-level gate control method. Left: overall view. Right: side view.](image)
The device current is measured by a Rogowski coil (CWTMini HF06B, *PEM*) with sensitivity of 50 mV/A. The measured current can be either observed by an oscilloscope or processed directly by data acquisition system. Oscilloscope (MDO4104B-3, *Tektronix*) is adopted here for demonstration purpose.

The two test voltages $V_{GS1}$ and $V_{GS2}$ are designed to meet saturation region criteria. It is desired to have gate-to-source voltage slightly higher than threshold voltage to avoid excessive switching loss. Here, $V_{GS1}$ and $V_{GS2}$ are designed to be 3.86 V and 4.68 V, respectively. Figure 5.6 shows the double pulse testing waveforms at room temperature. For the ease of observation, the timing periods of $V_{GS1}$ and $V_{GS2}$ are set to be relatively longer than the time required for current to settle. It can be observed that the actual current settling time is around 3 μs. In practical applications, device temperature can be estimated as long as the current settling time is well covered by clock duty time. For example, the current settling time can be sufficiently covered by a clock with switching frequency up to 50 kHz with 50% duty cycle.

![Figure 5.6. Double pulse testing waveforms of the multi-level gate control method at room temperature. (Top to bottom: drain-to-source voltage $V_{DS}$, gate-to-source voltage $V_{GS}$, output of the Rogowski coil with sensitivity of 50 mV/A.)](image-url)
Next, the threshold voltage at different temperature settings are measured. The junction temperature of $M_{SiC}$ is set by adjusting the hotplate temperature. Double pulse testing is performed at least 30 minutes after the temperature is set to allow $M_{SiC}$ to reach thermal equilibrium where the junction temperature can be assumed to be reached that of the hotplate. Soft turn-on is designed in the MLO generation block to avoid drastic current change for fast settling. In this demonstration, current data is obtained by averaging 5,000 data points captured by the oscilloscope right before $V_{GS}$ transitions as indicated by the black bars in Figure 5.6. Five measurements are taken to average out the random error contributed by the oscilloscope. The calculated $V_{th}$ of the five measurements are shown in Figure 5.7. The mean threshold voltages are plotted in Figure 5.8 together with the $V_{th}$ extracted from datasheet [70]. Both curves show similar negative temperature dependency. The temperature sensitivity of the measured data shows close agreement with the datasheet.

![Graph](image)

**Figure 5.7.** $V_{th}$ obtained from the proposed multi-level gate control method.

It can be observed that the $V_{th}$ measured by the proposed method are higher than those obtained from datasheet, which are characterized by the constant current method with $V_{DS} = V_{GS}$ and $I_d = 5$ mA. To gain a further insight, both the proposed method and
constant current method are simulated with the generic SPICE model of C2M0080120D provided by manufacturer. The simulated threshold voltages of both methods are plotted together in Figure 5.9. The same temperature sensitivity is observed, where the proposed method shows apparently higher $V_{th}$ compared to the constant current method.

![Figure 5.8](image)

**Figure 5.8.** Mean $V_{th}$ of the five measurements shown in Figure 5.7, linear fit of the measurement data and the $V_{th}$ extracted from datasheet.

![Figure 5.9](image)

**Figure 5.9.** Simulated threshold voltages with the proposed method and constant current method ($I_d = 5$ mA), respectively.

For further analysis, considering that $V_{th}$ is defined as the applied $V_{GS}$ when the strong inversion layer starts to form in the channel, where the channel diffusion current equals
to drift current. Since diffusion current dominates when $V_{GS} < V_{th}$ and it exhibits an exponential dependence on $V_{GS}$, a linear behaviour can be identified by taking the natural logarithm of the device current as a function of $V_{GS}$. The upper side of Figure 5.10 shows the simulated $V_{GS}$ dependence of $I_d$ at 25 °C, where drain-to-source voltage is fixed at 50 V, together with $\ln(I_d)$. Before $I_d$ has a significant rise from zero, a linear behaviour of $\ln(I_d)$ is identified, which follows by a slope transition. $V_{th}$ is the corresponding $V_{GS}$ of the transition point, which can be found by taking the second derivative of $\ln(I_d)$, as plotted at the lower side of Figure 5.10 and is found to be 3.4 V. The result is higher than the simulated $V_{th}$ with the constant current method at the same temperature, which is 2.69 V. It implies that the diode-connected configuration is likely to be operated at weak inversion region, which gives an explanation to the observation.

![Figure 5.10. Simulated device current $I_d$ versus $V_{GS}$ of C2M0080120D, $\ln(I_d)$ and the second derivative of $\ln(I_d)$.](image)

Figure 5.11 shows the temperature dependence of the measured square root of the saturation current. All five measurements of $\sqrt{I_{d1}}$ and $\sqrt{I_{d2}}$ have shown excellent linearity. The mean data are summarized in Figure 5.12. The good linearity suggests the promising applicability for effective temperature monitoring.

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Figure 5.11. Measured $\sqrt{I_{d1}}$ at $V_{GS} = 3.86$ V (upper) and $\sqrt{I_{d2}}$ at $V_{GS} = 4.68$ V (lower).

Figure 5.12. Averaged square root of the saturation currents of the five measurements of $\sqrt{I_{d1}}$ and $\sqrt{I_{d2}}$. 
5.5 Junction Temperature Monitoring on a Boost Converter

To evaluate the online monitoring potential of the proposed method, a boost converter with continuous-conduction mode (CCM) operation is built based on the schematic shown in Figure 5.13, with $L = 0.5$ mH, $C_{load} = 100$ μF and $R_{load} = 10$ Ω. A SiC MOSFET (P/N: C2M0080120D) and a SiC Schottky diode (P/N: C4D20120A) are adopted as $M_{SiC}$ and $D_s$, respectively. The device current $I_d$ equals to the inductor current $I_L$ when $M_{SiC}$ is switched on. The average inductor current $I_{L,avg}$ is determined by the average load current $I_{load,avg}$ and duty cycle $D$, as given by

$$I_{L,avg} = \frac{2I_{load,avg}}{1 - D} \quad (5.8)$$

The actual implementation of the boost converter for online junction temperature monitoring is shown in Figure 5.14. A heatsink with $M_{SiC}$ fixed on top of it is placing on the hotplate surface, where the environmental thermal effect is emulated by controlling the hotplate temperature. An analog temperature sensor (LMT70, Texas Instruments) is attached to the heatsink surface in adjacent to $M_{SiC}$ for heatsink temperature measurement.

![Figure 5.13. Boost converter for online junction temperature monitoring demonstration.](image)
Essentially, the temperature dependence of saturation current contains the temperature dependence of threshold voltage. Compared to threshold voltage, estimating junction temperature based on saturation current information offers two advantages: 1) Shorten the test time required; 2) Reduce the complexity of the calibration process. On these accounts, junction temperature monitoring is achieved by one-step gate control in this demonstration.

5.5.1 Calibration of the Temperature Dependence of Saturation Current

Prior to the online junction temperature monitoring is performed, the $T_j-I_{d,sat}$ relationship of the device under monitoring has to be established. The process is typically referred as “calibration”, which can be done by transfer characteristics measurement with an $I-V$ curve tracer. Figure 5.15 shows the device current as a function of $V_{GS}$ at various temperatures measured by an $I-V$ curve tracer (Tektronix 371A). Based on the measurement, the saturation current dependence of junction temperature at any given $V_{GS}$ can be obtained and modeled by least-square polynomial fit, as given by
\[ T_j = \sum_{i=0}^{n} p_i I_{d,sat}^i \]  

(5.9)

where \( n \) is the degree of the polynomial, and \( p_i \) is the fitting coefficient.

Figure 5.16 summarizes the saturation current dependence of \( T_j \) at the designed \( V_{GS} \), where the hollow dots are obtained based on the \( I-V \) curve tracer measurement, and the solid curve is the corresponding 3\textsuperscript{rd} degree polynomial fit.

Figure 5.16. The saturation current dependence of \( T_j \) at \( V_{GS} = 3.86 \) V.
The measurement-based fitting model can be adopted directly for $T_j$ estimation if the operating drain-to-source voltage $V_{DS}$ is same as that of the calibration process, which is 10 V in this demonstration. However, unlike clamped inductive load configuration, the $V_{DS}$ of a boost converter is varied with the output voltage $V_{out}$, which could affect the saturation current as $V_{DS}$ influences the parameter $\Delta L$ in equation (5.3). The effect is modelled by channel length modulation parameter $\lambda$. By assuming $\Delta L \ll L$, the term $\frac{L}{L-\Delta L}$ in equation (5.3) can be approximated to $(1 + \lambda V_{DS})$, where $\lambda V_{DS} = \frac{\Delta L}{L}$.

The influence of $V_{DS}$ is accounted by substituting $I_{d,sat}$ in equation (5.9) with

$$I_{d,sat} = \left(\frac{1 + \lambda V_{DS,cal}}{1 + \lambda V_{DS,meas}}\right) I_{d,meas}$$  \hspace{1cm} (5.10)

where $V_{DS,cal}$ is the drain-to-source voltage set during the calibration process, $V_{DS,meas}$ and $I_{d,meas}$ are the actual drain-to-source voltage and saturation current measured. The parameter $\lambda$ can be pre-characterized by an $I$-$V$ curve tracer. With known $V_{DS,meas}$, $\lambda$ can be calculated by re-arranging equation (5.10) into

$$\lambda = \frac{k - 1}{V_{DS,meas} - kV_{DS,cal}}$$ \hspace{1cm} (5.11)

where $k = I_{d,meas}/I_{d,sat}$. $I_{d,meas}$ is obtained at the known $V_{DS,meas}$, and with the same $V_{GS}$ and temperature settings as $I_{d,sat}$ that measured at $V_{DS,cal}$. After $\lambda$ is obtained, junction temperature can be estimated at any measured drain-to-source voltage with the following equation:

$$T_j = \sum_{i=0}^{n} p_i \left[ \left(1 + \lambda V_{DS,cal}\right) / \left(1 + \lambda V_{DS,meas}\right) \right]^{i} I_{d,meas}$$  \hspace{1cm} (5.12)

Figure 5.17 illustrates the influence of channel length modulation correction, where the temperature dependence of saturation current measured at $V_{DS} = 10$ V and 15 V,
respectively, with $V_{GS} = 3.5$ V and 4 V are shown. Due to channel length modulation effect, the saturation currents measured at $V_{DS} = 15$V are slightly higher than those measured at the same temperature and $V_{GS}$ settings but with $V_{DS} = 10$ V. Without correction, it will result in overestimation in $T_j$ if the actual operating $V_{DS}$ is higher than 10 V. Based on equation (5.10), the temperature dependences of saturation currents measured at $V_{DS} = 10$ V are corrected to that of $V_{DS} = 15$ V and plotted as dashed lines in Figure 5.17. The results have shown a better match with the measured data.

![Figure 5.17. Influence of channel length modulation correction.](image)

5.5.2 Measurement Results

For the ease of demonstration, test mode is applied to every clock cycle. Figure 5.18 shows the operation waveforms of the boost converter with 20 kHz switching frequency and 40% duty cycle. The average $V_{out}$ is controlled at 18 V. $V_{GS}$ is stepped up from the nominal turn-off voltage to 3.86 V at the beginning of each on-state period, so that the saturation current measurement can be performed every cycle.

Since the duty cycle is fixed, the boost converter will reach a thermal steady-state after $V_{out}$ is stabilized. Figure 5.19 shows the test sequence applied to the boost converter.
After power up, the boost converter is operated at room temperature for > 10 minutes to reach the thermal steady-state, followed by 20 cycles of $I_d$, $V_{DS}$ and heatsink temperature ($T_s$) measurements. Then, the hotplate is turned on to emulate the ambient condition.

**Figure 5.18.** Operation waveforms of the boost converter with online junction temperature monitoring. $I_d$ is measured by a Rogowski coil (CWTMini HF06B, PEM) with sensitivity of 50 mV/A.

**Figure 5.19.** Test sequence for junction temperature monitoring at different emulated ambient conditions.
with high temperature. To let both the hotplate and boost converter to reach their thermal steady-state, a longer operation is allowed before another measurement. The hotplate temperature is changed for a few times to observe the changes of different ambient conditions. Figure 5.20 shows the device current waveforms of one cycle at different $T_s$. As the junction temperature of $M_{SiC}$ increases with the rising hotplate temperature, larger saturation current is observed at higher $T_s$.

![Figure 5.20. Device current waveforms at different heatsink temperatures.](image)

$T_j$ is estimated based on the measured saturation current right before $V_{GS}$ transition to the nominal turn-on voltage, the estimated $T_j$ are shown in Figure 5.21 with small fluctuations observed, which is reasonable as the boost converter has reached its thermal steady-state.

Based on the thermal impedance definition shown in equation (2.15), by choosing heatsink as the reference plane, we can have

$$T_{js}(t) = Z_{th,js}P_{loss}(t)$$

(5.13)

where $T_{js}$ is the junction-to-heatsink temperature, $P_{loss}$ is the power dissipated by $M_{SiC}$, and $Z_{th,js}$ is the thermal impedance between the die and heatsink, which is treated as unchanged as $M_{SiC}$ is assumed to be fault-free during the test process. Since the elevated
junction temperature leads to higher $R_{ds(on)}$ and $P_{loss}$, $T_{js}$ is expected to be higher. This inference is supported by Figure 5.22. The demonstration suggests the potential of applying the proposed method in degradation diagnosis. At a given operating point, the increase in $T_{js}$ can be treated as an early sign of degradation, as both $Z_{th,js}$ and $P_{loss}$ are become higher when degradation occurs.

**Figure 5.21.** Estimated junction temperatures of $M_{SiC}$ at different $T_s$.

**Figure 5.22.** Calculated junction-to-heatsink temperatures of $M_{SiC}$ at different $T_s$ based on the estimated $T_j$ shown in Figure 5.21.
5.5.3 *Comparison with $T_j$ Estimation Using $R_{dson}$*

For further investigation, junction temperature is estimated via $R_{dson}$ measurement and compared to the results based on the proposed method. Firstly, the temperature dependence of $R_{dson}$ is calibrated by an I-V curve tracer. Then, the junction temperature as a function of $R_{dson}$ and device current can be represented by a surface model, as shown in Figure 5.23.

![Figure 5.23. Junction temperature as a function of $R_{dson}$ and device current.](image)

Figure 5.23 shows the measured device current and the on-state voltage measured by the IVM at three different $T_s$ at thermal steady-state, where the input of the boost converter $V_{DC}$ is fixed at 10 V. Larger device current and on-state voltage are observed at higher $T_s$, as expected. $T_j$ is estimated right before $V_{GS}$ transition and after the on-state voltage is stabilized from saturation current and $R_{dson}$, respectively, as indicated on Figure 5.24. Since the timeframe between the two estimation points is relatively short compared to the switching period, the transient thermal impedance is assumed to be small and similar junction temperature is expected, as shown in Figure 5.25. Compared to $R_{dson}$-based method, the proposed method is much less prone to system noise.
Figure 5.24. Measured device current (upper) and on-state voltage (lower) at thermal steady-state.

Figure 5.25. Comparison of the $T_j$ estimated by saturation current and $R_{ds(on)}$. 
5.6 Summary

This chapter proposes a multi-level gate control method that leverages the temperature dependence of device saturation current ($I_{d,sat}$) for SiC MOSFETs’ real-time junction temperature estimation. The merit lies in the simplified measurement process, which requires only device current measurement with relaxed bandwidth requirement, and the successful extraction of threshold voltage ($V_{th}$).

The multi-level gate control circuit can be merged with the conventional gate driver to provide junction temperature monitoring when needed without the disruption of system operation. This method provides flexibility on choosing load-independent temperature estimator from $I_{d,sat}$, $\sqrt{I_{d,sat}}$, and $V_{th}$. The first two estimators have the advantage of a shorter test time, where $\sqrt{I_{d,sat}}$ has shown excellent linear relationship with temperature compared to $I_{d,sat}$. The experiments have demonstrated the feasibility of the proposed method for junction temperature monitoring on a live system. It also suggests the potential of the proposed method to be an aid for the development of future electronic health monitoring (EHM) system.
Chapter 6

CONCLUSION AND FUTURE WORK

6.1 Conclusion

In the era of more electric power conversion systems, reliability enhancement of power electronic converters is crucial for sustaining operation, cost-effective maintenance and catastrophic failure prevention. Power devices are recognized as one of the most failure-prone components in a power electronic converter. By applying degradation diagnosis techniques, incipient faults of power devices can be identified before drastic system destruction.

This thesis presents methods for resolving the challenges of degradation diagnosis for power devices. SiC power MOSFET is adopted for the study due to its promising features for future applications that require high-frequency operation and high-temperature endurability. The main contributions of this thesis are the highlights of the practical challenges of degradation diagnosis and the proposed countermeasures, including:

1. A voltage monitoring circuit with embedded isolation is proposed to relax the data rate bottleneck of the data transmission interface of a degradation monitoring system for high switching rate power converters. Its functionality at 100 kHz switching frequency is validated. With embedded isolation, the measured data is free from the EMI of the switching circuit; also, the system integration effort is reduced as the measured data can be directly processed by digital processors.
2. A nonintrusive measurement method based on the inductive coupling method for offline deterioration diagnosis is proposed to overcome the challenges of identifying the subtle changes associated with degradation in time domain. It has demonstrated that the proposed frequency-domain diagnosis method provides more visible changes for detecting small electrical variations that linked to degradation, which is challenging for conventional time-domain-based methods, as they are easily affected by system’s noise and operating conditions. The proposed method has the flexibility of enhancing the signal-to-noise ratio by adjusting the amplitude of the injected signal.

3. A multi-level gate control method capable of online transient temperature monitoring for power MOSFETs is proposed and validated. The estimated junction temperature is suitable for both over-temperature protection and degradation diagnosis purposes. Compared to existing methods, the measurement effort is minimized. The method has demonstrated its flexibility, fully-integratable feature, and the potential as an aid in the development of future EHM system.

Over the years, various sensing and monitoring techniques have been developed in response to the gaining importance of degradation diagnosis for failure prevention. With the increasing attention on wide-bandgap devices, online diagnosis methods have to accommodate high switching frequency. Overall, further efforts are still in need to improve the robustness and effectiveness of diagnosis methods. The concepts and techniques proposed in this thesis have shown their potential toward effective and reliable diagnosis of power devices’ degradation.
6.2 Future Work

The methods proposed in this thesis have tackled several shortcomings of existing techniques. Besides the works presented, there are several topics worth for further exploration.

1. **Explore online diagnosis methods for systems with high switching rate**

   In Chapter 3.3.3, degradation diagnosis based on on-state resistance is presented at 20 kHz switching rate. As switching rate further increases, capturing meaningful data becomes more difficult. Besides, the cost of measurement circuits is expected to be higher as the bandwidth requirement is more stringent. There are still rooms for further exploration on methods for online diagnosis that may not limited to device level, but system level.

2. **Replace the inductive coupling probes with printed coils on PCB**

   The two current probes for the offline deterioration diagnosis method proposed in Chapter 4 occupied a certain physical space. For the ease of measurement, a standalone and highly compact test fixture will be beneficial. Further works can be carried out to replace the current probes with printed coils on PCB. The possibility of adopting air-core is worth considering as well.

3. **Assess the possibility of online degradation diagnosis based on the inductive coupling approach**

   The proposed degradation diagnosis method based on the inductive coupling approach discussed in Chapter 4 is limited to offline measurement for a single power device. However, owing to its ability to allow measurement without disturbing the operating condition of the device to be measured, the method has the potential for online degradation diagnosis. One of the opportunities is to detect the variation of a system’s overall impedance; the other is to establish a
small signal path for the element of interest. Unlike offline implementation, the influence of varying thermal conditions has to be addressed.

4. **Feasibility assessment of applying the proposed $T_j$ estimation method on IGBTs**

   Although the proposed $T_j$ estimation method is dedicated to power MOSFETs, it is possible to apply this method to IGBTs. As the structure of an IGBT is equivalent to the series connection of a MOSFET and a diode, and the device current exhibits temperature dependence when the device is not fully turn-on. Typically, the device current at saturation region of an IGBT is higher than that of a power MOSFET with the same aspect ratio (channel width over channel length). The test voltage and test sequence will require further optimization to avoid excessive switching loss.

5. **Extend the proposed $T_j$ estimation method to degradation diagnosis**

   With junction temperature information, the integrity of the thermal path from junction to a predefined reference plane can be monitored either by thermal impedance calculation, or by junction-to-reference-plane temperature change at a given operating point. The concept has been discussed in Chapter 5.5.2. It can be further extended to monitor device degradation on a live system.
Appendix

THE MEASURED $ABCD$-PARAMETERS OF $M_{inj}$ AND $M_{rec}$

$M_{inj}$ and $M_{rec}$ are two-port networks formed by clamping the injecting probe and receiving probe, respectively, onto the circuit wiring. The same type of current probe (Tektronix CT6) is adopted for both injecting and receiving probes in the demonstrations presented in Chapter 4. Figure A.1 and A.2 show the measured magnitudes of the $ABCD$-parameters of $M_{inj}$ and $M_{rec}$, respectively.

**Figure A.1.** Magnitudes of the $ABCD$-parameters of $M_{inj}$. 
Figure A.2. Magnitudes of the $ABCD$-parameters of $M_{\text{rec}}$. 
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