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Analysis and Mitigation of Voltage Measurement Errors for Three-Phase Parallel Voltage Source Inverters

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Abstract—In islanded microgrids, distributed generations (DGs) have been increasingly employed through voltage source inverters (VSIs). When multiple VSIs operate in parallel, it is important to properly share the load power among them. This paper reveals that voltage measurement errors may deteriorate the power-sharing performance by injecting both positive- and negative-sequence circulating currents. To solve this problem, a combined feedforward and feedback voltage control scheme is proposed. Specifically, the feedforward control is utilized to attenuate the negative impact caused by voltage measurement errors, while the feedback control is adopted for the harmonic mitigation. One salient advantage is that the proposed control scheme is fully decentralized and hence does not require any communications among DGs. Finally, Hardware-in-loop (HIL) simulation results are provided for verification.

Keywords—islanded microgrids; parallel inverters; droop control; voltage measurement errors.

I. INTRODUCTION

Recently, distributed generations (DGs) are increasingly employed as high-quality power supplies in modern electric power grids. As a consequence, the concept of microgrid is formed when a cluster of DGs are coupled together through voltage source inverters (VSIs). When the main grid is not available, a microgrid can run autonomously in the islanded mode and the grid-forming functionality will be performed by multiple parallel VSIs cooperatively [1]. To fully utilize the VSI capacity and avoid overloads, it is desired that the total load power of an islanded microgrid should be properly shared according to the VSI power ratings.

Inspired by the characteristics of synchronous generators, droop control and virtual synchronous generator control are proposed for the parallel operation of multiple parallel VSIs [2]–[3]. These techniques can achieve a decentralized power sharing by linking the VSI frequency and voltage magnitude with the active and reactive power, respectively. Despite that the active power sharing is always accurate, the reactive, unbalance and harmonic power sharing accuracy cannot be guaranteed due to mismatched grid impedances [4]–[5].

To overcome this defect, virtual impedance controls are widely adopted in the literature [6]–[7]. By feeding the VSI output current to its reference voltage through an impedance transfer function, grid impedances are equivalently modified. As a result, the power-sharing performance is also enhanced. Generally, a successful implementation of virtual impedance would require the voltage controller to accurately track the reference voltage. Such an objective is normally achieved by either employing the resonant controller in the stationary $ab$ frame [8], or the proportional integral (PI) controller in the synchronous $dq$ frame [9].

However, most of the existing works assume that voltage sensor measurements are accurate and precise, which may not hold in practical situations. It is believed that dc offsets and scaling errors will inevitably exist because of imperfect calibrations and component thermal drifts. Previously, the impacts of sensor tolerances have been investigated for the motor drive system [10] and the grid-connected DC/AC inverter [11]. Besides, some compensation schemes are also reported to mitigate the negative impact of measurement errors. [12]–[13]. Nevertheless, when it comes to parallel-VSI systems, it becomes more challenging to compensate sensor measurement errors, as each VSI can only acquire its local measurements.

It is shown in this paper that voltage measurement errors may introduce considerable positive- and negative-sequence circulating currents among parallel VSIs, given that voltage controllers are well designed and can accurately track the VSI output voltages. As affected by this phenomenon, the reactive and unbalance power-sharing performance will be significantly degraded. Although the introduced circulating current can be suppressed by large virtual impedances, the voltage quality at the point of common coupling (PCC) will be compromised [14]. Alternatively, communication-based power-sharing approaches may also deal with this issue [15], whereas the cost issue as well as the reliability issue will arise accordingly.

To solve this problem in a decentralized way, this paper proposes a combined feedback and feedforward voltage control scheme for the operation of parallel VSIs. In specific, the fundamental reactive and unbalanced power sharing are regulated by directly feeding the VSI output current to the PWM modulation block, whereas the harmonic mitigation functionality is performed by incorporating multi-resonant controllers into the feedback voltage control loop. By doing so, the negative impacts of voltage measurement errors can be effectively mitigated. Moreover, the microgrid voltage quality and the load power-sharing performance can also be improved at the same time.

The rest of the paper is organized as follows: Section II analyses the impact of voltage measurement errors. The proposed voltage control scheme is introduced in Section III. Hardware-in-loop (HIL) simulation results from an islanded microgrid with two parallel VSIs are provided in Section IV. Finally, Section V concludes the whole paper.
II. ANALYSIS OF VOLTAGE MEASUREMENT ERRORS

Fig. 1 shows the circuit and control block diagram of a grid-forming voltage source inverter (VSI). \( L_c \) and \( C_r \) are the filter inductance and filter capacitance. \( L_g \) and \( R_g \) represent the grid inductance and resistance, respectively. The overall control scheme contains an outer control loop and an inner control loop. The outer control loop facilitates the power sharing by providing the reference voltage, where \( k_{ref}, k_0, V_0 \) are droop coefficients, nominal voltage magnitudes and frequency, respectively. The inner control loop, on the other hand, adopts the voltage controller \( G(s) \) to eliminate the voltage tracking error. In this paper, \( G(s) \) is implemented as a resonant controller in the \( a\beta \) frame, yet it could also be a proportional-integral (PI) controller in the synchronous \( dq \) frame. In addition to \( G(s) \), virtual impedance control \( Z_v(s) \) is also implemented to improve the reactive, unbalance and harmonic power sharing performance.

Assume that the three-phase reference voltages are well balanced, i.e.:

\[
v_{\text{ref}}(t) = V_f \cos(o t + \phi_0) \quad (1)\\
v_{\text{ref}}(t) = V_f \cos(o t + \phi_0 - 2\pi / 3) \quad (2)\\
v_{\text{ref}}(t) = V_f \cos(o t + \phi_0 + 2\pi / 3) \quad (3)
\]

where \( \phi_0 \) is the initial phase angle. Through the Alpha–Beta transformation, the voltages in the \( a\beta \) frame are derived as:

\[
\begin{bmatrix} v_{\text{ref}}(t) \\ v_{\beta\text{ref}}(t) \end{bmatrix} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ 0 & 1/\sqrt{3} & -1/\sqrt{3} \end{bmatrix} \begin{bmatrix} v_{\alpha\text{ref}}(t) \\ v_{\beta\text{ref}}(t) \end{bmatrix} \quad (4)
\]

\[
v_{\text{ref}}(t) = V_f \cos(o t + \phi_0) \quad (5)\\
v_{\beta\text{ref}}(t) = V_f \sin(o t + \phi_0) \quad (6)
\]

Taking the voltage measurement errors into account, the relationships between the real VSI output voltages and the measured ones are depicted as:

\[
v_{\text{am}}(t) = v_a(t) \cdot (1 + \Delta k_a) + X_{ad} \quad (7)\\
v_{\text{bm}}(t) = v_b(t) \cdot (1 + \Delta k_b) + X_{bd} \quad (8)\\
v_{\text{cm}}(t) = v_c(t) \cdot (1 + \Delta k_c) + X_{cd} \quad (9)
\]

where \( \Delta k_a, \Delta k_b, \) and \( \Delta k_c \) are scaling errors; \( X_{ad}, X_{bd}, \) and \( X_{cd} \) are the DC offsets. \( v_a(t), v_b(t), \) and \( v_c(t) \) represent the real VSI voltages, while \( v_{\text{am}}(t), v_{\text{bm}}(t), \) and \( v_{\text{cm}}(t) \) stand for the measured voltages. Given that the voltage control \( G(s) \) is well designed (can suppress DC offsets and accurately track fundamental voltages in the \( a\beta \) frame), it is clear that:

\[
v_{\text{am}}(j \omega) = v_{\text{ref}}(j \omega) \quad (10)\\
v_{\text{bm}}(j \omega) = v_{\text{ref}}(j \omega) \quad (11)
\]

Meanwhile, since there is no zero-sequence voltage in the system, the sum of three-phase voltages equals zero.

\[
v_a(t) + v_b(t) + v_c(t) = 0 \quad (12)
\]

According to (5)–(12), the real three-phase voltages are calculated and expressed as:

\[
v_a(t) = 2 + \frac{\Delta k_a + \Delta k_b}{\sqrt{3} M} \cdot V_f \cos(o t + \phi_0) + \frac{\Delta k_a - \Delta k_b}{3 M} \cdot V_f \sin(o t + \phi_0) \quad (13)\\
v_b(t) = 3 + \frac{2 \Delta k_a + \Delta k_b}{\sqrt{3} M} \cdot V_f \cos(o t + \phi_0) + \frac{2 \Delta k_a - \Delta k_b}{3 M} \cdot V_f \sin(o t + \phi_0) \quad (14)\\
v_c(t) = 3 + \frac{2 \Delta k_b + \Delta k_c}{\sqrt{3} M} \cdot V_f \cos(o t + \phi_0) + \frac{2 \Delta k_b - \Delta k_c}{3 M} \cdot V_f \sin(o t + \phi_0) 
\]

where:

\[
M = \frac{2 \sqrt{3} + 4 \sqrt{3}}{9} (\Delta k_a + \Delta k_b + \Delta k_c) + \frac{2 \sqrt{3}}{9} (\Delta k_a \Delta k_b + \Delta k_a \Delta k_c + \Delta k_b \Delta k_c) \quad (16)
\]

Based on the method of symmetrical component, the real output three-phase voltages can be expressed as the sum of balanced positive- and negative-sequence voltages:

\[
\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = V_p \begin{bmatrix} \cos(o t + \phi_p) \\ \cos(o t + \phi_p - 2\pi / 3) \\ \cos(o t + \phi_p + 2\pi / 3) \end{bmatrix} + V_n \begin{bmatrix} \cos(o t + \phi_n) \\ \cos(o t + \phi_n - 2\pi / 3) \\ \cos(o t + \phi_n + 2\pi / 3) \end{bmatrix} \quad (17)
\]

where \( V_p \) and \( V_n \) are the magnitudes of the positive- and negative-sequence voltages, respectively. \( \phi_p \) and \( \phi_n \) are the corresponding phase angles. Their values can be calculated as:

\[
V_p = \frac{6 + 2(\Delta k_a + \Delta k_b + \Delta k_c)}{3 \sqrt{3} M} \cdot V_f \quad (18)\\
V_n = \frac{2}{3 \sqrt{3} M} (\Delta k_a^2 + \Delta k_b^2 + \Delta k_c^2 - \Delta k_a \Delta k_b - \Delta k_a \Delta k_c - \Delta k_b \Delta k_c)^{1/2} \cdot V_f 
\]

\[
\phi_p = \phi_0 \quad (20)\\
\phi_n = \phi_0 - \arctan \left[ \frac{\sqrt{3} \Delta k_a - \sqrt{3} \Delta k_b}{\Delta k_b + \Delta k_c - 2 \Delta k_a} \right] \quad (21)
\]
In practical situations when the scaling errors $\Delta k_a$, $\Delta k_b$, and $\Delta k_c$ are not zero, the value of $V_p$ will differ from that of $V_r$. Similarly, the value of $V_n$ is also nonzero. Therefore, extra positive- and negative-sequence voltages are imposed on the ideal reference voltages due to the sensor tolerances. It needs to be emphasized that the imposed voltages are mainly fundamental components, simply because harmonic voltages have quite small magnitudes and can hence be neglected.

Next, multiple parallel VSI scenarios are studied. The system equivalent circuits are established in the positive-sequence domain, i.e., Fig. 2(a) and the negative-sequence domain, i.e., Fig. 2(b), respectively.

![System equivalent circuit. (a) in the positive-sequence domain. (b) in the negative-sequence domain.](image)

Since VSI impedance $Z_o$ and grid impedance $Z_g$ provide little blocking effect at the fundamental frequency, there will be considerable positive-sequence circulating current $i_{cwp}$ and negative-sequence circulating current $i_{con}$, which are calculated as:

\[
i_{cwp} = \frac{V_{p1} - V_{p2}}{Z_{o1} + Z_{o2} + Z_{g1} + Z_{g2}} \tag{22}
\]

\[
i_{con} = \frac{V_{o1} - V_{o2}}{Z_{o1} + Z_{o2} + Z_{g1} + Z_{g2}} \tag{23}
\]

Due to the uncertainty of sensor measurement errors, the imposed extra voltages are unknown and mismatched for different VSIs. Therefore, it would be difficult to eliminate the undesired circulating current, especially when there is no information exchange among multiple VSIs. Note that $i_{cwp}$ is mainly responsible for the inaccurate reactive power sharing, and $i_{con}$ degrades the unbalanced power sharing.

### III. PROPOSED VOLTAGE CONTROL SCHEME

#### A. Proposed Voltage Control Scheme

In order to address the aforementioned issue, a combined feedback and feedforward control scheme is proposed in this paper. Fig. 3 shows the control and circuit block diagram, where $G_{d}(s)$ refers to the digital control system delay. $Z_{l1}(s)$ and $Z_{l2}(s)$ represent the harmonic and fundamental virtual impedances, respectively. Note that the control scheme is implemented in the stationary $a\beta$ frame.

![Proposed voltage control scheme in the $a\beta$ frame.](image)

The voltage controller $G_{c}(s)$ is intentionally designed as:

\[
G_{c}(s) = \sum_{k=5,7,11,13...} \frac{k_h \cdot s}{s^2 + h^2 \omega^2} \tag{24}
\]

At the fundamental frequency, the gain of $G_{c}(s)$ equals:

\[
G_{c}(j\omega) = \sum_{k=5,7,11,13...} \frac{k_h}{(h^2 - 1) \cdot \omega} \tag{25}
\]

which is a quite small value since the denominator is much larger than the nominator. In other words, $G_{c}(s)$ provides a strong blocking effect against the fundamental component, but high open-loop gains at harmonic frequencies.

To better understand the principle of the control scheme, the block diagram shown in Fig. 3 is further decomposed in the frequency domain, which is subsequently illustrated in Fig. 4. In Fig. 4(a), the modulation signal is provided by directly feeding the droop-generated reference voltage $V_{ref}$ as well as the output current $i_o$. Since the feedback loop is equivalently bypassed, voltage sensor measurement errors will have little influence. For such case, the VSI output impedance can be derived as:

\[
Z_{e}(s) = \frac{Z_{l1}(s) + G_{d}(s) \cdot Z_{l2}(s)}{Z_{l1}(s) \cdot Z_{l2}^{-1}(s) + 1 + G_{d}(s) \cdot G_{c}(s)} \tag{26}
\]

At the fundamental frequency, the following conditions are satisfied:

\[
G_{c}(j\omega) = e^{-1.5 \cdot ja_{f}} \approx 1 \tag{27}
\]

\[
G_{d}(j\omega) \ll 1 \tag{28}
\]

\[
Z_{c}(j\omega) \gg Z_{l2}(j\omega) \tag{29}
\]

With these assumptions, (26) can be approximated as:

\[
Z_{e}(j\omega) \approx Z_{l1}(j\omega) + Z_{l2}(j\omega) \tag{30}
\]

From (30), the VSI output impedance can be regarded as a series connection of the filter inductor impedance and the virtual impedance.
At harmonic frequencies, the effect of the feedforward control is overlapped by the feedback control, as illustrated in Fig. 4(b). The VSI harmonic impedances are determined by the virtual impedance transfer function $Z_v(s)$.

### B. Design of Virtual Impedance

To improve the reactive, unbalance, and harmonic power sharing, $Z_3(s)$ and $Z_4(s)$ are designed to be adaptive in this paper. For clarification [16], the unbalance and harmonic powers of a three-phase VSI are defined as:

$$ Q_{un} = \frac{3}{2} V_s \cdot (I_{\alpha N}^2 + I_{\beta N}^2)^{1/2} $$

$$ Q_{har} = \frac{3}{2} V_s \cdot (I_{\alpha 5}^2 + I_{\beta 5}^2 + I_{\alpha 7}^2 + I_{\beta 7}^2 + ...)^{1/2} $$

where $I_{\alpha N}$ and $I_{\beta N}$ are the negative sequence currents, $I_{\alpha h}$ and $I_{\beta h}$ are the harmonic currents. The transfer function of $Z_v(s)$ is designed as:

$$ Z_v(s) = \frac{k}{S_N} Q_{har} $$

where $S_N$ is the VSI power rating, $k$ is a proportional gain, the value of whom should be properly tuned to reach a compromise between the PCC voltage quality as well as the harmonic power sharing accuracy. The detailed design guideline has already been elaborated in [17], and hence not presented in this paper. Suppose that a VSI provides more harmonic power than its opponents, it will have a greater harmonic impedance according to (33). As a result, the harmonic power sharing error is reduced.

On the other hand, $Z_3(s)$ is designed so that the positive-sequence impedance of VSI becomes zero as the reactive power reaches the max allowed value $Q_{max}$, and equals $Z_d$ when there is no reactive power. Similarly, the negative-sequence impedance of VSI is expected to be eliminated when delivering the maximum unbalance power $Q_{un max}$, and become zero when delivering no unbalance power. Fig. 5 illustrates the implementation of the feedforward virtual impedance. It should be mentioned that the positive- and negative-sequence currents can be readily extract through the reduced order generalized integrator (ROGI) [18].

![Control block diagram of the feedforward virtual impedances](image)

**IV. HARDWARE-IN-LOOP (HIL) SIMULATION RESULT**

In order to validate the proposed control scheme, a typical islanded microgrid with two parallel three-phase VSIs was established in Typhoon HIL 602+. Meanwhile, the ADC samplings as well as digital controls were implemented by a dSPACE MicroLabBox. Fig. 6 shows the laboratory setup, and Table I. provides the key system parameters for the simulations.

![Laboratory setup for the HIL simulation](image)

| **TABLE I. SYSTEM PARAMETERS** |
|-----------------------------|--------------------|
| **Descriptions** | **Symbols** | **Values** |
| Dc-link voltage | $V_n$ | 200 V |
| AC voltage magnitude | $V_V$ | 80 V |
| Filter inductor | $L_f$ | 1 mH |
| Filter capacitor | $C_f$ | 15 μF |
| Line inductance of VSI1 | $L_{a1}$ | 1 mH |
| Line inductance of VSI2 | $L_{a2}$ | 1.2 mH |
| Line Resistance of VSI1 | $R_{a1}$ | 0.4 Ω |
| Line Resistance of VSI2 | $R_{a2}$ | 0.5 Ω |

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<th><strong>Measurement errors</strong></th>
<th><strong>Values</strong></th>
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<tr>
<td>Measurement errors (VSI1)</td>
<td>$\Delta V_{a1}$: +1% $X_{a1}$: +2.0 V</td>
</tr>
<tr>
<td>$\Delta k_2$: +0.8% $X_{a2}$: −1.6 V</td>
<td></td>
</tr>
<tr>
<td>$\Delta k_3$: −0.6% $X_{a3}$: −0.4 V</td>
<td></td>
</tr>
<tr>
<td>Measurement errors (VSI2)</td>
<td>$\Delta V_{a1}$: −1.2% $X_{a1}$: −1.0 V</td>
</tr>
<tr>
<td>$\Delta k_2$: +0.2% $X_{a2}$: −1.9 V</td>
<td></td>
</tr>
<tr>
<td>$\Delta k_3$: −0.5% $X_{a3}$: +0.9 V</td>
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In the first scenario, there is only a balanced three-phase load connected to the PCC. A conventional well-designed feedback control scheme is firstly tested, which can eliminate the voltage tracking errors. Fig. 7 shows the VSI current waveforms.

![VSI currents with the conventional scheme](image)

(a) VSI1. (b) VSI2.
In Fig. 7, it can be seen that VSI currents are unbalanced even unbalance loads do not exist in the microgrid. This can happen because of the voltage measurement scaling errors. Ironically, the better tracking ability the voltage controllers have, the worse current unbalance will occur. As a contrast, the proposed combined feedforward and feedback voltage control scheme is also verified, and the results are shown in Fig. 8. It is clear that the undesired circulating currents are effectively attenuated and the fundamental power sharing is improved.

For the next scenario, an unbalanced three-phase load is connected at the PCC, and the VSIs are desired to equally share the unbalance power. Fig. 9 shows the VSI current waveforms with the proposed control scheme. It can be observed that the total negative-sequence current can be properly shared between the two VSIs.

Finally, a three phase diode rectifier is connected at the PCC as a nonlinear load, and the injected harmonic current is also expected to be accurately shared between the parallel VSIs. Fig. 10 shows the VSI voltage and current waveforms with the proposed control scheme. It is clear that harmonic sharing and compensation functionalities are well performed by the feedback control loops that take effect at harmonic frequencies.

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V. CONCLUSIONS

This paper analyses the impacts of voltage measurement errors on parallel-VSI system. It is found out that scaling errors may inject considerable circulating currents if voltage controllers are well designed and can accurately regulate the output voltages. To solve this issue, a combined feedback and feedforward control scheme is proposed and verified by HIL simulation results. The proposed control scheme can effectively reduce the negative effect of measurement errors and is implemented in a fully decentralized manner.

REFERENCES