<table>
<thead>
<tr>
<th><strong>Title</strong></th>
<th>Design and optimization of the extended true single-phase clock-based prescaler (Published)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Author(s)</strong></td>
<td>Yu, Xiao Peng; Do, Manh Anh; Lim, Wei Meng; Yeo, Kiat Seng; Ma, Jianguo</td>
</tr>
<tr>
<td><strong>Date</strong></td>
<td>2006</td>
</tr>
<tr>
<td><strong>URL</strong></td>
<td><a href="http://hdl.handle.net/10220/5950">http://hdl.handle.net/10220/5950</a></td>
</tr>
</tbody>
</table>

IEEE Transactions on Microwave Theory and Techniques © 2006 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE. This material is presented to ensure timely dissemination of scholarly and technical work. Copyright and all rights therein are retained by authors or by other copyright holders. All persons copying this information are expected to adhere to the terms and constraints invoked by each author's copyright. In most cases, these works may not be reposted without the explicit permission of the copyright holder. http://www.ieee.org/portal/site.
Design and Optimization of the Extended True Single-Phase Clock-Based Prescaler

Xiao Peng Yu, Member, IEEE, Manh Anh Do, Senior Member, IEEE, Wei Meng Lim, Kiat Seng Yeo, and Jian-Guo Ma, Senior Member, IEEE

Abstract—The power consumption and operating frequency of the extended true single-phase clock (E-TSPC)-based frequency divider is investigated. The short-circuit power and the switching power in the E-TSPC-based divider are calculated and simulated. A low-power divide-by-2/3 unit of a prescaler is proposed and implemented using a CMOS technology. Compared with the existing design, a 25% reduction of power consumption is achieved. A divide-by-8/9 dual-modulus prescaler implemented with this divide-by-2/3 unit using a 0.18-μm CMOS process is capable of operating up to 4 GHz with a low-power consumption. The prescaler is implemented in low-power high-resolution frequency dividers for wireless local area network applications.

Index Terms—CMOS integrated circuit, D flip-flop (DFF), frequency divider, frequency synthesizer, high-speed digital circuit, phase-locked loops (PLLs), true single-phase clock (TSPC).

I. INTRODUCTION

THE high-speed frequency divider is a key block in frequency synthesis. The prescaler is the most challenging part in the high-speed frequency-divider design because it operates at the highest input frequency. A dual-modulus prescaler usually consists of a divide-by-2/3 (or 4/5) unit followed by several asynchronous divide-by-2 units. The operation of the divide-by-2/3 unit at the highest input frequency makes it the bottleneck of the prescaler design. To achieve the two different division ratios, D flip-flops (DFFs) and additional logic gates, which reduce the operating frequency by introducing an additional propagation delay, are used in the unit. The power consumption of this divide-by-2/3 unit, which is the greatest portion of the total power consumption in the prescaler, significantly increases due to the power consumption of the additional components. In modern wireless communication systems, the power consumption is a key consideration for the longer battery life. The MOS current mode logic (MCML) circuit, which is of high power consumption, is commonly used to achieve the high operating frequency, while a true single-phase clock (TSPC) dynamic circuit, which only consumes power during switching, has a lower operating frequency. In [2], the extended true single-phase clock (E-TSPC) logic is proposed to increase the operating frequency. However, this causes additional power consumption. Moreover, the impacts of the modified topology over the operating frequency and power consumption have not been fully investigated. In this paper, the power consumption and operating frequency in the E-TSPC logic style is evaluated. The two major sources of power consumption, namely, the short-circuit power and the switching power, in the E-TSPC divide-by-2 unit is calculated and simulated. Based on the analysis, a new divide-by-2/3 unit is proposed to achieve the low-power consumption by reducing the switching activities and the short-circuit current in the DFFs of the unit, and a dual-modulus prescaler implemented with the unit is proposed. Finally, the proposed prescalers are implemented in the high-resolution low-power frequency divider.

II. KEY CONSIDERATIONS

The most important parameters of high-speed digital circuits are the operating frequency and power consumption. The operating frequency is decided by the propagation delay. For the pipelined divide-by-2 unit such as the toggled TSPC divide-by-2 unit, the maximum operating frequency is given by [3]}

\[ f_{\text{max}} = \frac{1}{2 \times \max(t_{\text{PLL}}, t_{\text{PHL}})} \]  

(1)

where \( t_{\text{PLL}} \) and \( t_{\text{PHL}} \) are the propagation delays of the low-to-high and high-to-low transitions, respectively.

The power consumption of the CMOS digital circuit is mainly decided by the switching power, which is linearly proportional to the operating frequency [4]. The switching power is given by [4]

\[ P_{\text{switching}} = C_L f_{\text{clk}} V_{dd}^2 \]  

(2)

where \( C_L \), \( f_{\text{clk}} \), and \( V_{dd} \) are the load capacitance, input clock frequency, and supply voltage, respectively. In a static digital CMOS circuit, if the pMOS and nMOS are simultaneously turned on, there will be a direct path from the supply voltage to ground, which introduces the short-circuit power given by [5]

\[ P_{\text{short}} = I_{\text{SC}} V_{dd} \]  

(3)

where \( I_{\text{SC}} \) is the short-circuit current. In the CMOS circuit, only for a very small period within which the pMOS and the nMOS are turned on simultaneously. Thus, the direct path power consumption is considered as negligible in [5]. However, at high frequencies, this short-circuit power consumption can increase significantly.
III. TSPC AND E-TSPC DIVIDE-BY-2 UNIT

A. Propagation Delay

The toggled TSPC DFF is the most popular divide-by-2 unit in the high-speed frequency divider design, while the E-TSPC DFF is proposed to increase the operating frequency. Fig. 1(a) and (b) shows the topology of a TSPC DFF and an E-TSPC DFF, respectively. When performing the divide-by-2 function, the output $S_3$ is fed back to $D$. The operation of divide-by-2 is shown in Fig. 2.

An analysis of propagation delay can be obtained from [4] as the $RC$ delay. The propagation delay of the E-TSPC unit is smaller than that of the TSPC unit because of the reduction of load capacitance. From the method proposed in [4], the manual calculation of the propagation delay for the two units can be obtained. Fig. 3 shows the calculated and simulated propagation delay for the two units using the same MOS transistor’s size. The E-TSPC achieves a higher operating frequency, as reported in [2]. This is based on the schematic level simulation. After layout, the parasitic capacitance cause by interconnection needs to be considered as well. For example, in [1], for a node with a total capacitance of 15 fF, the interconnection may introduce 4.5 fF. This will cause an approximate 20% increase in the propagation delay.

B. Power Consumption

By reducing the load capacitance during charging and discharging, from (2), the switching power consumption can be reduced as well. However, in the E-TSPC unit, there is a period during which a direct path from supply voltage to ground is established in the operation of divide-by-2. The shaded areas in Fig. 2 mark the transition during which the short circuit takes place.

The behavior of the short circuit in a single stage of the E-TSPC DFF is analyzed in Fig. 4. The short-circuit current depends on the aspect ratio $W/L$ of the pMOS and nMOS. Depending on the configuration, the operation region of the pMOS and nMOS can be the triode or saturation region. Fig. 4(b) shows the short-circuit current and the output voltage versus $W_p/W_n$, where $W_p$ and $W_n$ are the widths of the pMOS and nMOS transistors, respectively. If $W_p/W_n \geq \mu_n/\mu_p$, the short-circuit current is decided by the PMOS, and its operation region changes from the triode region to the triode region with the increase of $W_p/W_n$. When $W_p/W_n \leq \mu_n/\mu_p$, with
the increase of $W_p/W_n$, the nMOS shifts from the triode region to the saturation region. $V_{on}$ increases with the increase of $W_p/W_n$ before the nMOS transistor reaches saturation.

As marked in Fig. 2, for all the three stages in the E-TSPC unit, there is a quarter of the period during which the direct path is established from supply to ground. From the above analysis, the two sources of power consumption in the E-TSPC unit exhibit different characteristics. In the E-TSPC unit, the short-circuit current and the power of each stage is decided by the sizes of the MOS transistors only. For the switching power, it is linearly proportional to the input frequency for a fixed size of the MOS transistors. The two types of power consumption can be determined using the process parameters [4]. One stage of the E-TSPC unit, as shown in Fig. 4, is examined. For simplicity, $W_p/W_n$ is 2, as proposed in [6], and the channel length for all the transistors are 0.18 $\mu$m. Here, $W_n$ is 2 $\mu$m. The input signals of Fig. 4 are logically low for the pMOS and logically high for NMOS. For a comparison, an inverter with the same transistor size, but with the input signal as a square wave ranging from 2 to 5 GHz, is also simulated for the power consumption. To evaluate the different switching powers of the E-TSPC and TSPC due to different capacitive loads, the load of one pMOS for the E-TSPC unit and the load of one pMOS plus one nMOS for the TSPC unit are used in the calculation and simulation. Fig. 5 shows the results of the two sources of power consumption in an E-TSPC and a TSPC unit. The E-TSPC unit has a lower switching power. However, its short-circuit power is much larger than the switching power. Within the operating frequency range, the E-TSPC unit has a larger total power consumption than that of the TSPC unit.

### IV. E-TSPC-BASED PRESCALER

The E-TSPC divide-by-2 unit has the merit of high operating frequency compared with the traditional TSPC divide-by-2 unit. In [2], a simplified topology of the divide-by-4/5 unit is proposed to achieve high operating frequency. To make less components work at full speed, a divide-by-2/3 is used in [1]. Since the divide-by-2/3 unit consists of two toggle DFFs and additional logic gates, one way to effectively reduce the delay and power consumption is to integrate the logic gates to the divide-by-2/3 unit [7]. In [1], a gate-integrated dual-modulus prescaler based on the dynamic circuit has been proposed to achieve the high operating frequency and low power consumption. This design uses two DFFs, while the divide-by-4/5 unit in [2] uses three DFFs. The divide-by-2/3 unit in [1] is shown in Fig. 6. When the modulus control signal $MC$ is logically low, it performs the divide-by-3 function. If the output of DFF2 is logically low, the node $S_1$ of DFF2 is disabled, thus nodes $S_2$ and $S_3$ of DFF2 will have no switching activities, therefore, no switching power dissipation. DFF1 operates all the time, while DFF2 only operates when the output of DFF2 is logically high. When $MC$ is logically high, the output of DFF1 will be disabled to achieve the divide-by-2 function. However, the nodes $S_1$ and $S_2$ of DFF1 still have switching activities since the output of DFF2 still feeds back to DFF1. Thus, both DFFs switch at half of the input frequency even if DFF1 does not participate in the divide-by-2 function. As a result, the divide-by-2 unit dissipates more power even only if one toggled DFF is needed. Such a topology introduces unnecessary power consumption, which is a significant part of the total power consumption. Moreover, during a quarter of the period, the short-circuit power still exists in DFF1.

The difficult of low-power design for the divide-by-2/3 unit is to minimize the overall power consumption. During the divide-by-2 operation, it is not necessary for both DFFs to operate at full speed since only one toggled DFF is needed to perform the divide-by-2 function. If only one DFF is active during the divide-by-2 operation, theoretically a 50% reduction of power consumption is achieved. In [1], the output of DFF1 is manually pull down by the $MC$-controlled NMOS, but DFF1 still works at full speed. To reduce the unnecessary power consumption, a new divide-by-2/3 unit, which can effectively block the switching activities and the short circuit, is proposed as shown in Fig. 7. Different from [1], in this topology, two AND gates are used instead of one OR gate and one AND gate, as shown in [7], to achieve a symmetrical architecture. By changing the $MC$-controlled nMOS at the output of DFF1 to an $MC$-controlled PMOS, DFF1 is blocked at the input when $MC$ is high. As a result, nodes $S_1$, $S_2$, and $S_3$ of DFF1, which have the logical

![Fig. 6. Divide-by-2/3 unit in [1].](image-url)
values of “1,” “0,” and “1,” respectively, are blocked. DFF1 only has the short-circuit path in the first stage, while the following stages have no switching activities or short circuits while DFF2 functions as a toggled divide-by-2 unit. Hence, the proposed divide-by-2/3 unit has a significant power-consumption reduction in the divide-by-2 operation. Even for the divide-by-3 operation, due to the complementary logic type, the power consumption is also slightly reduced due to the reduction of short-circuit power consumption in DFF1. To further verify the advantages of this proposed prescaler, a divide-by-8/9 dual-modulus prescaler using the same architecture in [1], but with the proposed divide-by-2/3 unit, is implemented. In this divide-by-8/9 prescaler, the proposed divide-by-2/3 unit is followed by two stages of the toggled TSPC divide-by-2 units. Fig. 8 shows the topology of the prescaler in [1], but with the new divide-by-2/3 unit proposed in Fig. 7.

The power consumption in this prescaler can be determined based on the previous analysis. The power consumption of the divide-by-2/3 unit can be expressed as $2P_{DFF} + 2P_{gate}$, which consists of the power consumption in two DFFs and two logic gates. For the divide-by-3 operation, the proposed unit has a similar power consumption with the unit in [1]. However, for the divide-by-2 operation, the proposed unit has a lower power...
TABLE I
COMPARISON WITH OTHER STUDIES

<table>
<thead>
<tr>
<th>Design Parameters</th>
<th>Work in [1] Resimulated</th>
<th>Work in [1] Measured</th>
<th>This work (Sim/Measured)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process (µm CMOS)</td>
<td>0.25</td>
<td>0.18</td>
<td>0.18</td>
</tr>
<tr>
<td>Supply Voltage (V)</td>
<td>2.5</td>
<td>1.8</td>
<td>1.8</td>
</tr>
<tr>
<td>Max. frequency (GHz)</td>
<td>2.8</td>
<td>4.5/4</td>
<td>4.5/4</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>3.05</td>
<td>3.1/2.9</td>
<td>2.5/3.3</td>
</tr>
</tbody>
</table>

consumption, which is the sum of the power consumption in DFF2 and short circuit in the first stage of DFF1

\[
P_{2/3Pro} = P_{\text{switch-DFF2}} + P_{\text{short-DFF2}} + P_{\text{short-S1-DFF1}}
\]

where \( C_{Li} \) is the load capacitance of the node S1, S2, and S3 and out in DFF2, where the switching frequency is half of the input frequency \( f_{in} \). The load capacitance of these four nodes is given by [4].

The short-circuit power is the average of the short-circuit current times time period. The input signal is a high-frequency sine wave, and the waveforms will deviate from a square signal. This short-circuit current is modeled as a triangle, as shown in [4]. The average of the short-circuit current is half of the peak value. For the following TSPC divide-by-2 unit, the major power is the switching power. The two units operate at \( f_{in}/4 \) and \( f_{in}/8 \) if the prescaler performs divide-by-8. Their power consumption can be determined by the above equations as well. The
major power consumption, switching power in the two units, $P_{\text{switching-DIV2}}$, is given by

$$P_{\text{switching-DIV2}} = \sum_{i=1}^{4} \frac{3C_L f_{\text{in}} V^2_{\text{dd}}}{8}.$$  \hspace{1cm} (6)

Here, the load capacitance $C_L$ is higher than that of the divide-by-2/3 unit. It is observed that the divide-by-2/3 unit has the major power consumption for its highest operating speed. If all the DFF are identical, the proposed divide-by-2/3 only takes approximately 50% of the total power consumption.

For the unit in [1], the power consumption $P_{2/3\text{Lit}}$ is

$$P_{2/3\text{Lit}} = P_{\text{switching-DFF1/2}} + P_{\text{short-DFF1/2}}.$$  \hspace{1cm} (7)

Thus, the power consumption of this unit will account for more than 60% of the total power consumption.

V. SIMULATION AND SILICON VERIFICATIONS

A comparison of the performances of this new divide-by-2/3 unit and the E-TSPC unit in [1] is carried out on the grounds that the design in [1] achieves the best performance in the literature thus far. The simulations are performed by using the Cadence SPECTRE RF for a 0.18-$\mu$m CMOS process. The pMOS and nMOS devices of the two units are of the same size. Fig. 9 shows the simulation results of the power consumption versus operating frequency of the two units for the operations of divide-by-2 and divide-by-3. In the divide-by-3 operation, the proposed unit has approximately 10% lower power consumption compared with that of the unit in [1]. In the divide-by-2 operation, the proposed unit dissipates less than 40% of the power consumption of the unit in [1] due to the former’s reduced switching activities and short circuit in DFF1. If the two operations are of equal probabilities in the dual-modulus prescaler, a 25% reduction in power consumption is achieved for the proposed unit. With an input of 4.5 GHz, the power consumption is only 790 $\mu$W, while the divide-by-8/9 prescaler has a power consumption of 1.5 mW for this configuration.

For silicon verification, the proposed prescaler is fabricated using the Chartered 1P6M 0.18-$\mu$m CMOS process. It has been implemented with two versions: one is with large-size MOS transistors to avoid process variation, while the other is based on the small-size MOS transistors. Their minimum transistor sizes are 16 $\mu$m/0.18 $\mu$m and 2 $\mu$m/0.18 $\mu$m respectively, instead of 0.5 $\mu$m/0.2 $\mu$m, as in [1], to reduce the impact of parasitic and process variations. The operating speed of the proposed design can be increased if the proper transistor sizing is carried out [1], [6].

Fig. 10 shows a die photograph of the two proposed divide-by-8/9 dual-modulus prescaler. On-wafer tests are carried out using an RF probe station. The input signal for the measurement is provided by the Anritsu 68347C 10-MHz–20-GHz signal generator, while the output signals are captured by the Lecroy Wavemaster 8600A 6G oscilloscope. The power dissipation for the measured chip is 28 mW with the supply voltage of 1.8 V for a 4.2-GHz input in the first version because of the large size of MOS transistors. In the prescaler with smaller transistor sizes, the power consumption reduced to 3.3 mW for an input of 4 GHz at 1.8-V supply voltage, as shown in Fig. 11. Due to the simplified model in the calculation, the power consumption is lower than the simulated result even if the parasitic capacitor is added. The gap between the post-layout simulation and measurement result is due to the inaccurate model, insufficient extraction of parasitic capacitance, and resistance at high
frequency. Here, the post-layout simulation of the prescaler in the literature is presented as well. All the configurations are the same as the proposed one besides the divide-by-2/3 unit. Fig. 12 shows the output waveform of the prescaler with 4-GHz input. Table I compares the performance of this prescaler with that in [1], which achieves the best performance reported thus far.

VI. DESIGN OF HIGH-RESOLUTION FREQUENCY DIVIDER

The proposed prescaler is suitable for the applications of a low-power programmable divider. For example, it can be integrated with all-stage programmable counters, as in [9], to form a high-resolution integer-N frequency divider. It is based on the conventional pulse-swallow frequency divider, but both and are fully programmable [9]. The above two frequency dividers are the division ratios of , where is an integer and and are the division ratios of the two counters, respectively. If a divide-by-4/5 prescaler is implemented by removing one TSPC divide-by-2 unit, the number of available division ratios is increased since and are fully programmable [9]. The above two frequency dividers have been simulated and fabricated by adding two digital counters to the proposed prescalers. Fig. 13 presents the design of the integer-N dividers with divide-by-8/9 and divide-by-4/5 prescalers, respectively, but with the same counters. The prescaler can work properly from 1 to 4 GHz. The measured power consumption versus operating frequency with 1.5-V supply voltage is summarized in Fig. 14.

Here, the transistor size of the prescaler is optimized to achieve a better tradeoff between the power consumption and robustness against process variations. If the proposed low power prescaler is used, the total power consumption will be less than 5 mW. In these two designs, high-resolution frequency divisions are achieved with relatively low power consumption. Fig. 15 shows the output transient waveform of the frequency divider with 4-GHz input.

VII. CONCLUSIONS

The design and optimization of a high-speed E-TSPC-based prescaler has been carried out by investigation of the operating frequency and power consumption of the E-TSPC circuit. A new divide-by-2/3 unit with low power consumption has been proposed. It is suitable for the high-speed CMOS prescaler design. A divide-by-8/9 dual-modulus prescaler implemented with the proposed unit has been implemented to achieve the ultra-low-power consumption. The dual-modulus operation above 4 GHz in the TSPC-based prescaler has first been achieved. The prescaler has been implemented in high-resolution frequency dividers. It is suitable for the wireless communication system below 4 GHz. The operation of this proposed prescaler and frequency divider have also been silicon verified.

REFERENCES


Xiao Peng Yu (S’05–M’06) was born in Zhejiang, China, in 1976. He received the B.Eng. degree in optical engineering from Zhejiang University, Yu Quan, Hangzhou, China, in 1998, and the Ph.D. degree in electrical and electronic engineering from Nanyang Technological University (NTU), Singapore, in 2006.

Prior to joining NTU in 2002, he was with the Global Telecom Solution Sector (GTSS), Motorola, Hangzhou, China. From September 2005 to September 2006, he was a member of the research staff with NTU. In September 2006, he joined the Institute of VLSI Design, Zhejiang University, as a faculty member. His research interests include CMOS RF integrated circuits for wireless communication, low-power phase-locked loops, and clock data-recovery circuits for high-speed data communications using submicrometer CMOS technology.

Manh Anh Do (M’05–SM’05) received the B.Sc. degree in physics from University of Saigon, Saigon, Vietnam, in 1969, and the B.E. degree (Hons.) in electronics and Ph.D. degree in electrical engineering from the University of Canterbury, Canterbury, New Zealand, in 1973 and 1977, respectively.

From 1977 to 1989, he held various positions including Research and Development Engineer and Production Manager with Radio Engineering Ltd., Research Scientist with the Fisheries Research Centre, Wellington, New Zealand, and Senior Lecturer with the National University of Singapore. In 1989, he joined the School of Electrical and Electronic Engineering, Nanyang Technological University (NTU), first as a Senior Lecturer, became an Associate Professor in 1996, and a Professor in 2001. He has been a consultant for numerous projects in the Singapore electronic industry, and was the principal consultant for the design, testing, and implementation of the $200 million Electronic Road Pricing (ERP) island-wide project in Singapore (1990–2001). From 1995 and 2005, he was Head of the Division of Circuits and Systems, School of Electrical and Electronic Engineering, NTU. He is currently the Director of Centre for Integrated Circuits and Systems (CICS), NTU. He has authored or coauthored over 180 papers in the areas of electronic and communication circuits and systems. His current research concerns digital and mobile communications, RF integrated-circuit (IC) design, mixed-signal circuits, and intelligent transport systems. Prior to that, he specialized in sonar design, biomedical engineering, and signal processing.

Dr. Do is a Fellow of the Institution of Electrical Engineers (IEE), U.K., a Chartered Engineer in the U.K., and a Professional Engineer (Singapore). He
was a council member of the IEE from 2001 to 2004. Since April 2005, he has been an associate editor for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES.

Wei Meng Lim received the B.E. (Hons.) and M.E. degrees from Nanyang Technology University (NTU), Singapore, in 2002 and 2004, respectively. Upon graduation, he joined NTU as a member of the research staff. His research interests include RF circuit design, RF device characterization, and modeling.

Kiat Seng Yeo received the B.E. (Hons.) degree in electronics and Ph.D. degree in electrical engineering from Nanyang Technological University, Singapore, in 1993 and 1996, respectively. In 1996, he joined the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, as a member of the academic staff. He is currently the Head of the Division of Circuits and Systems. He provides consulting to statutory boards and multinational corporations in the areas of semiconductor devices and IC design.

Jian-Guo Ma (M’96–SM’97) received the B.Sc. and M.Sc. degrees (with honors) from the Lanzhou University of China, Lanzhou, China, in 1982 and 1988, respectively, and the Doctoral degree in engineering from the Gerhard-Mercator University, Duisberg, Germany, in 1996. From January 1982 to March 1991, he was with the Lanzhou University of China, where he was involved with RF and microwave engineering. Prior to joining Nanyang Technological University in 1997, he was with the Technical University of Nova Scotia, Halifax, NS, Canada. He was an Associate Professor and Director of the Center for Integrated Circuits and Systems, Nanyang Technological University, Singapore. Since December 2005, he has been with the University of Electronic Science and Technology of China (UESTC), Chengdu, China. He has authored or coauthored over 190 technical papers. He has authored two books. He holds 6 patents in CMOS RFICs. His research interests are RF IC designs for wireless applications, RF characterization and modeling of semiconductor devices, RF interconnects and packaging, system-on-chip (SoC) and applications, electromagnetic compatibility (EMC)/electromagnetic interference (EMI) in RF ICs, and monolithic microwave integrated circuits (MMICs) and applications. Dr. Ma was the associate editor for the IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS from 2004 to 2005.