Title	A review of 0.18-μm full adder performances for tree structured arithmetic circuits(Published)
Author(s)	Chang, Chip Hong; Gu, Jiang Min; Zhang, Mingyan
Citation	Chang, C. H., Gu, J. M., & Zhang, M. (2005). A review of 0.18-μm full adder performances for tree structured arithmetic circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 13(6), 686-695.
Date	2005
URL	http://hdl.handle.net/10220/6013
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A Review of 0.18-μm Full Adder Performances for Tree Structured Arithmetic Circuits

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***Abstract*—The general objective of our work is to investigate the area and power-delay performances of low-voltage full adder cells in different CMOS logic styles for the predominating tree structured arithmetic circuits. A new hybrid style full adder circuit is also presented. The sum and carry generation circuits of the proposed full adder are designed with hybrid logic styles. To operate at ultra-low supply voltage, the pass logic circuit that cogenerates the intermediate XOR and XNOR outputs has been improved to overcome the switching delay problem. As full adders are frequently employed in a tree structured configuration for high-performance arithmetic circuits, a cascaded simulation structure is introduced to evaluate the full adders in a realistic application environment. A systematic and elegant procedure to scale the transistor for minimal power-delay product is proposed. The circuits being studied are optimized for energy efficiency at 0.18-μm CMOS process technology. With the proposed simulation environment, it is shown that some survival cells in stand alone operation at low voltage may fail when cascaded in a larger circuit, either due to the lack of drivability or unsatisfactory speed of operation. The proposed hybrid full adder exhibits not only the full swing logic and balanced outputs but also strong output drivability. The increase in the transistor count of its complementary CMOS output stage is compensated by its area efficient layout. Therefore, it remains one of the best contenders for designing large tree structured arithmetic circuits with reduced energy consumption while keeping the increase in area to a minimum.**

***Index Terms*—Adders, CMOS digital integrated circuits, digital arithmetic, logic devices.**

I. Introduction

DIGITAL signal processors and application specific integrated circuits rely on the efficient implementation of arithmetic circuits to execute dedicated algorithms such as convolution, correlation and digital filtering. Very often, the utmost integrated circuit performances are restricted by how best the arithmetic operators are implemented in the cell library provided to the designer for the synthesis. As the complexity of arithmetic circuits grows with increasing processor bus width, energy consumption is becoming more important now than ever due to the increase in the number and density of transistors on chip and faster clock. Different CMOS logic styles have evolved for the development of cell libraries. They are likely to perpetuate the ability to further reduce the cost-per-function and improve the performance of integrated circuits. With the lowering of threshold voltage in ultra deep submicron technology, lowering the supply voltage appears to be the most eminent means to reduce power consumption. However, lowering supply voltage also increases circuit delay and degrades the drivability of cells designed with certain logic styles. Recently, clustered voltage scaling (CVS) and dual voltage supply (dual-VS) schemes have been proposed to maintain the chip throughput by selectively lowering the supply voltage for noncritical subcircuits [1], [2]. For such techniques to be effective, it is imperative that the performances of the basic cells dominating the critical path be characterized in the targeted technology and application environment over various ranges of supply voltage.

Full adder is the core element of complex arithmetic circuits like addition, multiplication, division, exponentiation, etc. [3]–[6]. The role of full adders in computer arithmetic can be classified into two main categories. One category involves the chain structured applications [7], [8], such as ripple carry adders (RCA) and array multipliers. In these applications, the critical path often traverses from the carry-in to the carry-out of the full adders. It is demanded that the generation of the carry-out signal is fast. Otherwise, the slower carry-out generation will not only extend the worst case delay, but also create more glitches in the later stages, hence, dissipate more power. The other category involves the tree structured applications, which is frequently used in Wallace–Dadda tree multipliers and multiplierless digital filters [6], [8], [9]. Full adders in these applications form a tree of several layers to compress the partial products to a carry-saved number before a final carry propagation adder converts it to a normal binary number. The tree structured architecture is widely accepted as being faster than its chain structured counterpart. However, VLSI implementations of large tree structured arithmetic circuits have irregular structure and complicated and long wiring interconnections. Irregular structure makes the layout difficult and incurs high-silicon area wastage. Long wiring interconnections have potential to degrade the performance in ultra deep submicron process. A strategy has been proposed in [9] to maximize the silicon area efficiency by allocating full adders to eliminate as many cross-stage interconnections (connections between nonadjacent stages) as possible, without sacrificing the local connectivity. To provide the flexibility to redistribute the cells, the three input ports of a full adder are equally likely to accept a legitimate output from another cell. Under this premise, it is highly desirable that the outputs, sum and carry-out, of the full adder be generated simultaneously to minimize the glitches in

Manuscript received July 28 2003; revised August 30, 2004. This work was supported in part by the Panasonic Singapore Laboratory under CHiPES-PSL Joint R&D Account M4890001.

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Digital Object Identifier 10.1109/TVLSI.2005.848806

the lower stages. The published literatures on full adder circuit optimization pay no attention to the specific layout requirements and the stringent drivability of the latter application. In this paper, we target the tree structured application for the evaluation of full adders with the optimization and simulation pursued in the proposed tree structure simulation environment.

The goal to extend the battery life span of portable electronics is to reduce the energy expended per arithmetic operation, but low-power consumption need not necessarily implies low energy. To execute an arithmetic operation, a circuit can consume very low power by clocking at extremely low frequency but it may take a very long time to complete the operation. One of the objectives of our work is to investigate, as supply voltage reduces, the optimal energy efficiency of the full adders designed with different logic styles based on the same 0.18-μm CMOS process technology. We measure the energy consumption by the product of average power and worst case delay. The power-delay product (PDP) represents a tradeoff to be optimized between two conflicting criteria of power dissipation and circuit latency in transistor sizing. In this paper, a systematic and unified approach to size the transistors of different full adder cells to optimize their power-delay product performance is suggested. The proposed transistor sizing procedure is proven to be convergent. Through the review of the pros and cons of various CMOS logic design styles, a new hybrid full adder cell constructed with mixed logic styles in its constituent modules is proposed. The proposed hybrid full adder features balanced outputs, making it easy for large tree structured arithmetic circuits to maximize area efficiency without unduly degrading the VLSI power and delay. It dissipates next to the lowest energy and occupies the smallest layout area among all simulated full adder cells that are operable below 1 V.

The rest of this paper is organized as follows. Section II explores the full adder designs in different logic styles. In Section III, the proposed hybrid full adder cell is analyzed in three constituent modules. To optimize and analyze the performance of the different full adders, a tree structured setup is proposed for the simulation environment in Section IV. A transistor optimization procedure is also described. In Section V, the circuits are simulated for power, delay and power-delay product performances and the results are analyzed and compared.

II. Review of Full Adder Design of Different CMOS Logic Styles

Several variants of static CMOS logic styles have been used to implement low-power 1-b adder cells [5], [10]–[12]. In general, they can be broadly divided into two major categories: the complementary CMOS and the pass-transistor logic circuits.

The complementary CMOS full adder (C-CMOS) of Fig. 1(a) is based on the regular CMOS structure with pMOS pull-up and nMOS pull-down transistors. The series transistors in the output stage form a weak driver. Therefore, additional buffers at the last stage are required to provide the necessary driving power to the cascaded cells. The advantage of complementary CMOS style is its robustness against voltage scaling and transistor sizing, which are essential to provide reliable operation at low voltage and arbitrary transistor sizes. Moreover, the layout of complementary CMOS circuit is straightforward and area-efficient due to the complementary transistor pairs and smaller number of interconnecting wires.

The complementary pass transistor logic (CPL) [8] full adder with swing restoration is shown in Fig. 1(b). Its dual-rail structure uses 32 transistors (henceforth "n transistors" is abbreviated as nT). The basic difference between the pass-transistor logic and the complementary CMOS logic styles is that the source side of the pass logic transistor network is connected to some input signals instead of the power lines [12], [13]. The advantage is that one pass-transistor network (either pMOS or nMOS) is sufficient to implement the logic function, which results in smaller number of transistors and smaller input load. However, pass-transistor logic has an inherent threshold voltage drop problem. The output is a weak logic "1" when "1" is passed through a nMOS and is a weak logic "0" when "0" is passed through a pMOS. Therefore, output inverters are also used to ensure the drivability.

A transmission function full adder (TFA) [14] based on the transmission function theory is shown in Fig. 1(c). A transmission-gate adder (TGA) [15] using CMOS transmission gates is shown in Fig. 1(d). Transmission gate logic circuit is a special kind of pass-transistor logic circuit [13], [15]. It is built by connecting a pMOS transistor and a nMOS transistor in parallel, which are controlled by complementary control signals. Both the pMOS and nMOS transistors will provide the path to the input logic "1" or "0," respectively, when they are turned on simultaneously. Thus, there is no voltage drop problem whether the 1 or the 0 is passed through it. The main disadvantage of transmission gate logic is that it requires double the number of transistors of the standard pass-transistor logic or more to implement the same circuit. Smaller transistor count adder circuits have been proposed, most of which exploit the nonfull swing pass transistors with swing restored transmission gate techniques. This is exemplified by the state-of-the-art design of 14 T in Fig. 1(e) [16] and 10 T in Fig. 1(f) [17]. These adders differ in their transistor counts and the way their intermediate nodes are generated.

Evidently, different logic styles tend to favor one performance aspect at the expense of the other. Layout regularity and wiring complexity have also nonnegligible impact on the cost/performance for large arithmetic circuit that uses many such instances. To summarize, the following performance criteria are considered in the design and evaluation of adder cells for the tree structured arithmetic circuits [5], [11]–[13], [18], which are working supply voltage range, voltage swing, delay, power-delay product, output skew, driving capability, and silicon area. As an illustration, we will present the design of a novel low-voltage full adder with a hybrid logic style in the next section. The unique features possessed by this hybrid full adder will be analyzed.

III. Hybrid Full Adder

As shown in Fig. 2, the proposed hybrid full adder circuit can be decomposed and analyzed in three submodules as in [5]. The logic expressions for the intermediate signals and outputs are given as follows:

$$Y = A \oplus B \tag{1}$$

$$Y' = \overline{A \oplus B} \tag{2}$$

$$Sum = Y \oplus C_{\text{in}} \tag{3}$$

$$C_{\text{out}} = A \cdot B + C_{\text{in}} \cdot Y. \tag{4}$$

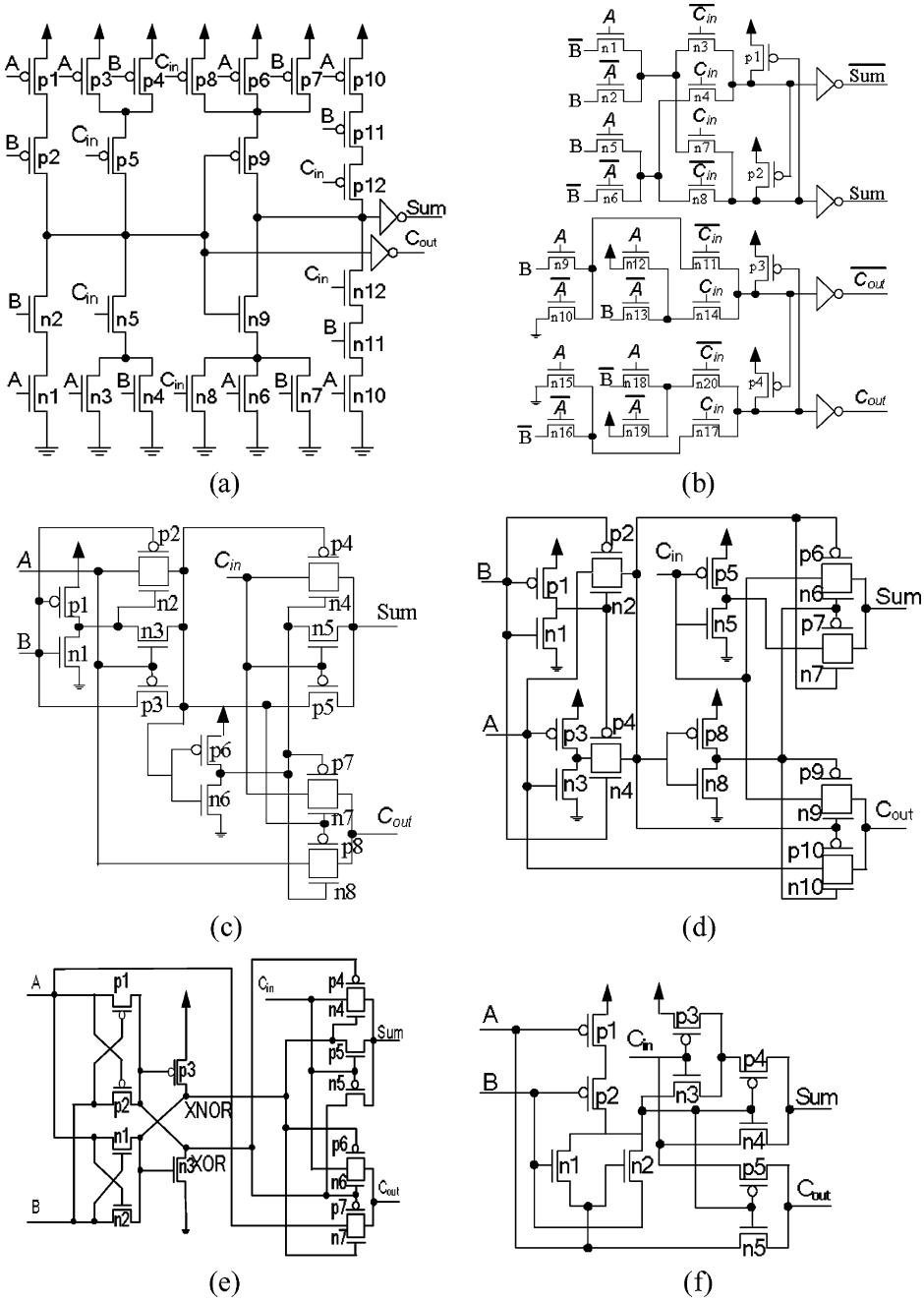

Fig. 1. Full adder cells of different logic styles. (a) C-CMOS. (b) CPL. (c) TFA. (d) TGA. (e) 14 T. (f) 10 T.

A. *Module 1: XOR/XNOR*

One approach to realize the exclusive OR and exclusive NOR (XOR/XNOR) functions is to synthesize the XOR function and generate the XNOR function through an inverter (e.g., TFA and TGA). This type of design has the disadvantage of delaying one of the Y and Y' outputs, giving rise to skewed signal arrival time to the successive modules. This will increase the chance of producing spurious switching and glitches in the last two modules. A better approach is to use different sets of transistors to generate the XOR and XNOR functions separately, with the possibility of introducing a larger transistor count [19]. To reduce the number of transistors, we use a similar pass transistor circuit as in [10] and [16] with only six transistors to generate the balanced XOR and XNOR functions, as shown in Fig. 3(a). Comparing with those designs that use an inverter to generate the complement signal, the switching speed is increased by eliminating the inverter from the critical path. The two complementary feedback transistors restore the weak logic caused by the pass transistors. They restore the non full-swing output by either pulling it up through pMOS to the power supply or down through nMOS to ground so that sufficient drive is provided to the successive modules. In addition, since there is no direct path between the power supply and ground, short-circuit current has been reduced.

However, this circuit suffers from the same threshold voltage drop problem as any other pass-transistor logic circuits. The worst-case delay happens at the transition from 01 to 00 for inputs AB. This could be explained with the aid of Fig. 3(b).

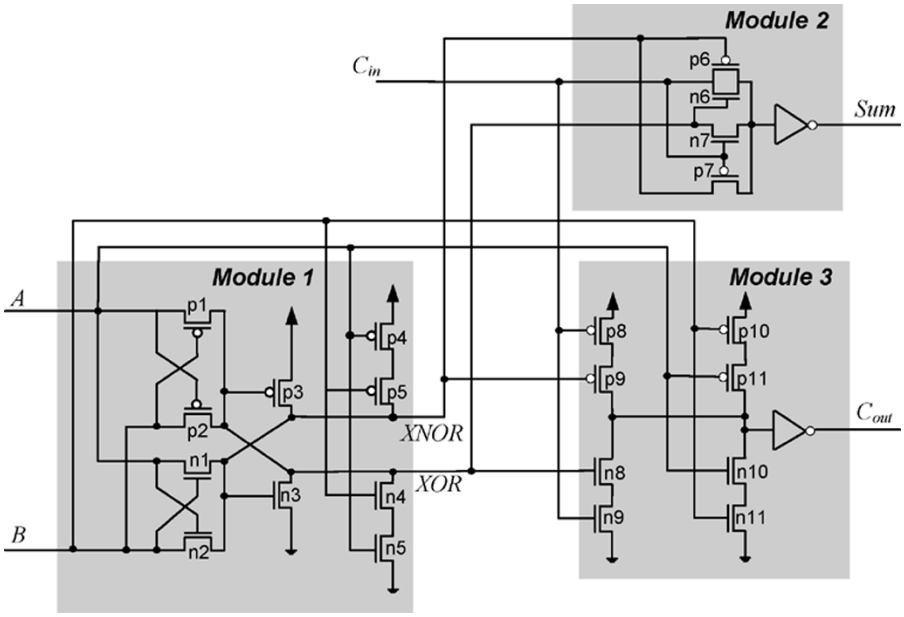

Fig. 2. Three submodules of the proposed hybrid full adder circuit.

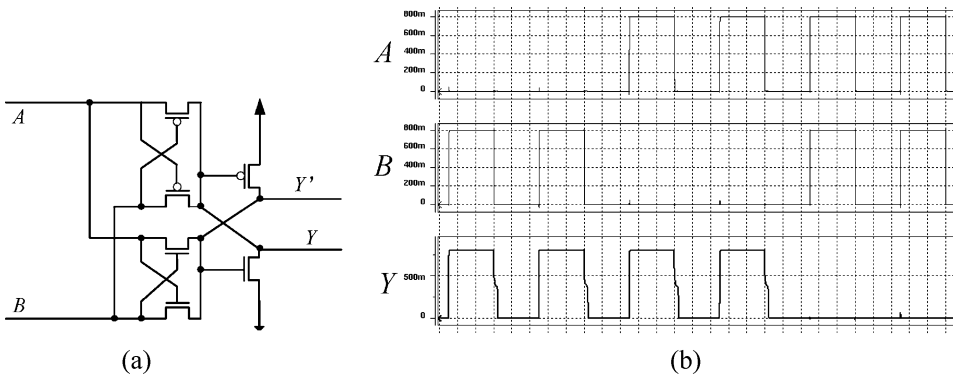

Fig. 3. XOR-XNOR 6 T gate and its worst-case delay waveform.

When the circuit is at the state of 01 for AB, logic "0" is passed through the nMOS transistor and "1" through the pMOS transistor. However, when the next state of 00 for AB arrives, a weak "0" $(\mathrm{V_{thp}})$ is passed through two pMOS pass transistors to the XOR output, and XNOR is at high impedance state initially. This "0" turns on the feedback pMOS so that the XNOR output is pulled up to logic "1," which turns on the feedback nMOS to discharge the XOR output completely to ground. Thus, a voltage step occurs at the output node, XOR. Although similar situation happens at the transition from 10 to 11 for AB, owing to the lower $\mathrm{V_{thn}}$ and high electron mobility of nMOS transistor, the entire process is faster than the previous case, which relies heavily on the pMOS switch. This slow response problem is more critical in low-voltage operation.

Due to the unsatisfactory performance at low-supply voltage, we modified the circuit of Fig. 3(a) to Fig. 4. Two series pMOS transistors are added to solve the worst-case delay problem of transition from 01 to 00 for AB. Two series nMOS transistors are added to solve the problem of transition from 10 to 11 for AB. When the state of $AB = 00$ arrives, the XNOR output could obtain a strong "1" through two series pMOS pull-up transistors to the power supply, which avoid the high-impedance state as in the previous case. Similarly, the XOR output could obtain a strong "0" through two series nMOS pull-down transistors to ground when the state of AB transits to 11.

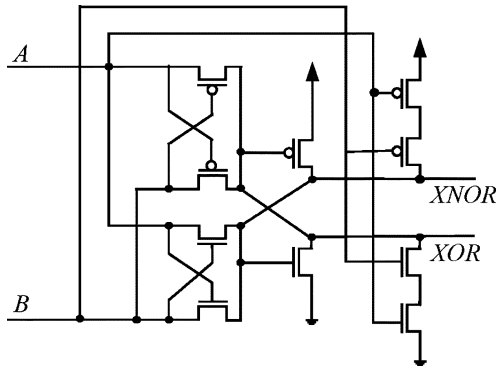

Fig. 4. Modification of Module 1.

B. Module 2: XOR

There are several choices for Module 2. Since its logic expression is similar to that of Module 1, the crossback 6-transistor

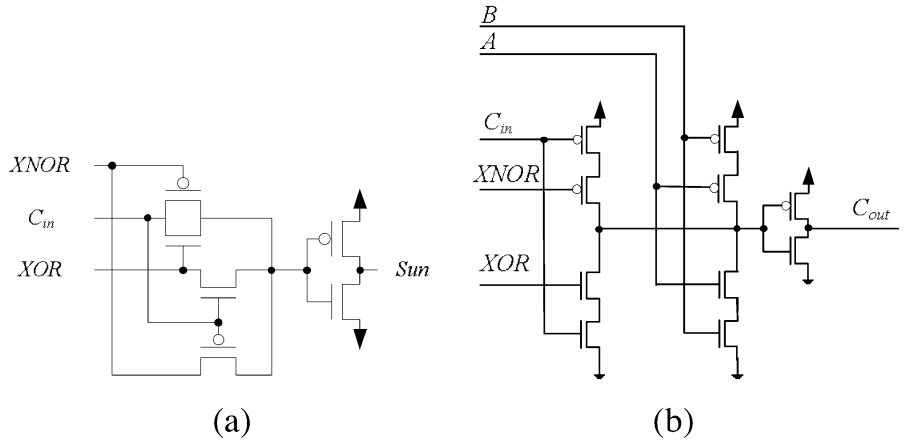

Fig. 5. (a) Module 2 and (b) Module 3.

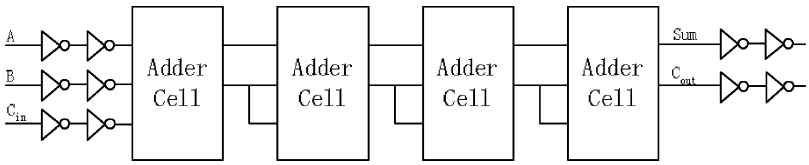

Fig. 6. Simulation setup suggested in [5].

circuit can also be used [10], [16]. However, it suffers from insufficient driving power due to the pass transistors. Therefore, we use a similar circuit as that of TFA and 14 T, but fully exploit the available XOR and XNOR outputs from Module 1 to allow only a single inverter to be attached at the last stage. The circuit is shown in Fig. 5(a). The output inverter guarantees that sufficient drive is provided to the cascaded cell.

C. Module 3: MUX

The smallest number of transistors for generating the $C_{\rm out}$ signal is two (circuit 10 T), but it suffers from the threshold voltage drop problem. Although a 4-transistor circuit can be used to generate a full swing $C_{\rm out}$ signal, it does not provide enough driving power. This can be proven in the later section when it is compared with our proposed circuit. The new circuit is based on complementary CMOS logic style, as shown in Fig. 5(b) [20]. Its logic expression is given by

$$C_{\rm out} = A \cdot B + C_{\rm in}(A \oplus B). \tag{5}$$

This circuit has inherited the advantages of complementary CMOS logic style, which has been proven in [12] to be superior in performance to all pass transistor logic styles for all logic gates except XOR at high supply voltage. Its robustness against voltage scaling and transistor sizing (high-noise margins) enables it to operate reliably at low voltage and arbitrary (even minimal) transistor size.

IV. Simulation Environment and Transistor Sizing Optimization

A. Simulation Environment

It has been a common practice to treat the adder cell as a stand alone cell in simulation [10], [14], [16], [17]. It is also not unusual that the adder cells that perform well in such simulation still fail upon actual deployment because of the lack of driving power. This is because adder cells are normally cascaded to form a useful arithmetic circuit. Therefore, the adder cells must possess sufficient drivability to provide the next cell with clean inputs [5]. In short, the driving cell must provide almost full-swing outputs to the driven cells. Otherwise the performance of the circuit will be degraded dramatically or become nonoperative at low-supply voltage. For this reason, the adder cells of TFA, TGA, 14 T, and 10 T cannot be cascaded without additional buffers attached to the outputs of each cell. This will be further verified.

The authors of [5] suggested one circuit structure, which is made of four cascaded adder cells, as shown in Fig. 6. This structure simulates the circuits like regular multipliers and binary adders that use full-adder cells as the building block. The inputs are fed from the buffers (two cascaded inverters) to give more realistic input signals and the outputs are loaded with buffers to give proper loading condition. All the required input-pattern-to-input-pattern transitions are included in the test patterns. The power consumption value is measured for the four cascaded adder cells, in addition to the intermediate buffers, while the delay is measured from the moment the inputs are applied to the first cell, until the latest of the Sum and $C_{\rm out}$ signals of the fourth cell is produced. However, this structure has some shortcomings. First, although the first adder has exercised all the input-pattern-to-input-pattern transitions, the subsequent adders may not have all the input-pattern-to-input-pattern transitions exercised. Thus, it is not appropriate to consider the four cascaded cells as a whole and then divide the average power by 4. As the last three adders are likely to consume lower power than the first adder, this simulation tends to produce more optimistic power dissipation. Instead, it would be better to measure only the power dissipated by the first adder. Second, it is also no-

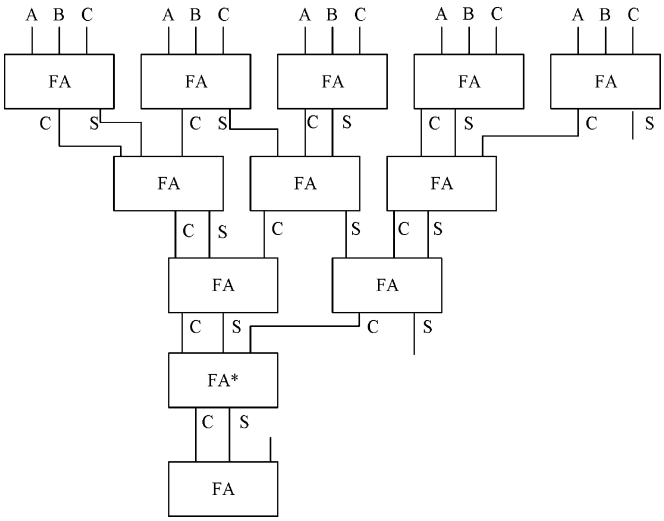

Fig. 7. Proposed simulation setup.

```
Initialize width w_k(T_i) for i = 1 to N;
Compute the power-delay product, Θ_k ;
Θ_min = Θ_k ;
do {
    for (i = 1 to N) {
        for (j = −m to m excluding j = 0) {
            w_j(T_i) = w_k(T_i) + jψ;
            Compute (Θ_k)_ij;
            if ((Θ_k)_ij < Θ_min) {
                Θ_min = (Θ_k)_ij;
                w_opt(T_i) = w_j(T_i); }}
        Update width of T_i, w_k(T_i) = w_opt(T_i); }
    k = k+1;
    Θ_k = Θ_min;
} while ( (Θ_k−1 − Θ_k)/Θ_k > ε );
```

Fig. 8. Transistor sizing procedure for optimizing the power-delay product.

ticed that every $C_{\rm out}$ has two fan-outs while Sum has only one fan-out. The loading of the two outputs is unbalanced.

Our proposed simulation structure is shown in Fig. 7, which emulates the tree structure of a parallel multiplier. Altogether 12 identical full adders are used, with the full adder (FA) marked with "$*$" being the cell of interest. Input signals of FA$*$ are fed from the outputs of FA in the preceding stage, while the outputs of FA$*$ are used to drive a FA in the following stage. This arrangement of full adders ensures that either the $C_{\rm out}$ or Sum output of each FA drives only one input of the FA in the next stage. The reason of cascading three levels of FAs preceding FA$*$ is to examine the output drivability of the FA cells. If the FAs cannot provide enough driving power, the output signals after three successive stages will become very weak. Under this situation, FA$*$ may fail to function.

B. Transistor Sizing Optimization

As shown in [21], the transistor sizing for optimal performance is technology dependent. To provide a fair and insightful evaluation of all the full adders presented earlier based on the same TSMC 0.18-μm CMOS process technology, a systematic and effective way of sizing the transistors for optimal performance is necessary. To provide a good tradeoff between the conflicting sizing requirements for power and delay performances, the goal of optimization is to minimize the power-delay product, i.e., the energy consumption. For a certain technology the channel lengths of all transistors are fixed at the minimal feature size, 0.18 μm in our example, so the only variable to be optimized is the channel width of each transistor. The proposed procedure for sizing the transistors is described by the pseudocodes in Fig. 8.

Initially, the sizes of the transistors in the circuit are reasonably set. The scaling operations are carried out in several iterations transistor by transistor. In Fig. 8, $w_j(\mathrm{T}_i)$ is the width of the ith transistor at Step j and Θ_k is the power-delay product of the full adder circuit of the kth iteration. For every optimization iteration, one transistor at a time is tuned for minimal power-delay product in $2 \times m$ steps with a step resolution of $\pm\psi$. The optimization stops when the performance difference in two successive iterations is smaller than a given error ε. More than one iterations may be necessary because each time a new transistor is sized in the current run, the other transistors sized in the previous run may no longer maintain their optimality.

In order to obtain enough coverage so that the optimal or quasi-optimal sizing will fall in the search region, the step resolution, ψ is made variable. Large step size is used at the first few iterations and smaller step size is used for fine tuning in the remaining iterations. Two optimization strategies are adopted in the previous procedure of transistor sizing to accelerate the process. First, the corresponding pMOS and nMOS in a complementary pair are optimized in successive runs because the output transitions of the node driven by one transistor is often influenced most by the driving capability of its complementary counterpart. Second, series transistors or parallel transistors of the same type that source current to or sink current from the same node have equal size and can be optimized simultaneously.

V. Results and Analysis

The six circuits C-CMOS, CPL, TFA, TGA, 14 T, 10 T of Fig. 1 and the proposed hybrid adder cell are prototyped and simulated using the TSMC 0.18-μm CMOS process with Level 49 technology file. The threshold voltages of the pMOS and nMOS transistors are around 0.46 and 0.48 V, respectively. These full adder circuits are all optimized using the procedure presented in Section IV. For the six previously reported full adders, the starting sizes of the transistors are based on the aspect ratio reported in [8] and [14]–[17]. The initial sizes of the transistors of our hybrid cell are estimated from standard practices and past experience. The step size of the first optimization run of each transistor in our example is set to 0.05 μm, which is around 10% to 20% of the initial channel width. The step size of the subsequent iterations is reduced to 0.02 μm. Thus, the final transistor sizes have the precision of 10% of the channel length, which is 0.18 μm for our targeted technology. The termination error is set to 1%. Optimization of the transistor sizing is carried out at two different voltages, 0.8 V and 1.8 V for C-CMOS, CPL, TFA, TGA and hybrid. As

TABLE I
TRANSISTOR SIZES (μm) OF HYBRID FULL ADDER OPTIMIZED FOR PDP

	p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11
0.8V	0.33	0.33	0.4	0.6	0.6	0.31	0.3	0.58	0.58	0.5	0.5
1.8V	0.42	0.42	0.31	0.8	0.8	0.4	0.3	0.7	0.7	0.5	0.5
	n1	n2	n3	n4	n5	n6	n7	n8	n9	n10	n11
0.8V	0.3	0.3	0.26	0.3	0.3	0.31	0.56	0.3	0.3	0.3	0.3
1.8V	0.6	0.6	0.25	0.3	0.3	0.3	0.3	0.4	0.4	0.3	0.3

14 T can only work above 1.0 V, this cell is optimized at 1.0 V and 1.8 V. The lowest voltage that 10 T can function under the proposed simulation setup is 1.8 V, so it is optimized only at 1.8 V. The final optimized transistor widths for the hybrid full adder cell are listed in Table I.

Star HSPICE is the circuit simulator used. For each simulation, HSPICE will generate an average power consumption value. The circuits are simulated at supply voltages range from 0.8 to 2.4 V. The operating frequency is set at 100 MHz. Backward derivation is performed to find a group of input test patterns which offers all the 56 different transitions from one input combination to another to FA$*$ [11]. For each transition, the delay is measured from 50% of the input voltage swing to 50% of the output voltage swing. The maximum delay of these 56 transitions is taken as the cell delay. Buffers are attached to the TFA, TGA, 14 T, and 10 T circuits to enhance their driving capability. Fig. 9 shows the output waveforms of those four adders before and after the insertion of buffers, which prove how important the drivability of adder cell is to the correct functionality of the circuit.

The power, delay and power-delay product at supply voltage ranges from 0.8 V to 2.4 V of hybrid, C-CMOS, CPL, TFA, TGA, 14 T, 10 T are listed in Table II for comparison. The transistor sizes optimized at 0.8 and 1 V are used for the simulation at the lower supply voltage range of 0.8–1.2 V and the transistor sizes optimized at 1.8 V are used for the simulation at the higher supply voltage range.

The simulation results show that the 10 T adder cell fails to function at low voltage. The lowest voltage it can operate at 100 MHz is 1.8 V. The excessive power dissipation and long delay are attributed to the threshold voltage drop problem and the poor driving capability of some internal nodes at input combinations that create non full-swing transitions.

The speed of the 14 T decreases faster with supply voltage than other adder cells, so does its power-delay product. Because of the XOR/XNOR generation circuit of 14 T, it suffers from the same threshold voltage drop problem that has been discussed in Section III. Therefore, 14 T fails to function below 0.8 V.

The simulation results also show that C-CMOS, TFA, TGA, CPL, and hybrid can work reliably at supply voltage as low as 0.8 V. Although TFA and TGA have lesser transistor count, due to the lack of drivability, additional buffers are required at each output, which increase their short-circuit power as well as switching power.

It is shown that hybrid and C-CMOS full adder are the most power efficient cells. hybrid is slightly faster than C-CMOS and as a result, it exhibits smaller power-delay-product than C-CMOS except at very low voltage of 0.8 V. Due to the decoupling of the input and output circuitries, good drivability can be achieved by the proposed hybrid cell. The full swing restoring transistors in Module 1 of the hybrid cell overcome the weak

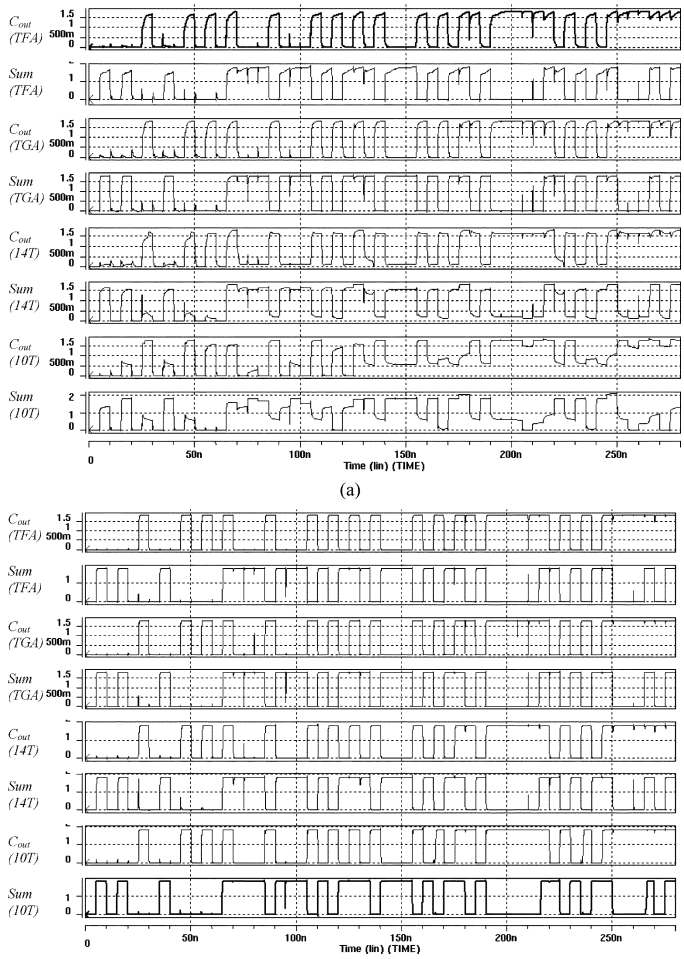

Fig. 9. Waveform snapshots of the circuits (1.8 V, 100 MHz). (a) Without buffer. (b) With attached buffers.

TABLE II
POWER, DELAY AND POWER-DELAY-PRODUCT COMPARISON OF FULL ADDERS

Vcc(V)	0.8	1.0	1.2	1.4	1.6	1.8	2.0	2.2	2.4
Power (μW)									
Hybrid	0.918	1.50	2.35	3.49	4.75	6.39	8.71	12.3	15.9
C-CMOS	0.84	1.45	2.12	3.63	4.91	6.23	8.77	12.4	15.9
CPL	1.03	1.70	2.64	4.08	5.64	7.72	11.2	14.0	17.7
TFA	1.50	2.28	3.60	4.56	6.25	8.25	10.6	14.9	17.6
TGA	1.49	2.20	3.30	4.29	6.12	8.47	10.0	12.6	16.5
14T		3.66	7.62	8.14	9.82	12.7	18.8	26.0	31.0
10T						44.4	56.5	70.7	86.4
Delay (ns)									
Hybrid	1.40	0.708	0.479	0.412	0.320	0.275	0.256	0.239	0.231
C-CMOS	1.42	0.756	0.531	0.397	0.333	0.292	0.269	0.252	0.244
CPL	0.908	0.468	0.321	0.236	0.197	0.184	0.179	0.172	0.173
TFA	1.53	0.777	0.511	0.385	0.322	0.288	0.270	0.255	0.252
TGA	1.42	0.721	0.497	0.383	0.321	0.294	0.274	0.257	0.250
14T		8.30	2.06	0.902	0.531	0.382	0.303	0.271	0.268
10T						3.61	1.85	0.986	0.584
Power Delay Product (fJ)									
Hybrid	1.285	1.062	1.126	1.438	1.520	1.757	2.230	2.940	3.673
C-CMOS	1.193	1.096	1.126	1.441	1.635	1.819	2.359	3.125	3.880
CPL	0.935	0.796	0.847	0.963	1.111	1.420	2.005	2.408	3.062
TFA	2.295	1.772	1.840	1.756	2.012	2.376	2.862	3.799	4.435
TGA	2.116	1.586	1.640	1.643	1.965	2.490	2.740	3.238	4.125
14T		31.33	27.66	5.97	4.75	4.78	5.94	7.18	7.94
10T						160.3	104.5	69.7	50.5

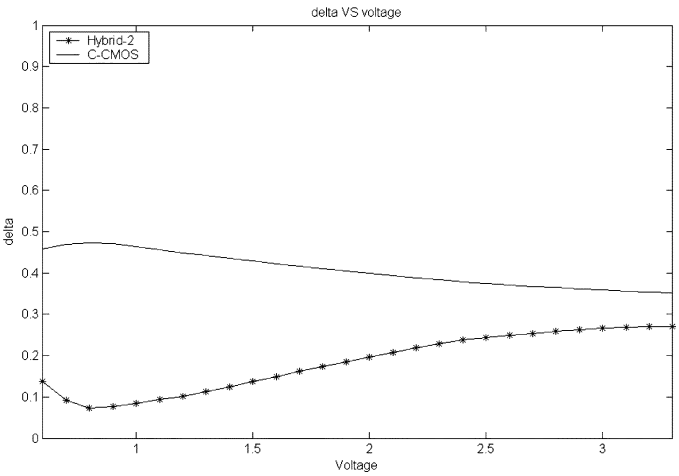

Fig. 10. Normalized delay differences of hybrid and C-CMOS cells.

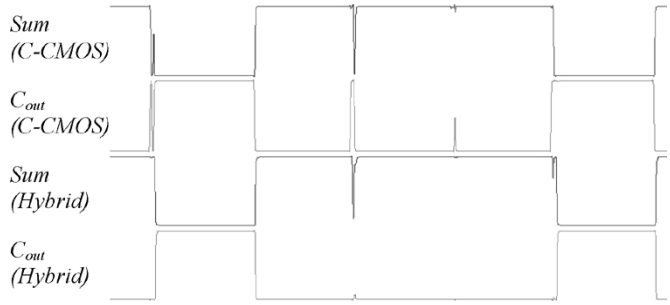

Fig. 11. Comparison of output waveforms between hybrid and C-CMOS.

logic problem, allowing it to operate reliably down to an ultra low voltage of 0.8 V.

C-CMOS works reliably at all voltage range especially at very low voltage. However, as already mentioned in Section II, to generate Sum signal, the signal of $C_{\rm out}$ is used as one of the inputs, which causes the unbalanced outputs. These unbalanced outputs also lead to more spurious transitions to the cascaded stage. We define a normalized delay difference, δ as follows:

$$\delta = \frac{(t_{\max} - t_{\min})}{t_{\max}} \tag{6}$$

where $t_{\max}$ is the larger delay value of the Sum and $C_{\rm out}$ outputs, and $t_{\min}$ is the smaller delay value of the two output signals.

The δ values of hybrid cell and C-CMOS cell are plotted against supply voltage in Fig. 10. It is shown that the outputs of hybrid cell are more balanced than those of C-CMOS especially at low voltage.

Fig. 11 shows a snapshot of the sum and carry outputs of hybrid and C-CMOS full adder cells. Due to the unbalanced output of C-CMOS adder, its outputs generate more glitches than those of hybrid cell for the same input transitions.

The skew of the sum and carry outputs causes the carry-save outputs of the Wallace–Dadda tree [9] to have irregular input arrival profile. Although the fast $\rm C_{out}$ can be consumed in the critical path of the adder in the next stage and the slower sum be consumed in the faster path of the next stage for constructing an optimized adder tree [22], such construction will annihilate the flexibility to redistribute the adder cells to maximize the area efficiency and to eliminate cross-stage interconnections described by the technique presented in [9]. Therefore, if the length of wiring and area efficiency are prominent cost function elements, which is the case for large arithmetic circuit in ultra deep submicron technology, balanced delays without jeopardizing the worst case delay can be a desirable attribute.

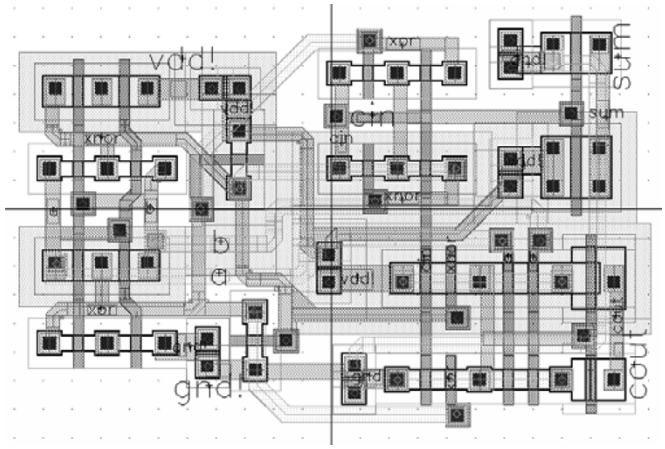

Fig. 12. Layout of the hybrid cell.

TABLE III
AREA COMPARISON OF THE FULL ADDERS

	Hybrid	C-CMOS	CPL	TFA	TGA	14T	10T
Length (μm)	7.18	17.37	11.20	9.58	14.07	12.10	11.2
Width (μm)	10.97	5.76	12.20	10.08	9.59	5.64	6.30
Area (μm^2)	78.76	100.05	136.64	96.57	134.88	68.24	70.56

Despite being the fastest circuit, CPL consumes higher power than hybrid and C-CMOS because of its dual-rail structure and the substantial number of internal nodes. The additional inverters used to generate the complement inputs have also increased the power consumption. This excessive overhead offsets the advantages of efficient XOR realization offered by this logic design style. Although CPL has achieved an overall good power-delay product due to its excellent speed, the performance is highly sensitive to the transistor scaling as observed in the optimization process described in Section IV-B. Besides, the need to generate complementary signals for all the surrounding circuits also limits the usage of CPL. The layout of the hybrid cell is shown in Fig. 12.

All full adder cells are laid out with optimized sizings and spacings in compliance to the design rules of TSMC 0.18-μm CMOS process. The values of the length, width and overall area of the adder cells are listed in Table III. The layouts of CPL and TGA full adders occupy the most silicon area. CPL adder needs more metal lines to connect the complementary inputs. Besides, the style of the transistor connection of CPL is not suitable for area-efficient layout. TGA adder is composed of transmission gates, which occupies more area due to the inefficient usage of the n-type wells. The layout of the hybrid cell occupies a much smaller silicon area, which is less than 60% of the area of the CPL. It is only slightly larger than 14 T and 10 T adders. The area ascendancy of 14 T and 10 T is due primary to their smaller number of transistors, but the area gained from the reduced transistor count is offset by the penalty of the irregular circuit structure of pass transistors. Besides, their overall performances are also inferior.

VI. Conclusion

For full adder cell design, pass-logic circuit is thought to be dissipating minimal power and have smaller area because it uses less number of transistors. Thus, CPL adder is considered to be able to perform better than C-CMOS adder in [12]. However, in our opinion, pass-logic circuit usually has irregular structure, which increases the wiring complexity and its performance is highly susceptible to transistor sizing. On the other hand, the complementary CMOS logic circuit has the advantages of layout regularity and stability at low voltage. Therefore, it is the different design constraints imposed by the applications that each logic design style has its place in the cell library development.

In the past, full adders are often evaluated in isolation without concern on how they are deployed in the actual circuit [10], [14], [16], [17]. We argue that a 1-b full adder cell that functions correctly in stand alone simulation is not sufficient to validate its actual performance or even functionality when it is integrated into a larger circuit. Inadequate consideration in simulation setup tends to produce the level of performance optimistically above the capability of the circuit being simulated. In this paper, we proposed a reasonably simple architecture to simulate the adder cell in an environment realistic to its actual deployment in most frequently used parallel multiplier structure.

Based on the simulation environment, an effective circuit optimization algorithm is proposed. The proposed method systematically scales the channel width of each transistor of the cell for minimal energy consumption.

Lastly, a hybrid full adder cell consisting of the XOR/XNOR, sum and carry out subcircuits, is proposed. The pass logic design style is used to efficiently generate the XOR and XNOR functions simultaneously and a good drivability carry out is generated by a complementary CMOS style circuit with regular layout. In addition, the last-stage inverter de-couples the output and input to improve the driving capability. Despite having higher transistor count than the recently reported designs, the proposed circuit has shown to be highly energy efficient over a wide supply voltage range. The balanced sum and carry outputs also offer considerable flexibility in allocating the adder cells in tree structured circuit to eliminate as many cross-stage interconnections and to reduce the maximum length of in-stage interconnections without affecting the critical path delay as there is no discrimination on any port for any legitimate connections [9]. Although its power-delay performance is comparable to C-CMOS and poorer than CPL, the area efficient layout makes it a good choice for implementing large tree structured arithmetic circuit when the overall performance and area efficiency are prominent cost function elements.

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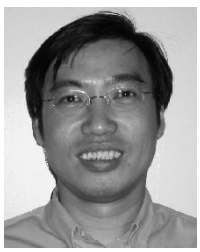

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