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<td>Author(s)</td>
<td>Shi, Xiaomeng; Yeo, Kiat Seng; Ma, Jianguo; Do, Manh Anh; Li, Erping</td>
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Complex Shaped On-Wafer Interconnects Modeling for CMOS RFICs

Xiaomeng Shi, Kiat Seng Yeo, Jian-Guo Ma, Manh Anh Do, and Erping Li

Abstract—A model development methodology for complex shaped on-wafer interconnects is presented. The equivalent circuit of the entire interconnect is obtained by cascading basic subsegment models. The extracted parameters are formulated into empirical expressions. Thus, the proposed model can be easily incorporated with commercial electronic design automation (EDA) tools. The accuracy of the model is validated by the on-wafer measurements up to 20 GHz.

Index Terms—CMOS radio frequency integrated circuits (RFICs), equivalent circuit model, interconnects, on-wafer measurements.

I. INTRODUCTION

The recent decade has witnessed the growing interests in radio frequency integrated circuits (RFICs). As the operating frequency reaches RF spectrum, the interconnect has become one of the most crucial factors affecting the performance of the RFICs [1]. Thereafter, incorporating the interconnect into the RFIC design flow becomes increasingly essential. Thus, there is an urgent demand for precise and simple interconnect models which can be implemented into conventional electronic design automation (EDA) tools.

In order to develop desired interconnect models, there are mainly three stages to follow. First, the model structure has to be established. The main challenge in this stage is that the interconnect becomes frequency-variant at high frequencies [2]. Furthermore, most of the models reported in the literature are for straight-line interconnects [2], [3]. However, the interconnect shapes on a real chip are much more complicated. Interconnect models which handle straight lines only are far from sufficient. In this work, a lumped equivalent circuit model for complex shaped interconnect is proposed. It is capable of characterizing frequency-variant behaviors with frequency-independent components, hence can easily be implemented in any standard simulators such as SPICE. Second, after model construction, it comes to the stage of parameter extraction. Finally, the proposed model should be verified with on-wafer measurements to ensure accuracy.

In this work, interconnect test structures with various physical shapes are designed and fabricated employing a Chartered Semiconductor Manufacture Ltd. (CHRT) 0.18-μm RF CMOS technology. On-wafer measurements of S-parameters up to 20 GHz are used to verify the proposed interconnect model.

This paper is organized as follows. Section II interprets the proposed approach for the interconnect model development in detail. Section III presents the model parameter extraction. Section IV lists the extracted parameters and the formulated empirical expressions. Verifications are also given in this section. Finally, this paper is summarized and concluded in Section V.

II. MODEL DEVELOPMENT SCHEME

A. Test Structure Design and Measurement

In order to develop interconnect models with silicon verified accuracy, this work is based on on-wafer measurements of test structures. Since the top metal layer is commonly allocated for routing critical high frequency paths [2], the test structures are designed and fabricated on the top metal layer.

The top view of the fabricated test structures is illustrated in Fig. 1. Since 45° and 90° bends are most commonly used in RFICs, these two angles are selected for the test structures. The total length of the test structures is fixed at 300 μm, while the widths vary from 3, 5, 10, and 20 μm. Open structures [2] are employed for de-embedding purpose.

After fabrication, a Cascade Microtech Probe Station and an HP 8510C Vector Network Analyzer are employed for on-wafer S-parameter measurements from 50 MHz to 20 GHz. Then, the Y-parameter-based de-embedding [2] is carried out to exclude the parallel parasitics, while with the aid of an electromagnetic (EM) simulator (HFSS), series parasitics of the pads are extracted and de-embedded from the measurements.

B. Proposed Development Methodology of the Interconnect Model

According to the physical configuration of the test structures in Fig. 1, the whole trace of the interconnect can be divided into different sub-segments, i.e., straight-line segments and corner segments. The structure analysis and nomenclatures are given in Fig. 2. Herein, the model development methodology can be proposed. First, a complex shaped interconnect is decomposed into sub-segments, as shown in Fig. 3. Second, equivalent circuit models are developed for these
The problem of the parameter extraction of this work can be formulated as an objective function. As shown in Fig. 2, three straight-line segments and two corner segments are cascaded in a sequence. In order to get the ABCD matrix of the whole trace, five corresponding ABCD matrixes of each segment should be modified. Hence, an additional parameter \( \alpha (0 < \alpha < 1) \), which is multiplication factor, is introduced to represent this variation of the inductance. In Fig. 3, the segments to be modified are highlighted as shaded boxes, i.e., inductance \( L \) in the second \( \Pi \)-network of Straight-line Segment 1, \( L \) in both of two \( \Pi \)-networks of Straight-line Segment 2 and \( L \) in the first \( \Pi \)-network of Straight-line Segment 3 are multiplied with the multiplication factor \( \alpha \). As for the shunt blocks of the straight-line segments, the influences of the corner can be omitted, so the parameters are kept unchanged.

III. MODEL PARAMETER EXTRACTION

The lumped equivalent circuit model for microstrip bends has been introduced in [4]. However, that model cannot sufficiently characterize the lossy substrate of the CMOS process, which is currently widely used for RFIC designs.

Based on the understanding of the physical structure, a T-network as shown in Fig. 5 is proposed for the interconnect bends of CMOS processes by adding the substrate effects.

At the corner, the current’s flow in the conductor is distributed unevenly such that most of the flows crowd at the inner edge [4]. Hence, the resistance reduces. Given the sheet resistance of straight lines to be \( R_{\text{sheet}} \), the sheet resistance of the corner is approximately \( 0.6 \times R_{\text{sheet}} \) [5]. Additionally, considering the relative smaller physical size compared with the straight line, \( R \) in the series branch can be removed. Thus, the model can be further simplified as shown in Fig. 6.
$T_{11}$ can be described in (3)–(7)

$$T_{11} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}$$ (3)

where

$$A = 1 + \frac{j \omega C_{ox} \left(j \omega C_{mab} + \frac{1}{\tau_{mab}}\right) \left(j \omega L_s + R_s + \frac{j \omega L_b R_b}{j \omega L_b + j \omega L_s + R_s + R_b}\right)}{j \omega C_{ox} + j \omega C_{mab} + \frac{1}{\tau_{mab}}}$$

$$B = j \omega L_s + R_s + \frac{j \omega L_b R_b}{j \omega L_b + j \omega L_s + R_s + R_b}$$

$$C = \frac{2j \omega C_{ox} \left(j \omega C_{mab} + \frac{1}{\tau_{mab}}\right) \left[j \omega L_s + R_s + \frac{j \omega L_b R_b}{j \omega L_b + j \omega L_s + R_s + R_b}\right]^2}{j \omega C_{ox} + j \omega C_{mab} + \frac{1}{\tau_{mab}}}$$

$$D = 1 + \frac{j \omega C_{ox} \left(j \omega C_{mab} + \frac{1}{\tau_{mab}}\right) \left[j \omega L_s + R_s + \frac{j \omega L_b R_b}{j \omega L_b + j \omega L_s + R_s + R_b}\right]}{j \omega C_{ox} + j \omega C_{mab} + \frac{1}{\tau_{mab}}}$$ (7)

The previous matrix elements presented in (3)–(7) are for a II-network without the corner influence. The corner-influenced II-network $T_{11\text{corner}}$ is similar to $T_{11}$, just replacing the item $L_s$ with $\alpha \cdot L_s$ to account for the corner effect.

By using the obtained formulas mentioned in Section II-C, values of all components in the straight-line segment can be calculated. Therefore, after the ABCD matrix of the entire complex shaped interconnect can be interpreted as functions of $L_b$, $C_b$, $R_b$, and $\alpha$. Consequently, corresponding $S$-parameters can be expressed in functions of these variables with the aid of the ABCD to $S$-parameter transform formulas.

The proposed objective function $F_0(X)$ can then be obtained as

$$F_0(X) = \left(\sum_{i=1}^{m} \left(f_1^2(X) + \left|f_1(X) - F_{1\text{mean}}\right|^2 \right) + f_2^2(X) + \left|f_2(X) - F_{2\text{mean}}\right|^2 \right)$$

where $m$ is the total number of the frequency points under consideration. $f_1$ is the error between the simulated $S_{11}$ and those corresponding ones acquired from measurement results at each frequency point $i$. It is stated in (9). $f_2$ is the error between the simulated $S_{21}$ and the measurement results at each frequency point $i$, which is stated in (10). $F_{1\text{mean}}$ and $F_{2\text{mean}}$ are the mean errors of $S_{11}$ and $S_{21}$ at each frequency point $i$, respectively, as illustrated in (11) and (12). Given the symmetry of the interconnect test structure, it is known that $S_{1j} = S_{ji}$ and $S_{2j} = S_{j2}$ [7]. Therefore, we use the average value of measured $S_{11}$ and $S_{22}$, $S_{12}$ and $S_{21}$ in the following steps, denoted as $S_{11}$ and $S_{22}$, respectively.

$$f_1(X) = \frac{S^\text{11}_{1\text{simulated}} - S^\text{11}_{1\text{measured}}}{S^\text{11}_{1\text{measured}}}$$ (9)

$$f_2(X) = \frac{S^\text{21}_{1\text{simulated}} - S^\text{21}_{1\text{measured}}}{S^\text{21}_{1\text{measured}}}$$ (10)

$$F_{1\text{mean}} = \frac{1}{m} \sum_{i=1}^{m} f_1(X)$$ (11)

$$F_{2\text{mean}} = \frac{1}{m} \sum_{i=1}^{m} f_2(X)$$ (12)

The optimization algorithm used in [2] is applied to search for the optimal model parameters, i.e., $L_b$, $C_b$, $R_b$, and $\alpha$, which can minimize the objective function $F_0(X)$. The returned component values are the optimized set that makes the simulation results fit the measurement data best.

### IV. EXTRATION RESULTS AND MODEL VERIFICATIONS

#### A. Extraction

The extracted model parameters are summarized in Table I. It is observed that $\alpha$ is always smaller than 1. The value of $\alpha$ of 90° corner segment is smaller than that of 45° corner segment. This can be explained as stated in Section II-E that the multiplication parameter applied to $L_s$ is introduced to characterize the inductance reduction which is a result of the mutual inductance cancellation of different sub-segments. The general trend is that the larger curvature an interconnect has, the smaller the inductance is. Hence, $\alpha$ should be always smaller than 1 and reversely proportional to the curvature of the interconnect.

#### B. Formulation

Empirical formulas of the model parameters are summarized as functions of design parameters. Thus, provided with the geometrical information, characteristics of the complex shaped interconnect can be obtained by following the algorithm presented in Section II. The empirical formulas of the straight-line segment can be found in our previous work [2]. Formulas of the corner segment are listed in the following. The formulated expressions for the 45° bends are defined in (13)–(15). The corresponding coefficients are shown in Table II. Equations (16)–(18) are expressions for the 90° bends. The coefficients are presented in Table III.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>$W=3\mu m$</th>
<th>$W=5\mu m$</th>
<th>$W=10\mu m$</th>
<th>$W=20\mu m$</th>
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<tr>
<td>$L_b$ (pH)</td>
<td>18.7</td>
<td>19.4</td>
<td>22.1</td>
<td>28.5</td>
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<tr>
<td>$C_b$ (pF)</td>
<td>12.3</td>
<td>18.6</td>
<td>27.9</td>
<td>31.5</td>
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<tr>
<td>$R_b$ (kΩ)</td>
<td>99.5</td>
<td>82.3</td>
<td>61.2</td>
<td>47.6</td>
</tr>
<tr>
<td>$\alpha$</td>
<td>0.86</td>
<td>0.86</td>
<td>0.86</td>
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</table>

<table>
<thead>
<tr>
<th>Coefficient</th>
<th>$L_b$</th>
<th>$C_b$</th>
<th>$R_b$</th>
</tr>
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<tbody>
<tr>
<td>a</td>
<td>1.828E1</td>
<td>-1.055E1</td>
<td>7.710E1</td>
</tr>
<tr>
<td>b</td>
<td>5.087e-2</td>
<td>-1.144E-2</td>
<td>-2.502</td>
</tr>
<tr>
<td>c</td>
<td>-1.266E-3</td>
<td>1.331E1</td>
<td>8.949E1</td>
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### TABLE III

<table>
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<tr>
<th>Coefficient</th>
<th>$L_b$</th>
<th>$C_b$</th>
<th>$R_b$</th>
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<tbody>
<tr>
<td>a</td>
<td>3.647</td>
<td>1.092E1</td>
<td>1.152E2</td>
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<tr>
<td>b</td>
<td>4.994</td>
<td>1.379</td>
<td>-7.894</td>
</tr>
<tr>
<td>c</td>
<td>1.650E1</td>
<td>2.512E-1</td>
<td>4.365E-2</td>
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</table>
C. Verification

Simulations of the proposed model are performed using MATLAB. Since $S_{ij} = S_{ji}$ and $S_{ii} = S_{jj}$ [7], only $S_{11}$ and $S_{21}$ are compared here. The simulated $S$-parameters are compared with the corresponding measured ones. Four different dimensions of the test structures are examined in the simulation as described in Section III-A. The lengths are fixed at 300 μm. The widths range from 20, 10, 5, and 3 μm.

\begin{align}
C_s &= a + b W^{1.5} + c W^2 \quad (17) \\
R_s &= a + b W + c W^{2.5} \quad (18)
\end{align}

From Figs. 7 and 8, satisfactory agreements between the simulated $S$-parameters and the measurement results over the whole frequency range have been achieved. The error is less than 9%. It demonstrates that the proposed model and the extracted parameters are capable of accurately characterizing the on-wafer interconnect with bends over a large range of frequencies up to 20 GHz. In Figs. 7 and 8, simulation results by using straight-line interconnect model in Fig. 4 are also plotted. Values of model parameters are obtained from empirical formulas [2] with the total length ($L$) and width ($W$) of the interconnects with bends ($L = 300$ μm, $W = 3$ μm, 10 μm, and 20 μm). From Figs. 7 and 8, it is clear that the straight-line interconnect model is not adequate to
model interconnect with bends. Hence, the proposed cascading method is more appropriate.

It is important to note that the given formulas of the model parameters are fit to our specific test chip and process. Moreover, these formulas are only valid within a geometrical range, which is within the coverage of our test structures. For the corner segments, the valid range for the length is from 3 to 20 \( \text{mm} \) and the angles are 45° and 90°. However, as stated in Section II-A and [2], most of the on-wafer interconnects used in RFICs are within this range.

V. CONCLUSION

An equivalent circuit model is proposed for real on-wafer CMOS RFIC interconnects. The equivalent circuit of the entire complex shaped interconnect is obtained by cascading basic sub-segment models according to the physical structure. The model parameters are extracted from the on-wafer S-parameter measurements and formulated into empirical expressions. The validity of the proposed model is proved by the measurements of the test structures within a tolerance of 9\%. It is highlighted that with the geometrical information, i.e., the length, width and angle of the bend, most of the commonly used on-wafer RF CMOS interconnect can be characterized by using this proposed model. Moreover, given the compact nature of the model, it can be easily implemented into commercial EDA tools.

REFERENCES


Multilevel-Huffman Test-Data Compression for IP Cores With Multiple Scan Chains

Xrysovalantis Kavousianos, Emmanouil Kalligeros, and Dimitris Nikolos

Abstract—Various compression methods have been proposed for tackling the problem of increasing test-data volume of contemporary, core-based systems. Despite their effectiveness, most of the approaches that are based on classical codes (e.g., run-lengths, Huffman) cannot exploit the test-application-time advantage of multiple-scan-chain cores, since they are not able to perform parallel decompression of the encoded data. In this paper, we take advantage of the inherent parallelism of Huffman decoding and present a generalized multilevel Huffman-based compression approach that is suitable for cores with multiple scan chains. The size of the encoded data blocks is independent of the slice size (i.e., the number of scan chains), and thus it can be adjusted so as to maximize the compression ratio. At the same time, the parallel data-block decoding ensures the exploitation of most of the scan chains’ parallelism. The proposed decompression architecture can be easily modified to suit any Huffman-based compression scheme.

Index Terms—Huffman encoding, test data compression.

I. INTRODUCTION

In order to meet the tight time-to-market constraints, contemporary digital systems embed predesigned and preverified Intellectual Property (IP) cores. The structure of IP cores is often hidden from the system integrator and as a result, neither fault simulation, nor test pattern generation can be performed for them; only a precomputed test set is delivered along with such a core. Various methods have been proposed for reducing both the test-data volume and test-application time of unknown-structure IP cores [1]–[7], [9], [10], [12]–[18], [20]–[25]. Many of them encode directly the statically or dynamically compacted test sets using various (usually classical) compression codes like Golomb [2], [3], [21], alternating run-length [4], frequency-directed run-length (FDR) [5], [18], statistical codes [7], [10], [12], nine-coded-based [23], and combinations of codes [22]. Unfortunately, these code-based methods cannot exploit the existence of multiple scan chains in a core. This shortcoming stems from the fact that parallel decompression is not possible due to either the nature of the code or the way it is used in the specific method. For example, the decoding of the various run-length codes is performed in a strictly serial manner. On the other hand, the straightforward approach for parallelizing selective Huffman decoding (i.e., by encoding slice-sized data blocks and then by loading the scan chains in parallel with a whole slice after the decoding of every codeword) leads to both large decompressors and very low compression ratios. Since the vast majority of the cores have multiple scan chains, a serial-in, parallel-out register must be used for spreading the decoded data in them and thus, no test-time savings, despite the existence of multiple scan chains, are possible. The solution of using multiple decoders in parallel is too