<table>
<thead>
<tr>
<th><strong>Title</strong></th>
<th>Dual nanowire silicon MOSFET with silicon bridge and TaN gate</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Author(s)</strong></td>
<td>Theng, A. L.; Goh, Wang Ling; Ng, C. M.; Chan, L.; Lo, Guo-Qiang</td>
</tr>
<tr>
<td><strong>Citation</strong></td>
<td>Theng, A. L., Goh, W. L., Ng, C. M., Chan, L. &amp; Lo, G. Q. (2008). Dual Nanowire Silicon MOSFET with Silicon Bridge and TaN Gate. IEEE Transactions on Nanotechnology. 7(6), 795-799.</td>
</tr>
<tr>
<td><strong>Date</strong></td>
<td>2008</td>
</tr>
<tr>
<td><strong>URL</strong></td>
<td><a href="http://hdl.handle.net/10220/6263">http://hdl.handle.net/10220/6263</a></td>
</tr>
<tr>
<td><strong>Rights</strong></td>
<td>© 2008 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE. This material is presented to ensure timely dissemination of scholarly and technical work. Copyright and all rights therein are retained by authors or by other copyright holders. All persons copying this information are expected to adhere to the terms and constraints invoked by each author’s copyright. In most cases, these works may not be reposted without the explicit permission of the copyright holder.</td>
</tr>
</tbody>
</table>
Abstract—This paper demonstrates a high performance silicon nanowire mosfet built on silicon-on-insulator (SOI) platform. Stress-limiting oxidation technique was exploited for dual nanowire channel formation. To further improve the performance of the device, TaN metal gate is used instead of the conventional polysilicon gate. The thin silicon bridge between the two nanowires provides a small boost in the drive current, without degrading the short channel performance. The novel structures are able to achieve excellent electrical performances, high drive current of 927 $\mu$A/um for p-channel and 554 $\mu$A/um for n-channel, near ideal subthreshold slope (SS), and low drain-induced barrier lowering (DIBL).

Index Terms—Silicon nanowire transistor, silicon-on-insulator (SOI) technology.

I. INTRODUCTION

TRANSISTOR scaling has led to the exploration of various nonclassical devices for the delivery of high performance devices. Double-gate FinFET [1], tri-gate [2], gate-all-around (GAA) [3], and the nanowire FinFETs [4]–[6] are some well-known structures reported. These devices are innate with good suppression of short-channel-effects (SCEs), high drive current and excellent $I_{on}/I_{off}$ ratio. Silicon nanowire transistors have been attracting the attention of researchers mainly for their improvement in the transport property [7] and their compatibility with CMOS process [5], [6]. The published results on polysilicon gate nanowire transistors [5], [6] have been well covered. Nevertheless, the performance of nanowire transistors can be further enhanced using high-$\kappa$ dielectric and metal gate [4].

In this paper, we present the dual nanowire field effect transistor (DNWFET) devices that are fabricated using HfO$_2$ and TaN as the gate dielectric and gate material, respectively. TaN metal gate is engaged to improve the work function of the nanowire transistors. Not only a suitable threshold voltage ($V_T$) can be attained, but also the leakage current is reduced. The top and bottom nanowires are bridged by a thin silicon layer to enhance the drive current without much degradation in the short channel performance. The nanowire channel is wrapped around by a TaN gate to provide optimum electrostatic control.

II. FABRICATION OF NANOWIRE MOSFET

The SOI wafers with 70 nm p-type ($\sim$10$^{15}$/cm$^3$) top silicon and 150 nm buried oxide (BOX) are used as starting materials. Lithography and resist trimming are performed to achieve a fin width of around 50 nm. The wafers are etched and sent for dry oxidation at 875 °C for 5 h. With well-controlled self-limiting oxidation process, dual nanowire channels that are connected by a thin silicon bridge can be established. The oxidation process makes use of the different oxidation rates of the various silicon planes to form the two nanowires. The sides of the fins that are at 1 1 0 plane oxidize two times faster than the top of the fin (at 1 0 0 plane). With the close proximity of the two nanowires, and the precisely controlled oxidation parameters and timings, a thin silicon bridge can be formed. The oxidized structure is later released with a dilute hydrofluoric acid (DHF) dip. The hydrofluoric acid (HF) dip also undercuts the BOX layer to facilitate the development of the wrap around gate.

Fig. 1(a) shows the dual nanowire upon oxide removal. A high quality gate oxide of 20 Å is then grown, followed by a 30 Å HfO$_2$ deposition to complete the gate dielectric stack. The 800 Å of TaN that wraps around the nanowire channel is then deposited using physical vapor deposition (PVD), for improving the electrostatic control of the device [see Fig. 1(b)]. The TaN gate electrode is patterned with a triple-layered hardmask (oxide–nitride–oxide) process. Two hardmask etching steps with additional wet processes in between are required to provide a clean TaN etch [see Fig. 1(c)]. BF$_2$ and As of dose 4 × 10$^{15}$ cm$^{-2}$ with 10 and 20 keV energy for the p- and n-DNWFETs are engaged for the implantation step. To form the source and drain, the device is given a short 10 s source/drain (S/D) activation anneal prior to contact formation and metallization for the device. The process finally ended with a sintering at 430 °C. Fig. 1(d) is the TEM cross section of a 5-nm diameter dual nanowire channel with a 1 nm silicon bridge, surrounded by gate dielectric and TaN gate. An overview of the processing steps is listed in Fig. 1(e). Fig. 2 provides the schematic views of the DNWFET structure.

III. RESULTS AND DISCUSSIONS

The $I_d$ vs $V_d$ and $I_d$ vs $V_g$ characteristics of the 350-nm long nanowire MOSFET devices are given in Fig. 3. At an operating...
Fig. 1. SEM pictures of the device after various processing steps. (a) Nanowires released after DHF dip. (b) TaN deposition causing deformation of nanowire channel. (c) TaN gate etch. (d) TEM image of dual 5-nm diameter nanowire with 1 nm silicon bridge wrapped around by TaN gate. (e) Summary of processing steps for DNWFET.

Voltage of 1.5 V, the $p$-DNWFET exhibits a drive current of 927 $\mu$A/µm, while the $n$-DNWFET achieving 554 $\mu$A/µm. The $p$- and $n$-DNWFET exhibits comparable leakage currents of 0.9 and 1.8 nA/µm, respectively, both taken at zero gate voltage. All currents are normalized with the nanowire diameters and silicon bridge width. This gives a spread of $I_{ON}/I_{OFF}$ ratio between $10^5$ and $10^6$. The high drive current is attributed to the volume inversions of the two silicon nanowires. Strain generated from the thermal oxidation process [8] and stress from the TaN deposition process provide mobility enhancement in the devices. The thin 1 nm silicon bridge is believed to contribute only a small current boost. The higher on current observed in $p$-DNWFET as compared that in $n$-DNWFET is mainly attributed to the difference in $V_T$, the higher total on resistance of $n$-DNWFET as compared to that of $p$-DNWFET, and also variation in the effective carrier mass between the two. These observations are also reported in [9]. Note that for DNWFET devices, this difference in ON current is made more severe by the large difference in the two $V_T$. Measurements show the $p$-DNWFET achieved a $V_T$ of $-0.29$ V, while the $n$-DNWFET has a high $V_T$ of...
0.56 V. Fixing an operating voltage of 1.5 V would indicate a lower overdrive ($V_g - V_{T}$) for $n$-DNWFET, and hence, yielding a lower drive current.

We should also note that after the gate etch, the expose portions of the nanowire [see Fig. 2(a) and (b)] is subjected to high dose S/D implantation. This may lead to amorphization of the exposed portions of the nanowire.

Without a template for subsequent recrystallization via solid phase epitaxy, the expose portions of the nanowire is unlikely to recrystallize after the S/D activation anneal. Thanks to the used of boron spcies in $p$-DWNFET, which have a higher threshold for amorphization, the expose nanowire portions of the $p$-DWNFET are able to remain crystalline. This results in a higher relative total resistance in $n$-DNWFET than $p$-DNWFET. The lower effective mass of hole as compared to electron of the [1 1 0] direction [9] shows that hole mobility is enhanced.

The wrap-around gate electrode provides a shield to block the drain field, yielding good immunity to the short channel effect.
devices. The elevation of the earlier in Fig. 3(a).

The midgap TaN gate elevates the $V_T$ to solve the low $V_T$ and high off-state leakage issues seen in polysilicon gate nanowire devices. The elevation of the $V_T$ shifts the PMOS $I_D$ vs $V_G$ curve to the left and NMOS curve to the right, as indicate in Fig. 5(a) and (b). This shift allows the TaN gate device to obtain lower leakages for as much as one order of magnitude as compared to the polysilicon gate device while maintaining high drive current. Although the use of TaN metal gate further increases the $V_T$ of the $n$-DNWFET, this issue can be moderated with a $V_T$ adjustment implant or an $n$-type SOI substrate.

The $G_m$ as a function of the $V_T$ plot of Fig. 4 illustrates the fast response of the transconductance to gate voltage. The transconductance saturates after peaking, and this indicates that these devices are enjoying low field mobility even at high gate voltages. This is attributed to the cylindrical channel morphology [10] and the undoped channel. The DNWFET devices are also immune to the substrate bias, whereby the $V_T$ remains constant when the substrate bias is swept from $-6$ to $6$ V for both the $n$- and $p$-DNWFET. This immunity is further verified with the reference planar SOI devices that are built on the same wafer. The $V_T$ of the reference devices change with substrate bias swept from positive to negative for PMOS and vice versa for NMOS. The substrate bias immunity is a result of the wrapped around gate shielding the channel from unwanted signals. This is illustrated in Fig. 6.

IV. CONCLUSION

We have successfully fabricated TaN gate DNWFET structures. A high drive current is achieved along with excellent SS and DIBL. The $p$-DNWFET surpassed the performance of the $n$-DNWFET due to the higher total resistance of $n$-DNWFET and the lower effective hole mass. The TaN gate is clearly able to improve the gate work function to attain a higher $V_T$, thereby achieving a lower leakage current.

ACKNOWLEDGMENT

The authors would like to thank the staffs of the Institute of Microelectronics (IME), Singapore, for their assistance in device fabrication.

REFERENCES


A. L. Theng is a Technology Development Engineer with Chartered Semiconductor Manufacturing Ltd., Singapore. He received the B.S. and M.S. degree in Electrical and Electronic Engineering (EEE) from Nanyang Technological University (NTU), Singapore, in 2004 and 2008. His research interest focuses mainly on advanced sub-micron semiconductor devices and structures.
W. L. Goh is an Associate Professor at the School of Electrical and Electronic Engineering (EEE) at the Nanyang Technological University (NTU) in Singapore. She obtained both her B.Eng and Ph.D. degrees from the department of Electrical and Electronic Engineering at the Queen’s University of Belfast (QUB) in United Kingdom. She is also the Assistant Head of Division at the Division of Circuits and Systems. Dr. Goh’s research interests are on silicon device process technology, Nanowire SOI devices, and digital and mixed-signal IC designs for low-power application. Dr. Goh has to-date co-authored 1 book, filed 16 patents (granted), and published more than 70 research papers in international journals and conferences.

G. Q. Lo, photograph and biography not available at the time publication.

L. Chan is a Fellow with Chartered Semiconductor Manufacturing Ltd., Singapore. He received his Ph.D. degree in Chemical Engineering from the University of Minnesota in 1985. Previously, he has held various engineering positions with Perkin-Elmer, Honeywell and Hewlett-Packard. He joined Chartered in 1993 and led a team of R&D engineers to work on 0.8 to 0.13 µm technologies, which included process module development, test chip design, and the fabrication of RF passive components. Currently, he is directly and indirectly supervising a team of fifty postgraduate students to work on advanced CMOS processes. His research interests include ultra shallow junction, next generation lithography, source/drain engineering, gate dielectric reliability, modeling/simulation, strained Si MOS device fabrication. Published more than 120 journal publications in various areas of IC device fabrication. More than 140 US patents awarded, all in the area of semiconductor IC manufacturing.

C. M. Ng, photograph and biography not available at the time publication.