Title	High self-resonant and area efficient monolithic transformer using novel intercoil-crossing structure for silicon RFIC
Author(s)	Lim, Chee Chong; Yeo, Kiat Seng; Chew, Kok Wai Johnny; Gu, Jiang Min; Cabuk, Alper; Lim, Suh Fei; Boon, Chirn Chye; Qiu, Ping; Do, Manh Anh; Chan, Lap
Citation	Lim, C. C., Yeo, K. S., Chew, K. W. J., Gu, J. M., Cabuk, A., Lim, S. F., et al. (2008). High self-resonant and area efficient monolithic transformer using novel intercoil-crossing structure for silicon RFIC. IEEE Electron Device Letters. 29(12), 1376-1379.
Date	2008
URL	http://hdl.handle.net/10220/6272
Rights	

High Self-Resonant and Area Efficient Monolithic Transformer Using Novel Intercoil-Crossing Structure for Silicon RFIC

Chee-Chong Lim, Kiat-Seng Yeo, Kok-Wai Chew, Jiang-Min Gu, Cabuk Alper, Suh-Fei Lim, Chirn Chye Boon, Ping Qiu, Manh Anh Do, and Lap Chan

***Abstract*—Novel on-chip multiport symmetrical transformer that has high self-resonant frequency and good area efficiency is presented. This technique involves the unique way of intercrossing the transformer's primary and secondary coil using multiple metallization layers. A stacked transformer, with the same area utilization as the proposed device, is selected for performance comparison. The proposed design has demonstrated a higher self-resonant frequency in differential transmission line transformer configuration, i.e., $f_{d-\mathrm{SRF(Stacked)}} = 8$ GHz and $f_{d-\mathrm{SRF(Sym)}} = 10.35$ GHz. The structure presented is fully compatible with standard CMOS foundry processes. The silicon data reported in this letter are based on Chartered Semiconductor Manufacturing's 0.13-μm RFCMOS technology node.**

***Index Terms*—Coils, inductance, inductors, modeling, transformers.**

I. Introduction

In RECENT years, the need for the on-chip transformers has become more profound in RF circuit designs. This is mainly because many RFIC designers have started to integrate transformer blocks into their RF circuits such as VCO and PA [1]–[5]. Moreover, majority of the work reported has demonstrated enhancement in circuit performance when compared to a nontransformer integrated design. Additionally, device area consumption is a limiting factor in RFIC design, and the system-on-chip on silicon trend has also driven the need for monolithic transformers due to more than 50% area reduction provided by these structures in comparison to two-inductor designs.

Commonly, there are two main types of monolithic transformer structures: 1) interleaved and 2) stacked. These are widely used in two kinds of differential orientation: 1) flux-linkage (FL) and 2) transmission line transformer (TLT) orientation. An FL transformer is usually limited to lower frequency applications by its inherent distributed winding capacitance. Thus, the TLT is introduced for higher frequency applications. The ideal way of constructing the TLT is the use of transmission line, but this method is often too bulky for high-inductance on-chip applications. Therefore, monolithic transformer implementation has been introduced to realize a TLT in the expense of lowering the operation bandwidth. It has been proven that achieving a turn ratio of $1:n$ is relatively simpler than realizing an ideal $1:1$ monolithic transformer [2]. With this challenge identified, Lee [6] has proposed a new type of transformer structure that demonstrates a nearly $1:1$ ratio. However, Lee's proposed design is not area efficient as additional silicon area is needed to facilitate the interconnection.

In this letter, a novel method that produces an area efficient symmetrical monolithic transformer is proposed and compared with the existing stacked transformer structure. The proposed design demonstrates higher self-resonant frequency with excellent area efficiency.

II. Proposed Transformer Design

The fundamental concept of this design is derived by combining the two existing transformer configurations: stacked and interleaved. This is realized using several metallization layers for interconnects overpasses, and underpasses [7]. Inevitably, the impedance of the two coils is expected to be similar as they are physically equalized through the intercoil crossing. The 3-D view of the proposed transformer design is shown in Fig. 1, where the proposed structure is classified into two segments along the Y'–Y" axis. Each half will experience a switching from top layer to the bottom layer; the same goes for the bottom layer as shown in the cross-sectional view of the proposed design. The intercoil routing of the design can be better described by isolating one winding from the design. Fig. 2 shows the primary winding of the proposed design. The winding has an equal amount of metallization layers from various metal schemes, while maintaining the same physical length and number of turns, irrespective of the layers. In general, Fig. 1 can be summarized into an effective four-turn transformer with each coil having four half-turns of the top and bottom layers.

In the conventional transformer design, the mutual coupling is *laterally* or *vertically* unidirectional for interleaved [8] or

Manuscript received July 31, 2008. Current version published November 21, 2008. The review of this letter was arranged by Editor A. Z. Wang.

C.-C. Lim and P. Qiu are with the Division of Circuits and Systems, School of Electrical and Electronics Engineering, Nanyang Technological University, Singapore 639798, and also with the Chartered Semiconductor Manufacturing, Singapore 738406 (e-mail: limc0042@ntu.edu.sg; QIUP0001@ntu.edu.sg).

K.-S. Yeo, J.-M. Gu, C. Alper, C. C. Boon, and M. A. Do are with the Division of Circuits and Systems, School of Electrical and Electronics Engineering, Nanyang Technological University, Singapore 639798 (e-mail: EKSYEO@ntu.edu.sg; JMGu@ntu.edu.sg; ACabuk@ntu.edu.sg; ECCBoon@ntu.edu.sg; EMADO@ntu.edu.sg).

K.-W. Chew, S.-F. Lim, and L. Chan are with the Chartered Semiconductor Manufacturing, Singapore 738406 (e-mail: chewkw@charteredsemi.com; limsf@charteredsemi.com; chanlap@charteredsemi.com).

Digital Object Identifier 10.1109/LED.2008.2006765

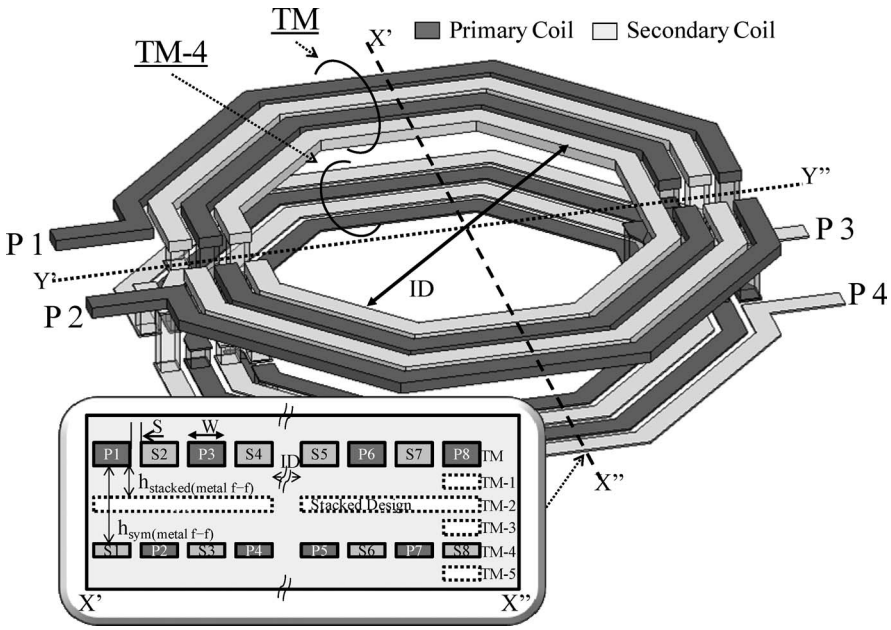

Fig. 1. Three-dimensional view of the proposed transformer design with cross-sectional view along X'–X" axis.

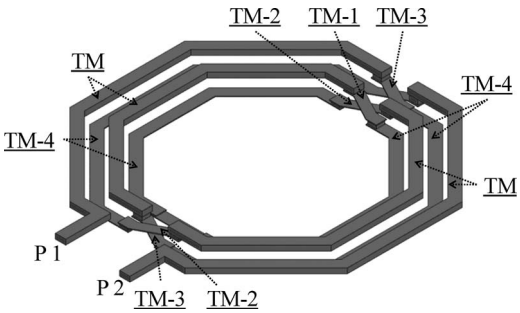

Fig. 2. Proposed design's primary winding that demonstrates the novel intercoil crossing using multiple metallization layers.

stacked design [9], respectively. However, as shown in the cross-sectional view of Fig. 1, in the proposed transformer design, a bidirectional mutual coupling can be achieved, i.e., P1 is vertically coupled with S1 and horizontally coupled with S2. The routing of the layers must also ensure that—at any time—the current does not travel in opposite direction within the same coil. This is crucial as the reverse current produces a negative self-inductance effect that will substantially reduce the overall coil inductance.

The proposed transformer's unique way of intercoil-crossing requires six metallization layers. TM and TM-4 are the layers forming the main coil, whereby TM-1, TM-2, TM-3, and TM-5 are used to form underpasses for this design. TM being the topmost metal layer and TM-5 being the bottommost layer.

III. Results and Discussion

In this letter, octagonal-shaped inductors has been taken as standard for evaluation. From the manufacturer's point of view, octagon is the closest approximation to a circle without violating any design rule. Recently, the differential circuits have become popular as they can better suppress common mode noise. Therefore, the TLT orientation with wider bandwidth has been selected to be the benchmark for all differential comparison in this letter. The measurement data are obtained using Agilent E8364B Performance Network Analyzer and Physical Layer Test System on Cascade S300 probe station. G-S-G-S-G type of Infinity probes with 100-μm pitch are carefully calibrated using SOLR (short, open, load, reciprocal thru) on Impedance Standard Substrate (ISS: 129-239) to ensure no measurement errors are brought over to the device data. The measured data are subsequently de-embedded using simple four port de-embedding techniques, as expressed in the following:

$$\begin{aligned}
[Y_{\text{less-open}}] &= [Y_{\text{DUT}}] - [Y_{\text{open}}] \\
[Y_{\text{short-open}}] &= [Y_{\text{short}}] - [Y_{\text{open}}] \\
[Z_{\text{final}}] &= [Z_{\text{less-open}}] - I \cdot [Z_{\text{short-open}}] \\
&\quad + \begin{bmatrix} a & 0 & 0 & 0 \\ 0 & a & 0 & 0 \\ 0 & 0 & b & 0 \\ 0 & 0 & 0 & b \end{bmatrix} \\
I &= \text{unit matrix} \\
a &= \frac{Z_{12(\text{short})} + Z_{21(\text{short})}}{2} \\
b &= \frac{Z_{34(\text{short})} + Z_{43(\text{short})}}{2}
\end{aligned} \tag{1}$$

where Y_{DUT} is the admittance of the DUT, Y_{open} is the admittance of the open structure, Y_{short} is the admittance of the short structure, and Z_{short} is the impedance of the short structure. All the admittance/impedance in (1) is derived from the measured S-parameters. The final Z_{final} is converted back to S-parameter for performance evaluation, i.e., S_{final}.

The de-embedded single-ended coil inductances are then extracted based on the configuration shown in Fig. 3(a). Next, the single-ended to differential mode conversion is performed based on the standard single-to-differential mode conversion

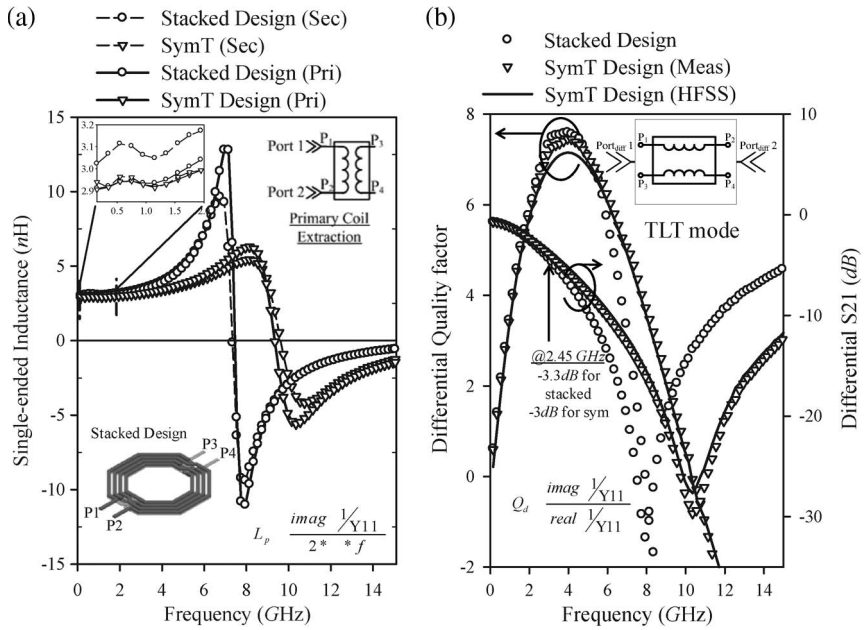

Fig. 3. (a) Individual coil inductance plot of the stacked and the proposed transformer designs together with the 3-D and the cross-sectional view of the stacked design. (b) Differential Q and S_{d21} plots of the stacked and the proposed transformer designs.

equations [10] for TLT comparison, using configuration shown in Fig. 3(b).

The design parameters for the proposed structure are as follows: Number of turns $(N)=4$, Width $(W)=6$ μm, Inner Diameter (ID) $=100$ μm, Turn spacing $(s)=2$ μm, Silicon Area $=228.28$ μm^2, Silicon thickness $(h_{\rm sil})=150$ μm, Top Metal thickness $(T_{\rm TM})=3.03$ μm, Metal 1–5 thickness $(T_{\rm TM-1}$ to $T_{\rm TM-5})=0.465$ μm, and Intermetal oxide thickness $=0.42$ μm. Among the various existing transformer configurations such as stacked, vertical coupled and Interleaved, lateral coupled, the stacked design is chosen to be the suitable candidate because it occupies the same amount of silicon area as the proposed design (228.28 μm^2). This selection is necessary, in order to conduct a fair performance comparison.

The extracted individual coil Inductance, differential quality factor (Qd), and differential S21 (S_{d21}) between the two transformers are extracted and shown in Fig. 3(a) and (b), together with the corresponding extraction technique. The experimental and EM-simulated S_{d21} (dB) and Qd are shown in Fig. 3(b). These two parameters are considered the most fundamental requirements in transformer design. In Fig. 3(b), the proposed transformer is able to attain a comparable transmission power with $|S_{d21}|$ ranging from 0.7 to 3.3 dB at lower frequency band (50 MHz–2.45 GHz). At 2.45 GHz, the proposed design demonstrates 0.3-dB enhancement in $|S_{d21}|$ as compared to stacked design. Concurrently, the stacked design has its S_{d21} roll-off faster than that of the proposed design as frequency moves beyond 6 GHz. In summary, the proposed design has also demonstrated a higher differential self-resonant frequency. The $f_{d-{\rm SRF(Stacked)}}=8$ GHz for stacked design, and the $f_{d-{\rm SRF(Sym)}}=10.35$ GHz for proposed design. This improvement in the $f_{\rm SRF}$ is attributed to the larger separation of the windings' vertical plate-to-plate distance. As shown in the cross-sectional view of Fig. 1, $h_{\rm stacked(metal\ }{}_{f-f)} < h_{\rm sym(metal\ }{}_{f-f)}$ results in a smaller overall winding capacitance. The stacked transformer is formed using layer TM and TM-2 [Fig. 3(a)] whereas the proposed design uses layer TM and TM-4.

The $\rm Qd_{peak}$ of the stacked design demonstrates a slightly higher value compared to the proposed design [Fig. 3(b)]. This phenomenon can be attributed to the increase in the overall effective coil resistance of the proposed design that is due to the mixture of thick (TM) and thin (TM-4) metal layers within the same winding.

Nevertheless, design optimization can still be incorporated into the proposed design to further enhance its performance with no additional manufacturing cost. This is achieved by via-connecting multiple thin lower metal layers (i.e., TM-2 + TM-3 + TM-4), the overall effective coil resistance will be reduced, improving the quality factor of the device.

IV. Conclusion

A monolithic transformer with excellent area efficiency has been developed. Based on the comparison with the existing stacked transformer design, the proposed structure is able to achieve up to 30% higher self-resonant frequency without degrading the differential quality factor significantly. $f_{d-{\rm SRF(Stacked)}}=8$ GHz and $f_{d-{\rm SRF(Sym)}}=10.35$ GHz for stacked and symmetrical design, respectively. In conclusion, a transformer design that is suitable for high-frequency applications, with no additional cost, has been discussed and confirmed with measured silicon databased on Chartered Semiconductor Manufacturing's 0.13-μm process.

Acknowledgment

The content presented in this letter are pending patent filed in United States of America and Singapore with the application number as *11/750,341 on 18 May 2007.*

REFERENCES

[1] J. J. Zhou and D. J. Allstot, "Monolithic transformers and their applications in a differential CMOS RF low-noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 2020–2027, Dec. 1998.

[2] J. R. Long, "Monolithic transformers for silicon RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1368–1382, Sep. 2000.

[3] D. J. Cassan and J. R. Long, "A 1-V transformer-feedback low-noise amplifier for 5-GHz wireless LAN in 0.18 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 427–435, Mar. 2003.

[4] M. Straayer, J. Cabanillas, and G. M. Rebeiz, "A low noise transformer-based 1.7 GHz CMOS VCO," in *Proc. IEEE ISSCC*, Feb. 3–7, 2002, vol. 1, pp. 286–287.

[5] W. L. Ping and S. I. Long, "A 5 GHz CMOS low phase noise transformer power combining VCO," in *Proc. IEEE RFIC Symp.*, Jun. 11–13, 2006, pp. 4–7.

[6] S.-G. Lee, "Area efficient and symmetric design of monolithic transformers for silicon RF ICs," in *Proc. IEEE Region 10th TENCON*, Sep. 15–17, 1999, vol. 2, pp. 880–882.

[7] C. C. Lim, K. W. Chew, K. S. Yeo, S. F. Lim, M. A. Do, and L. Chan, "Integrated transformer," U.S. Patent Applicat. 11/750,341, May 18, 2007.

[8] W. Gao and Z. Yu, "Scalable compact circuit model for differential spiral transformers in CMOS RFICs," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 2187–2194, Sep. 2006.

[9] C. C. Lim, K. S. Yeo, C. Y. Tan, K. W. Chew, J. G. Ma, M. A. Do, and L. Chan, "Equivalent circuit model of a stacked inductor for high-Q on chip RF applications," *Proc. Inst. Elect. Eng.—Circuits, Devices, Syst.*, vol. 153, no. 6, pp. 525–532, Dec. 2006.

[10] J. Martens, D. Judge, and J. Bigelow, "Multiport vector network analyzer measurement," *IEEE Microw. Mag.*, vol. 6, no. 4, pp. 72–81, Dec. 2005.