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K-locked-loop and its application in Time Mode ADC

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Abstract—VCO is commonly used in time mode ADC to convert analog input voltage to time/phase information, where the time/phase information is subsequently converted to digital code using time-to-digital converter. Although high speed high resolution time-to-digital converters are currently available, the inherent nonlinear property of VCO however has become the bottle neck for time mode ADC. In this paper, a new concept named K-locked-loop is proposed to solve the nonlinearity issue of VCO within a time mode ADC. A 9-bit, 0.5MS/s time mode ADC has been modeled using SIMULINK tool in Matlab. Some of the circuits are simulated using Spectre simulator tool in Cadence using the 0.18µm CSM process, and the simulation result is back annotated to SIMULINK model to make the behavioral modeling more comprehensive and accurate.

Index Terms—K-locked-loop, time mode ADC, VCO

I. INTRODUCTION

Time mode ADC has begun to gain popularity recently due to its more digital intensive circuit topology as compared to conventional voltage-mode ADC. Conventional voltage-mode ADC such as flash, SAR, and pipelined ADC use voltage comparator and op-amps as the analog processing blocks. As the technology move towards deep submicron regime, the performance of analog device, e.g., the $g_{m}/g_{ds}$ ratio degrades considerably. The signal-to-noise ratio (SNR) also suffers as the voltage is scaled down continuously however noise does not scale accordingly [1]. Since time resolution improves despite the reduction in supply voltage, time-mode signal processing offers a better solution compared to that of existing voltage-based method [5].

The operating principle of a time-mode ADC is well described in the literature [2]-[6]. In general, two main approaches are currently used in Nyquist rate time-mode ADC. The first approach uses nonlinear inverter chain as the voltage-to-time converter, and the nonlinearity error is corrected later by digital post-processing. The delay time $t_d$ of a CMOS gate is in general a nonlinear function of supply voltage and is given by the following equation [2] – [4]:

$$t_d = \frac{bC_1V_{in}}{(V_{in} - V_{th})^a}$$

where $b$ and $a$ are constants, $C_1$ is the load capacitance, $V_{th}$ is the threshold voltage, and the power-supply is the analog input voltage $V_{in}$. If $V_{in}$ is held constant during $T_s$ and one delay unit composed of two CMOS gates, then the number of delay unit passages of the propagating pulse within each sampling time $T_s$ has been proven [2] to be given by

$$S_j(V_{in}, T_s) = \int_{(j-1)T_s}^{jT_s} \frac{(V_{in} - V_{th})^a}{2bC_1V_{in}} dt = \frac{(V_{in} - V_{th})^a}{2bC_1V_{in}} - T_s$$

As can be seen from (2), the relationship between digital output $S_j(V_{in}, T_s)$ and input voltage $V_{in}$ is monotonic but not linear [2]. The nonlinearity error can be corrected by digital post-processing using reference points [4]. This approach has the benefit of an all-digital implementation and therefore scale well with technology. However, the digital output result is rather inaccurate at high temperature as the characteristic of the delay chain drift with temperature change. The second approach uses linear delay line, e.g., current-starved VCO as the voltage-to-time converter [5]-[6], thereby ensures a linear relationship between digital output and analog input. However, utilizing current-starved inverter as the delay element suffers from a limited linearity range problem, as the current-starved inverter is only linear around a fixed biasing point.

II. THE CONCEPT OF K-LOCKED-LOOP

The nonlinearity of time-mode ADC stems from the fact that the delay time $t_d$ of a delay element is a complicated function of analog input voltage $V_{in}$ as in (1). One possible way to ensure a linear relationship between digital output $S_j(V_{in}, T_s)$ and analog input voltage $V_{in}$ is by ensuring the average value of the delay time $t_d$ denoted here as $t_{d\_avg}$ is related to $V_{in}$ as follows:

$$t_{d\_avg} = \frac{K_{eff}}{V_{in}}$$
where $K_{\text{eff}}$ is a constant value, and $V_{\text{in}}$ is held constant during $T_e$. The digital output can then be proven to be related to $V_{\text{in}}$ by a simple linear function as follows:

$$S_f(V_{\text{in}}, T_e) = \frac{T_s}{t_{\text{avg}}} = \frac{V_{\text{in}}}{K_{\text{eff}}^*} T_s$$

(4)

This leads to a new concept named here as K-locked-loop—keeping $K_{\text{eff}}$ constant by ensuring $t_{\text{avg}} = \frac{V_{\text{in}}}{K_{\text{eff}}^*}$ to be a constant value for all the input voltage prior to sampling clock $T_e$. The block diagram of the K-locked-loop is shown in Fig. 1(a), which consists of a dual-controlled ring oscillator, a digital controller, and a K-comparator.

Since the delay time $t_d$ of a delay element is a function of $V_{\text{in}}$ and $C_i$ as in (1), the K value, which is defined as $K = \frac{1}{\Delta V_{\text{in}}}$, can be changed by any variation in $V_{\text{in}}$ and/or tuning of $C_i$. The key component in the K-locked-loop is the dual-controlled ring oscillator as shown in Fig. 1(b). In addition to the voltage control, the load capacitance of each delay element can be changed through the capacitance control input to change the K value.

To illustrate the working principle of the K-locked-loop, the concept of effective K will have to be introduced. Assume that at time $t_i$ a start pulse is applied at the input in the NAND gate of a dual-controlled ring oscillator in Fig. 1(b), and the pulse initiated the oscillation in the ring oscillator. At each instant the pulse appears at the $N$th delay element, we denote the instant of time as $t_i$ for $i=1, 2,..., n$. We denote $\Delta t_i = t_{i+1} - t_i$ as the time interval between two instant of time pulses appear at the $N$th delay element. We can then derive the equation for the effective K at the $n$th instant,

$$K_{\text{eff,n}} = V_{\text{in}} / t_{\text{avg}} = \frac{V_{\text{in}}}{n} (t_{d1} + t_{d2} + ... + t_{dn})$$

(5)

$$K_{\text{eff,n}} = V_{\text{in}} / n \sum_{i=1}^{n} \Delta t_i = \frac{1}{n} \sum_{i=1}^{n} K_i$$

(6)

where $t_{di} = \Delta t_i / N$ ($N = \text{no of delay element in dual-controlled ring oscillator, (which is 16 in this design).}$) At each instant $t_i$, the K-comparator will compare $K_{\text{eff,n}}$ with $K_{\text{ref}}$. The output of K-comparator is then passed to the digital controller which has the implementation of the K locking algorithm. The output of the digital controller will then control the load capacitance of the dual-controlled ring oscillator in such a manner as to bring the $K_{\text{eff}}$ to $K_{\text{ref}}$. When $|K_{\text{eff,n}} - K_{\text{ref}}| < \sigma K$, where the value of $\sigma K$ is the largest allowable deviation of $K_{\text{eff}}$ from $K_{\text{ref}}$, the system is said to be in K-locked.

III. DUAL-CONTROLLED RING OSCILLATOR

The first delay element of a dual-controlled ring oscillator consists of a current-starved NAND gate, while the remaining $N-1$ delay elements each consists of two cascaded current-starved inverters with the input and output nodes connected to the digitally-controlled varactor cells as shown in Fig. 2. The digitally controlled varactor cell base on NAND gate type is shown in Fig. 2(b). When the digital control signal is set to ‘1’, the gate capacitance seen at the node $C_L$ is higher [7]. An $n$-bit resolution digitally-controlled varactor will have $2^n$ cells attached to the $C_L$ nodes, having $(2^n-1)C_{\text{LSB}}$ change in load capacitance, or equivalently $(2^n-1) K_{\text{LSB}}$ changes in K value.

Fig. 3 shows the variation of K value for different combination of $V_{\text{in}}$ and digital control signal $D$. In order for the dual-controlled ring oscillator to be useful in the K-locked-loop, the value for $K_{\text{eff,n}}$ must be locked to $K_{\text{ref}}$ prior to the rising edge of sampling clock $T_e$. This condition can only be fulfilled if $K_{\text{max}}(D) > K_{\text{ref}}$ and $K_{\text{max}}(D) < K_{\text{ref}}$. At the beginning of each A/D conversion, the digital code $D$ is set at the middle value, e.g. “1000000000” for a 10-bit digitally-controlled varactor. The $D$ value is changed in such a manner to bring the $K_{\text{eff}}$ value to $K_{\text{ref}}$ prior to the rising edge of the sampling clock according to the K-locking algorithm performed by digital controller, which will be explained next.

IV. DIGITAL CONTROLLER

The K-locking algorithm can be divided into 2 phases. The 1st phase of K-locking algorithm is to coarsely determine the initial K value as illustrated by the flow chart in Fig. 4. At $t_1$, if K-comparator output $b = 0$, the initial K value is immediately known to be less than $K_{\text{ref}}$. The load capacitance then switched to $C_{\text{LSB}}$ (or equivalently change the K value to $K_{\text{ref}}$). Using (6), $K_{\text{eff2}}$ can be calculated to be $0.5(2K_{\text{ref}} - 2K_{\text{max}})$, $K_{\text{eff1}}$ can be calculated to be $0.5(2K_{\text{ref}} - 2K_{\text{max}})$. If K-comparator output $b = 0$ at $t_2 (K_{\text{eff2}} < K_{\text{ref}})$, we can conclude that $K_{\text{ref}} > 2K_{\text{max}}$. The rest of the decision path can be analyzed in the similar manner. Once the initial K value is known, the system will switch the K value close to the $K_{\text{ref}}$, and the 2nd phase of the K-locking algorithm starts.

In the second phase of K-locking, the K value will oscillate around $K_{\text{ref}}$ with $\Delta K_1 > \Delta K_2 > \Delta K_3 > \Delta K_4$. The number of load capacitance changes between two consecutive sign change at
the output of the K-comparator is stored. The digital controller then changes the load capacitance to half the stored value in the opposite direction, bringing $\Delta C$ closer to $\Delta C_{\text{ref}}$ each time with a smaller change in effective K value. The working principle of the 2nd phase of the K-locking algorithm is shown in Fig. 5, while the value of $\Delta K$ and the associated $\Delta C$ in the 2nd phase of K-locking is summarized in TABLE I.

V. K-COMPARATOR

At each instant of $t_i$, the K-comparator will compare the value of $K_{\text{eff,i}}$ with $K_{\text{ref}}$. The output of K-comparator equal to ‘1’ if $K_{\text{eff,i}} > K_{\text{ref}}$, else the K-comparator will output a ‘0’. One possible implementation for the K-comparator is shown in Fig. 6.

At each $i$-th instant, the voltage at the positive input of voltage comparator is given by:

$$\frac{g_m}{C} \int_0^{t_i} V_{\text{in}} dt = \frac{g_m}{C} V_{\text{in}} t_i = \frac{g_m}{C} V_{\text{in}} \sum_{w=1}^{i} \Delta t_w = \frac{g_m}{C} \sum_{w=1}^{i} K_{\text{w}}$$

While the voltage at the negative input of voltage comparator at $i$-th instant is given by

$$i \times \frac{V_{\text{ref}}}{2^y - 1}$$

Where $y$ = no. of bits of the DAC. Setting the value of $g_m/C$ to be

$$\frac{g_m}{C} N = \frac{V_{\text{ref}}}{2^y - 1} \frac{1}{K_{\text{ref}}}$$

The system is effectively comparing $K_{\text{eff,i}}$ with $K_{\text{ref}}$ at each $i$-th instant. For higher linearity requirement, the RC-type integrator might be used instead. In this design, 7-bit DAC with 10-bit accuracy are required. The system converges to the desired K value within $2^y$ cycles. For higher resolution requirement, e.g., 12-bit, such a system will converge within $2^y$ cycles, which will require an 8-bit DAC with 13-bit accuracy.

VI. SIMULINK MODEL AND SIMULATION RESULTS

The SIMULINK model for the time mode ADC is shown in Fig. 7. Each of the SIMULINK model is described below.

- Dual-controlled ring oscillator: $\text{fcn1}$ is used to model the K dependence on analog input voltage when half of the digitally controlled varactor cells are switched at ‘1’. The relationship can be modeled by a nonlinear function $y=\text{A}u^\text{B}$, where $\text{A} = 1.072e^9$, $\text{B} = 0.9869$. These values are obtained from simulation of the dual-controlled ring oscillator circuit using Spectra simulator in Cadence, and the data is curve fitted to obtain the nonlinear function as well as the corresponding value for A and B. The second function $\text{fcn2}$ is used to model $t_i = K/V_{\text{in}}$. The $t_i$ signal is then used to control the propagation delay of ‘variable time delay’ block, which is used to model a delay element.

Time-to-digital: The time-to-digital converter operates by first resetting the counter and initiates the pulse to propagate around the ring oscillator. The number of edges appears at the ‘variable time delay’ block is counted by a dual-edge triggered counter. To model the instant of time when the pulse appears at the end of ring oscillator circuit which consists of $N=16$ delay units, a ‘mod’ function is used. $M = \text{mod} (\text{counter output, } 16)$. The instant of time when $M = 0$ is $t_i$.

K-comparator: K-comparator consists of a triggered DAC and a sampled integrator as shown in Fig. 7. The latency of the K-comparator is modeled as well.
**Digital controller:** the digital controller is modeled using stateflow® together with the SIMULINK models. The algorithm has been described in section IV.

**Clock generator:** clock generator generates the start signal \( PA \) and the sampling clock signal \( PB \) from a reference clock as shown in Fig. 7. When the start signal (PA) is high, the system will reset the counter, enable the ring oscillator and reset the DAC. At the rising edge of the sampling clock \( T_s \), the system will latch the output of the counter and reset the analog integrator. The process will repeat itself for all the subsequent clock cycles.

A 9-bit, 0.5MS/s time mode ADC is modeled in SIMULINK. The linearity is simulated by sweeping \( V_{in} \) for 513 points from 1.2V to 1.6V (V_LSB =0.78125mV). The result is plotted in Fig. 8 and found to be linear up to 9-bit without any missing codes. The variation of K value during the beginning phase of K-locking for \( V_{in} = 1.4V \) is plotted in Fig. 9, following the K-locking algorithm as described in section IV.

**VII. CONCLUSION**

The K-locked-loop is proposed to solve the nonlinearity issue by ensuring the effective K value locked to \( K_{ref} \) across the entire input voltage range (400mV). A 9-bit, 0.5MS/s time mode ADC is modeled as a proof of concept, the speed can be improved with a better dual-controlled ring oscillator topology or with smaller feature-size technology. Scaling in technology is beneficial for the K-locked-loop due to its digital intensive implementation, except for its K-comparator. Future research work should therefore focus on digital implementation of the K-comparator, thereby achieving all-digital-K-locked-loop.

**REFERENCES**


