This document is downloaded from DR-NTU, Nanyang Technological University Library, Singapore.

Title	Comparative study of non-standard power diodes
Author(s)	Tan, Cher Ming; Raghavan, Nagarajan; Sun, Lina; Hsu, Chuck; Wang, Chase
Citation	Tan, C. M., Raghavan, N., Sun, L., Hsu, C., & Wang, C. (2009). Comparative study of non-standard power diodes. IEEE Conference on Industrial Electronics and Applications (4th:2009:Xian,China)
Date	2009
URL	http://hdl.handle.net/10220/6291
Rights	© 2009 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE. This material is presented to ensure timely dissemination of scholarly and technical work. Copyright and all rights therein are retained by authors or by other copyright holders. All persons copying this information are expected to adhere to the terms and constraints invoked by each author's copyright. In most cases, these works may not be reposted without the explicit permission of the copyright holder. http://www.ieee.org/portal/site This material is presented to ensure timely dissemination of scholarly and technical work. Copyright and all rights therein are retained by authors or by other copyright holders. All persons copying this information are expected to adhere to the terms and constraints invoked by each author's copyright. In most cases, these works may not be reposted without the explicit permission of the copyright holder.

Comparative Study of Non-Standard Power Diodes

Cher Ming Tan[1, *] *(Senior Member, IEEE)*
Division of Circuits & Systems
School of Electrical & Electronics Engineering (EEE)
Nanyang Technological University (NTU), Singapore.
Email: ecmtan@ntu.edu.sg

Nagarajan Raghavan[2] *(Member, IEEE)*
Advanced Materials for Micro & Nano Systems
Singapore-MIT Alliance (SMA)
National University of Singapore (NUS), Singapore.
Email: g0702024@nus.edu.sg

Lina Sun[3]
Division of Circuits & Systems
School of Electrical & Electronics Engineering (EEE)
Nanyang Technological University (NTU), Singapore.

Chuck Hsu[4], Chase Wang[5]
Sino-American Silicon Products Inc.
No. 8 Industrial East Road 2
Science-based Industrial Park
Hsinchu, Taiwan.

***Abstract*— Various non-standard power diode structures have been proposed which are superior in performance in comparison to the standard power diode. However, each of these structures help optimize certain electrical parameters with corresponding trade-offs for others. In this work, the electrical parameters of three non-standard diode structures viz. SPEED diode, BUFFER diode and CLC (Carrier Lifetime Control) diode are evaluated in comparison to those of the conventional P^+NN^+ standard diode. A Design of Experiment (DOE) combined with extensive MEDICI simulation is performed, followed by Response Surface Methodology (RSM) to empirically relate the electrical parameters with the diode structural and doping parameters. A global optimization algorithm, known as Simulated Annealing (SA) is used to optimize each individual electrical parameter. Sensitivity analysis for the optimized electrical parameter is also performed to study the effects of inherent process variations on the device electrical parameters, indicating the manufacturability of the non-standard power diodes.**

***Index Terms*— SPEED diode, BUFFER diode, CLC diode, MEDICI Simulation, Response Surface Method, Sensitivity Analysis, Simulated Annealing, Manufacturability.**

I. INTRODUCTION

The quest for faster switching, lower forward voltage drop and higher reverse blocking voltage in power diodes has been on-going for more than a decade, and it is becoming more crucial as most of the other power semiconductor devices are able to achieve high switching speed and low loss operation. The difficulty in achieving the required high performance for power diodes stems from its simple device structure such that all the electrical performances of a diode are closely linked to one another through just a few device structural and doping parameters. As a result, extensive device simulation combined with statistical optimization algorithms is required to optimize the electrical performance parameters of the diode.

Various non-standard power diode structures have been proposed in the past based on different principles in order to optimize its electrical performance parameters. From the understanding of the device physics of power diodes, three main principles are employed in order to achieve high diode performance, namely the drift region control method, carrier injection method and carrier lifetime control method [1].

BUFFER diode structure was first reported in 1981[2] where the drift region control technique was employed. A lightly doped N^- layer is inserted between the P^+ and N layers of a *standard diode*. This N^- layer helps in achieving softer recovery, higher punchthrough voltage and reduced voltage spikes. Subsequently, the *SPEED (Self-Adjusting P-Emitter Efficiency Diode)* structure was proposed using the *carrier injection (emitter efficiency) control* method [1, 3] in which a thick lightly-doped p-emitter region is integrated with a highly doped P^+ region at the surface. This structure improves the reverse recovery characteristics, reduces forward voltage drop and maintains a high reverse blocking voltage. Lastly, the *CLC (Carrier Lifetime Control)* method is to engineer the minority carrier lifetime profile in a diode so as to reduce the leakage current, turnoff time and peak reverse recovery current [4, 5].

Although the non-standard power diode structures mentioned above generally perform better than the standard power diode, not all the electrical parameters of the diodes can be optimized at the same time. While a few parameters are optimized, others might be more degraded as compared to the standard diode. It is therefore necessary to span the large parameter space of the possible structural and doping parameters to determine the optimal value of the electrical parameters in each device and investigate the practicality of their implementation with respect to the values of the other non-optimized parameters. Furthermore, the sensitivity of the optimized parameters with respect to inherent process variations of power diode manufacturing must be examined in order to examine its manufacturability where a high sensitivity implies non-manufacturability at reasonable cost. It is the purpose of this work to explore the practicality and manufacturability of the various power diode structures in

Authorized licensed use limited to: Nanyang Technological University. Downloaded on March 03,2010 at 20:44:52 EST from IEEE Xplore. Restrictions apply.

comparison to the simple standard diode structure.

Medici device simulator is employed in this work. Design of Experiment methodology (DOE) is used to examine the large parameter space effectively, and Simulated Annealing (SA) is applied to determine the global optimal values of the electrical parameters of the diodes.

II. Power Diode Structures and Definitions

A. Standard Power Diode

The structure of a standard power diode (P^+NN^+) is shown in Fig 1 where N_d^+ is fixed at 1×10^{21} cm^{-3} in order to reduce the number of parameters in the full factorial DOE matrix. The range of values for each of the input parameters is given in Table 1. These values are according to the standard practice in the power diode industry.

The standard power diodes generally have poor switching speed, large peak reverse recovery current, high reverse transient currents and voltage spikes when they are used in high voltage applications with low forward voltage drops [3]. This is the main motivation behind the exploration of other non-standard diode structures.

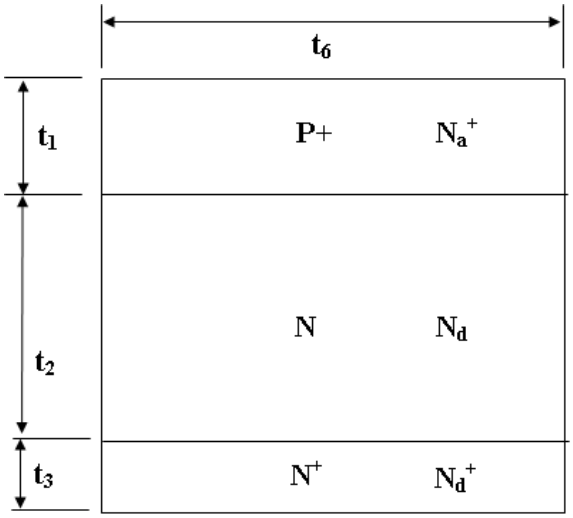

Fig.1 Structure of the STANDARD power diode.

B. SPEED Diode

The structure of the SPEED power diode (P^+PNN^+) is shown in Fig 2 where the thickness of the N^+ layer (t_4) is fixed at 50 μm and the sum ($t_5 + t_6$) is fixed at 600 μm. The range of values for other input device parameters labeled in the figure is given in Table 1.

The SPEED power diode is based on the *emitter efficiency control* technique. By controlling the carrier injection efficiency in the P^+ interface regions, reverse recovery characteristics can be improved. The thick lightly-doped p-emitter region causes injection efficiency to be low thereby reducing the total stored charge in the drift region. The lower the stored charge is, the faster the reverse recovery behavior. The P^+ regions at the surface are implanted in order to minimize forward voltage drop while keeping high reverse blocking voltage [1].

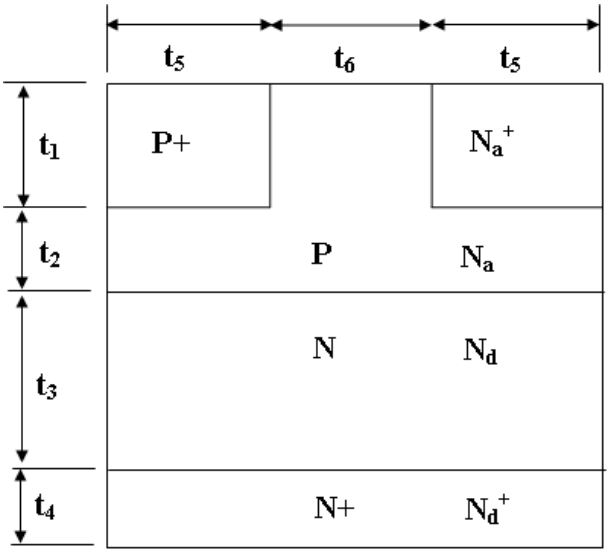

Fig.2 Structure of the SPEED power diode.

C. BUFFER Diode

The structure of the *buffer* power diode ($P^+N^-NN^+$) is shown in Fig 3 with N_d^+ set to 1×10^{21} cm^{-3} and t_4 set to 50 μm. The range of other parameters for this buffer diode is given in Table I.

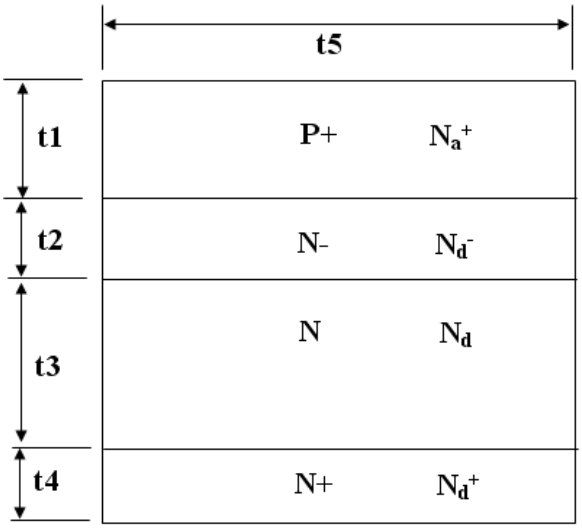

Fig.3 Structure of the BUFFER power diode.

Buffer diodes are based on the *drift region control* method where the lightly doped epitaxially grown extra N^--layer along with highly doped N-layer help prevent punchthrough and increase residual stored charge, thus ensuring softer recovery. This is in contrast to a short standard power diode which

Authorized licensed use limited to: Nanyang Technological University. Downloaded on March 03,2010 at 20:44:52 EST from IEEE Xplore. Restrictions apply.

frequently exhibits snappy recovery. However, due to the longer structure of buffer diodes, they tend to have higher forward bias voltage and peak forward recovery voltage which is undesirable as it leads to higher power consumption. [1].

D. Carrier Lifetime Control (CLC) Diode

The structure of the *CLC* power diode (P^+NN^+) investigated in this study is shown in Fig 4 with t_3 fixed at 50 μm and N_d^+ fixed at $1x10^{21}$ cm^{-3}. Other parameters vary as defined by the DOE matrix. The range of the input structural and doping parameters is shown in Table I. The carrier lifetimes are reduced by introducing recombination centers through various means in order to reduce the leakage current and the peak reverse recovery current.

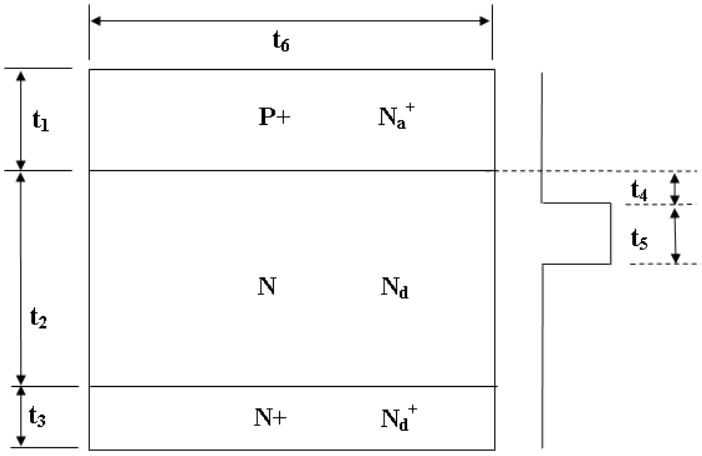

Fig. 4 Structure of the CLC power diode.

E. Parameter and Signal Definitions

To assess the electrical output performances of the four diodes studied here, including the standard power diode, an appropriate standard input waveform must be provided, as shown in Fig 5. The values of the input signal parameters are determined such that the maximum peak inverse voltage (PIV) is 80% of the breakdown voltage of the diodes as is usually done in actual measurement, and the dV/dt is maintained for all the diodes. The value of V_o is such that I_F = 2A.

The expected output current transient waveform for the input waveform is shown in Fig 6 with the parameters of interest described in Table II.

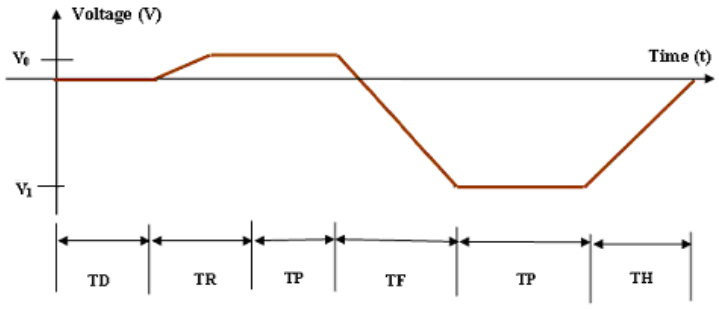

Fig.5 Input waveforms for the diode under study.

TABLE I
RANGE OF INPUT PARAMETER VALUES FOR DIFFERENT DIODE STRUCTURES

Parameter	MIN	MAX		Parameter	MIN	MAX
STANDARD POWER DIODE						
t_1 (μm)	10	100		t_6 (mm)	0.7	1.1
t_2 (μm)	50	200		N_a^+ (cm^{-3})	$1x10^{18}$	$1x10^{21}$
t_3 (μm)	50	50		N_d (cm^{-3})	$1x10^{14}$	$1x10^{17}$
SPEED POWER DIODE						
t_1 (μm)	10	50		t_6 (mm)	100	500
t_2 (μm)	10	50		N_a^+ (cm^{-3})	$1x10^{18}$	$1x10^{21}$
t_3 (μm)	50	200		N_a (cm^{-3})	$1x10^{14}$	$1x10^{18}$
t_4 (μm)	50	50		N_d (cm^{-3})	$1x10^{14}$	$1x10^{18}$
t_5 (μm)	100	500		N_d^+ (cm^{-3})	$1x10^{18}$	$1x10^{21}$
BUFFER POWER DIODE						
t_1 (μm)	10	100		N_a^+ (cm^{-3})	$1x10^{18}$	$1x10^{21}$
t_2 (μm)	5	50		N_d^- (cm^{-3})	$1x10^{12}$	$1x10^{15}$
t_3 (μm)	5	150		N_d (cm^{-3})	$1x10^{14}$	$1x10^{18}$
t_5 (μm)	700	1100				
CLC POWER DIODE						
t_1 (μm)	10	100		t_6 (mm)	700	1100
t_2 (μm)	50	100		N_a^+ (cm^{-3})	$1x10^{14}$	$1x10^{17}$
t_4 (μm)	0	25		N_d (cm^{-3})	$1x10^{18}$	$1x10^{21}$
t_5 (μm)	0	25				

TABLE II
DEFINITIONS FOR THE ELECTRICAL OUTPUT PARAMETERS

V_R	Reverse Breakdown Voltage
V_F	Forward Voltage Drop
I_{RM}	Reverse Transient Peak Current
S	Softness Factor
t_s	Time difference between I = 0 and I = I_{RRM}
t_{rr}	See Fig 6
M1	S/t_{rr}
M2	$1/(t_{rr}V_F)$
M3	$1/(t_{rr}I_R)$

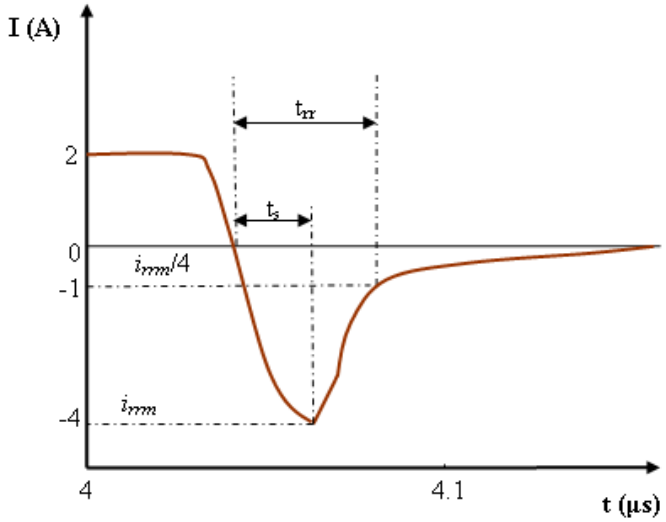

Fig. 6 Output power diode current waveform signal illustrating the definitions of various electrical parameters.

III. MEDICI SIMULATION AND STATISTICAL ANALYSIS

Given the range of values for the doping and structural parameters for each type of diode, different combination of the various device parameters can be obtained using a full-

Authorized licensed use limited to: Nanyang Technological University. Downloaded on March 03,2010 at 20:44:52 EST from IEEE Xplore. Restrictions apply.

factorial design of experiment (DOE) matrix [7]. The output electrical parameters of each type of diode are obtained from the MEDICI simulation for a given combination of the device parameters.

Following the extraction of the output electrical parameter values for different combinations of the device doping and structural parameter values, Response Surface Method (RSM) [8] is used to obtain an empirical relationship showing the dependence of the respective output electrical parameters on the input device parameters. The expressions for all the output electrical parameters of a STANDARD diode obtained using RSM is shown in the Appendix A as an illustration.

Having obtained the above-mentioned empirical relationships, the most significant doping and structural parameters that have the greatest impact on the electrical output parameter value for each of the diodes are identified using *analysis of variance* (ANOVA) [9] and the results of this analysis are indicated in Table III below.

TABLE III
SIGNIFICANT DEVICE PARAMETERS (*) FOR EACH ELECTRICAL OUTPUT PARAMETER

STANDARD DIODE									
	V_F	V_R	I_{RM}	S	t_s	t_{rr}	M1	M2	M3
t_2	*	*	*	*	*	*	*	*	*
t_6				*		*			
N_a^+			*						*
N_d	*	*	*		*		*	*	
SPEED DIODE									
	V_R	V_F	I_{RM}	S	t_s	t_{rr}	M1	M2	M3
t_1	*	*		*				*	
t_2	*	*						*	
t_3	*	*	*	*					*
t_5	*	*	*	*				*	
N_a^+		*			*	*			
N_a	*	*		*		*		*	*
N_d	*	*	*	*		*	*	*	*
N_d^+		*					*		
BUFFER DIODE									
	V_F	V_R	I_{RM}	S	t_s	t_{rr}	M1	M2	M3
t_1								*	
t_2	*	*	*	*	*	*	*	*	
t_3	*	*	*				*	*	*
t_5			*	*				*	*
N_a^+	*				*				
N_d^-	*	*		*			*		
N_d	*	*		*	*	*	*	*	*
CLC DIODE									
	V_F	V_R	I_{RM}	S	t_s	t_{rr}	M1	M2	M3
t_1	*	*	*	*	*	*	*	*	*
t_2		*		*					*
t_3									
t_4		*			*	*		*	*
t_5		*		*				*	*
t_6				*	*	*		*	*
N_a^+	*	*		*				*	*
N_d	*	*	*		*	*	*	*	*

IV. SIMULATED ANNEALING FOR GLOBAL OPTIMIZATION

To compare the optimum performance capabilities of all the four diodes, it is necessary to optimize their electrical output parameters given by the empirical equations as illustrated for the case of the STANDARD diode in Appendix A. Since most of these equations have 4 – 8 input variables and *global optimization* to find the most optimal value of an electrical parameter is required, an efficient *n-dimensional global optimization* based metaheuristics algorithm is needed. In this work, *Simulated Annealing (SA)* algorithm [10, 11] is chosen because of its efficiency and effectiveness.

We apply SA to optimize the empirical diode electrical parameter equations. In this case the objective function $\boldsymbol{F}$ corresponds to electrical parameters such as V_F, V_R, t_s, t_{rr}, I_{RM}, S etc… and the input vector $\boldsymbol{x}$ represents the set of structural and doping parameters $\{N_D, N_A, t_4, t_6 \ldots\}$.

Once the optimal values of the doping and structural parameters for the device are found, the optimal output electrical parameter value and the values for the other non-optimized output parameters are determined from the empirical equation as determined using RSM as mentioned earlier. This is repeated for other output electrical output parameters of all the other diodes. The results are summarized in Appendix B.

V. SENSITIVITY ANALYSIS

Having determined the optimal values of each individual electrical output parameter for every diode, it is necessary to examine the magnitude of change of the electrical parameter value when certain percentage change in the structural/doping parameter value occur. This is because fabrication processes are frequently subject to variations of around 10% in power diode manufacturing. The effects of these variations on the electrical parameters must be examined in order to investigate its manufacturability. If the electrical output parameters for a given diode are very sensitive to the variation of the doping/structural parameters, then it is not suitable for manufacturing at reasonable cost.

Sensitivity of an n-dimensional function *f* with respect to one of its variables x_i is simply defined as a partial derivative $\frac{\partial f(x_1,\ldots,x_n)}{\partial x_i}$. With this definition, the sensitivity analysis is performed for all the electrical output parameters with respect to all the structural/doping input parameters for the four diodes examined. A 10% change in the input variable is considered and the percentage change in the corresponding output variable is calculated. The sensitivity analysis is performed only with respect to the significant variables identified in the *ANOVA* analysis. Appendix C lists the effect of 10% variation of a single input parameter on the electrical output parameter for all the four diodes.

Since most of the structural/doping factors are subject to process-induced variations simultaneously, it would be useful

Authorized licensed use limited to: Nanyang Technological University. Downloaded on March 03,2010 at 20:44:52 EST from IEEE Xplore. Restrictions apply.

also to assess the impact on the electrical output parameter by varying all the input parameters simultaneously by ±10%. Table IV shows the results for this analysis.

TABLE IV
SENSITIVITY ANALYSIS OF EACH ELECTRICAL PARAMETER WHEN ALL THE INPUT PARAMETERS CHANGE BY 10%

Output Parameter [% CHANGE]				
STANDARD DIODE				
V_R	V_F	I_{RM}	S	t_s
6.46 %	0.74 %	1270.43 %	56.50 %	11.96 %
t_{rr}	M_1	M_2	M_3	
9510.36 %	7.72 %	8.00 %	31.29 %	
SPEED DIODE				
V_R	V_F	I_{RM}	S	t_s
9.21 %	21.43 %	2120.37 %	11.91 %	145400 %
t_{rr}	M_1	M_2	M_3	
219.09 %	4.18 %	10.88 %	19.92 %	
BUFFER DIODE				
V_R	V_F	I_{RM}	S	t_s
9.63 %	0.98 %	15175.59 %	9.27 %	23465.57 %
t_{rr}	M_1	M_2	M_3	
2051.04 %	4.51 %	4.00 %	30.50 %	
CLC DIODE				
V_R	V_F	I_{RM}	S	t_s
4.73 %	80.73 %	61.58 %	17.01 %	42628.82 %
t_{rr}	M_1	M_2	M_3	
7296.73 %	13.49 %	10.29 %	13.39 %	

VI. RESULTS & DISCUSSION

From Appendix B, we can see that the CLC diode has the highest reverse breakdown voltage (V_R) and the highest values of M_1 and M_2 as compared to the other type of diodes. Moreover, it has a reasonably low value of t_{rr}. However, both the leakage current I_{RM} and forward voltage drop V_F are increased as a result. It can also be seen that I_{RM} is the highest for the CLC diode, and V_F for CLC diode is also relatively high compared with other non-standard diodes. But the large M_1 and M_2 values imply that the CLC diode has a better balance between the switching speed and the softness of reverse recovery, as well as the switching speed and forward voltage drop.

In comparison, SPEED diodes have the lowest optimal forward voltage drop (V_F) and lowest storage time, t_s as expected. The reduced storage charge in the drift region also reduces the leakage current. The highly doped P^+ regions provide high injection efficiency only at high current densities to minimize forward voltage drop (V_F). The reduced storage charge implies high *di/dt* during recovery, causing voltage spikes and snappy recovery to occur. Thus, the softness factor (S) is the lowest for SPEED diodes.

As for the BUFFER diode, leakage current (I_{RM}) and recovery time t_{rr} are quite low and reverse breakdown voltage (V_R) is relatively high as compared to the other type of diodes as can be seen in Appendix B. However, due to the presence of the lightly doped N^- layer of BUFFER diode, the forward voltage drop (V_F) is one of the highest amongst the other devices.

The STANDARD diode, on the other hand, is superior as compared to the non-standard structures in two aspects viz. softness factor (S) and M_3. Since there is adequate charge storage in the drift region of standard diodes, recovery is slow and smooth, thus causing the softness factor (S) to be the highest. Large M_3 indicates a better performance for the conventional diode on the trade-off between switching speed and leakage current. As for the other electrical output performance parameters, the non-standard device structures have better optimal performance as compared to the standard diode.

Our analysis so far has focused only on the value of each of the individual optimized parameter values. We have not considered the values of the non-optimized electrical output parameters of a diode with the doping and structural parameters that give the optimal value of the output parameter considered. For example, while V_R = -3650V is the highest reverse breakdown voltage, which is found in a CLC diode, the corresponding non-optimized V_F value is as large as 6.20V, which is too high to be practical. Similarly, while V_F = 0.421V is the lowest forward voltage drop observed in a SPEED diode, the corresponding value of reverse bias breakdown (V_R) is only -102.37V, which could be too small for some applications. Therefore, consideration of optimized parameters alone is not sufficient, and it is more useful to compare the devices using M_1, M_2 and M_3 which have a combination of a few electrical parameters embedded in them. In this work, we show that M_1 and M_2 are the highest for CLC diodes whereas M_3 is the highest for the standard diode.

We next analyze the sensitivity analysis data in Table IV. For the STANDARD diode, the I_{RM} value is highly sensitive to t_2 and N_D while t_{rr} is highly sensitive to t_2 and t_6. S is also found to be very sensitive to t_6. All the other parameters are relatively insensitive to any process variations. Similar conclusions for the other type of diodes can be made.

On the whole, we can see that I_{RM}, t_s and t_{rr} are the three most critical electrical output parameters which vary significantly with respect to minor process variations. Sensitivity for I_{RM}, t_s and t_{rr} are the lowest in CLC, Standard and SPEED diodes respectively in ascending order. All these three parameters are extremely sensitive in the case of a BUFFER diode. Therefore, it may be concluded that the BUFFER diode structure has poor manufacturability.

VII. CONCLUSION

A comprehensive device simulation over a large parameter space of the structural and doping concentrations for STANDARD, SPEED, BUFFER and CLC diodes has been conducted. Followed by a sequence of rigorous statistical algorithms such as Response Surface Method, ANOVA analysis, Simulated Annealing and Sensitivity Analysis, the optimal electrical performance of these type of diodes and their sensitivity is computed.

Authorized licensed use limited to: Nanyang Technological University. Downloaded on March 03,2010 at 20:44:52 EST from IEEE Xplore. Restrictions apply.

The results of the analysis reveal that although the non-standard power diode structures perform better than the standard diode structures for most of the electrical parameters, the high sensitivity of the peak dynamic leakage current (I_{RM}) and recovery times {t_{rr}, t_s} with respect to the doping and structural parameters in the non-standard power diodes could deter their manufacturability. Also, we found that while focusing on the optimal performance of a single electrical parameter, it is also very important to examine whether the values of the non-optimized electrical output parameters are realistic enough for practical implementation.

Since the sensitivity of all the three parameters {I_{RM}, t_s, t_{rr}} is extremely large for the BUFFER diode, it is not a preferred diode in favor of the other three type of diode structures which show far better sensitivity results.

ACKNOWLEDGMENT

The authors would like to thank *Sino-American Silicon Product Inc.*, *Hsinchu, Taiwan* for their financial support in this research work.

APPENDIX A

RSM EQUATIONS FOR THE STANDARD DIODE

$$V_R = -62612.0 + 3.03t_1 - 29.22t_2 - 2.43t_6 + 221.16\log_{10}(N_a^+) + 7759.25\log_{10}(N_d) - 0.0109t_1^2 - 0.000920t_1t_2 + 0.0000172t_1t_6 - 0.0865t_1\log_{10}(N_a^+) - 0.00183t_1\log_{10}(N_d) + 0.00873t_2^2 + 0.0000989t_2t_6 + 0.324t_2\log_{10}(N_a^+) + 1.29t_2\log_{10}(N_d) + 0.00000642t_6^2 + 0.0621t_6\log_{10}(N_a^+) + 0.0751t_6\log_{10}(N_d) - 9.41\log_{10}^2(N_a^+) + 3.69\log_{10}(N_a^+)\log_{10}(N_d) - 247.14\log_{10}^2(N_d) \quad (1)$$

$$V_f = 13.37 + 0.00362t_1 + 0.00131t_2 + 0.000991t_6 - 0.634\log_{10}(N_a^+) - 0.855\log_{10}(N_d) + 0.00000160t_1^2 + 0.00000134t_1t_2 + 1.72\times10^{-8}t_1t_6 - 0.000201t_1\log_{10}(N_a^+) + 0.00000315t_1\log_{10}(N_d) + 0.00000983t_2^2 - 7.77\times10^{-7}t_2t_6 - 0.0000146t_2\log_{10}(N_a^+) - 0.0000803t_2\log_{10}(N_d) + 2.94\times10^{-7}t_6^2 - 0.0000126t_6\log_{10}(N_a^+) - 0.0000731t_6\log_{10}(N_d) + 0.00763\log_{10}^2(N_a^+) + 0.0226\log_{10}(N_a^+)\log_{10}(N_d) + 0.0147\log_{10}^2(N_d) \quad (2)$$

$$t_s = 1\times10^{-8}\begin{pmatrix} 3.26 - 0.00218t_1 + 0.113t_2 + 0.0354t_6 + 3.43\log_{10}(N_a^+) - 6.53\log_{10}(N_d) \\ + 0.000112t_1^2 - 0.0000725t_1t_2 - 0.00000330t_1t_6 + 0.0000275t_1\log_{10}(N_a^+) \\ + 0.000114t_1\log_{10}(N_d) - 0.000111t_2^2 - 0.0000200t_2t_6 + 0.000314t_2\log_{10}(N_a^+) \\ - 0.00404t_2\log_{10}(N_d) + 0.00000160t_6^2 + 0.00000722t_6\log_{10}(N_a^+) \\ - 0.00221t_6\log_{10}(N_d) - 0.0669\log_{10}^2(N_a^+) - 0.0522\log_{10}(N_a^+)\log_{10}(N_d) \\ + 0.290\log_{10}^2(N_d) \end{pmatrix} \quad (3)$$

$$t_{rr} = 1\times10^{-8}\begin{pmatrix} -14023.8 + 2.11t_1 + 22.68t_2 + 0.505t_6 + 719.68\log_{10}(N_a^+) \\ + 662.58\log_{10}(N_d) - 0.0184t_1^2 - 0.0000875t_1t_2 - 0.00000301t_1t_6 \\ - 0.00297t_1\log_{10}(N_a^+) - 0.000975t_1\log_{10}(N_d) + 0.0215t_2^2 - 0.0320t_2t_6 \\ - 0.0145t_2\log_{10}(N_a^+) - 0.0381t_2\log_{10}(N_d) + 0.00288t_6^2 \\ - 0.000320t_6\log_{10}(N_a^+) - 0.0691t_6\log_{10}(N_d) - 17.29\log_{10}^2(N_a^+) \\ - 2.71\log_{10}(N_a^+)\log_{10}(N_d) - 17.58\log_{10}^2(N_d) \end{pmatrix} \quad (4)$$

REFERENCES

[1] M.T.Rahimo and N.Y.A. Shammas, "A review on fast power diode development and modern novel structures", *IEE Colloqium on New Developments in Power Semiconductor Devices*, 2/1-12, 21June, 1996.

[2] Wolley E.D., Bevacqua S.F., "High Speed, Soft Recovery, Epitaxial Diodes for Power Inverter Circuits", 5th European Conference on power electronics and applications. BRIGHTON, U.K., Sept. 1993 page 368-373.

[3] S.Sawant and B.J.Baliga, "A comparative study of high voltage (4kV) power rectifiers PiN/MPS/SSD/SPEED", *11th International Symposium on Power Semiconductor Devices and ICs*, 153-156, 1999.

[4] Ettore Napoli, "Bidimensional lifetime control for high-speed low loss p-i-n rectifiers", *IEEE Transactions on Power Electronics*, Vol. 15, No. 4, pp.791 – 798, July 2000.

[5] Hazdra, P. and Komarnitskyy, V., "Lifetime control in Silicon power p-i-n diode by ion irradiation: Suppression of undesired leakage", *Microelectronics Journal*, Vol. 37, No. 3, pp.197 – 203, March 2006.

[6] "MEDICI Two Dimensional Device Simulation Program", *Version 4.1, MEDICI User Manual*, 1998.

[7] Montgomery, D.C, "Design and Analysis of Experiments", John Wiley & Sons, 6th Edition, 2004.

[8] Khuri, Andre, "Response Surface Methodology and related topics', World Scientific, 2006.

[9] Stevenson, R., "Analysis of Variance and the Design of Experiments", Lionheart Press, 1989.

[10] Brooks, S.P. and Morgan, B.J.T, "Optimization using Simulated Annealing", *The Statistician*, Vol. 44, No. 2, pp.241-257, 1995.

[11] Li, Y., Yao, J. and Yao, D., "An efficient composite simulated annealing algorithm for global optimization", *International Conference on Communication, Circuits & Systems*, Vol. 2, 2002, pp.1165-1169.

$$S = -4915.94 + 0.736t_1 + 7.85t_2 + 0.132t_6 + 247.83\log_{10}(N_a^+) + 240.10\log_{10}(N_d) - 0.00662t_1^2 + 0.000119t_1t_2 + 0.00000215t_1t_6 - 0.00115t_1\log_{10}(N_a^+) - 0.000193t_1\log_{10}(N_d) + 0.00777t_2^2 - 0.0112t_2t_6 - 0.00994t_2\log_{10}(N_a^+) - 0.00532t_2\log_{10}(N_d) + 0.00102t_6^2 - 0.000127t_6\log_{10}(N_a^+) - 0.0220t_6\log_{10}(N_d) - 6.08\log_{10}^2(N_a^+) - 0.595\log_{10}(N_a^+)\log_{10}(N_d) - 6.69\log_{10}^2(N_d) \quad (5)$$

$$M_1 = -6.48\times10^8 - 255965.0t_1 - 149889.0t_2 - 423707.0t_6 + 1.01\times10^8\log_{10}(N_a^+) - 1.96\times10^7\log_{10}(N_d) + 634.21t_1^2 + 2132.96t_1t_2 + 39.14t_1t_6 - 6896.3t_1\log_{10}(N_a^+) - 525.93t_1\log_{10}(N_d) + 2129.38t_2^2 + 475.32t_2t_6 - 59160.0t_2\log_{10}(N_a^+) + 3768.89t_2\log_{10}(N_d) + 63.91t_6^2 - 770.0t_6\log_{10}(N_a^+) + 15845.1t_6\log_{10}(N_d) - 565066.0\log_{10}^2(N_a^+) - 4.50\times10^6\log_{10}(N_a^+)\log_{10}(N_d) + 3.25\times10^6\log_{10}^2(N_d) \quad (6)$$

$$M_2 = 3.02\times10^8 - 210370.0t_1 - 615261.0t_2 - 52742.9t_6 - 7.56\times10^6\log_{10}(N_a^+) - 2.27\times10^7\log_{10}(N_d) + 55.58t_1^2 + 136.46t_1t_2 + 5.47t_1t_6 + 9485.19t_1\log_{10}(N_a^+) - 540.37t_1\log_{10}(N_d) - 385.37t_2^2 + 222.43t_2t_6 + 2280.71t_2\log_{10}(N_a^+) + 27939.3t_2\log_{10}(N_d) - 28.31t_6^2 + 850.0t_6\log_{10}(N_a^+) + 3388.31t_6\log_{10}(N_d) + 82383.8\log_{10}^2(N_a^+) + 118600.0\log_{10}(N_a^+)\log_{10}(N_d) + 630845.0\log_{10}^2(N_d) \quad (7)$$

$$M_3 = -1.23\times10^{15} - 1.14\times10^{11}t_1 + 5.01\times10^{12}t_2 - 2.51\times10^{11}t_6 + 1.49\times10^{14}\log_{10}(N_a^+) - 4.70\times10^{13}\log_{10}(N_d) + 1.04\times10^9t_1^2 - 46118.3t_1t_2 - 202592.0t_1t_6 - 1.94\times10^6t_1\log_{10}(N_a^+) - 265926.0t_1\log_{10}(N_d) - 1.26\times10^9t_2^2 + 148667.0t_2t_6 - 2.45\times10^{11}t_2\log_{10}(N_a^+) - 7.44\times10^6t_2\log_{10}(N_d) + 7.19\times10^7t_6^2 - 740083.0t_6\log_{10}(N_a^+) + 7.67\times10^9t_6\log_{10}(N_d) - 3.15\times10^{12}\log_{10}^2(N_a^+) - 9.24\times10^8\log_{10}(N_a^+)\log_{10}(N_d) + 1.28\times10^{12}\log_{10}^2(N_d) \quad (8)$$

$$I_{RM} = -0.0953 - 0.0000553t_1 - 0.000113t_2 + 0.0000400t_6 - 0.00903\log_{10}(N_a^+) + 0.0228\log_{10}(N_d) - 1.16\times10^{-7}t_1^2 - 6.88\times10^{-8}t_1t_2 + 8.99\times10^{-8}t_1t_6 - 3.64\times10^{-7}t_1\log_{10}(N_a^+) - 2.33\times10^{-8}t_1\log_{10}(N_d) - 5.94\times10^{-7}t_2^2 + 6.23\times10^{-8}t_2t_6 + 0.0000204t_2\log_{10}(N_a^+) - 0.00000826t_2\log_{10}(N_d) - 7.70\times10^{-9}t_6^2 - 8.55\times10^{-8}t_6\log_{10}(N_a^+) - 0.00000247t_6\log_{10}(N_d) + 0.000123\log_{10}^2(N_a^+) + 0.0000868\log_{10}(N_a^+)\log_{10}(N_d) - 0.000699\log_{10}^2(N_d) \quad (9)$$

Authorized licensed use limited to: Nanyang Technological University. Downloaded on March 03,2010 at 20:44:52 EST from IEEE Xplore. Restrictions apply.

APPENDIX B
OPTIMAL VALUES FOR EACH ELECTRICAL PARAMETER AND THE CORRESPONDING NON-OPTIMAL PARAMETERS

OPTIMIZED PARAMETER	STANDARD DIODE	NON-OPTIMIZED PARAMETER VALUES								
		V_R	V_F	I_{RM}	S	t_s	t_{rr}	M_1	M_2	M_3
	V_R	-1.14×10^{3}	-13.54	-144.31	-79.89	-63.46	-32.68	-63.35	-94.64	-559.95
	V_F	0.997	0.868	1.031	0.876	0.872	0.890	0.873	0.889	1.145
	I_{RM}	-0.00333	-0.00660	-9.84×10^{-5}	-0.0105	-0.00927	-0.00553	-0.00896	-0.00414	-1.65×10^{-4}
	S	3.698	35.61	0.3187	253.58	196.23	0.836	24.76	7.45	102.32
	t_s	5.24×10^{-8}	1.10×10^{-8}	3.12×10^{-8}	1.09×10^{-8}	1.01×10^{-8}	1.70×10^{-8}	1.02×10^{-8}	1.62×10^{-8}	3.45×10^{-8}
	t_{rr}	2.49×10^{-7}	9.90×10^{-7}	5.23×10^{-8}	7.18×10^{-6}	5.55×10^{-6}	2.22×10^{-8}	6.61×10^{-7}	2.18×10^{-7}	3.00×10^{-6}
	M_1	2.30×10^{7}	6.32×10^{7}	2.09×10^{7}	6.84×10^{7}	6.60×10^{7}	5.12×10^{7}	7.32×10^{7}	5.47×10^{7}	2.08×10^{7}
	M_2	6.39×10^{6}	2.25×10^{7}	1.15×10^{7}	1.89×10^{6}	1.98×10^{7}	2.25×10^{7}	2.26×10^{7}	2.52×10^{7}	2.77×10^{6}
	M_3	-2.99×10^{12}	-1.70×10^{13}	-9.78×10^{12}	-8.29×10^{12}	-1.54×10^{13}	-3.14×10^{12}	-6.62×10^{12}	-9.55×10^{11}	-4.89×10^{13}
	CLC DIODE	NON-OPTIMIZED PARAMETER VALUES								
		V_R	V_F	I_{RM}	S	t_s	t_{rr}	M_1	M_2	M_3
	V_R	-3.65×10^{3}	-77.57	-86.94	-161.68	-737.03	-840.90	-159.39	-38.97	-233.77
	V_F	6.20	0.752	0.877	0.901	1.96	2.12	0.968	1.06	1.12
	I_{RM}	-0.0297	-0.0174	-0.00786	-0.0189	-0.0239	-0.0174	-0.0206	-0.0199	-0.0122
	S	3.26	5.03	0.318	9.21	4.88	0.396	9.17	5.00	5.01
	t_s	4.43×10^{-7}	1.48×10^{-7}	2.17×10^{-7}	2.15×10^{-7}	2.29×10^{-10}	2.42×10^{-9}	9.03×10^{-8}	3.42×10^{-8}	1.17×10^{-7}
	t_{rr}	8.24×10^{-7}	4.99×10^{-7}	2.47×10^{-7}	6.67×10^{-7}	2.40×10^{-7}	2.75×10^{-9}	5.19×10^{-7}	2.31×10^{-7}	3.05×10^{-7}
	M_1	1.58×10^{8}	5.58×10^{8}	4.76×10^{8}	7.21×10^{8}	5.25×10^{8}	4.30×10^{8}	7.38×10^{8}	6.90×10^{8}	6.32×10^{8}
	M_2	9.80×10^{7}	2.74×10^{8}	2.49×10^{8}	3.21×10^{8}	2.61×10^{8}	2.40×10^{8}	3.31×10^{8}	3.26×10^{8}	3.04×10^{8}
	M_3	-2.92×10^{11}	-5.73×10^{11}	-6.26×10^{11}	-6.88×10^{11}	-5.18×10^{11}	-6.30×10^{11}	-6.82×10^{11}	-6.28×10^{11}	-7.78×10^{11}
	BUFFER DIODE	NON-OPTIMIZED PARAMETER VALUES								
		V_R	V_F	I_{RM}	S	t_s	t_{rr}	M_1	M_2	M_3
	V_R	-1.31×10^{3}	-52.19	-344.16	-332.85	-777.70	-309.93	-204.00	-103.34	-314.73
	V_F	0.931	0.849	0.988	0.997	0.978	0.945	0.925	0.893	0.938
	I_{RM}	-9.86×10^{-4}	-0.0247	-3.81×10^{-5}	-0.0602	-0.0269	-0.0385	-0.0708	-0.105	-0.0548
	S	3.63	0.782	2.93	6.47	5.76	2.63	4.41	0.897	1.45
	t_s	1.37×10^{-7}	4.11×10^{-8}	5.33×10^{-9}	6.61×10^{-9}	2.44×10^{-11}	1.00×10^{-9}	2.72×10^{-8}	1.87×10^{-8}	3.58×10^{-8}
	t_{rr}	4.79×10^{-7}	1.36×10^{-7}	2.78×10^{-8}	4.17×10^{-8}	2.38×10^{-8}	1.92×10^{-9}	4.85×10^{-8}	2.64×10^{-8}	5.48×10^{-8}
	M_1	1.52×10^{7}	2.51×10^{7}	5.86×10^{7}	1.24×10^{8}	9.68×10^{7}	6.93×10^{7}	1.29×10^{8}	8.06×10^{7}	9.29×10^{7}
	M_2	5.93×10^{6}	2.78×10^{7}	1.96×10^{7}	2.39×10^{7}	1.78×10^{7}	2.61×10^{7}	3.53×10^{7}	4.60×10^{7}	3.79×10^{7}
	M_3	-1.14×10^{9}	-1.76×10^{9}	-2.95×10^{9}	-9.38×10^{9}	-6.13×10^{9}	-4.08×10^{9}	-1.50×10^{10}	-2.54×10^{9}	-3.40×10^{10}
	SPEED DIODE	NON-OPTIMIZED PARAMETER VALUES								
		V_R	V_F	I_{RM}	S	t_s	t_{rr}	M_1	M_2	M_3
	V_R	-925.18	-102.37	-122.29	-485.25	-18.57	-70.77	-180.23	-137.73	-20.27
	V_F	3.28	0.421	0.594	1.36	1.01	0.869	0.480	0.795	1.81
	I_{RM}	-0.00202	-0.00289	-3.83×10^{-5}	-0.00773	-0.00813	-0.00498	-0.00103	-0.00236	-0.0111
	S	1.21	1.19	1.00	2.95	1.65	0.942	1.38	1.99	1.134
	t_s	2.42×10^{-8}	1.17×10^{-8}	1.63×10^{-8}	7.27×10^{-9}	1.28×10^{-12}	1.22×10^{-9}	9.69×10^{-10}	1.82×10^{-10}	1.25×10^{-9}
	t_{rr}	5.09×10^{-8}	1.77×10^{-8}	1.67×10^{-8}	4.65×10^{-8}	2.24×10^{-8}	2.02×10^{-9}	5.72×10^{-9}	7.22×10^{-9}	7.81×10^{-9}
	M_1	4.47×10^{7}	2.95×10^{8}	2.82×10^{8}	6.03×10^{7}	2.32×10^{8}	2.24×10^{8}	3.61×10^{8}	2.57×10^{8}	1.85×10^{8}
	M_2	1.26×10^{7}	1.34×10^{8}	8.35×10^{7}	1.64×10^{7}	1.02×10^{8}	1.56×10^{8}	1.52×10^{8}	1.94×10^{8}	1.61×10^{8}
	M_3	-7.85×10^{10}	-2.19×10^{9}	-3.22×10^{10}	-2.58×10^{9}	-7.43×10^{10}	-3.47×10^{10}	-5.09×10^{10}	-3.37×10^{10}	-1.84×10^{11}

Authorized licensed use limited to: Nanyang Technological University. Downloaded on March 03,2010 at 20:44:52 EST from IEEE Xplore. Restrictions apply.

APPENDIX C

SENSITIVITY ANALYSIS OF EACH OPTIMAL ELECTRICAL OUTPUT PARAMETER WITH RESPECT TO 10% CHANGE IN THE DIODE STRUCTURE / DOPING PARAMETER

Structure Parameter	SENSITIVITY OF ELECTRICAL PARAMETERS								
	STANDARD DIODE								
	V_F	V_R	I_{RM}	S	t_s	t_{rr}	M_1	M_2	M_3
t_2	0.15 %	2.27 %	-732.64 %	-7.75 %	8.12 %	-8.76×10^2 %	-3.65 %	1.36 %	26.03 %
t_6	-----	-----	-----	55.61 %	-----	6.81×10^3 %	-----	-----	-----
N_a^+	-----	-----	-11.97 %	-----	-----	-----	-----	-----	2.84 %
N_d	-0.0921%	-4.12 %	41.55 %	-----	-0.61 %	-----	1.12 %	1.20 %	-----
	CLC DIODE								
t_1	64.95 %	1.11 %	16.18 %	7.44 %	24900 %	3010.35 %	12.19 %	9.09 %	8.73 %
t_2	-----	0.985 %	-----	7.96 %	-----	-----	-----	-----	1.13 %
t_3	-----	-----	-----	-----	-----	-----	-----	-----	-----
t_4	-----	0.326 %	-----	-----	387.41 %	827.38 %	-----	0.0130 %	0.10 %
t_5	-----	0.173 %	-----	0.683 %	-----	-----	-----	0.0157 %	1.45 %
t_6	-----	-----	-----	5.11 %	12300 %	2003.87 %	-----	0.0621 %	3.47 %
N_a^+	3.11 %	0.266 %	-----	0.340 %	-----	-----	-----	0.286 %	0.0358 %
N_d	5.89 %	1.65 %	2.25 %	-----	370.28 %	116.81 %	1.01 %	1.00 %	1.29
	BUFFER DIODE								
t_1								0.121 %	
t_2	0.183 %	4.68 %	2799.35 %	3.38 %	2776.90 %	358.85 %	0.806 %	0.539 %	
t_3	8.34×10^{-2} %	1.86 %	6190.79 %				0.388 %	0.469 %	7.45 %
t_5			5569.56 %	5.37 %				2.65 %	30.74 %
N_a^+	6.70×10^{-2} %				4145.08 %				
N_d^-	15.9 %	1.15 %		0.466 %			0.394 %		
N_d	4.23×10^{-2} %	1.39 %		1.06 %	810.26 %	42.66 %	0.672 %	0.105 %	1.69 %
	SPEED DIODE								
t_1	0.93 %	2.85 %	-----	3.67 %	-----	-----	-----	0.39 %	-----
t_2	4.97×10^{-2} %	0.630 %	-----	-----	-----	-----	-----	2.25 %	-----
t_3	4.9 %	15.64 %	117.72 %	3.12	-----	-----	-----	-----	5.59 %
t_5	1.85 %	2.69 %	769.48 %	0.80 %	-----	-----	-----	5.59 %	-----
N_a^+	-----	0.389 %	-----	-----	2.21×10^4 %	16.59 %	-----	-----	-----
N_a	0.301 %	0.464 %	-----	1.23 %	-----	51.04 %	-----	0.91 %	1.76 %
N_d\	3.43 %	3.61 %	327.68 %	1.28 %	-----	15.07 %	1.13 %	1.00 %	1.92 %
N_d^+	-----	0.548 %	-----	-----	-----	-----	0.49 %	-----	-----

Authorized licensed use limited to: Nanyang Technological University. Downloaded on March 03,2010 at 20:44:52 EST from IEEE Xplore. Restrictions apply.