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THD of Closed-Loop Analog PWM Class-D Amplifiers

Wei Shu and Joseph S. Chang

***Abstract*—This paper presents an analytical modeling of the mechanisms of total harmonic distortion (THD) of second-order based single-feedback and double-feedback Class-D amplifiers (CDAs). We show that the overall THD in these closed-loop CDAs comprises the THD of their open-loop counterparts reduced by the Loop Gain+1 and the THD due to the combined phase and duty cycle error that is due to feedback, hence unique to closed-loop CDAs. We show that the latter THD can be large and is the dominant THD at high input frequencies ($>$ 3 kHz), and that the mechanisms therein are the phase and duty cycle errors. By means of double Fourier series analysis, analytical expressions for the harmonic components and thereafter a THD expression for closed-loop CDAs are derived. The derived expressions depict the parameters that affect THD, and are insightful to designers to optimize/vary pertinent parameters to reduce THD. The derived THD expression is verified against HSPICE and on the basis of measurements on a prototype CDA IC and other CDAs realized discretely.**

***Index Terms*—Class-D amplifier (CDA), duty cycle error, phase error, total harmonic distortion (THD).**

I. Introduction

CLASS-D amplifiers (CDAs) have gained general acceptance in the electronics audio community and is increasingly replacing their classical analog Class-A and Class-AB amplifier counterparts. This is primarily due to their substantially higher power-efficiency arising from the switching-mode operation of its output stage. The higher power-efficiency is a very worthwhile attribute as this practically translates to longer battery life for portable devices and reduces the form factor due to smaller/absence of heatsinks [1]. Of the modulation techniques used in CDAs, the pulsewidth modulation (PWM) [2] is probably the most prevalent modulation technique employed in analog CDAs, and is the modulation of interest in this paper. Its prevalence is largely due to its relatively lower switching frequency, high stability at near 100% modulation [3] as well as a simpler architecture.

It is generally accepted within the audio amplifier community [4] that other than the high power-efficiency advantage of CDAs over a large modulation index range, CDAs have yet to be accepted into the mainstream high-fidelity audio. This is largely because CDAs suffer from sensitivity to power supply ripple, poor frequency response linearity and relatively high noise/distortion [5] compared to their linear counterparts.

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We had previously investigated the sensitivity of CDAs to power supply ripple [6], [7] for three common CDA topologies—the open-loop CDA, the prevalent practical second-order closed-loop single-feedback CDA (1FB-CDA) and the second-order closed-loop double-feedback CDA (2FB-CDA) . We showed that the power supply ripple not only introduces the usual noise qualified by power-supply rejection ratio (PSRR), it further introduces power-supply ripple induced intermodulation distortion (PS-IMD) due to the intermodulation between the supply noise and the input signal. We further showed that closed-loop designs are advantageous over open-loop designs in terms of PSRR and PS-IMD. These advantages are attributed to the feedback mechanism and high loop gains of closed-loop designs, and this phenomenon is largely analogous to that in linear amplifiers.

Of the various parameters that qualify the fidelity of a CDA, total harmonic distortion (THD) is one of the primary parameters. The established definition of THD is

$$\%\mathrm{THD} = \frac{\sqrt{V_{\mathrm{out@}2f}^2 + V_{\mathrm{out@}3f}^2 + V_{\mathrm{out@}4f}^2 + \cdots}}{V_{\mathrm{out@}f}} 100\% \tag{1}$$

where $V_{\mathrm{out@}f}$ is the output fundamental component at f; $V_{\mathrm{out@}2f}, V_{\mathrm{out@}3f}$ and $V_{\mathrm{out@}4f}$ are the output harmonic components at $2f$, $3f$ and $4f$, respectively.

Classical linear high-fidelity amplifiers can feature extremely low THD ($<0.01\%$) and the mechanisms for THD therein are well established. Although there is considerable research effort to reduce THD of CDAs, to our knowledge, only the mechanisms for THD of open-loop CDAs have thus far been adequately modeled. These mechanisms include the modeling of the dead time of the output stage [8] and the dead time has been shown to be the primary mechanism. We [9] have modeled the nonlinear triangular carrier at the pulsewidth modulator, and showed that this is the primary mechanism of THD in some open-loop CDAs whose primary design emphases include hardware simplicity and micropower operation.

In the case of closed-loop CDAs, the mechanisms of THD remain largely inadequate because the model employed thus far [10], [11] was assumed to be linear (the pulsewidth modulator is assumed to be linear). However, as depicted in the established double Fourier series expression for the PWM signal [12], the pulsewidth modulator is in fact nonlinear. Due to this inadequacy, the THD of negative feedback closed-loop CDAs may inadvertently be estimated to be simply equal to the THD of its open-loop CDA counterpart $(\mathrm{THD_{op}})$ reduced by the Loop Gain+1 $(\mathrm{THD_{op}}/(1+GH)$ where G and H are

the forward and feedback transfer functions, respectively); for brevity, $\mathrm{THD}_{\mathrm{op}}/(1+GH)$ will be referred to as the THD predicted by the linear model. However, as we will later show (see Section IV), the actual THD of closed-loop CDAs can be much larger than that predicted analytically by the linear model. This is because the overall THD of closed-loop CDAs comprises not only $\mathrm{THD}_{\mathrm{op}}/(1+GH)$ but also the THD due to the combined phase and duty cycle error introduced by the negative feedback therein, and because the latter THD mechanisms are more significant and dominant than $\mathrm{THD}_{\mathrm{op}}/(1+GH)$ at high frequency inputs (>3 kHz).

The THD due to the combined phase and duty cycle error is unique to closed-loop CDAs due to the nonlinear pulsewidth modulation process and to negative feedback, and is absent in open-loop CDAs. We will later show that this THD is small when the input is at low frequencies (<3 kHz) and rises rapidly when input signal frequency increases. In our view, the THD in the specification of many commercial CDAs is contentious because the quoted THD is often only specified at 1 kHz—where the THD is low, for example ∼0.01%—whereas the THD should be specified for the range of the input signals whose significant harmonics are within the audio band; in linear amplifiers, their THD is often specified over the entire audio band. Put simply, a precise modeling of the THD due to the combined phase and duty cycle error in closed-loop CDAs is highly desirable. This model would depict the mechanisms of the dominant THD, particularly when the input is at relatively high frequency. This ultimately provides insight on how THD can be reduced including the optimization/variation of the pertinent parameters and/or the compromise to various parameters to meet a given set of specifications.

In this paper, the mechanisms of the THD due to the combined phase and duty cycle error are investigated by means of Fourier series analysis. We derive the harmonic components due to these errors for the prevalent and practical closed-loop 1FB- and 2FB-CDA topologies. We further derive an expression for THD. From our analysis, we will show that the THD at low frequency (<3 kHz) is very small due to the negative feedback mechanism (and that this THD can largely be predicted by the linear model), and that the dominant THD occurs at high frequency (>3 kHz) due to the negative feedback and the combined phase and duty cycle error. We also show that the 2FB-CDA, in spite of its higher loop gain than the 1FB-CDA, does not exhibit improved THD performance at high frequency due to the abovementioned errors—this contradicts what is expected in linear amplifiers. Put simply, in the overall context of feedback for THD of CDAs, feedback reduces the THD of the open-loop CDA by Loop Gain+1, but conversely introduces THD due to the combined phase and duty cycle error. The derived analytical expressions are verified by comparing them against HSPICE simulations and on the basis of experiment measurements on a fabricated prototype CDA IC and on other CDAs realized discretely. Examples are provided to depict how the THD of CDAs can be reduced without excessive hardware overhead.

This paper is organized in the following manner. In Section II, the open-loop CDA and closed-loop first-order, 1FB- and 2FB-CDAs are briefly reviewed. In Section III, the Fourier series expressions to determine the nonlinearity components of the THD

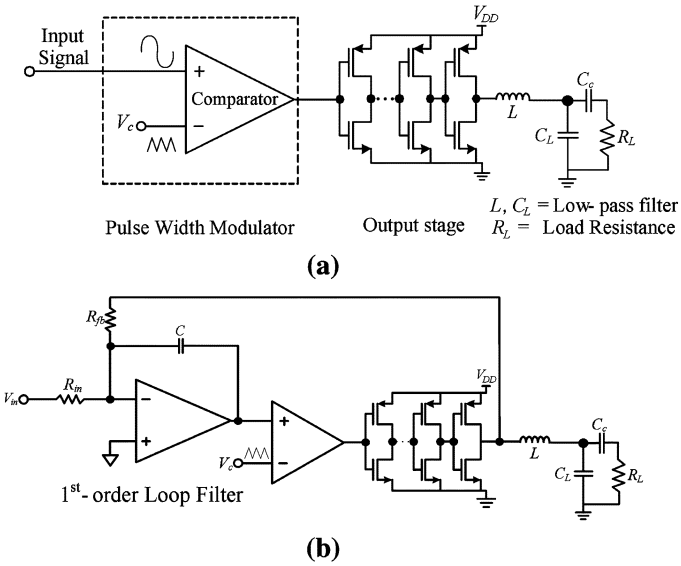

Fig. 1. Schematic of an (a) open-loop CDA and (b) a first-order CDA.

of the 1FB- and 2FB-CDAs, and thereafter an analytical expression for THD, are derived. In Section IV, the theoretical derivations are verified against simulations and measurements on a prototype IC and on other hardware realizations. Finally, conclusions are drawn.

II. Review of CDA Designs

This section succinctly reviews current-art analog CDA designs and serves as a preamble to the analysis of THD in the latter sections. The simplest CDA is an open-loop design depicted in Fig. 1(a). We [7] have shown that this design is not practical largely because of its low PSRR (−6 dB) and high PS-IMD (12 dB at full modulation index, $M = 1.0$), and the THD of this design is also usually poor, typically $\geq 0.5\%$. This CDA is often applicable only in applications without stringent fidelity requirements for example, hearing aids. We have shown that there are no parameters available to designers to reduce the power supply related distortions.

Fig. 1(b) depicts the simple closed-loop first-order CDA. We have shown that its PSRR [7], PS-IMD [7], and THD [10] are improved by ∼30, ∼20, and ∼10 dB, respectively, compared to the open-loop CDA, where the first two parameters are for the condition where the supply noise frequency is 100 Hz, the input signal frequency, $f_{\mathrm{in}} = 10$ kHz, and $M = 0.7$, and the last parameter is for the condition where $f_{\mathrm{in}} = 1$ kHz and $M = 0.7$. Although, the improvement is substantial, these parameters remain inadequate for high-fidelity applications, largely limited by the small loop gain provided for by the first-order loop filter.

In practice, the closed-loop CDA designs with sufficient high loop gain are required for low noise and these include the practical and commercial 1FB- and 2FB-CDA designs depicted in Figs. 2 and 3, respectively,. We have shown that the PSRR and PS-IMD of these CDAs are significantly improved over the first-order CDA. In the case of THD, we will now show that although 1FB- and 2FB-CDAs with high loop gains can feature excellent THD performance at low frequency, they still result in unacceptably high THD at relatively high frequency compared to linear

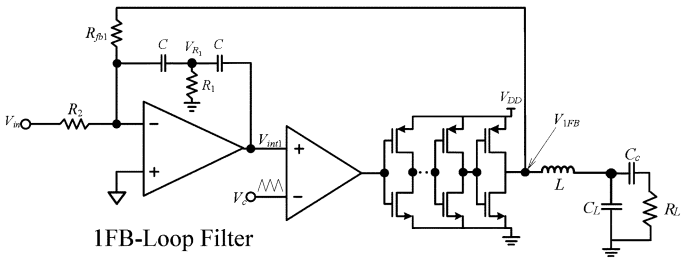

Fig. 2. Schematic of a 1FB-CDA.

amplifiers. To understand this phenomenon, we will now investigate the mechanisms of the THD in the 1FB- and 2FB-CDAs.

III. THD OF THE 1FB- AND 2FB-CDAS

In the time domain, the PWM signal is a series of pulses. The three parameters that describe the PWM pulses include the: 1) amplitude; 2) phase; and 3) duty cycle. The amplitude of the PWM pulses is determined by the power supply rails, and the variations of the amplitude relate to the power supply ripple [7]. The phase and duty cycle of the PWM pulse are the information encoded within the output signal, and if there are errors in the phase and/or duty cycle, THD may manifest.

In an ideal open-loop CDA, the PWM output signal that arises from the natural sampling between the triangular signal and the input signal, has 0% THD [9], [12]. In the case of the closed-loop CDA, the sampling is between the triangular signal and the combined signal of the amplified input signal and the attenuated carrier signal (refer to the 1FB-CDA in Fig. 2). Due to the combined signal (instead of the input signal alone), the generated PWM output signal possibly has some THD arising due to the phase error and the duty cycle error.

These errors will be now discussed for the 1FB- and 2FB-CDAs. In Section III-A, the mechanisms and pertinent parameters affecting harmonic distortion components in the 1FB-CDA due to the phase error and that due to the duty cycle error are investigated. In Section III-B a similar investigation into the pertinent parameters affecting harmonic distortion components is extended to the 2FB-CDA. For simplicity of the derivations, the gain of the pulsewidth modulator is assumed to be unity in the analysis of both 1FB- and 2FB-CDAs, and this assumption does not affect the generality of the derived THD.

A. THD of 1FB-CDA

1) Phase Error: Fig. 4 depicts the normalized waveforms of $V_{\rm int1}, V_{R_1}, V_c$ and $V_{\rm 1FB}$ at the pulsewidth modulator of the 1FB-CDA. The PWM output of the ideal open-loop CDA $V_{\rm open-loop}$ is also depicted in Fig. 4 and this serves as the reference (due to its 0% THD). Note that for ease of analysis (without loss of generality) and for the sake of brevity, all the signals in the following derivation are normalized with respect to $V_{\rm DD}$. For the derivation of the PWM signal, $V_{\rm in}$ is assumed to be constant within one period because the carrier frequency, $f_c, \gg$ input signal frequency $f_{\rm in}$. For the sake of illustration, Fig. 4 depicts a somewhat exaggerated phase shift in $V_{\rm 1FB}$ relative to $V_{\rm open-loop}$. We derive this phase shift, φ (refer to Appendix A), as

$$\varphi = 2\pi f_{\rm in}\frac{T_c^2\left[\frac{1}{4}-\left(\frac{\tau_2}{\tau_1}V_{\rm in}\right)^2\right]}{4\tau_2} = \frac{\pi f_{\rm in}T_c^2\left[1-(M\cos 2\pi f_{\rm in}t)^2\right]}{8\tau_2} \quad (2a)$$

where

M modulation index;
$T_c = 1/f_c$ period of the carrier signal;
$f_{\rm in}$ frequency of the input signal;
$\tau_1 = R_2C;\ \tau_2 = R_{fb1}C.$

From (2a), it is noted that φ is affected by the instantaneous magnitude of the input signal, $M\cos 2\pi f_{\rm in}t$. The resulting harmonic components, $V_{H\varphi}(t)$, due to this phase shift error at $V_{\rm 1FB}$ can be derived (refer to Appendix A)

$$V_{H\varphi}(t) = \frac{M}{2}\sum_{p=-\infty}^{+\infty} J_p\left(\frac{xM^2}{2}\right) \times \cos\left[2(2p+1)\pi f_{\rm in}t + x - \frac{p}{2}\pi\right] \quad (3a)$$

where

$$x = \pi f_{\rm in}/8\tau_2 f_c^2. \quad (3b)$$

Equation (3a) is interpreted as follows. The amplified replica of the input signal $@f_{\rm in}$ is obtained when $p = 0$ and -1. The remaining components are the corresponding odd harmonics, and the third harmonic components are obtained when $p = 1$ and -2. Similarly, the higher harmonic components are obtained by their associated values of p. The higher-order harmonic components (beyond the third harmonic) are negligible (due to the properties of the Bessel function) and the significant third harmonic component, $V_{3H\varphi}$, can be shown to be

$$\begin{aligned} V_{3H\varphi}(t) &= \frac{M}{2}J_1\left(\frac{xM^2}{2}\right)\cos\left(6\pi f_{\rm in}t + x - \frac{\pi}{2}\right) \\ &\quad + \frac{M}{2}J_2\left(\frac{xM^2}{2}\right)\cos\left(6\pi f_{\rm in}t - x + \pi\right) \\ &\approx \frac{M}{2}J_1\left(\frac{xM^2}{2}\right)\cos\left(6\pi f_{\rm in}t - \frac{\pi}{2}\right). \end{aligned} \quad (4)$$

Equation (4) is insightful as it depicts that the four parameters that influence the third harmonic component $V_{3H\varphi}$ due to the phase error, are as follows.

i) *Modulation Index M*
As expected, as M increases, $V_{3H\varphi}$ increases and the same is observed in linear amplifiers.

ii) *Input Signal Angular Frequency $f_{\rm in}$*
Similar to i), this is expected, and that is as $f_{\rm in}$ increases, $V_{3H\varphi}$ increases (assuming that the third harmonic of $f_{\rm in}$ is within the audio band). The same is observed in linear amplifiers.

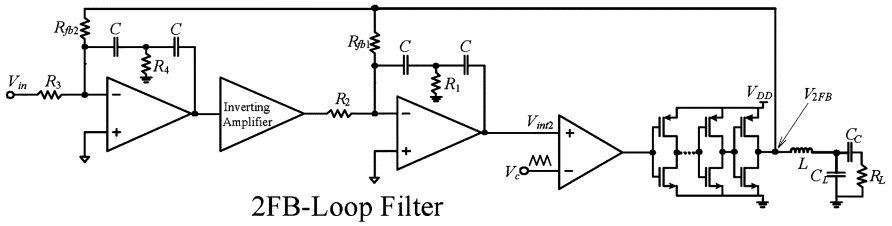

Fig. 3. Schematic of a 2FB-CDA.

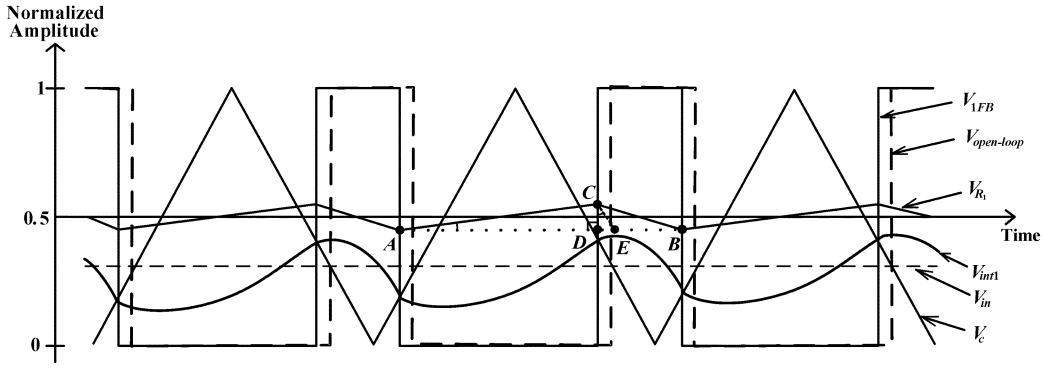

Fig. 4. Waveforms of $V_{\mathrm{int}1}, V_{R_1}, V_{\mathrm{c}}, V_{1\mathrm{FB}}, V_{\mathrm{in}}$, and $V_{\mathrm{open-loop}}$ in the 1FB-CDA.

iii) *Carrier Frequency* f_c
From (3b), as f_c increases, x decreases, and consequently from (4), $V_{3H\varphi}$ decreases. This is one parameter available to the designer although a higher f_c has implications to power dissipation.

iv) *Time Constant* τ_2
Similar to iii) above, as τ_2 increases, $V_{3H\varphi}$ decreases. From (2b), τ_2 can be increased by increasing the external (to the IC) passive components, R_{fb1} and/or C. These values are predetermined by the design of the loop filter (and its stability) and the designer has some but limited freedom to increase τ_2.

In summary, to reduce $V_{3H\varphi}$ due to the phase error, we recommend that f_c be increased (at the cost of reduced power efficiency), and where possible τ_2 be increased.

2) Duty Cycle Error: As delineated previously, the loop filter output signal, $V_{\mathrm{int}1}$, consists of the combined amplified input signal and attenuated carrier signal, that is

$$V_{int1}(t) = \frac{\tau_2}{\tau_1} V_{\mathrm{in}}(t) + V_{\mathrm{ac}}(t) \tag{5}$$

where $V_{\mathrm{ac}}$is the attenuated carrier signal which is the low-pass filtered (by the integrator) high frequency carrier signal.

On the basis of the established PWM model [12] and considering $V_{\mathrm{int}1}$ at the positive input, the expression for the harmonic components, $V_{H\gamma}(t)$, due to the duty cycle error at $V_{1\mathrm{FB}}$ can be derived (refer to Appendix B)

$$V_{H\gamma}(t) = \frac{1}{1+GH} \sum_{m=1}^{\infty} \sum_{q=1,3,5}^{\infty} 2yJ_m\left(\frac{mA\pi}{2}\right) \times \cos m\theta J_q\left(\frac{mM\pi}{2}\right) \sin\left(2q\pi f_{\mathrm{in}} t + q\frac{\pi}{2}\right) \tag{6}$$

where

GH is the loop gain
$A \approx \dfrac{2J_0\left(\pi\frac{M}{2}\right)}{\pi} \sin 2\pi f_c t \times GH_{@f_c}$
the amplitude of the attenuated carrier
$y = 2(-1)^m/(m\pi).$ (7)

Equation (6) is interpreted as follows. The amplified replica of the input signal $@f_{\mathrm{in}}$ is obtained when $q = 1$. The remaining components are odd harmonics of the amplified replica of the input signal, and the third harmonic components are obtained when $q = 3$. Similarly, the higher-order harmonic components are obtained by their corresponding values of q. As in the phase error, the higher harmonic components (beyond the third harmonic) are negligible (due to the properties of the Bessel function), and the significant third harmonic component is

$$V_{3H\gamma}(t) = \frac{-1}{1+GH_{@3f_{\mathrm{in}}}} \sum_{m=1}^{\infty} 2yJ_m\left(\frac{mA\pi}{2}\right) \times \cos m\theta J_3\left(\frac{mM\pi}{2}\right) \cos 6\pi f_{\mathrm{in}} t. \tag{8}$$

Equation (8) is insightful as it depicts that the four parameters that influence the third harmonic component, $V_{3H\gamma}$, due to the duty cycle error, are as follows.

i) *Modulation Index* M
As expected, when M increases, $V_{3H\gamma}$ increases, and the increase is more rapid than that of $V_{3H\varphi}$ for the same value of M.

ii) *Input Signal Angular Frequency* f_{in}

As f_{in} increases, $GH_{@3f_{\text{in}}}$ decreases, and hence $V_{3H\gamma}$ increases. This is expected because of the effect of negative feedback.

iii) *Carrier Frequency f_c*
From (7), as f_c increases, $GH_{@f_c}$ decreases and A decreases, and hence $V_{3H\gamma}$ decreases. Note that an increase in f_c is able to reduce both $V_{3H\gamma}$ and $V_{3H\varphi}$.

iv) *Loop Gain GH*
The two loop gains involved are $GH_{@3f_{\text{in}}}$ and $GH_{@f_c}$. Due to the effect of negative feedback described in ii) above, when $GH_{@3f_{\text{in}}}$ increases, $V_{3H\gamma}$ decreases. When $GH_{@f_c}$ increases, A increases, and hence $V_{3H\gamma}$ increases. To put this interpretation in perspective, consider the usual methodology applied in linear amplifiers with feedback to reduce THD. The usual methodology is to increase the loop gain *GH* as THD would be reduced by $1 + GH$. However, in the 1FB-CDA, increasing $GH_{@3f_{\text{in}}}$ would usually correspondingly increase $GH_{@f_c}$ and these have opposite effects on THD. In other words, increasing the loop gain may not necessarily improve the THD and this is somewhat converse to what is known in linear amplifier designs.

In summary, to reduce $V_{3H\gamma}$ due to the duty cycle error, we recommend that f_c and $GH_{@3f_{\text{in}}}$ be increased and $GH_{@f_c}$ be reduced. Practically, $GH_{@f_c}$ can be reduced without affecting $GH_{@3f_{\text{in}}}$ by augmenting a low-pass filter (in the loop filter) whose magnitude response is unity within the audio band and attenuated thereafter (hence $GH_{@f_c}$ is low).

3) Overall THD: Taking into account the expressions for the third harmonic components due to the phase error (4) and the duty cycle error (8), the expression of the overall THD for the 1FB-CDA can be expressed as shown in (9) at the bottom of the page. Note that (9) does not account for other harmonic components (e.g., due to dead time, voltage drop across the switches in the output stage, and the trapezoidal shape of the PWM output pulses, etc.) because their contribution to THD is insignificant (largely mitigated by the feedback with a high loop gain). Examples will be exemplified in Sec IV to verify (9).

In summary, the important and available parameters for designing the 1FB-CDA with low THD are high f_c, high $GH_{@3f_{\text{in}}}$ and low $GH_{@f_c}$.

B. THD of 2FB-CDA

Arguably, it is a general opinion within the CDA community that the 2FB-CDA would feature improved THD over the 1FB-CDA due to its higher loop gain. However, by means of deriving a THD expression for the 2FB-CDA (also measurements in Section IV), we will show that this is not necessarily the case.

Similar to the 1FB-CDA, the 2FB-CDA also suffers from THD due to the combined phase and duty cycle error. It can be shown that the associated third harmonic components in the 2FB-CDA due to the phase error and the duty cycle error can similarly be expressed by (4) and (8), respectively, and hence the overall THD by (9).

The effect of the phase error on the THD of the 2FB-CDA is the same as that in the 1FB-CDA because x in (9) remains unchanged. However, the effect of the duty cycle error on the THD of the 2FB-CDA is slightly different due to the increased values of both $GH_{@3f_{\text{in}}}$ and $GH_{@f_c}$. As delineated earlier, it is somewhat paradoxical that the benefit of an increased $GH_{@3f_{\text{in}}}$ is defeated by the increased $GH_{@f_c}$, and hence the THD of the 2FB-CDA due to the duty cycle error is not improved—it is in fact worse than that of the 1FB-CDA. For example, we will show in Section IV later that for a particular design, the THD@6 kHz $\approx 0.3\%$ in the 2FB-CDA, and this is larger than THD@6 kHz $\approx 0.25\%$ in the 1FB-CDA, despite the former having a higher loop gain. This finding is significant in the sense that it contravenes the general or "classical" opinion in the electronics audio community that a higher loop gain is able to attain lower nonlinearity. As delineated earlier, this phenomenon can be explained by the nonlinear PWM process in CDAs, and linear amplifiers have no analogous phenomenon.

C. General Discussion

The overall THD of closed-loop CDAs comprises the THD predicted by the linear model $(\text{THD}_{\text{op}}/(1+GH))$ and the THD due to the combined phase and duty cycle error given by (9). The former THD can be easily reduced by a properly-designed loop filter with sufficient loop gain, and this negative feedback design methodology is well established. On the other hand, the latter THD that arises due to feedback and due to the combined phase and duty cycle error, is often significant in closed-loop CDAs, particularly at high input frequencies, and this is not well recognized in literature. For example, when the input signal, $f_{\text{in}} = 6$ kHz is relatively high, the THD of 1FB- and 2FB-CDAs is dominated by the THD due to the combined phase and duty cycle error and due to feedback. Design examples will be presented in the next section.

For completeness, it is worthwhile to note that the relative importance of the phase and duty cycle errors is primarily determined by the loop gain of the filter embodied in the CDAs. In the case of 1FB- and 2FB-CDAs, the THD due to the phase error is relatively less significant than that due to the duty cycle error, largely because of the characteristics of the second-order loop filter therein. Nonetheless, in CDAs with other loop filter topologies, the THD due to the phase error may be larger than that due to the duty cycle error.

$$\%\text{THD} \approx \sqrt{\left[\frac{1}{2}J_1\left(\frac{xM^2}{2}\right)\right]^2 + \left[\frac{1}{M\,(1+GH_{@3f_{\text{in}}})}\sum_{m=1}^{\infty} 2yJ_m\left(\frac{mA\pi}{2}\right)\cos m\theta J_3\left(\frac{mM\pi}{2}\right)\right]^2} \times 100\% \tag{9}$$

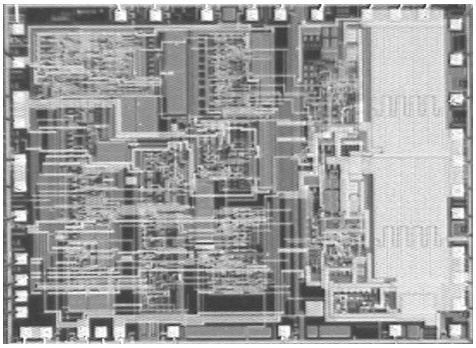

Fig. 5. Microphotograph of the 1FB-CDA.

TABLE I
OPERATING PARAMETERS OF THE 1FB- AND 2FB-CDAS

Parameter	Value
Switching frequency	f_c=150kHz or 300kHz
Supply voltage	V_{DD}=10V
Noise floor	100μV
Load	4Ω

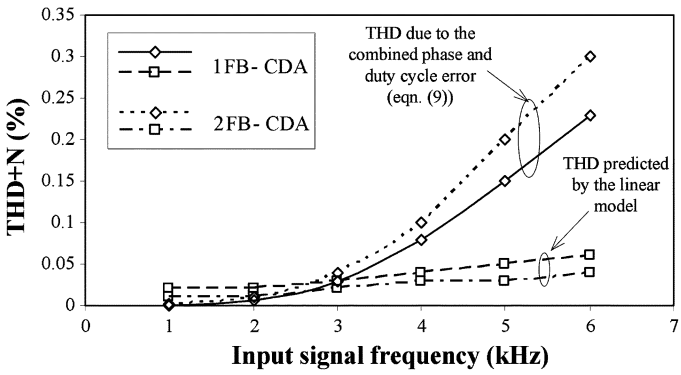

Fig. 6. THD+N against frequency in the 1FB- and 2FB-CDAs with $M = 0.7$.

IV. MEASUREMENT RESULTS

In this section, the THD obtained analytically from (9) for 1FB- and 2FB-CDAs is verified against HSPICE simulations and measurements on a prototype CDA IC and on other CDAs constructed discretely. The operating conditions for the 1FB- and 2FB-CDAs are tabulated in Table I. Note that for the 1FB- and 2FB-CDAs, the maximum modulation index, $M_{\max}$, is 0.7 due to the circuit conditions where $f_c = 150$ kHz. In the case of the circuit condition where $f_c = 300$ kHz, $M_{\max}$ increases to 0.85. For the purpose of comparison, we will only show the associated THDs against the modulation index in the range of $M = 0.1$–0.7. The microphotograph of the prototype IC embodying the 1FB-CDA is depicted in Fig. 5.

Fig. 6 depicts the THD of the 1FB- and 2FB-CDAs due to the combined phase and duty cycle error obtained analytically from (9) and that predicted by the linear model ($\mathrm{THD_{op}}/(1+GH)$) against the input signal frequency (1 kHz-6 kHz) at $M = 0.7$ and $f_c = 150$ k; 6 kHz is the maximum input signal frequency whose dominant third harmonic component (18 kHz) is within the audio band. The THD predicted analytically from (9) will be compared against measurements in Figs. 7 and 9 later. $\mathrm{THD_{op}}/(1+GH)$ is based on measurements on the open-loop CDA and is obtained in three steps.

1) All the harmonic components of the open-loop CDA are measured.
2) The attenuated harmonic components are obtained by dividing each measured harmonic component by the specific Loop Gain+1 of the 1FB- and 2FB-CDAs.
3) Finally, the attenuated harmonic components are substituted to (1), and the THD is obtained.

On the basis of Fig. 6, the following comments are made.

i) As expected, both THDs due to the combined phase and duty cycle error and that THD predicted by linear model increase as the input signal frequency increases. In latter

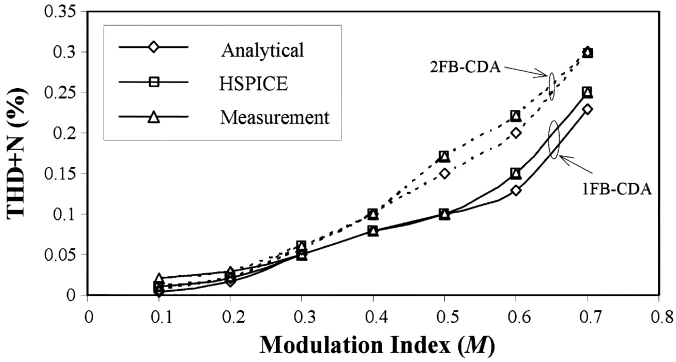

Fig. 7. THD+N@6 kHz for 1FB- and 2FB-CDAs ($f_c = 150$ kHz)

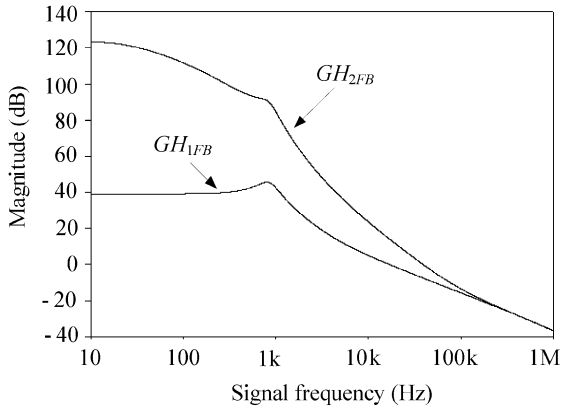

Fig. 8. Loop gain of the 1FB- and 2FB-CDAs.

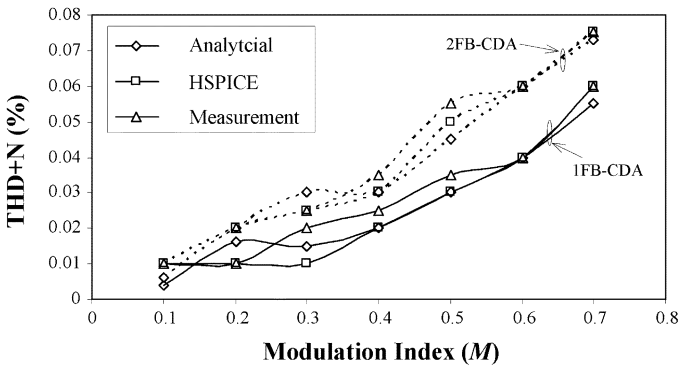

Fig. 9. THD+N@6 kHz for the 1FB- and 2FB-CDAs ($f_c = 300$ kHz)

THD, this is due to the reduced loop gain at higher frequencies.

ii) When input signal frequency is low (<3 kHz), $\mathrm{THD}_{\mathrm{op}}/(1+GH)$ is larger than the THD due to the combined phase and duty cycle error. As a case in point, when $f_{\mathrm{in}} = 1\mathrm{kHz}, \mathrm{THD}_{\mathrm{op}}/(1+GH) = \sim 0.01\%$ is dominant and the $\mathrm{THD} = \sim 0.003\%$ due to the combined phase and duty cycle error is negligible.

iii) When input signal frequency increases beyond 3 kHz, the THD due to the combined phase and duty cycle error becomes dominant over the THD of the linear model. As a case in point, when $f_{\mathrm{in}} = 6$ kHz, the THD due to the combined phase and duty cycle error is 0.25–0.3% while $\mathrm{THD}_{\mathrm{op}}/(1+GH)$ is a relatively insignificant 0.03%.

Fig. 7 plots the THD@6 kHz predicted by (9) and that obtained from simulations and on the basis of measurements against M, for the 1FB- and 2FB-CDAs at $f_c = 150$kHz. The loop gains of these CDAs are given in Fig. 8. Following the comments above, note that at 6 kHz, the THD due to combined phase and duty cycle error dominates. On the basis of Fig. 7, the following comments are made.

i) The derived analytical THD expression given by (9) agrees well with the HSPICE simulations and with practical measurements, hence verifying the analysis herein.

ii) As expected, the THDs of both the 1FB- and 2FB-CDAs increase as M increases, and the THDs are poor at large M. As a case in point, when $M = 0.7$, the THDs of 1FB- and 2FB-CDAs are 0.25% and 0.3%, respectively—beyond the high fidelity specifications. This poor THD is despite their high loop gain, and the THD is due to the combined phase and duty cycle error, a consequence of negative feedback and the associated loop gain. [see (4) and (6)].

iii) As predicted from (9), the THD of the 2FB-CDA is in general worse than the 1FB-CDA despite its higher loop gain.

Fig. 9 plots the THD@6 kHz predicted by (9) and that obtained from simulations and on the basis of measurements against M, for the 1FB- and 2FB-CDAs at a higher f_c, $f_c = 300$kHz. The following comments are made.

i) As before, the derived analytical expression (9) agrees well with the HSPICE simulations and with the practical measurements, hence verifying the analysis herein.

ii) As expected and similar to the THD in Fig. 7 when $f_c = 150$kHz, the THD of the two CDAs increases as M increases, and the THD of the 1FB-CDA is in general slightly better than that of the 2FB-CDA.

iii) When compared to Fig. 7 where $f_c = 150$kHz, the THD of the two CDAs improved markedly when f_c is increased to $f_c = 300$kHz. As a case in point, when $f_{\mathrm{in}} = 6$kHz and $f_c = 300$kHz, the THD of 1FB- and 2FB-CDAs are 0.06% and 0.075%, respectively against 0.25% and 0.3% for $f_c = 150$kHz.

Fig. 10 plots the THD@6 kHz and $M = 0.7$ (predicted by (9) and that obtained from simulations and on the basis of measurements) against f_c for the 1FB-CDA. For the sake of brevity, the plot for the 2FB-CDA is not shown because it shows a similar trend as the 1FB-CDA, and the comparison for THDs of two CDAs has been earlier discussed in the comments for Fig. 9. On the basis of Fig. 10, the following comments are made.

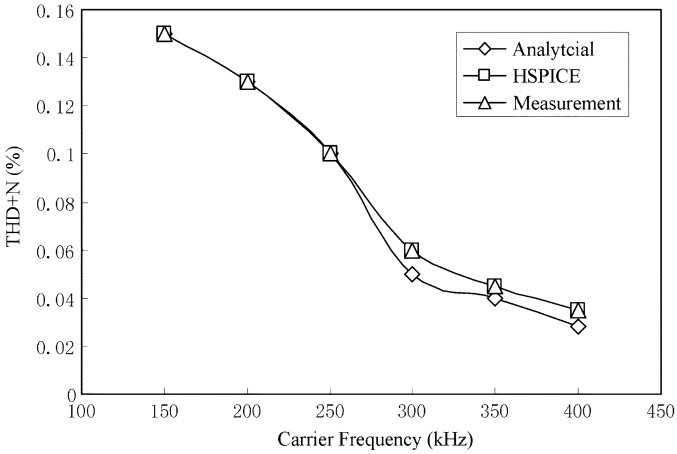

Fig. 10. THD+N@6 kHz against f_c for the 1FB-CDA ($M = 0.7$).

i) As before, the derived (9) agrees well with the HSPICE simulations and with the practical measurements, hence verifying the analysis herein. The small discrepancy between the analytical results and HSPICE and measurement results when f_c is high is attributed to the THD predicted by the linear model (not accounted for in (9)) that is due to the output stage therein (e.g., dead time, slew rate, etc.).

ii) As expected and similar to the THDs in Figs. 7 and 9, the THD of the 1FB-CDA generally decreases with the increase of f_c; in a recent design [13], the THD was reported to be extremely low (0.004% for $f_{\mathrm{in}} = 1$ kHz) with a very high carrier frequency ($f_c = 1$ MHz). Although (and as previously mentioned) f_c is one of the primary parameters to reduce THD of closed-loop CDAs, there is a point of diminishing return with increasing f_c.

In view of Figs. 6, 7, 9, and 10, it is apparent that to obtain low THD due to the combined phase and duty cycle error for closed-loop CDAs, it is imperative that f_c be high, that $GH_{@3f_{\mathrm{in}}}$ be high and that $GH_{@f_c}$ be low. These are the primary parameters available to a closed-loop CDA designer to mitigate THD. In some cases, it may be possible to improve the THD by increasing τ_2 of the loop filter.

V. Conclision

We have shown that the overall THD in closed-loop CDAs comprises the THD of their open-loop counterparts but reduced by the Loop Gain+1, and the THD induced by the combined phase and duty cycle error due to feedback. It has been shown that the latter THD mechanisms are dominant when the input frequency >3 kHz. On the basis of double Fourier series, we have derived analytical expressions for the harmonic components and a THD expression for closed-loop CDAs. The THD expression has been verified against HSPICE and measurements on a prototype CDA IC and other CDAs realized discretely. The THD expression has provided insight into the parameters of closed-loop CDAs that affect THD.

APPENDIX A
DERIVATION OF HARMONIC COMPONENTS DUE TO THE PHASE ERROR

From Fig. 4, the phase shift, φ, can be expressed as

$$\varphi = 2\pi f_{\text{in}}\left(\frac{\overline{AE}}{2} - \frac{\overline{AD}}{2}\right) = 2\pi f_{\text{in}}\frac{\overline{DE}}{2} = 2\pi f_{\text{in}} \times \overline{AD} \times \tan\angle CAD \times \tan\angle DCE. \quad \text{(A.1)}$$

By first-order integration at V_{R_1}, the following relations can be obtained:

$$\overline{AD} = \left(\frac{1}{2} + \frac{\tau_2}{\tau_1}V_{\text{in}}\right) \times \overline{AB} \quad \text{(A.2)}$$

$$\tan\angle CAD = \frac{1/2}{\tau_2} - \frac{V_{\text{in}}}{\tau_1} \quad \text{(A.3)}$$

$$\tan\angle DCE = \overline{AB}/2. \quad \text{(A.4)}$$

Substituting (A.2)–(A.4) into (A.1), φ can be derived

$$\varphi = 2\pi f_{\text{in}}\frac{T_c^2\left[\frac{1}{4} - \left(\frac{\tau_2}{\tau_1}V_{\text{in}}\right)^2\right]}{4\tau_2} = \frac{\pi f_{\text{in}}T_c^2\left[1 - (M\cos 2\pi f_{\text{in}}t)^2\right]}{8\tau_2}. \quad \text{(A.5)}$$

Equation (A.5) shows that φ varies with the instantaneous magnitude of the input signal. The resulting THD due to the variation of φ will now be derived.

The derived phase shift between $V_{1\text{FB}}$ and $V_{\text{open-loop}}$, φ, is in fact the phase shift of the input signal. Hence, on the basis of the (A.5) and the derived duty cycle in [7], the amplified replica of the input signal plus its harmonics at $V_{1\text{FB}}$ is,

$$V_{H\varphi}(t) = \frac{M}{2}\cos\left(2\pi f_{\text{in}}t + \varphi\right). \quad \text{(A.6)}$$

Substituting (A.5) into (A.6), (A.6) can be re-expressed

$$V_{H\varphi}(t) = \frac{M}{2}\sum_{p=-\infty}^{+\infty} J_p\left(\frac{xM^2}{2}\right) \times \cos\left[(2p+1)2\pi f_{\text{in}}t + x - \frac{p}{2}\pi\right]. \quad \text{(A.7)}$$

APPENDIX B
DERIVATION OF HARMONIC COMPONENTS DUE TO THE DUTY CYCLE ERROR

The derivation of the harmonic components due to the duty cycle error involves two steps. In Step 1, the harmonic components generated by the pulsewidth modulator is derived. In Step 2, the harmonic components at $V_{1\text{FB}}$ are thereafter derived.

Step 1 Derivation of the Harmonic Components Generated by the pulsewidth Modulator: The two signal components at V_{int1} ((5) can be expressed as

$$\frac{\tau_2}{\tau_1}V_{\text{in}}(t) \approx \frac{M}{2}\cos 2\pi f_{\text{in}}t \quad \text{(B.1)}$$

$$V_{\text{ac}}(t) \approx \frac{A}{2}\cos(2\pi f_c t + \theta) \quad \text{(B.2)}$$

where $V_{\text{ac}}(t)$ can be assumed to be a sinusoid signal @f_c and with constant phase θ, and A is the amplitude of $V_{\text{ac}}(t)$.

On the basis of the double Fourier series model [12] and by considering V_{ac} as the only input signal, the intermediate expression at the output of the pulsewidth modulator can be derived

$$\begin{aligned} V_{\text{intermediate}}(t) &= k + \frac{A}{2}\cos(2\pi f_c t + \theta) \\ &\quad + 2\sum_{m=1}^{\infty}\left(\frac{J_0(m\pi A)}{m\pi}\sin m2\pi f_c t \sin m\pi k\right) \\ &\quad + 2\sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty}\left(\frac{J_n(m\pi\frac{A}{2})}{m\pi}\cos((m+n)2\pi f_c t \right. \\ &\quad \left. \times + m\theta)\sin\left(\frac{n\pi}{2} + m\pi k\right)\right) \end{aligned} \quad \text{(B.3)}$$

where $k = 1/2$, is the offset of the input signal.

To augment $(M/2)\cos 2\pi f_{\text{in}}t$ into the model, the substitution of offset K in (B.3) by $k = 1/2 + (M/2)\cos 2\pi f_{\text{in}}t$ is made. On the basis of the substitution, the harmonic components can be derived from the last terms of (B.3) where $m + n = 0$. Note that the first three terms of (B.3) comprises DC term represented by k, and the components at multiple-integers of f_c only. Hence, the expression of the harmonic components generated by the pulsewidth modulator can be derived

$$V_{H\gamma by\,\text{PWM}}(t) = \sum_{m=1}^{\infty}\sum_{q=1,3,5}^{\infty} 2yJ_m\left(\frac{mA\pi}{2}\right)\cos m\theta \times J_q\left(\frac{mM\pi}{2}\right)\sin\left(2q\pi f_{\text{in}}t + q\frac{\pi}{2}\right). \quad \text{(B.4)}$$

Equation (B.4) shows that only the odd harmonic components are produced due to the duty cycle error.

Step 2 Derivation of the Harmonic Components at $V_{1\text{FB}}$*:* On the basis of the derived harmonic components (B.4) generated by the pulsewidth modulator, the expression of the harmonic components due to duty cycle error at $V_{1\text{FB}}$ can be easily derived

$$V_{H\gamma}(t) = \frac{1}{1+GH}\sum_{m=1}^{\infty}\sum_{q=1,3,5}^{\infty} 2yJ_m\left(\frac{mA\pi}{2}\right) \times \cos m\theta J_q\left(\frac{mM\pi}{2}\right)\sin\left(2q\pi f_{\text{in}}t + q\frac{\pi}{2}\right). \quad \text{(B.5)}$$

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