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An Ultra Low-Power CMOS EMG Amplifier with High Efficiency in Operation Frequency per Power

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Abstract—A new ultra low-power CMOS Electromyograph (EMG) amplifier is presented in this paper. It is based on the application of a novel capacitive load reduction circuit technique to the capacitive-reset switched-capacitor circuit architecture. This is achieved by adding a capacitor in series with the capacitive load of the amplifier so as to reduce the total effective load capacitance being seen by the op-amp for reducing power driving requirement. The amplifier is designed using CSM 1.8V 0.18µm triple-well CMOS process technology and simulated using realistic BSIM3 models. The amplifier dissipates only 15.14µW at a dual power supply of ±0.9V. It has a gain of 40dB at dc and 38.5dB at 3.2kHz. The estimated passband input-referred noise is 2.08μVrms.

I. INTRODUCTION

In designing Electromyograph (EMG) instrument to capture electrical signal produced by contracting muscles, EMG amplifier is treated as one of the important building blocks used to amplify the detected signal before it can be further processed by the rest of the EMG system.

EMG signal has the following characteristics: its energy mostly occupies low frequency domain, i.e. 0-500 Hz, the peak of its power spectrum is located between 50-100 Hz [1]-[2], and its amplitude varies between 0.01μV to 10mV [3]. Henceforth, the typical bandwidth specification of an EMG amplifier is 500 Hz. However, there are also larger bandwidth specifications such as 1000 Hz [4] or even 3000 Hz [5].

In EMG applications, such as prosthetic devices and portable EMG test equipments, low power demand is essential. Bio-amplifiers that address low power consumption are reported in [5]-[10]. Different circuit architectures have displayed different efficiency in terms of operation frequency per power consumption. This gives the design challenge on how to realize an ultra low power EMG amplifier that deals with the possible bandwidth of EMG bio-signals.

This paper presents the design of a new ultra low power EMG amplifier which is implemented using switched-capacitor circuit incorporating a reduced driving capacitive load technique. The amplifier, having differential input and single-ended output architecture, is dedicatedly designed to handle a maximum bandwidth of about 3 kHz whilst consuming very low power. Followed by the Introduction, Section II presents the proposed concept. Section III describes the circuit realization. Section IV gives the results and discussions. This is then followed by the concluding remarks in Section V.

II. PROPOSED CONCEPT

The proposed concept is to add a capacitor (\(C_S\)) in series with the capacitive load of the amplifier so as to reduce the total effective load capacitance being seen by the op-amp. As a result, it permits the reduction of op-amp’s power consumption in a capacitive based switched-capacitor amplifier design.

In practice, the amplifier may cease to function as the op-amp’s output saturates to either \(V_{DD}\) or \(V_{SS}\). To prevent this drawback, a reset switch is added between the terminals of the \(C_S\) capacitor. Fig. 1 shows the proposed circuit architecture. The \(C_S\) capacitor is reset once every half a clock period.

![Fig. 1. Amplifier circuit with added a \(C_S\) capacitor to reduce effective driving capacitive load](image)

The effective capacitive load (\(C_{eff}\)) seen by the op-amp is

\[
C_{eff} = \frac{(C_{ip} \cdot C_{fb}) + C_L \cdot C_S}{C_{ip} + C_{fb}}
\]

As can be seen in (1), for typical high capacitive output load \(C_L\) and small feedback capacitor \(C_{fb}\) in realizing a high-gain amplifier, the added series capacitor \(C_S\) will reduce the effective capacitive load seen by the op-amp. However, this technique has several trade-offs. They are bootstrapping internal signal swing and reduction of available open loop gain. Herewith, a term, bootstrap factor (\(BT\)), which is defined as the ratio between the change in voltage at the op-amp's output to the change in voltage at the amplifier's output. The change at op-amp's output is larger than the change at the amplifier's output. The bootstrapping factor is approximated as

\[
BT = 1 + \frac{C_L \cdot C_{ip}}{C_{fb} + C_{ip} / C_S}
\]
and the effective open loop gain ($A_{eff}$) of the complete amplifier is

$$A_{eff} = \frac{A}{BT}$$  \hspace{1cm} (3)

where $A$ is the dc open-loop gain of the standalone op-amp.

**III. REALIZATION OF PROPOSED EMG AMPLIFIER**

**A. Proposed EMG Amplifier**

The ultra low power EMG amplifier is depicted in Fig. 2. It is realized by the application of the proposed capacitive load reduction technique to a capacitive-reset differential-to-single-ended amplifier architecture [11]. Since it has advantage that the finite gain error of the amplifier is proportional to $1/A_{eff}^2$, the reduction of the open loop gain arising from the addition of series capacitance of the proposed technique is minimized. Note that $A_{eff}$ is the effective open-loop gain of the op-amp incorporating the series capacitive network. $A_{eff}$ can be calculated using (3) where $BT$ is given by

$$BT = 1 + \frac{C_1 + C_L + \frac{C_1 \cdot C_2}{C_1 + C_2}}{C_S}$$  \hspace{1cm} (4)

Besides, the sample-and-hold operation reduces power in the context of slew rate.

The transfer function [12] of the circuit in Z-domain can be expressed as

$$\frac{V_{out}}{V_{ip}} = C_1 \cdot a \cdot \frac{1}{\sqrt{1 + b^2 - 2 \cdot b \cdot \cos(2\pi f_{ip}) f_{clk}}}$$  \hspace{1cm} (5)

where

$$a = \left( \frac{1}{1 + \frac{C_1 + C_2}{C_2 \cdot A_{eff}}} \right) \cdot (1 - \frac{C_1 + C_2}{A_{eff} \cdot (C_3 + \frac{C_1 + C_2 + C_3}{A_{eff}})}),$$

$$b = \frac{C_1 + C_2}{A_{eff} \cdot (C_2 + C_3 + \frac{C_1 \cdot C_2}{A_{eff}})},$$

$$C_2 \cdot (1 + \frac{C_1 + C_2}{C_2 \cdot A_{eff}}) \cdot (C_3 + \frac{C_1 + C_2 + C_3}{A_{eff}}),$$

$A_{eff}$ = effective op-amp dc open loop gain, $f_{ip}$ = input signal frequency, and $f_{clk}$ = non-overlapping clock frequency. When $A_{eff}$ is infinite, the circuit has an amplification factor of $C_1/C_2$. Then, the lower the $A_{eff}$, the lower the amplification factor is. When $A_{eff}$ is finite, the amplification factor reduces as $f_{ip}$ approaches $f_{clk}$. This is not critical in this biomedical application because the precision gain is not necessary.

The circuit is driven by two non-overlapping clocks, $clk_1$ and $clk_2$ and two respective advanced clocks, $clk_1a$ and $clk_2a$, that turn off slightly earlier than $clk_1$ and $clk_2$ such that they help the reduction of signal-dependent charge injection [13]. The switches are implemented using MOSFETs. Minimum level of charge injection and clock feedthrough can be obtained by sizing the switches minimally. Refer to Fig. 2, the switches that connect ground/virtual ground node to another node does not need to be able to conduct signal from near $V_{DD}$ to near $V_{SS}$. Hence, normal NMOS switches can be used in between such nodes. However, the rest of the switches has to be able to conduct signal from near $V_{DD}$ to near $V_{SS}$. Native transistor switches are thus used in such situation. It is mainly because native transistors have low or even negative threshold voltage that enables them to handle larger signal swing.

The circuit samples and amplifies its input for half the non-overlapping clock period ($1/2f_{clk}$) and holds its output on the other half. Therefore, the circuit's output has to be able to settle under half a clock period, ($1/2f_{clk}$). Assuming the parasitic capacitance of the inverting input of op-amp is negligible small, the effective capacitive load seen by the op-amp during the charge transfer phase at $clk_1$ is estimated as

$$C_{eff} = \frac{(C_1 + C_L + \frac{C_1 \cdot C_2}{C_1 + C_2}) \cdot C_S}{C_S + (C_1 + C_L + \frac{C_1 \cdot C_2}{C_1 + C_2})}$$  \hspace{1cm} (6)

According to [11], under negative feedback configuration, if it is assumed that the op-amp only has one pole and 90-degree phase margin, the amplifier time constant, $\tau$, is given as

$$\tau = \frac{1}{\beta \cdot 2\pi f_T}$$  \hspace{1cm} (7)

where $f_T$ is the unity gain frequency of the op-amp used in the amplifier circuit and $\beta$ is the amplifier's feedback factor. For this circuit, $\beta$ is equal to $C_2/C_1$. To reduce the amplifier time constant to sustain for the broad bio-signal bandwidth, the amplifier architecture should be properly chosen in order to attain large $f_T$ value whilst consuming low power.

![Fig. 2. Schematic of the proposed ultra low-power EMG amplifier](image-url)
B. Op-Amp

The op-amp is a cascode OTA with push-pull output for power-bandwidth efficiency. The schematic of the op-amp is shown in Fig. 3. The dc open loop gain of the OTA is given by

\[ A = \frac{K \cdot g_m \cdot (r_{\text{cascA}} \parallel r_{\text{cascB}})}{2\pi \cdot C_L} \]  

where \( r_{\text{cascA}} \) is the output impedance of \( M_13 \) cascaded with \( M_14 \), \( r_{\text{cascB}} \) is the output impedance of \( M_9 \) cascaded with \( M_{10} \), \( g_m \) is the transconductance of \( M_1 \) or \( M_2 \) (equal size), and \( K \) is the multiplication ratio of the current mirror pairs, \( M_{12-14}, M_{8-10} \). Thus, the unity gain bandwidth (\( f_T \)) of the OTA is

\[ f_T = \frac{2\pi \cdot C_L \cdot g_m \cdot K}{n V_T} \]  

where \( C_L \) is the load capacitance of the OTA. Since the OTA is used under low power condition, its input transistors are biased to operate in weak inversion region. Hence, \( g_m \) is defined as

\[ g_m = \frac{I_{DS}}{n V_T} \]  

where \( I_{DS} \) is the transistor dc drain-to-source current, \( n \) is a constant having its typical value of 1.6 [14] and \( V_T \) is thermal voltage. Using (10) and defining \( I_{DS} \) in terms of total current consumed by the OTA (\( I_{TOT} \)), the \( f_T \) expression becomes

\[ f_T = \frac{K \cdot g_m}{3 + K} \cdot \frac{I_{TOT}}{2\pi \cdot C_L} \]  

As can be seen in (11), besides \( I_{TOT} \), by reducing the effective \( C_L \) in circuit means, the \( f_T \) value can be increased. In other words, reducing \( C_L \) permits the reduction of \( I_{TOT} \), hence gaining low power consumption, to keep a constant \( f_T \) in the design specification. This is the key objective of this proposal work.

IV. RESULTS AND DISCUSSIONS

\( C_1/C_2 \) is chosen to be 50pF/0.5pF = 100 so that the amplifier is able to have a gain of approximately 100 times at low frequency. The rest of the capacitors had a capacitance as follows: \( C_3 = 1pF, C_L = 8pF \) and \( C_S = 4pF \). Using (4) and (6), the bootstrapping factor of the circuit is \( B_T = 3.37 \) whereas the effective capacitive load seen by the op-amp is \( C_{eff} = 2.81 \text{ pF} \).

In Fig. 2, \( S_2, S_3, S_5, S_8, S_9, S_11 \) are normal NMOS switches whereas \( S_4, S_10 \) are dummy switches for charge injection compensation in critical nodes. Finally, \( S_1, S_6, S_7, S_12, S_13 \) and \( S_14 \) are realized as native switches.

For the op-amp depicted in Fig. 3, its input transistors \( W/L \) are designed to be very large such that they are biased in the weak inversion region. \( K \) is set to be 5. The resulting op-amp dc open loop gain = 2047.5 times, phase margin = 70.40 degree, and output swing is from \(-699\text{mV} \) to \(535\text{mV}\).

In switched capacitor circuits, the maximum input signal frequency (\( f_{ip} \)) is recommended to be at least 5 times smaller than the circuit's clock frequency (\( f_{clk} \)) due to anti-aliasing requirement [15]. Hence, if \( f_{clk} \) is 16kHz (16kHz is half of the 32kHz crystal frequency), the maximum operation frequency of the circuit is 3.2 kHz. Using (3) and (5), at this frequency, with \( A = 2047.5 \) and \( B_T = 3.37 \), the circuit can achieve a gain of 84.5 times. The accuracy of the equation is verified in Fig. 4, showing a 2mVpp, 3.2kHz sinusoidal signal amplified by 85.78 times, which is very close to the theoretical value. At this frequency, the power drawn by the op-amp (not including its biasing circuit) is 15.14\mu W. Under this power consumption, the settling time of the circuit is 26.5\mu s, which is smaller than half of the circuit's clock period, i.e. 26.5\mu s < 31.25\mu s. Henceforth, the circuit is able to operate properly at 16 kHz.

The EMG amplifier is designed on the basis of CSM 1.8V 0.18\mu m CMOS triple-well process technology with BSIM3 model parameters. The circuit performance is evaluated using an artificial EMG signal generated by a white noise generator whose signal is shaped using a filter such that its spectrum resembles the spectrum of an EMG signal. The spectrum of the artificial EMG signal is shown in Fig. 5. The un-amplified and amplified EMG signals are shown in Fig. 6. It can be seen that the amplified signal has displayed similar type of wave shape but with opposite phase whilst having no significant distortion.
There are several noise mechanisms associated with the amplifier. The dominant noise mechanism is op-amp thermal noise with a flat spectral density of $9 \times 10^{-16} \text{V}^2/\text{Hz}$. KT/C noise of the circuit is assumed small and neglected when the choice of capacitor is not too small. Op-amp 1/f noise is reduced due to the implementation of CDS scheme. Noise is thermal noise source are amplified and combined at the output capacitor load $C_L$. The estimated value is approximately $8000 \text{Hz}$, hence, $B_n = 8000 \text{Hz}$.

The estimated value is approximately $8000 \text{Hz}$, hence, $B_n = 8000 \text{Hz}$.

Taking into account the white noise, the equation used to estimate the sample noise [16] in oversampling case is

$$
\eta_{out}(f) = \eta_n \left( \frac{\tau_{SH} f}{f_{clk}} \right)^2 \left( 1 - \frac{\tau_{SH}}{f_{clk}} \right)^2
$$

(12)

where $\eta_n$ is the white noise spectral density of op-amp, $\tau_{SH}$ is the ratio of the circuit’s hold period over $f_{clk}$. For $\tau_{SH} = 0.5$, $f = 3.2 \text{kHz}$ and closed-loop gain of 100, and during $\Phi_2$, the input-referred sampled square noise voltage in signal-input capacitor $C_1$ is $0.5 \eta_n f$. During the final charge transfer phase $\Phi_2$, the dominant noise source from $C_1$, and the op-amp thermal noise source are amplified and combined at the output capacitor load $C_L$. The estimated value is approximately $1.5 \eta_n (100) \times 3200 \text{V}_\text{rms}^2$. With $\eta_n = 9 \times 10^{-16} \text{V}^2/\text{Hz}$, one can estimate the output noise of $208 \mu\text{V}_\text{rms}$, which is translated to the corresponding input-referred noise of $2.08 \mu\text{V}_\text{rms}$.

V. CONCLUSION

A new ultra low power EMG amplifier has been presented. The use of reduced driving capacitive load technique and the capacitive-reset switched-capacitor circuit architecture enable the design of an ultra low-power EMG amplifier having high efficiency in operation frequency per power. The Cadence Spectre simulations using realistic BSIM3 models have validated the proposed circuit technique. The performance comparison has also shown that the proposed EMG amplifier has achieved appreciable figure of merit when compared to the previously-published prior-art works.