<table>
<thead>
<tr>
<th>Title</th>
<th>A 0.18m CMOS 802.15.4a UWB transceiver for communication and localization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Author(s)</td>
<td>Zheng, Yuanjin; Arasu, Muthukumaraswamy Annamalai; Wong, King Wah; The, Yen Ju; Poh, Andrew Hoe Suan; Tran, Duy Duong; Yeoh, Wooi Gan; Kwong, Dim Lee</td>
</tr>
<tr>
<td>Date</td>
<td>2008</td>
</tr>
<tr>
<td>URL</td>
<td><a href="http://hdl.handle.net/10220/6369">http://hdl.handle.net/10220/6369</a></td>
</tr>
</tbody>
</table>

© 2008 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE. This material is presented to ensure timely dissemination of scholarly and technical work. Copyright and all rights therein are retained by authors or by other copyright holders. All persons copying this information are expected to adhere to the terms and constraints invoked by each author's copyright. In most cases, these works may not be reposted without the explicit permission of the copyright holder.
6.2 A 0.18μm CMOS 802.15.4a UWB Transceiver for Communication and Localization

Yuanjin Zheng, M. Annamalai Arasu, King-Wah Wong, Yen Ju The, Andrew Poh Hoe Suan, Duy Duong Tran, Won Gi Yoo, Dim-Lee Kwong

Institute of Microelectronics, Singapore, Singapore

Recently, IEEE 802.15.4a has specified a UWB PHY for low-rate communication with ranging capability for wireless personnel area and sensor network applications [1]. Related work is reported on low-rate energy-efficient UWB radios [2-4]. However, they are not fully standard compliant or localization enabled. 802.15.4a supports three bands of operation, i.e., sub-1GHz band (249.6 to 749.6MHz), low band (3.1 to 4.8GHz) and high band (6.0 to 10.6GHz) with 16 channels in total. A combination of the burst position modulation (BPM) and binary phase shift keying (BPSK) is adopted. With different coding rate, bursts per symbol, and chips per burst, the mean pulse repetition rate (PRF) could vary from 3.9 to 62.4MHz for data throughput of 120kHz to 31.2MHz. This work presents an UWB RF transceiver which supports 12 channels, variable date rate, and ranging capability as specified in IEEE802.15.4a.

Figure 6.2.1 shows the RF transceiver architecture. On the TX side, the digital clock (TX_clk) triggers a baseband pulse-shaping filter (BPSF). The output pulses are modulated by the TX binary data. The signal is then upconverted by a mixer and amplified by a driver amplifier (DA) prior to the antenna. On the RX side, the weak signal is amplified by an LNA, is downconverted by I/Q mixers and is low-pass filtered to recover the phase of the transmitted BPSK signals. A VGA, in each I and Q path, is then used to boost the signal level. The output of each VGA is used in two paths. In one path it is connected to an integrator followed by an ADC for recovering the digital data while in the other path it goes through a signal detector (squarers and a limiting amplifier) to recover the amplitude of the pulses. The upconvertor is a Gilbert-cell active mixer with an LC-tunable loading network. A double-balanced differential Gilbert cell is used as the mixer and its resistive loads are used to cover the entire UWB band. The combined RF front-end achieves a voltage gain of 30.4dB, a BW of 6GHz (3 to 9GHz), and maximum output power of 8dBm. The TX draws a peak current of 8mA when generating 8dB, a BW of 6GHz (3 to 9GHz), and maximum output power of 8dBm. The TX draws a peak current of 8mA when generating 500MHz PRF pulses.

The RX front-end circuits are shown in Fig. 6.2.4. The LNA is designed to operate at one channel at any given time, through bank switching and channel selection, to minimize power consumption. The capacitive cross-coupled input stage is used to boost the Gm of the stage, and reduce input-referred noise while achieving good input matching. The band switching between low and high band can be done by transistors M3/M4 and M5/M6. Within each band, there are two-stage cascaded amplifiers. The first stage is an LC-tuned load where the channel select is performed on the desired channel. The second stage is a common-source amplifier with an LC-tunable loading network. A double-balanced differential Gilbert cell is used as the mixer and its resistive loads are used to cover the entire UWB band. The combined RX front-end achieves a gain of 30.4dB, a BW of 6GHz (3 to 9GHz), and an IIP3 of −16.7/−10.7dB for low and high bands, respectively.

The RX LPF is implemented by a 3rd-order elliptical Gm-C filter with cut-off frequency of 250MHz. The five-stage cascaded dB-linear VGA achieves a dynamic range gain of −29 to 50dB with 400MHz BW. The variable BW integrator captures the reflected pulses from multipath and extends the duration of the demodulated pulses. For localization purpose, two squarers and one nonlinear low-pass filter (NLFP) [5] are used to regenerate RC clk, where the squarers are used to detect the signal energy and NLFP is used to boost signal level to roll-to-rail for the energy detection. The pulse train is turned on and off at the rising edge of TX clk and RC clk, respectively. A passive 5th-order RC LPF with cut-off frequency of 500kHz is applied to average the jitter and noise and hence to significantly improve the ranging accuracy. Operating at 500MHz PRF, the peak current of the RX is 31mA.

A nine-tone frequency generator is shown in Fig. 6.2.5. A digital frequency-tuning loop is used to lock the quadrature VCO (QVCO) output frequency to an external 15.6MHz crystal reference. Once the QVCO is tuned to the desired channel, as determined by the lock detector, the tuning loop is powered off. The VCO tuning voltage is stored as a digital word in an 11b latch, where 3 bits are used for coarse tuning and the 8b DAC output is used for fine tuning. The accuracy of frequency tuning is 10MHz, which is limited by clock frequency resolution. To significantly reduce the die size, a four-stage ring oscillator with a frequency doubler is used as the QVCO core. The ring oscillator generates 45/90° phase difference LOs covering 2.8 to 4.75GHz, and the frequency doubler generates quadrature LOs covering 5.6 to 9GHz. The measured QVCO start-up time is 5.39ns, and it has a phase noise of −90dBc/Hz at 1MHz offset for 4.5GHz LO with output power of −2.1dBm. The peak current is 40mA.

The transceiver IC is implemented in a 0.18μm CMOS technology. The chips are housed in a QFN48 package and mounted on Rogers PCB for evaluation. A transmitted data pattern (at the TX input), received pulse pattern (at the RX input), and demodulated data pattern (at the integrator output) are shown in Fig. 6.2.6. Also a measured ranging result is illustrated where the measured time delay is 14.9us which corresponds to the ranging distance of 221.5cm. Furthermore, the system can achieve 0.2ns resolution which translates to two-way ranging accuracy of 3cm [1]. The transceiver performance is summarized in Fig. 6.2.6. Targeting low-cost and high-energy-efficiency implementation, it achieves 0.74μW/pulse for TX and 6.5μW/pulse for RX while occupying 4.5mm² of die area. The chip micrograph is shown in Fig. 6.2.7.

References:
Figure 6.2.1: 802.15.4a BPM-BPSK UWB Transceiver System Architecture.

Figure 6.2.3: Measured transmitted pulses and their spectra.

Figure 6.2.4: Multi-channel front-end circuits.

Figure 6.2.2: Transmitter circuits.

Figure 6.2.5: Multi-tone frequency generator.

Continued on Page 600
**Figure 6.2.6:** Measured transceiver performance. 

**Figure 6.2.7:** TRX chip micrograph.

---

**Measured Receiver BPSK demodulation (31.2Mb/s, LO 7.89GHz):**

\[ \Delta t = 14.9\text{ns} \]

**Measured two-way Ranging (15.6Mb/s, LO 4.49GHz):**

\[ \Delta d = \Delta t \times c / 2; \]

where:
- \( \Delta d \): object distance,
- \( \Delta t \): time delay,
- \( c \): velocity of light.

<table>
<thead>
<tr>
<th>Transmitter</th>
<th>Receiver</th>
<th>Overall</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak PRF:</td>
<td>499.2/1000MHz</td>
<td>VDD: 1.8V (can be as low as 1V)</td>
</tr>
<tr>
<td>Modulation:</td>
<td>BPSK</td>
<td>Technology: 0.18µm CMOS</td>
</tr>
<tr>
<td>BW:</td>
<td>499.2/1331.2MHz</td>
<td>Freq. generator: Ring OQCVI based</td>
</tr>
<tr>
<td>Energy/pulse:</td>
<td><a href="mailto:0.74uJ@1.8V">0.74uJ@1.8V</a></td>
<td>Freq. range: 3 to 9GHz, 12 channels</td>
</tr>
<tr>
<td>Pulse duration:</td>
<td>2.1ns</td>
<td>Ranging accuracy: 3cm</td>
</tr>
<tr>
<td>Start-up time:</td>
<td>6.9ns</td>
<td>Size (die size): 4.5mm²</td>
</tr>
</tbody>
</table>

Received Pulse

Demodulation output

\[ \Delta d = 223.5\text{cm} \]

---

**Receiver gain (LB/HB):** 80/90dB

**Noise Figure (LB/HB):** 8.2/9.4dB

**Sensitivity (LB/HB):** \(-75/\) - 70dBm

**IIP3:** \(-12/\) - 8dBm

**Energy/pulse:** 6.51nJ/p@1.8V

**Start-up time:** 25.5ns

**Transmitter:***

**Peak PRF:** 499.2/1000MHz

**Modulation:** BPM-BPSK

**BW:** 499.2/1331.2MHz

**Energy/pulse:** 0.74uJ@1.8V

**Pulse duration:** 2.1ns

**Start-up time:** 6.9ns

**Modulation signal**

**Received Pulse**

**Demodulation output**

\[ \Delta t = 14.9\text{ns} \]

\[ \Delta d = 223.5\text{cm} \]

---

**VGA:**

**Integrator:**

**Reserved for integrating ADC and Digital Baseband etc.**

---

Please click on paper title to view Visual Supplement.