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<th><strong>Title</strong></th>
<th>A 0.18m CMOS 802.15.4a UWB transceiver for communication and localization</th>
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<td><strong>Author(s)</strong></td>
<td>Zheng, Yuanjin; Arasu, Muthukumaraswamy Annamalai; Wong, King Wah; The, Yen Ju; Poh, Andrew Hoe Suan; Tran, Duy Duong; Yeoh, Wooi Gan; Kwong, Dim Lee</td>
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Yuanjin Zheng, M. Annamalai Arasu, King-Wah Wong, Yen Ju The, Andrew Poh Hoe Suan, Duy Duong Tran, Wooi Gan Yeoh, Dim-Lee Kwong
Institute of Microelectronics, Singapore, Singapore

Recently, IEEE 802.15.4a has specified an UWB PHY for low-rate commutation with ranging capability for wireless personnel area and sensor network applications [1]. Related work is reported on low-rate energy-efficient UWB radios [2-4]. However, they are not fully standard compliant or localization enabled. 802.15.4a supports three bands of operation, i.e., sub-1GHz band (249.6 to 749.6MHz), low band (3.1 to 4.8GHz) and high band (6.0 to 10.6GHz) with 16 channels in total. A combination of the burst position modulation (BPM) and binary phase shift keying (BPSK) is adopted. With different coding rate, bursts per symbol, and chips per burst, the mean pulse repetition rate (PRF) can vary from 3.9 to 62.4MHz for data throughput of 120kHz to 3.12MHz. This work presents an UWB RF transceiver which supports 12 channels, variable data rate, and ranging capability as specified in IEEE802.15.4a.

Figure 6.2.1 shows the RF transceiver architecture. On the TX side, the digital clock (TX_clk) triggers a baseband pulse-shaping filter (BPSF). The output pulses are modulated by the TX binary data signal. The signal is then upconverted by a mixer and amplified by a driver amplifier (DA) prior to the antenna. On the RX side, the weak signal is amplified by an LNA, is downconverted by I/Q mixers and is low-pass filtered to recover the phase of the transmitted BPSK signals. A VGA, in each I and Q path, is then used to boost the signal level to rail-to-rail. Through the edge detector, a digital clock (RC_clk), respectively. A passive 5th-order RC LPF with cut-off frequency of 250MHz is used. The five-stage cascaded dB-linear amplifier achieve a gain of 30.4/21.3dB, an NF of 5.5/7dB, and an IIP3 of −16.7/−10.7dB for low and high bands, respectively.

The RX front-end circuits are shown in Fig. 6.2.4. The LNA is designed to operate at one channel at any given time, through bank switching and channel selection, to minimize power consumption. The capacitive cross-coupled input stage is used to boost the Gm of the stage, and reduce input-referred noise while achieving good input matching. The bank switching between low and high band can be done by transistors M3/M4 and M5/M6. Within each band, there are two-stage cascaded amplifiers. The first stage is an LC-tuned load which is a common-source amplifier bank with the desired channel. The second stage is a common-source amplifier with an LC-tunable loading network. A double-balanced differential Gilbert cell is used as the mixer and its resistive loads are used to cover the entire UWB band. The combined TX front-end achieves a voltage gain of 30.4/21.3dB, an NF of 5.5/7dB, and an IIP3 of −16.7/−10.7dB for low and high bands, respectively.

The RX LPF is implemented by a 5th-order elliptical Gm-C filter with cut-off frequency of 250MHz. The five-stage cascaded dB-linear VGA achieves a dynamic gain of −90dB to 60dB with 400MHz BW. The variable BW integrator captures the reflected pulses from multipath and extends the duration of the demodulated pulses. For localization purpose, two squarers and one nonlinear low-pass filter (NLFP) [5] are used to regenerate RC_clk, where the squarers are used to detect the signal energy and NLFP is used to boost signal level to rail-to-rail. The equalized pulse train is turned on and off at the rising edge of TX_clk and RC_clk, respectively. A passive 5th-order RC LPF with cut-off frequency of 900kHz is used to average the jitter and noise and hence to significantly improve the ranging accuracy. Operating at 500MHz PRF, the peak current of the RX is 31mA.

A nine-tone frequency generator is shown in Fig. 6.2.5. A digital frequency-tuning loop is used to lock the quadrature VCO (QVCO) output frequency to an external 15.6MHz crystal reference. Once the QVCO is tuned to the desired channel, as determined by the lock detector, the tuning loop is powered off. The VCO tuning voltage is stored as a digital word in an 11b latch, where 3 bits are used for coarse tuning and the 8b DAC output is used for fine tuning. The accuracy of frequency tuning is <10MHz, which is limited by the phase discriminator resolution. To significantly reduce the die size, a four-stage ring oscillator with a frequency doubler is used as the QVCO core.

The transceiver IC is implemented in a 0.18µm CMOS technology. The chips are housed in a QFN48 package and mounted on Rogers PCB for evaluation. A transmitted data pattern (at the TX input), received pulse pattern (at the RX input), and demodulated data pattern (at the integrator output) are shown in Fig. 6.2.6. Also a measured ranging result is illustrated where the measured time delay is 14.9ns which corresponds to the ranging distance of 225.5cm. Furthermore, the system can achieve 0.2ns resolution which translates to two-way ranging accuracy of 3cm [1].

The transceiver performance is summarized in Fig. 6.2.6. Targeting low-cost and high-energy-efficiency implementation, it achieves 0.44mJ/pulse for TX and 6.5mJ/pulse for RX while occupying 4.5mm2 of die area. The chip micrograph is shown in Fig. 6.2.7.

References:
Figure 6.2.1: 802.15.4a BPM-BPSK UWB Transceiver System Architecture.

Figure 6.2.2: Transmitter circuits.

Figure 6.2.3: Measured transmitted pulses and their spectra.

Figure 6.2.4: Multi-channel front-end circuits.

Figure 6.2.5: Multi-tone frequency generator.

Continued on Page 600
Measured Receiver BPSK demodulation
(31.2Mb/s, LO 7.89GHz)

\[ \Delta t = 14.9 \text{ns} \]

Received pulse

Squarer output

Measuring two-way Ranging (15.6Mb/s, LO 4.49GHz):
\[ \Delta d = \Delta t \times \frac{c}{2}; \]

\( \Delta d \): object distance,
\( \Delta t \): time delay,
\( c \): velocity of light.

VDD: 1.8V (can be as low as 1V)
Technology: 0.18\( \mu \)m CMOS
Freq. generator: Ring QVCO based
Freq range: 3 to 9GHz/12 channels
Ranging accuracy: 3cm
Die size (die size): 4.5mm\(^2\)

Overall
Receiver gain (LB/HB): 80/90dB
Noise Figure (LB/HB): 8.2/9.4dB
Sensitivity (LB/HB): \(-75/\ -70\)dBm
IIP3: \(-12/\ -8\)dBm
Energy/pulse: 6.51nJ/p@1.8V
Start-up time: 25.5ns

Transmitter
Peak PRF: 499.2/1000MHz
Modulation: BPM-BPSK
BW: 499.2/1331.2MHz
Energy/pulse: 0.74nJ/p@1.8V
Pulse duration: 2/1ns
Start-up time: 6.9ns

Overall
Receiver gain (LB/HB): 80/90dB
Noise Figure (LB/HB): 8.2/9.4dB
Sensitivity (LB/HB): \(-75/\ -70\)dBm
IIP3: \(-12/\ -8\)dBm
Energy/pulse: 6.51nJ/p@1.8V
Start-up time: 25.5ns

Figure 6.2.6: Measured transceiver performance.

Figure 6.2.7: TRX chip micrograph.