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A Low-Power Bio-Sensor Interface with Wide Measurement Range

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Abstract—A new low-power high dynamic range conductance-to-frequency converter, using relaxation oscillator approach, is proposed for bio-sensor interfacing applications. Enhanced by a leakage current compensation technique, the interface has immunity against input pad ESD leakage current as well as hum noise. The output frequency is linear with respect to sensor conductance, with the maximum systematic error of 0.58% and average error of 0.46% for nanowire sensor resistance from 100 MΩ to 1 GΩ. For 2% systematic error, the resistance range of the interfacing system can attain from 5 MΩ to 5 GΩ. The bio-sensor interface is designed using CSM 0.18 µm CMOS technology, which dissipates 37.2 µW at a single supply of 1.8V and the maximum sensor current.

I. INTRODUCTION

For complex diseases, like cancer, the availability of multiple biomarkers is believed to be especially important in the diagnosis procedure. Silicon nanowire field-effect sensors, in which distinct nanowires can be incorporated into arrays, can be applied to detect cancer markers or proteins at femtomolar concentrations [1]. The electric field changes from binding of a charged species onto nanowire body leads to impedance variations. By monitoring the change on resistance or conductance, nanowire can be used for bio-sensor applications. The development of interface circuit facilitates the process of embedding silicon nanowire in portable devices. For silicon nanowire, an interface performing conductance-to-frequency conversion is very attractive. First, nanowire’s conductance is positively proportional to cancer marker concentration. Second, compared with a voltage output, a frequency output offers better noise immunity and easiness in multiplexing [2].

One of the problems in integrating nanowires with CMOS chips is the potential influence of the leakage current arising from the input ESD pads. For applications using external nanowire sensor, the ESD pad becomes an issue. The leakage current in ESD pads may defeat the sensitivity because the current sensing in nanowire can be as small as in femtoampere level or sub-nanoampere level, while the leakage current in typical ESD ranges from picoamperes to sub-nanoamperes, dependent upon process, structure and area. Regarding the issue, the proposed design presents a bio-sensor interface with dedicated compensation circuit. The interface is suitable for portable applications and performs conductance-to-frequency conversion based on relaxation oscillator technique. In the design, the problem of ESD leakage disturbance is solved by the design of leakage current compensation circuit. The proposed interface circuit consumes low power and provides wide conductance sensing range without using sub-ranging design technique [3].

II. OVERVIEW OF THE INTERFACE CIRCUIT

The nanowire interface circuit is shown in Fig. 1, which comprises a sensor resistor, a V-I converter, PMOS current mirrors, a leakage current compensation circuit and a relaxation oscillator circuit. The oscillator part is further composed by a capacitor, a comparator, a dummy-compensated MOS switch and a digital frequency divider.

The electrical model of nanowire can be treated as a linear resistor when restricting to small Vds range, for instance, | Vds | ≤ 0.25 V in a heavily P-doped wire [4]. Biased with a stable bandgap voltage reference VREF, the sensor R_{sens} is independent from the oscillator circuit. VREF is set to 0.2 V for typical nanowire biasing potential. Unfortunately, such the sensor current I_{sens} can be comparable to the ESD leakage current. For simplification, the leakage current from ESD pad is represented as a current source I_{leak} in Fig. 1.

At Node A, the total current is a summation of I_{sens} and I_{leak}. With the same condition applied, the leakage current is regenerated in the compensation circuit formed by op-amp,
M2-M3, M6 and I_{leak}. Mirrored by PMOS pair M2-M3, I_{leak} is forced into Node B. This leads to the I_{ens} that is reproduced in the PMOS current mirror M1-M4 and further injected to the oscillator circuit at Node C. In this way, the influence of leakage current on sensing current is effectively prevented. The generated current I_{ens} feeds into a capacitor C, which behaves as an integrator. Once the voltage across the capacitor exceeds a boundary voltage V_{L}, control signal logic “1” is generated at the output of the comparator, thus closing the MOS switch and making the capacitor discharge. In the discharging process, once the voltage of the capacitor drops below V_{L}, logic “0” appears at the output of the comparator, thus opening the MOS switch and making the capacitor start charging again. The sequence of logic “1” and “0” are further captured by a flip-flop, which divides the frequency of the digital signal by half, making it suitable for a frequency counting device. The output signal frequency f_{osc} is directly proportional to the sensor conductance G, as shown below:

\[ \text{Slew rate} = \frac{I_{sens}}{C} = \frac{\Delta V}{\Delta T} \quad (1) \]

\[ \Delta T = \frac{\Delta V \cdot C}{I_{sens}} = \frac{\Delta V \cdot C}{V_{ref} \cdot G} \quad (2) \]

\[ T_{osc} = 2 \Delta T = \frac{2 \Delta V \cdot C}{V_{ref} \cdot G} = \frac{2 V_{L} \cdot C}{V_{ref} \cdot G} \quad (3) \]

\[ f_{osc} = \frac{1}{T_{osc}} = \frac{V_{ref}}{2V_{L} \cdot C} \cdot G \quad (4) \]

As a result, it can be shown that f_{osc} is proportional to G. Any change in G reflects change in frequency. This technique has the advantages of simplicity and suitable for large sensor array implementation. Each sub-block of the system will be described in the following subsections.

### III. INTERFACE BUILDING BLOCKS

#### A. The V-I converter

The V-I converter consists of a high-gain, micro-power amplifier and an NMOS transistor in feedback configuration. The output of the operational amplifier (op-amp) is connected to the gate of the MOSFET, which regulates the gate voltage to minimize the variation of the drain current via feedback and provides constant voltage bias to the nanowire resistor. With 0.2 V voltage bias applied, the nanowire current ranges from 199.81 pA to 1.9895 nA.

![Figure 2. Single-stage op-amp](image)

![Figure 3. ESD protection circuit](image)

Micro-power op-amp is realized using the weak-inversion design approach. The op-amp is a single-stage amplifier shown in Fig. 2. The input stage comprises a differential pair with an active load and a high-swing cascode biasing current source. The input stage performs as a combination of a differential gain stage and a differential-to-single-ended converter. Herewith, the biasing current is designed to be 600 nA using micropower active biasing technique [5] to reduce silicon area. The op-amp provides a DC gain of 60.24 dB, unity gain bandwidth of 353 kHz and phase margin of 50.89 degree at power consumption of 5.8 µW. The performance parameters are adequate for bio-interface application since the nanowire sensing signal is of very low frequency. With the structure of high-swing cascode for giving the headroom, the single-stage op-amp is able to withstand ±10% V_{dd} variations.

#### B. ESD protection circuit

To be interfaced with CMOS chips, silicon nanowires must go through ESD pads. The leakage current in ESD pads may defeat the sensitivity of nanowire sensing, especially when nanowire current becomes comparable to the leakage current. The objective of including ESD protection circuit into this interface design is to establish the leakage current compensation circuit for leakage current cancellation. Fig. 3 shows the protection diodes, with two types of PN junction structures – reverse biased diode and the MOS diode. The total leakage current obtained in the pad is the net leakage current arising from the difference of two leakage currents from two different diode types. Herewith, the net ESD leakage current at room temperature is 75.6 pA in the pad used. This may not be significant when compared to higher nanowire sensor currents. Unfortunately, the nanowire current, especially at lower limit of conductance, is about 2.6 times of the leakage current. The two currents become comparable. Therefore, the effectiveness of the leakage current compensation technique will be verified through the simulations of the bio-interface (Fig. 1) in section IV.

#### C. The comparator

The major components in the micropower comparator, as depicted in Fig. 4, are a folded-cascode op-amp stage, a push-pull stage and an inverter chain. A folded gain stage is used to realize the comparator but with push-pull output to have good slew rate performance. Because of using folded gain stage, low level output voltage down to 0.2 V can be handled by the micropower-based comparator without encountering input common-mode range problem.

In order to raise the speed of comparator while maintaining low power to avoid unnecessary over biasing condition, the concept of a dynamic biasing scheme is added to the static biasing currents in Fig. 5. For a static biasing current I_{o} (100nA in this example) comes from a current reference, there is a total 4.5 times of I_{o} static bias resulted in each folded branch. This type of current remains constant, regardless of the variation brought by nanowire current because the current is derived from current biasing circuit [4].
To increase the comparator speed further for wide frequency operation range, the dynamic biasing current sources are added, with the dedicated scaled nanowire currents $I_{dy}$. As nanowire current is very small ($I_{nw(max)} \approx 2 nA$), a relative large scaling ratio has to be used. The magnitude of the dynamic current follows the value of nanowire current. The latter depends on nanowire conductance. The total current injected in each folded branch is 530 nA ~ 1250 nA in the design, hence modulating the speed of comparator accordingly.

A clamp transistor M17, at the output of the first stage, reduces the signal swing at the output port. The subsequent push-pull stage is able to sink and source large currents into the output capacitance. The inverter chains are used to increase the response of the comparator output signal. This inverter chain can also act as a driver stage such that the push-pull transistors can be made smaller to reduce the parasitic capacitance at their gates for a faster response.

The frequency-divider and clock generation unit

The objective of this digital section is to divide the frequency of comparator output by half so as to make the signal ready for a counting device. It consists of two parts: clocked D flip-flop and a clock generation unit. The latter is designed for the dynamic D flip-flop. The Dynamic D flip flop is preferred over the static design, because of faster speed and minimized initial uncertain states. Fig. 6 shows the design of clocked D flip-flop. The clocked D flip-flop is positive edge triggered. It is based on a master-slave concept and it is insensitive to clock overlap, as long as the rise and fall times of the clock edges are sufficiently small. The source of the clock signal is the comparator output. The clock generation unit is also shown in Fig. 6. Using a transmission gate and CMOS inverters, same amount of delay is taken into account during the inversion of comparator output signal Comp_CLK. Hence, CLK and CLK_bar signals are able to be generated simultaneously.

IV. RESULTS AND DISCUSSIONS

A. Leakage current compensation

To relate the sensor current $I_{sens}$ and oscillator input current $I_{out}$, the transistor-level simulation, which was based on CSM 0.18 μm BSIM3 models, was conducted by sweeping nanowire conductance from 1 nS to 10 nS at 27 °C. The responses (I vs. G) of compensated and uncompensated system are shown in Fig. 7.

Fig. 7 shows that both $I_{sens}$ and $I_{out}$ are linearly proportional to nanowire conductance G. The overlapping of $I_{sens}$ and $I_{out}$ in Fig. 7(a) shows better accuracy in duplicating $I_{sens}$ into oscillating system. This is because of the ability of leakage current compensation circuit in suppressing the ESD leakage. On the contrary, the uncompensated system exhibits an offset between the two currents as illustrated in Fig. 7(b).

B. Hum noise rejection

The hum noise was emulated by a 2 mVpp, 50Hz sinusoidal wave from the $V_{ref}$ of the op-amp. The simulation was carried out at 27 °C for nanowire conductance of 1nS at lower limit. The triangular waveform in Fig. 8 shows the charging and discharging of the integrating capacitor. The comparator output (Comp_CLK) is the pulse stream at the third row. The buffered output signal (Q_buf) after frequency divider is shown at the last row. The comparison between the two plots shows that besides suppressing ESD leakage current, the design of leakage current compensation also has the ability of suppressing $V_{ref}$ hum noise. In contrast, with the same type of hum noise applied, the system without compensation circuit...
has already shown instability at this stage, which is indicated by the distortion in the triangular wave and the irregularity in output bit stream.

C. **G-to-F conversion**

In Fig. 8, compared with the pulse stream, the buffered output signal shows that the period has been doubled which is suitable to feed into a counting device. The frequency is directly proportional to sensor conductance value. The simulated results in Fig. 9 have demonstrated that the converted output frequency is linearly proportional to nanowire conductance. Furthermore, shown in Table I, at typical case, all the error percentages are less than 0.6% for resistance range of 100 MΩ ~ 1 GΩ. The average level of systematic error on accuracy is 0.46%. Even ±5% change in ESD leakage current due to mismatch effect, there is no significant change on the simulated results.

Comparing the error percentage of compensated and uncompensated systems in Fig. 9, the compensated system provides higher precision in G-to-F conversion process. For instance, when nanowire current becomes comparable with ESD leakage current, the influence of leakage current is effectively removed by the compensation circuit. If the acceptable error percentage is 2%, based on simulation, the resistance range of the interface can be attained from 5 MΩ ~ 5 GΩ, contributing a wide dynamic range without the use of sub-ranging design technique.

**V. CONCLUSION**

A novel low-power bio-sensor interface architecture based on relaxation oscillator is proposed. Enhanced by an ESD leakage compensation circuit, the accuracy in G-to-F conversion is increased. The hum noise rejection is also enhanced. Improved by dynamic biasing design in comparator, the output frequency attains three-decade range without using sub-ranging technique whilst the nanowire sensing system is kept good linearity with respect to the change of nanowire conductance.

**REFERENCES**


