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Author(s)	Chang, Richard Weng Yew; See, Kye Yak; Soh, Wei-Shan; Oswal, Manish; Wang, Lin Biao
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Measurement of Output Driver Impedance for Signal Integrity Design Consideration

Weng-Yew Chang, Richard [#1], Kye-Yak See[*2], Wei-Shan Soh[*3], Manish Oswal[*4], Lin-Biao Wang[*5]

[#] *DSO National Laboratories, Guided Systems Division*
20 Science Park Drive, Singapore 118230, Singapore
[1]cwengyew@dso.org.sg
[*] *Nanyang Technological University*
Division of Circuits and Systems, School of EEE, Singapoe
[2]ekysee@ntu.edu.sg,[3]wssoh@ntu.edu.sg,[4]moswal@ntu.edu.sg,[5]wang0474@ntu.edu.sg

***Abstract* — Impedance matching is crucial in high-speed digital design to ensure signal integrity (SI). Accurate information of a device's output impedance allows precise selection of series resistor to match the device's output to the characteristic impedance of the connecting trace. This paper proposes an in-circuit measurement technique using two current probes to extract the output impedance information of an active device under its normal operating conditions. The measured impedance has been validated with the time-domain simulation results obtained from CST Design Studio.**

***Index Terms* — device characterization, in-circuit measurement, series termination.**

I. INTRODUCTION

The importance of interconnects termination designs in high-speed digital design has been well reported in many literature [1-4]. With integrated circuits (ICs) operate at much faster edge rates, proper terminations to ensure good impedance matching and signal integrity (SI) have become indispensable for functional reliability in high-speed systems. Excessive and prolong overshoot can damage devices, and together with undershoot, they cause eye closure in the eye diagram, which can lead to intermittent false triggering.

Due to its simplicity and ease of implementation, series termination is by far the most commonly used technique to match an IC driver output with an interconnecting trace. By doing so, it minimize the signal reflections at the interface between the driver output and the transmission line. The value of a series resistor is very much dependent on the driver output impedance and the trace's characteristic impedance. As the driver output impedance characteristic is often not readily available and changes with operating conditions, selection of the correct resistor can be a difficult task. Without the information of output driver impedance, the series termination design has to be carried out on a trial-and-error basis.

This paper presents a simple and yet reliable technique to extract the output impedance of the device up to 800 MHz under its intended operating condition.

II. MEASUREMENT SETUP

The dual current probes measurement technique for characterizing impedance of a device has long been researched since mid 60s and reported by various researchers [5-9]. However, most of the work mainly focuses on power related fields, such as power line impedance and common-mode choke characterization with measurement frequency range less than 100 MHz. This paper explores the feasibility of in-circuit active device impedance characterization up to 1 GHz. As the current probes do not require direct electrical contact to the device-under-test (DUT), the method minimizes the loading effect and disturbances to the DUT. Also, with a pre-measurement characterization process, the method has the ability to eliminate measurement error contributed by the measurement setup.

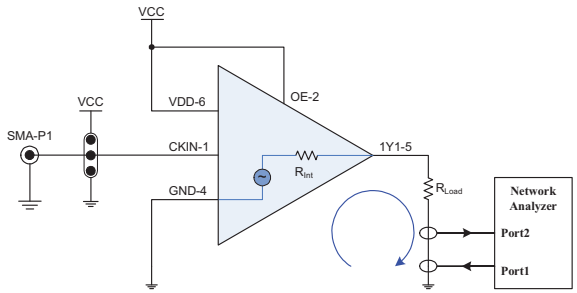

Figure 1. Circuit of the Two-Probe Setup

The basic concept of measuring the unknown impedance of a device using two-probe approach is illustrated in Fig. 1. The setup consists of an injecting current probe, a receiving current probe and a vector network analyzer (VNA). The two current probes couple to the circuit through inductive coupling without direct connection to the active circuit. By reflecting the primary circuits of the injecting and receiving probes in the coupled circuit loop, the equivalent circuit of the measurement setup can be represented as in Fig. 2. Z_{m1} and Z_{m2} are the reflected impedances of the injecting and receiving probe, respectively. V_{M1} is the reflected signal voltage in the coupling loop from the output signal source of port 1 of the VNA. R emulates the dc biasing current. L and r are the effective loop inductance and resistance, respectively.

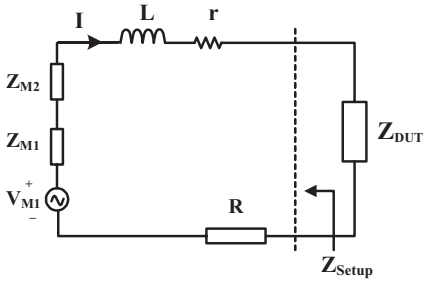

Figure 2. Simplified Equivalent Circuit of the Two-Probe Setup

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The resultant current flowing in the coupling loop due to the injecting signal is given by:

$$I = \frac{V_{M1}}{Z_{M1} + Z_{M2} + r + R + j\omega L + Z_{DUT}} \quad (1)$$

By letting $Z_{setup} = Z_{M1} + Z_{M2} + r + R + j\omega L$, equation (1) can be simplified as follows:

$$I = \frac{V_{M1}}{Z_{setup} + Z_{DUT}} \quad (2)$$

The induced voltage in the loop is given by:

$$V_{M1} = j\omega M_1 \left(\frac{V_1}{Z_{p1} + Z_1} \right) \quad (3)$$

Where M_1 is the mutual inductance between the injecting probe and the coupling loop, V_1 is the output source voltage of port 1, Z_1 is the output impedance of port 1 and Z_{p1} is the impedance of injecting probe seen by port 1.

The current I measured by the receiving probe is:

$$I = \frac{V_2}{Z_{T2}} \quad (4)$$

Where V_2 is the received signal at port 2 and Z_{T2} is the transfer impedance of the receiving probe.

By substituting equations (3) and (4) into (2), the unknown output impedance of the driver gate Z_{DUT} can now be determined as follows:

$$Z_{DUT} = \frac{kV_1}{V_2} - Z_{setup} \quad (5)$$

Where $k = \frac{j\omega M_1 Z_{T2}}{Z_{p2} + Z_1}$ is a frequency dependent coefficient. By replacing Z_{DUT} with a known precision standard resistor R_{std} and then with a short during the pre-measurement calibration process, Z_{setup} can be found as follows:

$$Z_{setup} = \frac{V_2\big|_{Z_{DUT}=R_{std}}}{V_2\big|_{Z_{DUT}=0} - V_2\big|_{Z_{DUT}=R_{std}}} R_{std} \quad (6)$$

Once the measurement setup is calibrated, it is ready to measure the unknown output impedance of the driver Z_{DUT} under in-circuit condition as follows:

$$Z_{DUT} = \frac{(R_{std} + Z_{setup})V_2\big|_{Z_{DUT}=R_{std}}}{V_2\big|_{Z_{DUT}=Driver}} - Z_{setup} \quad (7)$$

III. Clock Drive Output Measurement

In most cases, precise information of device output impedance is often not readily available in the standard device datasheet. Most designers are based on past experiences and decide an approximate value is. Although IBIS models are available but again not fully validated and users have to ensure correctness when using these models. With the proposed two probe measurement technique, it provides a relatively simple, reliable and accurate way to determine the output impedance of the device under intended operating conditions. The measurement can be implemented in a standalone device acceptance jig or integrated into the actual PCB design.

A. Practical Case Study

As a practical case study, the Texas Instrument 200MHz clock buffer (CDCV304PW) is used as a DUT to demonstrate the two-probe measurement technique. The measurement circuit is shown in Fig.3. The two identical current probes (Tektronix CT-6, bandwidth 1MHz-1GHz), one for injection and the other for measuring, are connected to the Vector Network Analyzer (Rohde&Schwarz ZVB8 8.5GHz).

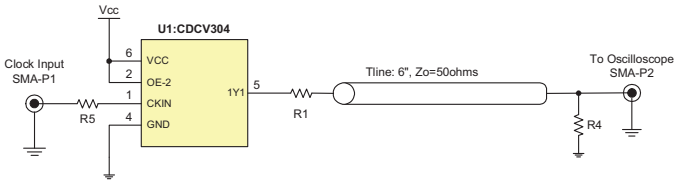

Figure 3. Test circuit Schematic for two Probe Measurement

The circuit is implemented on a PCB with its layout as shown Fig.4. Additional components require include a resistor R2 to provide the intended current due to the termination and two jumpers W3 & W4 for the connections to the CT6 probes. The final setup and connection is shown in Fig. 5.

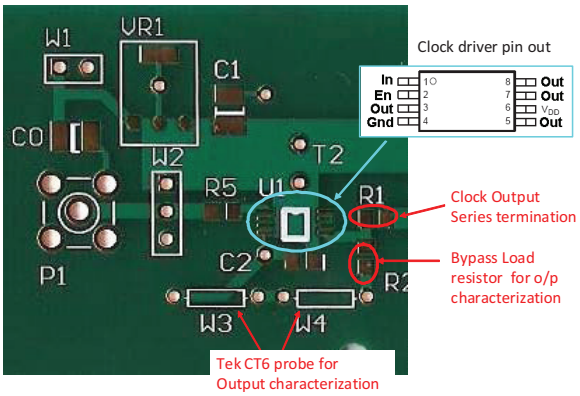

Figure 4. PCB Layout of Clock Circuit

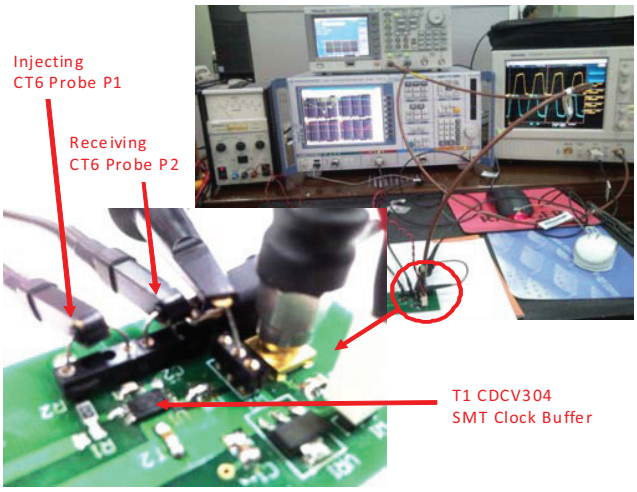

Figure 5. Two Probe Measurement Test Setup

Using a short and a known 50Ω resistor for the setup calibration, the values of k and Z_{setup} are determined and shown in Fig. 6 and Fig. 7, respectively. With the values of k and Z_{setup}, the setup is ready to measure the output impedance of the clock driver. The measured clock output driver impedance is found to be around 23 Ω, as shown in Fig.8.

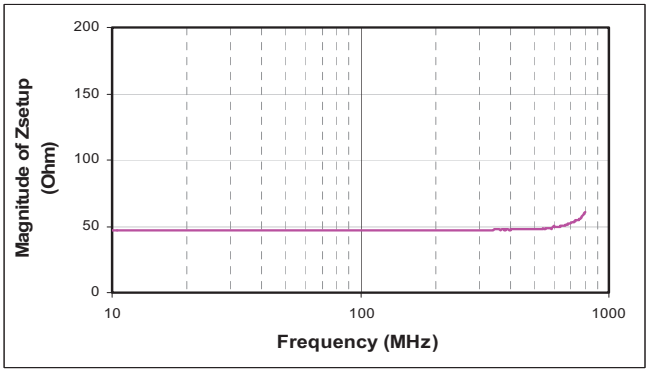

Figure 6. Measured Value of Z_{setup}

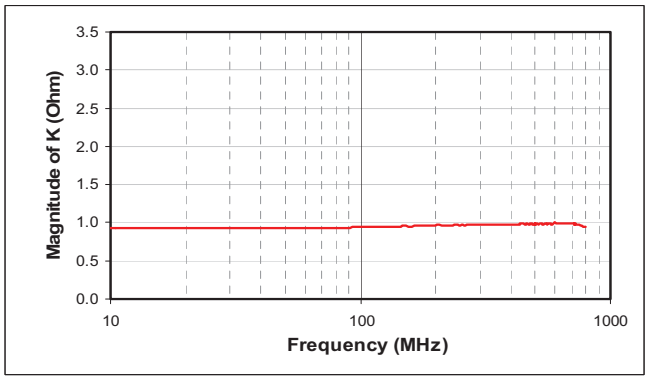

Figure 7. Measured Value of k

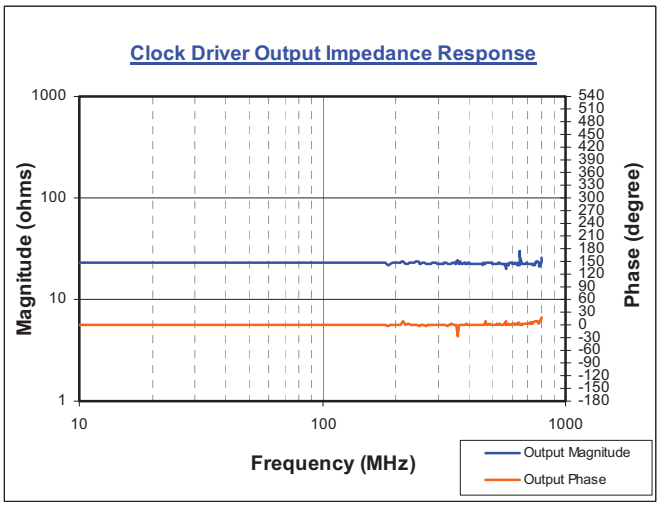

Figure 8. Measured Clock Driver Output Impedance Charcteristic

IV. Simulation Results Validation

The clock driver circuit is simulated on simulation tool, Computer Simulation Technology Design Studio (CST-DS), with IBIS model obtained from manufacturer website. The simulated circuit is shown in Fig. 9. The clock driver's output drives a 6" microstrip transmission line with the far-end of the transmission line terminated with an impedance equivalent to the Tektronix TAP3500 probe impedance.

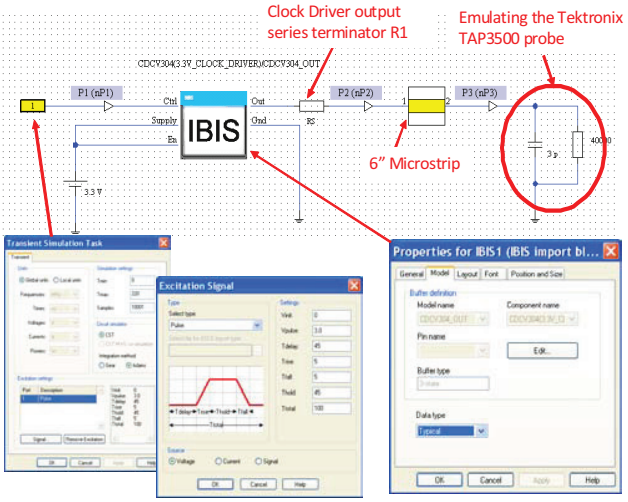

Figure 9. CST-DS IBIS Transient Simulation Setup

Using CST time-domain circuit simulation, a parameterized sweep on the output series terminator R1 across a range of values from 10 to 30 Ω is performed. The output overshoot behavior at the receiver is observed in Fig. 10 and 25 Ω appears to be most suitable value with minimize overshoot, which correlates well with 23 Ω value measured with the two-probe approach.

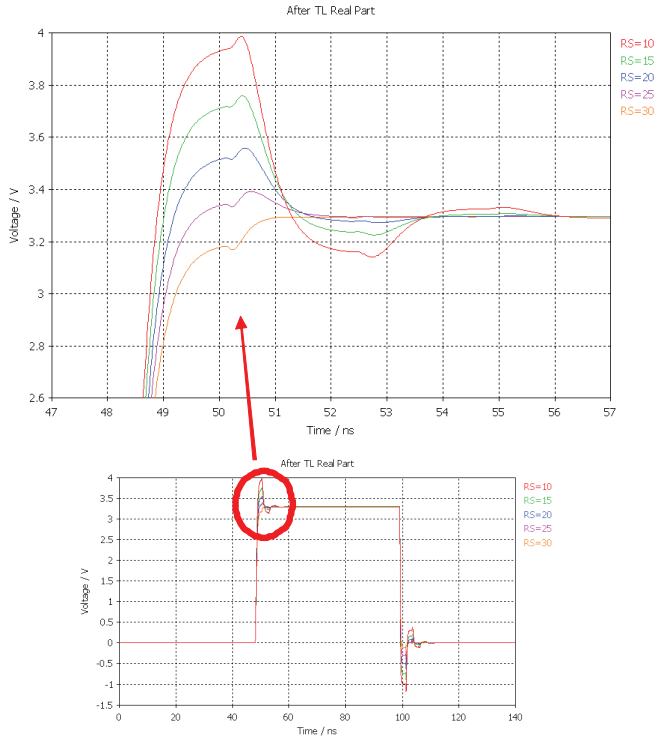

Figure 10. IBIS Simulation Using Parameter Sweep to Determine the Series Resistance R1

CONCLUSION

In high-speed digital application with edge rate in the sub-nano second region, the importance of knowing the device output impedance for proper series termination is highlighted. A novel in-circuit measurement technique using a non-contact two current probes approach to characterize a digital device output is presented. A practical case study using a high-speed clock driver is demonstrated and validated with the circuit-based simulation results. With the proposed measurement method, the output impedance of a device can be extracted with good accuracy. It will enhance the confident of the designer in digital termination design for optimized signal integrity performance.

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