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Memory Characteristics of MOSFETs With Densely Stacked Silicon Nanocrystal Layers in the Gate Oxide Synthesized by Low-Energy Ion Beam

C. Y. Ng, Student Member, IEEE, T. P. Chen, Member, IEEE, L. Ding, and S. Fung

Abstract—Densely stacked silicon nanocrystal layers embedded in the gate oxide of MOSFETs are synthesized with Si ion implantation into an SiO$_2$ layer at an implantation energy of 2 keV. In this letter, the memory characteristics of MOSFETs with 7-nm tunnel oxide and 20-nm control oxide at various temperatures have been investigated. A threshold voltage window of $\sim$ 0.5 V is achieved under write/erase (W/E) voltages of $+12$ V/$-12$ V for 1 ms. The devices exhibit good endurance up to $10^5$ W/E cycles even at a high operation temperature of 150 $^\circ$C. They also have good retention characteristics with an extrapolated ten-year memory window of $\sim$ 0.3 V at 100 $^\circ$C.

Index Terms—Low energy ion beam, memory effect, silicon nanocrystal (nc-Si).

I. INTRODUCTION

ANOCRYSTAL-BASED memory devices have recently attracted much attention due to their potential to overcome the limitations of current poly-silicon-based floating-gate memory. Since the first report of silicon nanocrystal (nc-Si) memory devices synthesized with chemical vapor deposition (CVD) method [1], [2], various CVD-based syntheses have been developed to precipitate nc-Sis that function as storage nodes [3]–[8]. The Si ion implantation method was also employed to introduce nc-Si into SiO$_2$ dielectric film [9], [10]. Recently, ultralow energy implantation ($0.65$–$1$ keV) to introduce nc-Si into a thin SiO$_2$ film has been demonstrated, and an average write/erase time of $\sim$ 10 ms of the nc-Si memory has been achieved [11], [12]. However, it is not practical for many CMOS fabrication facilities that are usually equipped with medium energy implanters (the implantation energy can be down to $\sim$ 2 keV) to use such an ultralow implantation energy. As such, it would be meaningful to explore the feasibility of utilizing the lowest implantation energy of a medium energy implanter (i.e., $\sim$ 2 keV) to synthesize the nc-Si for memory application. In this letter, we have synthesized nc-Si with an implantation energy of 2 keV using a medium energy ion implanter. MOSFETs with the gate oxide containing the nc-Si are found to be able to function as a nonvolatile memory device with good memory characteristics.

II. EXPERIMENT

Except for the additional steps of the nc-Si synthesis, n-channel MOSFETs with gate oxide containing the nc-Si are fabricated with a conventional 2-$\mu$m CMOS process. A 20-nm SiO$_2$ film is thermally grown on p-type Si(100) wafers in dry oxygen at 950 $^\circ$C. Si$^+$ ions with a dose of $5 \times 10^{16}$ cm$^{-2}$ are implanted at 2 keV into the oxide. The stopping and range of ions in matter (SRIM) simulation shows that the implanted Si distributions from the surface to a depth of $\sim$ 13 nm in the 20-nm thermal oxide, suggesting the existence of a tunnel oxide of $\sim$ 7 nm. An additional 20-nm SiO$_2$ is deposited on top of the previously grown oxide by low-pressure CVD (LPCVD) to form a 20-nm control oxide. Then, thermal annealing is carried out at 1000 $^\circ$C in N$_2$ ambient for 1 h to induce nc-Si formation. Fig. 1(a) shows the SRIM simulation of nc-Si distribution in the gate oxide. The mean nc-Si size ($D$) can be estimated from the X-ray diffraction measurement with Scherer’s equation $D = 0.9 \lambda / \Delta \theta \cos(\theta_B)$ [13], where $\lambda$ is the wavelength of the X-ray, $\theta_B$ is the Bragg angle, and $\Delta \theta$ is the full-width at half-maximum (FWHM) of the Bragg peak after correction for instrumental broadening. Here, $\lambda = 1.54$ Å, $\theta_B = 55.7$ $^\circ$, and $\Delta \theta = 0.0576$ (radian). Thus, the estimated nc-Si size is $\sim$ 4 nm. The cross-section transmission electron microscopy (TEM) image [Fig. 1(b)] of the memory device clearly shows the existence of densely stacked nc-Si layers. It also confirms the existence of $\sim$ 7 nm tunnel oxide and $\sim$ 20 nm control oxide. In the present study, the write/erase (W/E) operations are carried out with Fowler–Nordheim (FN) tunneling under a positive and negative gate voltage (all other terminals are grounded), respectively. Note that the write operation can also be carried out with channel hot electron (CHE) injection. It is observed that the CHE can yield a larger memory window and a better endurance. For simplicity, in this letter, all the discussions are based on the FN mechanism only.

III. RESULTS AND DISCUSSIONS

Fig. 2 shows the W/E behaviors under different gate voltages with various pulse widths ranging from 10 $\mu$s to 1 s. The threshold voltage shifts strongly depend on the magnitude and the duration of the W/E operations. A threshold voltage window of $\sim$ 0.5 V can be achieved under $+12$ V/$-12$ V for 1 ms. A larger threshold voltage window and a shorter W/E time can be achieved with a thinner tunneling oxide. In the following
discussions, the memory characteristics are measured with a W/E voltage of ±12 V and a W/E time of 1 ms.

Fig. 3 shows the endurance characteristics of the memory device. At room temperature, only a small drift of 0.1 V in the threshold voltage for both W/E operations is observed after $10^5$ W/E cycles, showing good endurance. At a temperature of 150 °C, the threshold voltage shift after $10^5$ W/E cycles is still less than 0.2 V for both write and erase operations. The drift-up in the threshold voltage is attributed to the electron trapping in the control oxide. The nanocrystal layer may be not able to capture all the injected electrons from the substrate, and some of the injected electrons are trapped in the control oxide [6]. Incomplete removal of the trapped electrons from both the control oxide and the nc-Si during the erase operation leads to an increase in the flatband voltage. Fig. 3 clearly shows that this effect is enhanced by a higher operation temperature.

The retention characteristics of the memory devices are shown in Fig. 4. The threshold voltage for both write and erase states is monitored after 1000 W/E cycles. There are no obvious changes in the threshold voltage for up to $10^4$ s of waiting time. The long-time extrapolation gives a ten-year memory window of ~0.3 V for operation temperatures of up to 100 °C, fulfilling the requirement of ten-year retention at 85 °C. However, the retention characteristics for the write state degrade (i.e., the threshold voltage decreases with waiting time) at 150 °C after $10^4$ s of waiting time, as shown in Fig. 4. The decrease of threshold voltage may be due to the escape process of the trapped electron at a higher temperature. At 150 °C, the threshold voltage for the erase state saturates at ~1.7 V after $10^4$ s of waiting time. The retention performance
IV. CONCLUSION

In this letter, densely stacked nc-Si layers embedded in the gate oxide of MOSFETs are synthesized with Si ion implantation into an SiO\textsubscript{2} layer at the lowest possible implantation energy (i.e., 2 keV) of a medium-energy implanter. The memory characteristics of the MOSFETs with 7-nm tunnel oxide and 20-nm control oxide at various temperatures have been investigated. A threshold voltage window of \( \sim 0.5 \) V is achieved under W/E voltages of \(+12\) V/\(-12\) V for 1 ms. The devices exhibit good endurance up to \( 10^5 \) W/E cycles even at a high operation temperature of \( 150 \) °C. They also have good retention characteristics with an extrapolated ten-year memory window of \( \sim 0.3 \) V at \( 100 \) °C.

REFERENCES