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Citation	Ng, C. Y., Chen, T. P., Zhao, P., Ding, L., Liu, Y., Tseng, A. A., et al. (2006). Electrical characteristics of Si nanocrystal distributed in a narrow layer in the gate oxide near the gate synthesized with very-low-energy ion beams. Journal of Applied Physics, 99, 1-3.
Date	2006
URL	http://hdl.handle.net/10220/6426
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Electrical characteristics of Si nanocrystal distributed in a narrow layer in the gate oxide near the gate synthesized with very-low-energy ion beams

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(Received 27 September 2005; accepted 8 March 2006; published online 25 May 2006)

A nanocrystal Si (nc-Si) distributed in a narrow layer in the gate oxide close to the gate is synthesized with Si ion implantation at 2 keV, and the electrical characteristics of the nc-Si structure are investigated. The onset voltage of the Fowler-Nordheim tunneling of the structure is lower than that of pure SiO_2 structure, and it decreases with the nc-Si concentration. The phenomenon is attributed to the reduction of the effective thickness of the tunneling oxide. The application of a positive or negative voltage causes electron or hole trapping in the nc-Si, leading to a positive or negative flatband voltage shift, respectively. A steplike flatband voltage shift as a function of charging voltage is observed, suggesting single electron or hole trapping in the nc-Si at room temperature. On the other hand, the nc-Si structure shows good charge-retention characteristics also. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2191737]

There are many recent studies on memory effect,[1–6] charge transport,[7,8] and optical or photoelectronic properties[9,10] of ion-beam synthesized nanocrystal silicon (nc-Si) embedded in SiO_2 thin films. In particular, recently it has been demonstrated that the synthesis of nc-Si with very-low-energy ion implantation can be used to fabricate nanocrystal-based flash memories.[3] With a low-energy ion implantation, the nc-Si can be confined in a very narrow layer embedded in the gate oxide. To investigate the memory effect of nc-Si, a common practice is to form the structure of gate/control oxide/nc-Si layer/tunnel oxide/Si substrate. In the present study, the above structure is simplified by using a single very-low-energy ion implantation into a SiO_2 thin film to eliminate the deposition of the control oxide.[11] In the simplified structure, the nc-Si is distributed in a narrow layer in the gate oxide near the gate. The simplified structure exhibits memory effect and shows good retention characteristics. In addition, the structure can be used for the studies of current transport and single-electron charging of the nc-Si. Some interesting phenomena have been observed with the structure. It is shown that the nc-Si layer can seriously affect the current transport across the gate oxide of the structure. The structure also exhibits a steplike flatband voltage shift as a function of charging voltage, suggesting that single electron or hole trapping in the nc-Si could occur at room temperature in such a simple structure.

A 30 nm SiO_2 thin film was thermally grown in dry oxygen at 950 °C on a *p*-type Si(100) wafer. Si^+ ions with a dosage of either 8×10^{16} (sample 1) or 1×10^{16} cm^{-2} (sample 2) were then implanted into the SiO_2 thin films at 2 keV. A control sample with the same oxide thickness without Si^+ ion implantation was prepared also. Thermal annealing was carried out for all implanted samples in N_2 ambient at 1000 °C for 1 h to induce nc-Si formation. The peak of Si concentration is located at ~6 nm underneath the SiO_2 surface as obtained from the stopping and range of ions in matter (SRIM) simulation. As revealed by the cross-sectional high-resolution transmission electron microscope (HRTEM) image shown in Fig. 1, the nc-Si size is ~5 nm, and the nc-Si is confined in a narrow layer with a layer thickness of about the same as the nc-Si size. Aluminum was deposited and patterned to form the top and bottom electrodes. Capacitance-voltage (*C-V*) measurement was performed at the frequency of 1 MHz with a HP4284A *LCR* meter. Current-voltage (*I-V*) measurement was performed at room temperature using a HP4156A semiconductor parameter analyzer.

Figure 2 shows the hysteresis effect in the *C-V* measurement from −8 to +6 V and then from +6 to −8 V. In con-

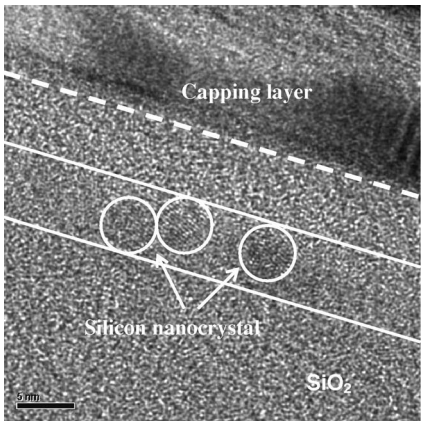

FIG. 1. Cross-sectional high-resolution TEM image of sample 2.

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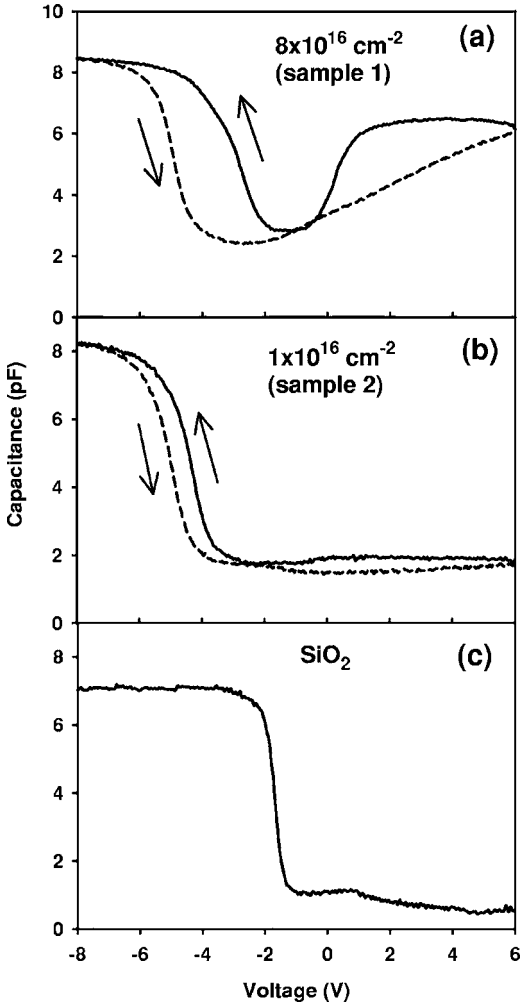

FIG. 2. Hysteresis behaviors in *C-V* measurement of sample 1 (a), sample 2 (b), and the pure SiO_2 sample (c).

trast to the control sample (i.e., without Si ion implantation) which doesnot show any hysteresis effect, both sample 1 (with a Si^+ dosage of 8×10^{16} cm^{-2}) and sample 2 (with a Si^+ dosage of 1×10^{16} cm^{-2}) show a large hysteresis effect. The hysteresis window is approximately ~1.8 V for sample 1 and ~0.6 V for sample 2, respectively, showing that a higher Si^+ dosage leads to a larger hysteresis effect. On the other hand, an increase in the capacitance at positive gate voltage is also observed for both sample 1 and sample 2 when the gate voltage is scanned from +6 to −8 V, as shown in Fig. 2. A higher Si^+ dosage leads to a large increase in the capacitance. The increase in the capacitance is due to the contribution of uncharged or neutral nanocrystals near the surface of SiO_2 to the total capacitance of the metal-oxide-semiconductor (MOS) structure.[5,6]

Figure 3 shows the gate current as a function of gate voltage for pure SiO_2 sample, sample 1, and sample 2. As shown in this figure, the introduction of nc-Si into the gate oxide leads to a reduction in the onset voltage of the Fowler-Nordheim (FN) tunneling, and the onset voltage decreases with the nc-Si concentration. This can be explained in the following. As the nc-Si distributes from the SiO_2 surface to a depth of ~10 nm in the 30 nm gate oxide, the gate oxide can be virtually divided into two regions: Region 1 is a pure SiO_2

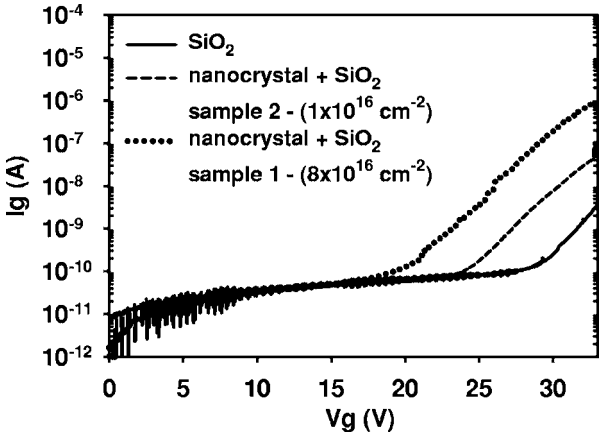

FIG. 3. Current-voltage characteristics of sample 1, sample 2, and the pure SiO_2 sample.

layer with a thickness T_1(~20 nm) and region 2 is a nc-Si-distributed region with a thickness T_2(~10 nm). When the FN tunneling occurs at the interface of gate oxide/substrate, it is determined by the electric field (E_1) in region 1 (i.e., the pure SiO_2 region). For the FN tunneling to occur, E_1 must be at least equal to the onset electric field ($E_{SiO_2}^{onset}$) for FN tunneling for pure SiO_2. Note that the $E_{SiO_2}^{onset}$ is a constant for pure SiO_2. The gate oxide voltage (V_{ox}^{onset}) required to achieve the $E_{SiO_2}^{onset}$ can be described by

$$V_{ox}^{onset} = E_{SiO_2}^{onset} T_1 + I^{onset} R_2, \tag{1}$$

where I^{onset} is the FN tunneling current at the electric field of $E_{SiO_2}^{onset}$, and R_2 is the resistance of region 2. When there is nc-Si distributed in region 2, the nc-Si can form conductive percolation tunneling paths[5,12] which reduce the R_2. In other words, the presence of nc-Si in region 2 leads to a lower R_2, and the R_2 decreases as the nc-Si concentration increases. Therefore, it can be concluded based on Eq. (1) that the onset voltage of the FN tunneling is lowered in the presence of nc-Si and it decreases with the nc-Si concentration.

The sample with nc-Si exhibits memory effect in terms of flatband voltage shift (ΔV_{fb}). As shown in Fig. 4, the application of a positive gate voltage causes a positive flatband voltage shift (i.e., $\Delta V_{fb} > 0$), while the application of a negative gate voltage leads to a negative flatband voltage shift (i.e., $\Delta V_{fb} < 0$). This indicates that the application of a positive or negative gate voltage results in electron or hole trapping in the nc-Si, respectively. For both electron and hole trappings, the flatband voltage shift strongly depends on the nc-Si concentration. For example, for the application of +25 V for 1 s, ΔV_{fb} is 5.85 V for sample 1 while it is only 0.60 V for sample 2. On the other hand, the magnitude of ΔV_{fb} for positive gate voltage is larger than that for negative gate voltage, showing that electron tunneling into the nc-Si is easier than hole tunneling into the nc-Si.

From Fig. 4, a steplike ΔV_{fb} can be observed for both positive and negative gate voltages. The phenomenon suggests single-electron trapping in nc-Si at room temperature. For the nc-Si with a size of ~5 nm in this study, the Coulomb charging energy of the nc-Si is estimated to be ~70 meV which is larger than the thermal energy (26 meV)

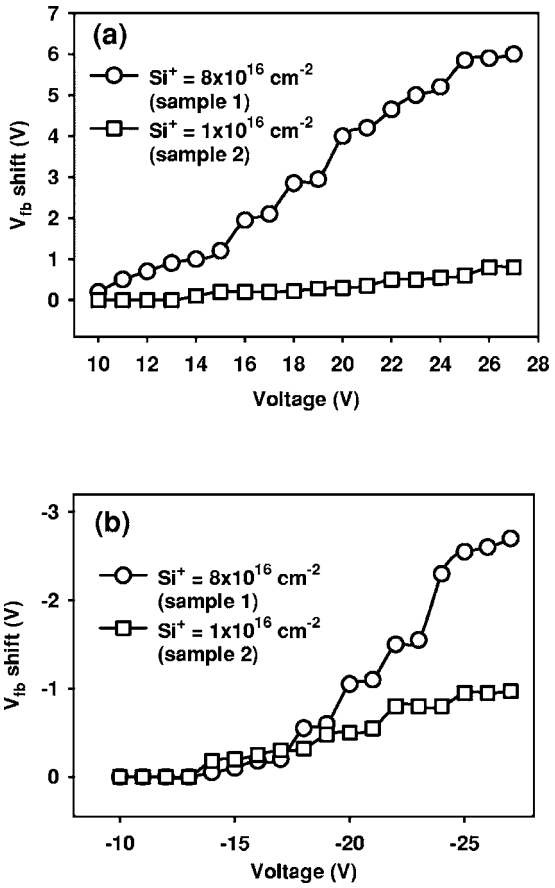

FIG. 4. Flatband voltage shift as a function of the applied positive (a) and negative (b) gate voltages. The duration of the application of a gate voltage is 1 s.

at room temperature.[13] Therefore, the Coulomb blockade effect could occur at room temperature. The threshold voltage shift (ΔV_{th}) due to electron trapping in nc-Si is given by[13,14]

$$\Delta V_{\text{th}} = \frac{npq}{\varepsilon_{\text{ox}}}\left(t_{\text{ctl}} + \frac{\varepsilon_{\text{ox}} t_{\text{nc}}}{2\varepsilon_{\text{Si}}}\right), \tag{2}$$

where n is the nanocrystal number density, p is the average number of electrons stored per nanocrystal, q is the electronic charge, ε_{ox} and ε_{Si} represent the permittivies of the oxide and Si, respectively, t_{ctl} represents the thickness of the control oxide, and t_{nc} is the linear dimension of the nanocrystal well. For nanocrystals that are 5 nm in dimension, a nanocrystal density of 2.5×10^{12} cm^{-2}, and a control oxide thickness of 6 nm, the threshold voltage shift is ~0.8 V for one electron per nanocrystal. This value is comparable with the experimentally observed steplike ΔV_{fb} which is ~0.5–~1 V. On the other hand, the Coulomb gap voltage for addition of a single electron to a nanocrystal can be calculated with the formula of e/C_{Σ}, where C_{Σ} is an approximation to the nanocrystal capacitance.[3,15] From the calculation, the Coulomb gap voltage is found to be ~+1.8 V, which is also comparable to the experimental observation that every increment of ~2 V of the gate voltage leads to a steplike ΔV_{fb}. The steplike ΔV_{th} (threshold voltage shift) behavior has also been observed in nc-Si structures by other researchers and is convincingly attributed to the single-electron trapping effect.[16,17] Of course, a more direct way to observe the single-electron effect is the measurement of the oscillation in the drain current of a MOS field-effect transistor (MOSFET) with nc-Si embedded in the gate oxide.[3,18] However, such a measurement requires that the transistor size must be very small (typically in the order of 10^{-16}m^2).

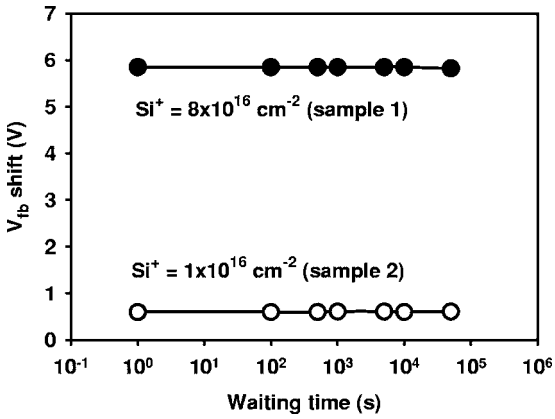

FIG. 5. Charge-retention characteristics of the nc-Si structure. Electron trapping in the nc-Si is achieved by the application of +25 V gate voltage for 1 s.

To investigate the charge retention in the nc-Si, a gate voltage of +25 V is applied for 1 s on both samples 1 and 2. Then *C-V* measurement is carried out to measure the flatband voltage shift as a function of waiting time. The result is shown in Fig. 5. There are no obvious changes in the flatband voltage shift for both samples 1 and 2 in the time frame of the measurement (10^5 s). Therefore, the actual charge-retention time is expected to be much longer than 10^5 s. This indicates that the ~6 nm SiO_2 between the metal gate and the nanocrystal layer is sufficient to hold the charge trapped in the nanocrystal.

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