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Lu$_2$O$_3$/Al$_2$O$_3$ gate dielectrics for germanium metal-oxide-semiconductor devices

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The future of semiconductor industries would depend on the continuous development of integrated circuit performance in order to meet the ever increasing demand for higher performance devices. The gate oxide thickness downscaling with conventional silicon dioxide will soon reach its limit for electron tunneling (~2 nm). With the decreased thickness, silicon dioxide is not a suitable material to be used due to the high leakage current, in which the gate current density will exceed the limit set by power dissipation considerations. It has therefore become necessary to replace the conventional SiO$_2$ with a high-k material for the continual improvement of next generation devices. Nevertheless, downscaling is not the only mean to achieve further improvement in device performances. High mobility semiconductors other than Si have been considered as an alternative channel material. Ge has attracted much interests as a possible replacement for Si due to the fact that both electron and hole mobilities in Ge are higher compared to that of Si. However, Ge has been known to have poor quality of its thermal oxide, which is unstable, water hydrolysable, and has poor electrical properties. It has been reported that Ge oxides thermally decompose and desorb from the surface at relatively low temperatures and induce point defects on the surface. These defects can easily act as recombination and generation centers because of the small bandgap of Ge. It has been shown that by depositing high-k material on Ge to replace the thermally oxidized layer of Ge, it is possible to obtain a thin equivalent oxide thickness (EOT) and high mobility. This has fueled the research into alternative channel material and dielectric materials. Rare earth oxides, such as La$_2$O$_3$, Yb$_2$O$_3$, and Lu$_2$O$_3$, are promising candidates for the next generation of high-k gate insulators, which are expected to be thermally stable in contact with Si even at high temperatures. Previously, Lu$_2$O$_3$ was reported to have a k value of 11–12 (Refs. 9 and 11) with a reported leakage current of $1.2 \times 10^{-3}$ A/cm$^2$ (at +1 V) for a 4.5 nm thick film. Lu$_2$O$_3$ is expected to have a good conduction band offset with Si and is a suitable high-k dielectric candidate because of the large band gap that is expected from Lu$_2$O$_3$ due to the completely filled 4f shell of Lu and its unique oxidation number (equal to 3), which avoids mixed Lu oxides stoichiometries with different electronic structures. In addition, the 2:3 metal:oxygen stoichiometry ratio promotes a low charge neutrality level and hence a high conduction band offset at the oxide/silicon interface. In order to achieve a stable high-k/Ge interface, it is very crucial to tailor the interfacial or passivation layer. One of the most common methods of Ge passivation is through the surface nitridation of the Ge substrate and through intentionally grown GeOn interfacial layer. Work on Al$_2$O$_3$ as a passivation layer on Ge is still limited although it has been widely used on Si substrate. In this work, we report the Lu$_2$O$_3$/Al$_2$O$_3$ gate dielectrics for germanium metal-oxide semiconductor devices.

The Ge substrate used was n-type wafers (111). Before film deposition on the Ge substrates, it is necessary to remove the native oxide present. We have used a conventional wet cleaning of cyclic HF (1:100 diluted HF solution) dip with rinsing in de-ionized water. The substrate was then treated with NH$_3$ plasma for the oxynitride passivation layer. Atomic layer deposition (ALD) was used to deposit a thin Al$_2$O$_3$ passivation layer using trimethylaluminium and O$_2$ plasma precursors. The ALD equipment used is Oxford FlexAL™ system. The Lu$_2$O$_3$ ultrathin films were deposited ex situ using the pulse laser deposition technique at a base pressure of $1.0 \times 10^{-7}$ Torr. A KrF excimer laser with a wavelength of 248 nm and an energy density of $\sim 1.5$ J/cm$^2$ was used. The frequency of the laser was set to 5 Hz. Rapid thermal annealing (RTA) was done on the samples in N$_2$ temperature for temperatures ranging from 300 to 600 °C. Top electrodes of Au with a diameter of 0.3 mm were sputtered using a physical mask. The bottom of the Si substrates was first cleaned using 1% HF to remove the native oxide before sputtering of gold to make the back contact. The film thickness and interfacial property were examined using high-

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resolution transmission electron microscopy (HRTEM) with JEOL 2010 microscope. The electrical characteristics of the fabricated metal-insulator-semiconductor devices were measured using a precision LCR meter (HP4284A) at a high frequency of 100 kHz for capacitance-voltage measurements (C-V) and semiconductor parameter analyzer (Keithley 4200) for the current density-voltage (J-V) measurements. For the high-resolution Rutherford backscattering spectroscopy (HRBS), a beam of 500 keV He⁺ is used. The beam was incident on the sample which was mounted on a high-precision five-axis goniometer installed in a UHV chamber. The incident angle of the beam is 59.5°. The HRBS spectrum is observed at a scattering angle of 65°. The secondary ion mass spectroscopy (SIMS) measurements were obtained using a TOFSIMS IV instrument, with 1 keV Cs⁺ as sputtering beam and 25 keV ⁶⁹Ga⁺ as analysis beam and detection of negative secondary ions.

Figure 1(a) shows a cross-sectional HRTEM image of Lu₂O₃/Al₂O₃ on the Ge substrate after RTA at 600 °C. As observed from the HRTEM micrograph, the thickness of the deposited films was approximately 7–8 nm. The film appeared to be amorphous throughout and there was no distinctive layer to indicate the deposited Al₂O₃. There was a clear abrupt edge between the substrate and the thin film, suggesting an absence of unstable interfacial layer. Comparing as-deposited and 600 °C Ge spectra from the SIMS analysis shown in the inset of Fig. 2, Ge updiffusion is evident. The above observation may be explained using the intermixing model proposed by Kamata,¹⁵ as illustrated in Fig. 1(b), whereby it is possible that both Al₂O₃ and Lu₂O₃ was able to mix with residual GeOₓ or out diffused elemental Ge as the case of ZrO₂ or Y₂O₃,¹⁶,¹⁷ such that the Lu₂O₃/Al₂O₃/GeOₓ/Ge stack was converted to Lu/Al-based germanate without an interfacial layer after annealing. It was shown in the HRBS spectrum in Fig. 2 that the Ge content in the high-k film increases with increasing annealing temperature. HRBS spectra fitting revealed that the introduction of annealing promoted the growth of the Lu-based germanate, partial conversion for the 300 °C sample and full conversion for the 400 and 600 °C sample.
Observed from the C-V curves, the accumulation capacitance increased with the increasing annealing temperature. A k value of 11.7 was obtained for the sample annealed at 600 °C in N₂ ambient, without taking into account the quantum mechanical tunneling effect. This translates to a capacitance equivalent thickness (CET) of 2.42 nm for the stack. This is close to the reported value for Lu₂O₃ of about 11–12.⁹,¹⁰ The electrical data seems to support earlier postulation that the higher annealing temperature allows better intermixing, thereby improving the electrical performance of the MOS stack. Increasing the annealing temperature from 300, 400, and 600 °C has improved the k value from 9.9, 10.8 to 11.7, respectively. In this case, the Al₂O₃ layer seems to suggest that it is an effective passivation layer. We believed that the Al₂O₃ may have had acted as an effective oxygen reaction barrier in preventing the formation of low quality interfacial GeO₂.¹⁸,¹⁹ This is plausible since GeO₂ and Al₂O₃ has a heat of formation of 43.9 and 1675 kJ/mol, respectively. Nevertheless, further effort in reducing the CET is required as the International Technology Roadmap for Semiconductors (ITRS) (Ref. 20) outlines that for a sub-22-nm technology, an EOT of <0.5 nm is required by 2016 to sustain gate terminal control of the charge carrier in the semiconductor channel.

The general trend of the J-V characteristic measured from the rapid thermal annealed samples is shown in Fig. 3(b). The leakage current at +1 V bias for the 300, 400, and 600 °C annealed samples was 2.19×10⁻⁴, 1.87×10⁻⁴, and 1.37×10⁻² A/cm², respectively. The reduction of leakage current is likely to have been caused through better intermixing at elevated temperature along with densification and defect alleviation in the film. In addition, it is observed that the leakage current was higher at 600 °C annealed sample as compared to the 400 °C annealed sample. One possible explanation is that although intermixing is a necessary condition to stabilize the interface and the leakage current, it is not entirely governed by the amount of Ge updiffusion. An excess Ge in the high-k layer is likely to quickly result in a poor electrical performance.¹⁵ Subsequently, the excessive Ge updiffusion may have caused defects in the film itself, which may contribute to leakage path and thus lead to the observed increase in the leakage current for the 600 °C annealed sample. HRBS spectra revealed an increasing trend of Ge content in the film with possible residual GeO that was present due to incomplete removal of the native oxide due to wet cleaning and/or outdiffused elemental Ge due to annealing, resulting in a Lu/Al based germanate. No interfacial layer was observed using HRTEM suggesting absence of GeO₂ based interfacial layer after annealing. HRBS spectrum revealed an increasing Ge signal intensity with increasing annealing temperature which suggests that there may be excessive Ge incorporation into the high-k film, which may degrade the electrical performance. This is reflected in the electrical measurement, although the k value is improved with annealing temperature, there is an increasing trend in the leakage current density suggesting degradation in electrical performance due to Ge incorporation. Our work suggests that 8.8 at. % of Ge in the film is excessive and result in degradation of the electrical performance of the device due to the increased leakage current.

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