<table>
<thead>
<tr>
<th>Title</th>
<th>Lu2O3/Al2O3 gate dielectrics for germanium metal-oxide-semiconductor devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>Author(s)</td>
<td>Darmawan, P.; Chan, Mei Yin; Zhang, T.; Setiawan, Y.; Seng, H. L.; Chan, T. K.; Osipowicz, T.; Lee, Pooi See</td>
</tr>
<tr>
<td>Date</td>
<td>2008</td>
</tr>
<tr>
<td>URL</td>
<td><a href="http://hdl.handle.net/10220/8038">http://hdl.handle.net/10220/8038</a></td>
</tr>
<tr>
<td>Rights</td>
<td>© 2008 American Institute of Physics. This paper was published in Applied Physics Letters and is made available as an electronic reprint (preprint) with permission of American Institute of Physics. The paper can be found at the following official URL: <a href="http://dx.doi.org/10.1063/1.2970036">http://dx.doi.org/10.1063/1.2970036</a>. One print or electronic copy may be made for personal use only. Systematic or multiple reproduction, distribution to multiple locations via electronic or other means, duplication of any material in this paper for a fee or for commercial purposes, or modification of the content of the paper is prohibited and is subject to penalties under law.</td>
</tr>
</tbody>
</table>
Lu$_2$O$_3$/Al$_2$O$_3$ gate dielectrics for germanium metal-oxide-semiconductor devices

P. Darmawan,$^1$ M. Y. Chan,$^1$ T. Zhang,$^1$ Y. Setiawan,$^1$ H. L. Seng,$^2$ T. K. Chan,$^3$ T. Osipowicz,$^3$ and P. S. Lee$^{1,*(a)}$

$^1$School of Materials Science and Engineering, Nanyang Technological University, 50 Nanyang Avenue, Singapore 639798, Singapore
$^2$Institute of Materials Research and Engineering, A*STAR (Agency for Science, Technology and Research), Singapore
$^3$Research Link, Singapore 117602, Singapore

$^a$Address all correspondence to this author. E-mail: pslee@ntu.edu.sg.

(Received 27 May 2008; accepted 22 July 2008; published online 13 August 2008)

The future of semiconductor industries would depend on the continuous development of integrated circuit performance in order to meet the ever increasing demand for higher performance devices. The gate oxide thickness downscaling with conventional silicon dioxide will soon reach its limit for high-technology devices. With the decrease in thickness, silicon dioxide is not a suitable material to be used as a gate dielectric. In the past few years, breakthroughs in high performance materials have been observed, which suggest that there may be good candidates for high-k gate material.

Effect of Ge out diffusion into Lu$_2$O$_3$/Al$_2$O$_3$ high-k dielectric stack was investigated. Increasing Ge signal intensity with increasing annealing temperature was observed, which suggests that there may be excessive Ge incorporation into the high-k film. The electrical measurement shows an improvement of the $k$ value with annealing temperature, as well as an increasing trend in the leakage current density suggesting degradation in electrical performance due to Ge incorporation. Our work suggests that 8.8 at. % of Ge in the film is excessive and results in degradation of the electrical performance of the device due to the increased leakage current.

Effect of Ge out diffusion into Lu$_2$O$_3$/Al$_2$O$_3$ high-k dielectric stack was investigated. Increasing Ge signal intensity with increasing annealing temperature was observed, which suggests that there may be excessive Ge incorporation into the high-k film. The electrical measurement shows an improvement of the $k$ value with annealing temperature, as well as an increasing trend in the leakage current density suggesting degradation in electrical performance due to Ge incorporation. Our work suggests that 8.8 at. % of Ge in the film is excessive and results in degradation of the electrical performance of the device due to the increased leakage current. © 2008 American Institute of Physics. [DOI: 10.1063/1.2970036]
resolution transmission electron microscopy (HRTEM) with JEOL 2010 microscope. The electrical characteristics of the fabricated metal-insulator-semiconductor devices were measured using a precision LCR meter (HP4284A) at a high frequency of 100 kHz for capacitance-voltage measurements (C-V) and semiconductor parameter analyzer (Keithley 4200) for the current density-voltage (J-V) measurements. For the high-resolution Rutherford backscattering spectroscopy (HRBS), a beam of 500 keV He⁺ is used. The beam was incident on the sample which was mounted on a high-precision five-axis goniometer installed in a UHV chamber. The incident angle of the beam is 59.5°. The HRBS spectrum is observed at a scattering angle of 65°. The secondary ion mass spectroscopy (SIMS) measurements were obtained using a TOF SIMS IV instrument, with 1 keV Cs⁺ as sputtering beam and 25 keV ⁶⁹Ga⁺ as analysis beam and detection of negative secondary ions.

Figure 1(a) shows a cross-sectional HRTEM image of Lu₂O₃/Al₂O₃ on the Ge substrate after RTA at 600 °C. As observed from the HRTEM micrograph, the thickness of the deposited films was approximately 7–8 nm. The film appeared to be amorphous throughout and there was no distinctive layer to indicate the deposited Al₂O₃. There was a clear abrupt edge between the substrate and the thin film, suggesting an absence of unstable interfacial layer. Comparing as-deposited and 600 °C Ge spectra from the SIMS analysis shown in the inset of Fig. 2, Ge updission is evident. The above observation may be explained using the intermixing model proposed by Kamata, as illustrated in Fig. 1(b), whereby it is possible that both Al₂O₃ and Lu₂O₃ was able to mix with residual GeOₓ or out diffused elemental Ge as the case of ZrO₂ or Y₂O₃, such that the Lu₂O₃/Al₂O₃/GeOₓ/Ge stack was converted to Lu/Al-based germanate without an interfacial layer after annealing. It was shown in the HRBS spectrum in Fig. 2 that the Ge content in the high-k film increases with increasing annealing temperature. HRBS spectra fitting revealed that the introduction of annealing promoted the growth of the Lu-based germanate, partial conversion for the 300 °C sample and full conversion for the 400 and 600 °C sample; suggesting intermixing in the film stack. In addition, the HRBS spectra fitting suggest that more Ge was found nearer to the film surface with higher annealing temperature. It was calculated from the HRBS spectra that the presence of Ge content increases for approximately 4% with 600 °C annealing as compared to the as-deposited sample. This result suggests a better intermixing with possible residual GeOₓ film or outdiffused Ge with increasing temperature.

The typical C-V measurement at 100 kHz is shown in Fig. 3(a). The curves obtained were relatively well-shaped albeit some humps are present, which normally attributed to the presence of slow traps and relatively large interface trap density as indicated by the relatively stretched out curve. The inset shows SIMS data illustrating the outdiffusion of Ge throughout the Lu₂O₃ film. The dashed spectrum representing the as-deposited condition.
Observed from the C-V curves, the accumulation capacitance increased with the increasing annealing temperature. A k value of 11.7 was obtained for the sample annealed at 600 °C in N₂ ambient, without taking into account the quantum mechanical tunneling effect. This translates to a capacitance equivalent thickness (CET) of 2.42 nm for the stack. This is close to the reported value for Lu₂O₃ of about 11–12. The electrical data seems to support earlier postulation that the higher annealing temperature allows better intermixing, thereby improving the electrical performance of the MOS stack. Increasing the annealing temperature from 300, 400, and 600 °C has improved the k value from 9.9, 10.8 to 11.7, respectively. In this case, the Al₂O₃ layer seems to suggest that it is an effective passivation layer. We believed that the Al₂O₃ may have had acted as an effective oxygen reaction barrier in preventing the formation of low quality interfacial GeO₂. This is plausible since GeO₂ and Al₂O₃ has a heat of formation of 43.9 and 1675 kJ/mol, respectively. Nevertheless, further effort in reducing the CET is required as the International Technology Roadmap for Semiconductors (ITRS) (Ref. 20) outlines that for a sub-22-nm technology, an EOT of <0.5 nm is required by 2016 to sustain gate terminal control of the charge carrier in the semiconductor channel.

The general trend of the J-V characteristic measured from the rapid thermal annealed samples is shown in Fig. 3(b). The leakage current at +1 V bias for the 300, 400, and 600 °C annealed samples was 2.19×10⁻², 1.87×10⁻⁴, and 1.37×10⁻⁴ A/cm², respectively. The reduction of leakage current is likely to have been caused through better intermixing at elevated temperature along with densification and defect alleviation in the film. In addition, it is observed that the leakage current was higher at 600 °C annealed sample as compared to the 400 °C annealed sample. One possible explanation is that although intermixing is a necessary condition to stabilize the interface and the leakage current, it is not entirely governed by the amount of Ge updiffusion. An excess Ge in the high-k layer is likely to quickly result in a poor electrical performance. Subsequently, the excessive Ge updiffusion may have caused defects in the film itself, which may contribute to leakage path and thus lead to the observed increase in the leakage current for the 600 °C annealed sample. HRBS spectra revealed an increasing trend of Ge content in the film with increasing annealing temperature. For the 300, 400, and 600 °C annealed sample, the Ge content is approximated to be about 5.0, 6.8, and 8.8 at. %, respectively. In the 600 °C annealed sample, the excess out-diffused Ge content in the film may have led to the creation of more defects in the film, which provide for leakage path resulting in higher leakage current density. Although the amount of Ge content in the film that will cause the degradation in the leakage current density is not precisely determined, our result offers a reference in which at 8.8 at. % degradation in the leakage current density is likely to be observed. A more detailed experimental work is needed to determine the exact excess Ge at. % that will degrade the electrical performance. Our work suggests that 400 °C is an optimum annealing temperature in which an acceptable k value of 10.8 and low leakage current density of 1.87×10⁻⁴ A/cm² was obtained.

In summary, the effect of annealing on the Lu₂O₃/Al₂O₃/Ge stack was studied. In the study, it was found that with annealing, there was intermixing of the high-k film with possible residual GeO₂ that was present due to incomplete removal of the native oxide due to wet cleaning and/or outdiffused elemental Ge due to annealing, resulting in a Lu/Al based germanate. No interfacial layer was observed using HRTEM suggesting absence of GeO₂ based interfacial layer after annealing. HRBS spectrum revealed an increasing Ge signal intensity with increasing annealing temperature which suggests that there may be excessive Ge incorporation into the high-k film, which may degrade the electrical performance. This is reflected in the electrical measurement, although the k value is improved with annealing temperature, there is an increasing trend in the leakage current density suggesting degradation in electrical performance due to Ge incorporation. Our work suggests that 8.8 at. % of Ge in the film is excessive and result in degradation of the electrical performance of the device due to the increased leakage current.

20www.irts.net.