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<td>2006</td>
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LaAlO$_3$ Nanocrystals Embedded in Amorphous Lu$_2$O$_3$ High-$k$ Gate Dielectric for Floating Gate Memory Application

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A novel method to fabricate the memory structure of LaAlO$_3$ nanocrystals embedded in amorphous Lu$_2$O$_3$ high-$k$ dielectric by the pulsed laser deposition method was successfully developed. The average mean size and aerial density of the LaAlO$_3$ nanocrystals are estimated to be about 6 nm and 1.1 $\times$ 10$^{12}$ cm$^{-2}$, respectively. Superior performances in terms of a large memory window, long data retention, and robust endurance were observed.

Manuscript submitted December 7, 2005; revised manuscript received March 6, 2006. Available electronically April 7, 2006.

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LaAlO$_3$ Nanocrystals Embedded in Amorphous Lu$_2$O$_3$ High-$k$ Gate Dielectric for Floating Gate Memory Application

A significant attention has been shifted to semiconductor nanoparticles embedded in the silicon dioxide (SiO$_2$) of a metal-insulator-semiconductor (MOS) device for future high speed and low power consuming logic and memory devices in the recent years. Conventional floating gate (FG) devices have their limitations; the most prominent one is the limited potential for continued scaling of the device structure. This is due to the stringent requirement placed on the tunnel oxide layer. There is often a trade-off between speed and reliability in a conventional flash gate to allow an acceptable charge transfer rate to and from the floating gate, with satisfactory charge retention. Therefore, in order to overcome the scaling limits of FG transfer rate to and from the floating gate, with satisfactory charge reliability in a conventional flash gate to allow an acceptable charge device structure. This is due to the stringent requirement placed on the tunnel oxide layer. There is often a trade-off between speed and reliability in a conventional flash gate to allow an acceptable charge transfer rate to and from the floating gate, with satisfactory charge retention. Therefore, in order to overcome the scaling limits of FG devices, floating gates incorporating isolated nanocrystals have been introduced. The use of nanocrystal nonvolatile memory devices would allow thinner injection oxides, thereby allowing better endurance, lower operating voltages, and faster write/erase speeds. Moreover, the presence of the isolated dots reduces the problems of charge loss encountered in conventional flash memories. The use of high-$k$ dielectric in place of the conventional SiO$_2$-based dielectric means that programming efficiency, and data retention, in the nanocrystal nonvolatile memories can be significantly improved. Presently, work on the integration of high-$k$ dielectric materials with nanodots is limited.

Lanthanide oxides are potential high-$k$ alternative candidates for gate insulators because of their desirable characteristics such as large bandgap, high relative dielectric constant, and low leakage current. Some of the lanthanide oxides show good properties without the preformed interfacial layer, and are regarded as promising candidates for next generation high-$k$ dielectrics. Among the lanthanide oxides, Lu$_2$O$_3$ has a moderately high dielectric constant around 12. and is predicted to be thermodynamically stable on Si. LaAlO$_3$ is stable in contact with silicon under standard metal oxide semiconductor (MOS) device processing conditions of 1026°C for 20 s. This makes LaAlO$_3$ a promising candidate material to be integrated in MOS devices.

An advantage of the pulsed laser deposition (PLD) method is the possibility for stoichiometric transfer of the ablated material from the target to the film. In this letter, we report a method to produce LaAlO$_3$ nanocrystals in amorphous Lu$_2$O$_3$ high-$k$ dielectric matrices using a variation of the pulsed-laser deposition method with a rotating target. This result opens up possibilities for new advances and applications in memory devices.

Experimental

Samples were prepared using the PLD method. Briefly, a KrF-pulsed laser beam of 248 nm wavelength and the energy density is 1.5 J/cm$^2$ with frequency of 5 Hz was used to ablate the target in an ultrahigh vacuum chamber. The targets to be laser ablated consisting of one piece of high-purity (99.999%) Lu$_2$O$_3$ round target (diameter $D = 25$ mm) and a piece of small, square, single-crystal LaAlO$_3$ target (of about 3 mm in length) were first prepared. The LaAlO$_3$ target was glued onto the surface of the Lu$_2$O$_3$ target making a two-material assembly with only physical, but not chemical, contact between them. During the PLD process, for the tunneling oxide layer deposition, we kept the target stationary while allowing the laser to ablate the Lu$_2$O$_3$. Then, to form the nanocrystals embedded in the Lu$_2$O$_3$ matrix, the LaAlO$_3$-Lu$_2$O$_3$ target assembly was set to spin slowly by its central axis and the laser beam vaporized the two component materials alternately. Finally, the laser beam was focused onto Lu$_2$O$_3$ for the control oxide layer deposition. The ablated materials were deposited on p-type Si(100) wafer substrates which were first cleaned using SC1, SC2 mixtures, and then dipped in a 1% HF solution to remove the native oxide. The deposition and growth of the films on the substrate were carried out in a high vacuum system with a background pressure of about 5 $\times$ 10$^{-7}$ Torr, with the target rotating at about 30 rounds/min and the substrate at room temperature. The distance between the target and substrate was 11 cm. After deposition, the thin film was subjected to a postdeposition annealing (PDA) at 400°C for 60 s in a nitrogen ambient. The film structure was examined using high-resolution transmission electron microscope (HRTEM) with a JEOL 2010 microscope. Top electrodes of Au with a dimension of 0.5 $\times$ 0.5 mm were evaporated for electrical measurement. The electrical characteristics of the fabricated metal-insulator-semiconductor (MIS) devices, capacitance-voltage (C-V), and capacitance-time (C-t) were measured using a precision LCR meter (HP 4284A). The OR-X 420 programmable function generator was connected to the HP 4284A through a switch and the C-V measurements were performed after the stress of the periodic pulses to identify the relationship of threshold voltage shift (memory window) vs pulse cycles.

Results and Discussion

Figure 1a shows the planar TEM image of the synthesized LaAlO$_3$ nanocrystals, with its corresponding electron diffraction pattern on the top left corner. The average diameters of the LaAlO$_3$ nanocrystals are approximately 6 nm, and the area density of the nanocrystals is estimated to be about 1.1 $\times$ 10$^{12}$ cm$^{-2}$. Figure 1b shows a cross-sectional HRTEM image of the Lu$_2$O$_3$ thin film on the Si substrate. The LaAlO$_3$ nanocrystals embedded in Lu$_2$O$_3$ can be clearly seen between the tunnel oxide and the control oxide, and the shape of the LaAlO$_3$ nanocrystals is almost spherical. In this sample with LaAlO$_3$ nanocrystals, Lu$_2$O$_3$ was used as the control and tunneling oxide layer in the trilayer memory structure of Lu$_2$O$_3$/LaAlO$_3$/Lu$_2$O$_3$. The total physical thickness, the thicknesses of the control and the tunneling oxide layer are about 15, 4, and 5 nm, respectively. It can also be confirmed that the Lu$_2$O$_3$ thin films still remained amorphous after PDA at 400°C, and there is no observable interfacial layer between Si substrate and Lu$_2$O$_3$ film. By controlling the exposed area ratio of Lu$_2$O$_3$:LaAlO$_3$ under the laser ablation along with the target rotation speed, the size and densities of nanocrystals, the distribution of these nanocrystals can also be controlled.

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Figure 2 shows the typical high-frequency (1 MHz) capacitance-voltage hysteresis of two MIS capacitors with and without LaAlO$_3$ nanocrystals after the bidirectional bias swept between 6 V and −6 V. It can be seen that under a low operating voltage, 6 V, a significant threshold voltage shift (~1.5 V) is observed from C-V hysteresis of the sample with LaAlO$_3$ nanocrystals. In contrast, the controlled sample without LaAlO$_3$ nanocrystals shows no obvious flatband voltage shift, suggesting that the large memory effect observed in the sample with LaAlO$_3$ nanocrystals is caused by the charges stored in the LaAlO$_3$ nanocrystals. Generally, the hysteresis may be introduced by the mixed effects of injected charges stored in the nanocrystals, essential trap charges existing in the oxide or interface states. Since the processes for fabricating the two samples are the same, except for the LaAlO$_3$ nanocrystals, the hysteresis effect produced by the essential trap charges and interfacial states should be the same for the two samples, and can, therefore, be ruled out. The injected charges stored in nanocrystals and/or at the interface of the nanocrystals$^{17}$ is a more plausible explanation for the large hysteresis of the sample with LaAlO$_3$ nanocrystals.

The memory data retention characteristics at room temperature and 125°C for this nanocrystal floating gate memory capacitor were also studied as shown in Fig. 3. The memory capacitor is first charged for 10 s at a bias voltage of 10 V. Then, the decayed capacitance measurement was carried out under a ~3 V bias voltage. It can be seen that after 700 s of stress, the decayed capacitance for the memory capacitor is only about 4% at room temperature and 17% at 125°C, suggesting a good charge retention characteristics.

Figure 1. (a) Planar TEM image of LaAlO$_3$ nanocrystals embedded in amorphous Lu$_2$O$_3$ dielectric matrix. Inset: we show the electron diffraction pattern for LaAlO$_3$ nanocrystals. (b) Cross-sectional TEM image of LaAlO$_3$ nanocrystals embedded in amorphous Lu$_2$O$_3$ dielectric matrix.

Figure 2. High-frequency (1 MHz) capacitance-voltage hysteresis of sample with LaAlO$_3$ nanocrystals embedded in amorphous Lu$_2$O$_3$ dielectric and reference sample without LaAlO$_3$ nanocrystals.

Figure 3. Normalized capacitance decay characteristics at room temperature (solid line) and 125°C (dash line) for LaAlO$_3$ nanocrystals embedded in amorphous Lu$_2$O$_3$ dielectric memory device.
our experiments, the LaAlO$_3$ nanocrystals have a dimension of ~6 nm, therefore, the coulomb’s blockade effect and the quantum confinement effect might be significant for the write/erase process. According to the work of Kim et al., the storage charges in the localized nanocrystals exhibit a long-term retention property.\(^{18}\) As shown in our figures, isolation of LaAlO$_3$ nanocrystals has been embedded at the middle of the dielectric matrix and results in a good memory storage effect.

Figure 4 shows the endurance characteristics obtained after cycling the structure between 6 V (write-electron injection to the nanocrystals) and −7 V (erase-electron ejection from the nanocrystals). The cycling was interrupted at specific times and CV measurements were recorded. Even though $10^7$ pulse cycles were performed, it retains a large memory window without catastrophic decline as the previous reports on nanocrystal memory devices.\(^{19,20}\)

Many methods have been explored by various groups in order to fabricate the nanocrystals embedded in the high-$k$ matrix.\(^{21-26}\) This work has managed to fabricate high density of nanocrystals embedded in high-$k$ matrix using in situ pulsed laser deposition followed by postdeposition annealing. In comparison, our method is much more simplified and straightforward, attaining a compatible memory window. Moreover, we offer the flexibility for controlling the size and densities of the nanocrystals by controlling the exposed area ratio of Lu$_2$O$_3$:LaAlO$_3$ under laser ablation and the target rotation speed. Further investigations are in progress in this aspect.

**Conclusions**

In summary, we have successfully developed a method to fabricate the memory structure of LaAlO$_3$ nanocrystals embedded in amorphous Lu$_2$O$_3$ high-$k$ dielectric using pulsed laser deposition. The mean size and arial density of the LaAlO$_3$ nanocrystals are estimated to be about 6 nm and $1.1 \times 10^{12}$ cm$^{-2}$, respectively. Good performances in terms of a large memory window, long data retention, and robust endurance were observed.

**Acknowledgments**

P.D. and Y.S. are grateful for the research scholarships provided by Nanyang Technological University. This work is financed in part by A*STAR SERC grant no. 042 114 0050.

Nanyang Technological University assisted in meeting the publication costs of this article.

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