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Demonstration of Schottky Barrier NMOS Transistors With Erbium Silicided Source/Drain and Silicon Nanowire Channel

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***Abstract*—We have fabricated silicon nanowire N-MOSFETs using erbium disilicide ($ErSi_{2-x}$) in a Schottky source/drain back-gated architecture. Although the subthreshold swing ($\sim$180 mV/dec) and drain-induced barrier lowering ($\sim$500 mV/V) are high due thick BOX as gate oxide, the fabricated Schottky transistors show acceptable drive current $\sim$900 $\mu A/\mu m$ and high I_{on}/I_{off} ratio ($\sim 10^5$). This is attributed to the improved carrier injection as a result of low Schottky barrier height (Φ_b) of $ErSi_{2-x}/n-Si$($\sim$0.3 eV) and the nanometer-sized ($\sim$8 nm) Schottky junction. The carrier transport is found to be dominated by the metal–semiconductor interface instead of the channel body speculated from the channel length independent behavior of the devices. Furthermore, the transistors exhibit ambipolar characteristics, which are modeled using thermionic/thermionic-field emission for positive and thermionic-field emission for negative gate biases.**

***Index Terms*—Erbium silicide, Schottky source/drain (S/D) MOSFET (SSDMOS), silicon nanowire (SiNW).**

I. Introduction

MOSFETs are reaching the scaling limit as confined by the physical laws of nature including higher subthreshold leakage current due to reduced threshold voltage, etc. [1]. An alternative MOSFET design is the Schottky source/drain (S/D) MOSFET (SSDMOS) which has enhanced scaling properties (i.e., reduced parasitic resistances) [2]. Erbium disilicide ($ErSi_{2-x}$) has several advantages including low formation temperatures ($\sim$350 °C) and low Schottky barrier height (Φ_{bn}) to $n-Si \sim 0.27-0.36$ eV [3]. FinFETs and gate-all-around (GAA) silicon nanowire (SiNW) transistors gain performance advantages by enhancing transistor gate-to-channel coupling, thus achieving reduced short channel effect (SCE) and improved drive currents [4], [5]. Using "top-down" CMOS processes, SSDMOSs incorporating $YbSi_{1.8}$ and various mid-gap silicides ($CoSi_2$, NiSi) for the S/D metal have been demonstrated [6]–[9].

In this letter, we utilized a "top-down" method to fabricate $ErSi_{2-x}$ SSDMOS using SiNW as the channel with much smaller dimensions ($\sim$8 nm width) than the previously reported devices [3]. The devices are evaluated in back-gated configuration. Despite the thick BOX as gate dielectric, the performance of the transistors is good.

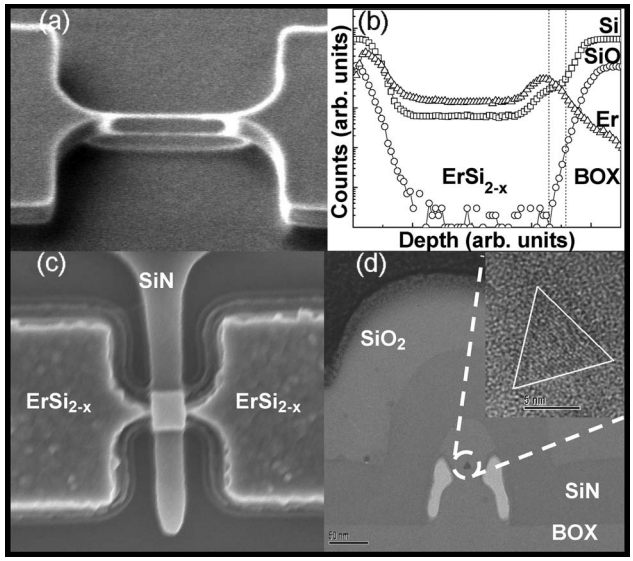

Fig. 1. (a) Tilted view SEM of two SiNWs immediately after the dry oxidation without gate oxide and silicon nitride dummy gate. The L_{ch} is approximately 500 nm. (b) SIMS depth profile of the S/D pad. (c) SEM micrograph of a completed $ErSi_{2-x}$ N-SSDNWMOS with $L_{ch} = 300$ nm. (d) Cross-sectional TEM of the SiNW channel showing a 8-nm-wide nanowire.

II. Device Fabrication

The device fabrication steps up to SiNW formation, shown in Fig. 1(a) as a SEM image, have been described in [5]. In

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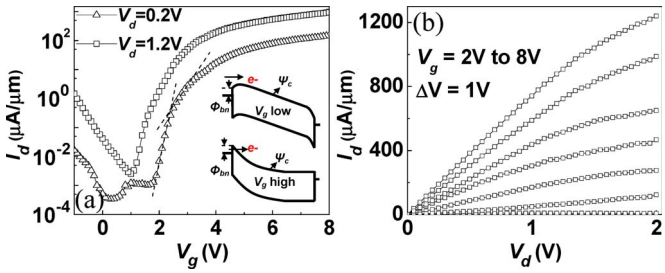

Fig. 2. (a) I_d–V_g and (b) I_d–V_d characteristics of an $ErSi_{2-x}$ N-SSDNWMOS with $L_{\rm ch} = 500$ nm. The dashed lines in (a) clearly shows the sequential SS. The inset of (a) shows the band diagram for both low and high positive V_gs. The current was normalized by using the width of the SiNW channel.

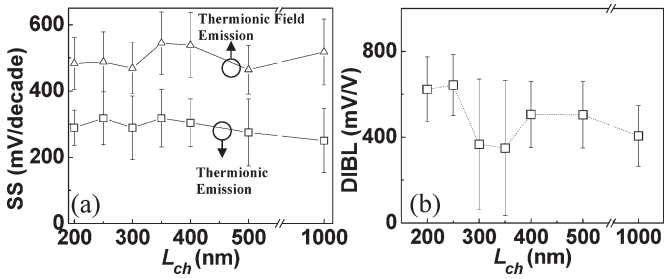

Fig. 3. Extracted transistor characteristics from I_d–V_g of the $ErSi_{2-x}$ N-SSDNWMOSs. (a) SS extracted from thermionic emission region (-□-) and SS extracted from thermionic-field emission region (-Δ-) against $L_{\rm ch}$ measured at $V_d = 0.2$ V and (b) DIBL against $L_{\rm ch}$.

addition, boron with 60-keV energy, at a dose of 4×10^{15} cm^{-2} was implanted on the Si wafer backside, followed by furnace activation for 30 min at 950 °C.

In this letter, the top nanowire was removed by a plasma dry etch process. It was followed by the formation of a silicon nitride dummy gate which serves to isolate the source and drain from the channel during the subsequent silicidation process. Erbium and capping layers of TiN/Ti were sequentially sputter deposited using a physical vapor deposition system followed by a rapid thermal annealing process at 450 °C for 60 s. The TiN/Ti and unreacted Er were removed by wet etching using a sulfuric peroxide mixture ($H_2SO_4 : H_2O_2 \sim 1 : 1$) for 5 min. The silicide composition and thickness were confirmed using secondary ion mass spectrometry (SIMS) analysis on the S/D pads, as shown in Fig. 1(b). The entire active Si pads were fully consumed as indicated by the SIMS profile, leading to the formation of $ErSi_{2-x}$/SiNW Schottky barrier at the two ends of the SiNW channel. The final $ErSi_{2-x}$ N-SSDMOS using SiNW as the channel body (N-SSDNWMOS) is shown in Fig. 1(c). A cross-sectional TEM micrograph of the SiNW channel shows that the nanowire is triangular in shape with a base of ∼8 nm, as shown in Fig. 1(d).

III. Results and Discussion

Fig. 2(a) shows the I_d–V_g characteristics of an $ErSi_{2-x}$ back-gated N-SSDNWMOS with a channel length $(L_{\rm ch}) = 500$ nm. The drive current is 900 μA/μm (measured at $V_g = V_t + 5$ V, where $V_t = 3.4$ V, $V_d = 1.2$ V) while the $I_{\rm on}/I_{\rm off}$ ratio is ∼10^5. Note that the gate oxide capacitance using a 145-nm-thick gate dielectric (i.e., the BOX layer for the back-gated configuration) requires $V_g \sim 4.5$ V to induce the same charge as a 6-nm-thick gate dielectric biased at $V_g = 1.2$ V [10]. The thick BOX layer, coupled with the voltage drop across the gate electrode, results in an increased gate voltage required to induce the same charge when compared with a conventional top-gated MOSFET.

The large drive current observed is a result of the superior electrostatics of a thin bodied SiNW structure [5], [20]–[22] and Schottky barrier thinning in a scaled nanosized metal semiconductor junction [13], [14]. The drain-induced barrier lowering (DIBL) and subthreshold swing (SS) are large, at ∼500 mV/V and ∼180mV/dec, respectively, and is a result of the thick gate dielectric [10]–[12]. However, the drain current is extremely responsive to V_g when compared with other reported back-gated devices [11], [12]. This responsiveness is attributed in part to the compensating effect of the fully depleted nanometer-sized channel [5], as well as improved carrier injection as silicon channel thickness is reduced [13].

The I_d–V_g characteristics exhibit a two-slope SS (∼180 and ∼450 mV/dec) with increasingly positive V_g, indicating thermionic emission of electrons from the source, followed by a thermionic-field emission [14]. However, with increasingly negative V_g, there is a single SS (∼660 mV/dec), indicating thermionic-field emission of holes from the drain without the prior occurrence of thermionic emission. This is due to the large Schottky barrier height $(\Phi_{\rm bp})$ of $ErSi_{2-x}$ to p-Si ∼0.76–0.85 eV [3].

The current conduction is illustrated in the band diagram [see inset of Fig. 2(a)]. At low V_g values, thermionic current dominates, and only carriers with energy greater than $\Phi_{\rm bn} + \Psi_c$ contribute to the current. Ψ_c is the channel conduction band potential which is modulated by V_g. In this V_g region, the SSDMOS behaves like a conventional MOSFET with SS ≈ $\ln 10$ (kT/q).

At higher V_g values, thermionic-field current dominates the current flow as the Schottky barrier is thinned. The SS of a thin body SSDMOS device in this region can be expressed as SS ≈ $\ln 10$ (kT/q)$(1 - \exp(-d/(\varepsilon_{\rm si} t_{\rm si} t_{\rm ox}/\varepsilon_{\rm ox})^{1/2}))^{-1}$ where d is the thickness of the Schottky barrier beyond which tunneling can be neglected, $\varepsilon_{\rm si}$ and $\varepsilon_{\rm ox}$ are the Si and SiO_2 dielectric constants, respectively, and $t_{\rm si}$ and $t_{\rm ox}$ are the Si and SiO_2 thicknesses, respectively [13]. Thus, SS in the thermionic-field region will be larger than in the thermionic region.

Fig. 2(b) shows the I_d–V_d characteristics of the same $ErSi_{2-x}$ N-SSDNWMOS. The characteristics show that the device does not exhibit any upwardly sloping sublinear curves for $V_g \leq 3$ V, which is typical of a Schottky barrier transistor and is the signature of a nonzero $\Phi_{\rm bn}$ at the drain [15]. The absence of the sublinear slope of the $ErSi_{2-x}$ N-SSDNWMOS, as compared to reported SSDMOS [3], is likely to be due to the improved carrier injection to the nanometer-sized SiNW channel.

Fig. 3 examines the $ErSi_{2-x}$ N-SSDNWMOSs' $L_{\rm ch}$ dependence on SS and DIBL. In MOSFETs, a reduction in $L_{\rm ch}$ causes a decrease in source barrier height. This causes the injection of extra carriers, thereby increasing the OFF-state leakage current leading to increased SS and DIBL which occurs even at long $L_{\rm ch}$ [16]. Fig. 3(a) shows the $ErSi_{2-x}$ N-SSDNWMOSs

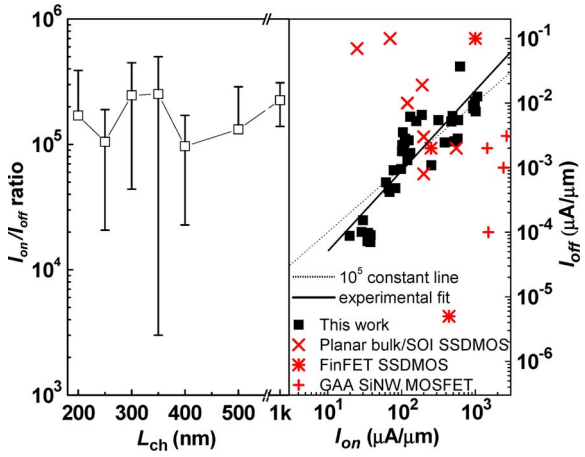

Fig. 4. (a) $I_{\rm on}/I_{\rm off}$ versus $L_{\rm ch}$, and (b) $I_{\rm on}/I_{\rm off}$ characteristics under $V_d = 0.2$ V and 1.2 V bias of the $ErSi_{2-x}$ N-SSDNWMOSs with various $L_{\rm ch}$. For $V_d = 0.2$ V: $I_{\rm off}$ measured at $V_g = V_t - 1.5$ V, $I_{\rm on}$ measured at $V_g = V_t + 3.5$ V. For $V_d = 1.2$ V: $I_{\rm off}$ measured at $V_g = V_t - 2$ V, $I_{\rm on}$ measured at $V_g = V_t + 3$ V. "X" indicates planar bulk/SOI SSDMOS [3]. "$*$" indicates FinFET SSDMOS [6], [8], [19]. "+" indicates GAA SiNW doped S/D MOSFET [5], [20]–[22].

variation of SSs with $L_{\rm ch}$ in the thermionc emission and thermionic-field emission region, respectively. Both SSs are almost constant at ∼300 and ∼500 mV/dec, respectively, for all $L_{\rm ch}$s (200 to 1000 nm). The constant SSs extracted from Fig. 3(a) shows that the source Schottky barrier is relatively insensitive to the drain electric field in both the thermionic and thermionic-field emission regions for the $L_{\rm ch}$ measured. Instead, it has been shown that device geometry, i.e., silicon body and gate oxide thickness, plays a greater part in the SS [13], [17]. Fig. 3(b) shows that the variation of DIBL with $L_{\rm ch}$ is almost constant at ∼500mV/V and is consistent with the SSs behavior. It has experimentally been shown that SCE has a significant impact only at $L_{\rm ch}$s ≤ 90 nm [8].

Fig. 4(a) shows the $I_{\rm on}/I_{\rm off}$ ratio against the $L_{\rm ch}$ for the $ErSi_{2-x}$ N-SSDNWMOSs indicating an average value of $\sim 10^5$ for all $L_{\rm ch}$s. The absolute values of $I_{\rm on}$ and $I_{\rm off}$ are also independent of $L_{\rm ch}$. In other words, the variations in the $I_{\rm on}/I_{\rm off}$ ratio observed is predominantly due to the slight differences in $\Phi_{\rm bn}$ and not due to the differences in $L_{\rm ch}$, consistent with the almost constant SS values in Fig. 3(a) and the reported values on "bottom up" NiSi SiNW transistors [18]. Fig. 4(b) shows the $I_{\rm on}/I_{\rm off}$ characteristics of various $ErSi_{2-x}$ N-SSDNWMOSs. The experimental fit shows a close approximation to the 10^5 constant line which is superior in comparison to most planar bulk/SOI-based SSDMOSs [3]. The $I_{\rm on}/I_{\rm off}$ characteristics of various devices found in the literature are also shown in Fig. 4(b) [3], [5], [6], [8], [19]–[22].

IV. Conclusion

We have demonstrated N-SSDMOSs utilizing Si nanowire as the channel body and $ErSi_{2-x}$ as the S/D metal silicide. The devices exhibited a sequential thermionic/thermionic-field characteristic for a positive gate bias. The carrier transport is mainly determined by the metal–semiconductor interface instead of the channel body. The device showed good $I_{\rm on}/I_{\rm off}$ characteristics because of the low $\Phi_{\rm bn}$ of $ErSi_{2-x}/n$-Si and the improved carrier injection to the nanometer-sized SiNW channel.

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References

[1] M. Ieong, B. Doris, J. Kedzierski, K. Rim, and M. Yang, "Silicon device scaling to the sub-10-nm regime," *Science*, vol. 306, no. 5704, pp. 2057–2060, Dec. 2004.

[2] J. Kedzierski, P. Xuan, E. H. Anderson, J. Bokor, T.-J. King, and C. Hu, "Complementary silicide source/drain thin-body MOSFETs for the 20 nm gate length regime," in *IEDM Tech. Dig.*, 2000, pp. 57–60.

[3] J. M. Larson and J. P. Snyder, "Overview and status of metal S/D Schottky-barrier MOSFET technology," *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 1048–1058, May 2006.

[4] B. Yu, L. Chang, S. Ahmed, H. Wang, S. Bell, C. Y. Yang, C. Tabery, C. Ho, Q. Xiang, T. J. King, J. Bokor, C. Hu, M. R. Lin, and D. Kyser, "FinFET scaling to 10 nm gate length," in *IEDM Tech. Dig.*, Dec. 2002, pp. 62–63.

[5] N. Singh, A. Agarwal, L. K. Bera, T. Y. Liow, R. Yang, S. C. Rustagi, C. H. Tung, R. Kumar, G. Q. Lo, N. Balasubramaniam, and D. L. Kwong, "High-performance fully depleted silicon nanowire (Diameter ≤ 5 nm) gate-all-around CMOS devices," *IEEE Electron Device Lett.*, vol. 27, no. 5, pp. 383–386, May 2006.

[6] R. T. P. Lee, A. E. J. Lim, K. M. Tan, T. Y. Liow, G. Q. Lo, G. S. Samudra, D. Z. Chi, and Y. C. Yeo, "N-channel FinFETs with 25-nm gate length and Schottky-barrier source and drain featuring Ytterbium Silicide," *IEEE Electron Device Lett.*, vol. 28, no. 2, pp. 164–167, Feb. 2007.

[7] A. Kinoshita, Y. Tsuchiya, A. Yagishita, K. Uchida, and J. Koga, "Solution for high-performance Schottky-source/drain MOSFETs: Schottky barrier height engineering with dopant segregation technique," in *VLSI Symp. Tech. Dig.*, Jun. 2004, pp. 168–169.

[8] A. Kaneko, A. Yagishita, K. Kubota, M. Omura, K. Matsuo, I. Mizushima, K. Okano, H. Kawasaki, T. Izumida, T. Kanemura, N. Aoki, A. Kinoshita, J. Koga, S. Inaba, K. Ishimaru, Y. Toyoshima, H. Ishiuchi, K. Suguro, K. Eguchi, and Y. Tsunashima, "High-performance FinFET with dopant-segregated Schottky source/drain," in *IEDM Tech. Dig.*, Dec. 2006, pp. 1–4.

[9] C. Ko, H. Chen, T. Wang, T. Kuan, J. Hsu, C. Huang, C. Ge, L. Lai, and W. Lee, "NiSi Schottky barrier process-strained Si (SB-PSS) CMOS technology for high performance applications," in *VLSI Symp. Tech. Dig.*, 2006, pp. 80–81.

[10] O. Wunnicke, "Gate capacitance of back-gated nanowire field-effect transistors," *Appl. Phys. Lett.*, vol. 89, no. 8, p. 083 102, Aug. 2006.

[11] S. M. Koo, M. D. Edelstein, Q. Li, C. A. Richter, and E. M. Vogel, "Silicon nanowires as enhancement-mode Schottky barrier field-effect transistors," *Nanotechnology*, vol. 16, no. 9, pp. 1482–1485, Sep. 2005.

[12] Y. Cui, Z. Zhong, D. Wang, W. U. Wang, and C. M. Lieber, "High performance silicon nanowire field effect transistors," *Nano Lett.*, vol. 3, no. 2, pp. 149–152, 2003.

[13] M. Zhang, J. Knoch, J. Appenzeller, and S. Mantl, "Improved carrier injection in ultrathin-body SOI Schottky-barrier MOSFETs," *IEEE Electron Device Lett.*, vol. 28, no. 3, pp. 223–225, Mar. 2007.

[14] J. Knoch and J. Appenzeller, "Impact of the channel thickness on the performance of Schottky barrier metal–oxide–semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 81, no. 16, pp. 3082–3084, Oct. 2002.

[15] B. Winstead and U. Ravaioli, "Simulation of Schottky barrier MOSFETs with a coupled quantum injection/Monte Carlo technique," *IEEE Trans. Electron Devices*, vol. 47, no. 6, pp. 1241–1246, Jun. 2000.

[16] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley, 1981.

[17] W. Saitoh, A. Itoh, S. Yamagami, and M. Asada, "Analysis of short-channel Schottky source/drain metal–oxide–semiconductor field-effect transistor on silicon-on-insulator substrate and demonstration of sub-50-nm n-type devices with metal gate," *Jpn. J. Appl. Phys.*, vol. 38, no. 11, pp. 6226–6231, Nov. 1999.

[18] W. M. Weber, L. Geelhaar, A. P. Graham, E. Unger, G. S. Duesberg, M. Liebau, W. Pamler, C. Cheze, H. Riechert, P. Lugli, and F. Kreupl, "Silicon-nanowire transistors with intruded nickel-silicide contacts," *Nano Lett.*, vol. 6, no. 12, pp. 2660–2666, Sep. 2006.

[19] C. P. Lin and B. Y. Tsui, "Characteristics of modified-Schottky-barrier (MSB) FinFETs," in *Proc. VLSI-TSA*, Apr. 2005, pp. 118–119.

[20] S. D. Suk, S. Y. Lee, S. M. Kim, E. J. Yoon, M. S. Kim, M. Li, C. W. Oh, K. H. Yeo, S. H. Kim, D. S. Shin, K. H. Lee, H. S. Park, J. N. Han, C. J. Park, J. B. Park, D. W. Kim, D. Park, and B. I. Ryu, "High performance 5 nm radius twin silicon nanowire MOSFET (TSNWFET): Fabrication on bulk Si wafer, characteristics, and reliability," in *IEDM Tech. Dig.*, Dec. 2006, pp. 717–720.

[21] K. H. Yeo, S. D. Suk, M. Li, Y. Y. Yeoh, K. H. Cho, K. H. Hong, S. Yun, M. S. Lee, N. Cho, K. Lee, D. Hwang, B. Park, D. W. Kim, D. Park, and B. I. Ryu, "Gate-all-around (GAA) twin silicon nanowire MOSFET (TSNWFET) with 15 nm length gate and 4 nm radius nanowires," in *IEDM Tech. Dig.*, Dec. 2006, pp. 1–4.

[22] N. Singh, F. Y. Lim, W. W. Fang, S. C. Rustagi, L. K. Bera, A. Agarwal, C. H. Tung, K. M. Hoe, S. R. Omampuliyur, D. Tripathi, A. O. Adeyeye, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, "Ultra-narrow silicon nanowire gate-all-around CMOS devices: Impact of diameter, channel-orientation and low temperature on device performance," in *IEDM Tech. Dig.*, Dec. 2006, pp. 1–4.