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Nickel-Silicided Schottky Junction CMOS Transistors With Gate-All-Around Nanowire Channels

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***Abstract*—We demonstrate high-performance Schottky CMOS transistors with NiSi source/drain and gate-all-around (GAA) silicon nanowire (∼5 nm) channels. The transistors exhibit good $I_{\rm on}/I_{\rm off}$ characteristics, along with fully controlled short-channel effects revealed by low drain-induced barrier lowering (∼10 mV/V) and near-ideal subthreshold swing (∼60 mV/dec). Although the N-MOSFET required dopant segregation to suppress the ambipolar behavior, excellent P-MOSFET characteristics could be achieved without the use of barrier modification techniques. We attribute this to the Schottky barrier thinning in a nanosized metal–semiconductor junction and superior gate electrostatic control in a GAA nanowire architecture.**

***Index Terms*—Gate-all-around (GAA) MOSFET, Schottky source/drain, silicon nanowire (SiNW).**

I. Introduction

THE CONTINUED scaling of source/drain (S/D) junction depth in conventional MOSFETs results in several limiting factors, including increasing sheet resistance $R_{\rm sh}$ beyond acceptable values, and limitations in doping/activation techniques to achieve sharp lateral doping profiles [1], [2]. A Schottky barrier MOSFET (SBMOS) architecture, in which the metallic S/D regions are in direct contact with the transistor channel, can essentially eliminate the S/D parasitic resistance and provide abrupt junction interfaces [3]–[11]. NiSi has emerged as the silicide of choice to be incorporated to future conventional MOSFET devices because of its low resistivity and high scalability [12]. "Top-down" nanowire transistors [13], due to enhanced drive current and better controllability of the channel potential, when integrated with an SBMOS, have recently been proposed as an ideal future transistor architecture [14].

In this letter, high-performance gate-all-around (GAA) complementary SBMOSs with NiSi S/D and silicon nanowire channel (SBNWFET) are fabricated and characterized. The SBNWFETs exhibited excellent transistor characteristics in terms of $I_{\rm on}/I_{\rm off}$, subthreshold swing (SS), and drain-induced barrier lowering (DIBL). In particular, the P-SBNWFET transistor characteristics were achieved without the use of any barrier modification techniques.

II. Device Fabrication

Two-hundred-millimeter p-type (100) SOI wafers with a resistivity of 5–10 $\Omega \cdot$ cm and a top silicon thickness of 120 nm on a 145-nm buried oxide (BOX) layer were used as the starting substrates. Some of the SOI wafers were implanted with P with a dose of 2×10^{11} cm^{-2} at 50 keV to convert the top silicon to N-type to fabricate P-SBNWFET devices. Active areas of thin fins connected to 200 μm $\times$ 200 μm S/D pads were initially patterned using KrF lithography with an alternating phase-shift mask. The unwanted Si was etched to the BOX layer followed by dry oxidation at 875 °C for 4.5 h, resulting in a twin-silicon nanowire (twin-SiNW) configuration—one at the top and the other at the bottom of the oxidized fin—as shown in the inset of Fig. 1(a). A poly-Si gate stack was defined by patterning a 9-nm SiO_2/130-nm α-Si (doped with P with a dose of 5.5×10^{15} cm^{-2} at 40 keV for NMOS and with BF_2 with a dose of 4×10^{15} cm^{-2} at 35 keV for PMOS). It was followed by 35-nm-wide SiO_2/SiN spacer formation. Fig. 1(a) shows the tilted-view SEM image of the transistor after spacer formation. A Ni film was deposited, and silicidation was done by rapid thermal annealing at 400 °C/60 s. The unreacted Ni was etched by immersing in a sulfuric peroxide mixture ($H_2SO_4 : H_2O_2 \sim 4 : 1$) for 5 min. SIMS depth profiling analysis indicates that the entire Si layer on the S/D was fully consumed to form NiSi. Fig. 1(b) shows the GAA NiSi SSDNWMOS after Ni-silicidation. For some of the NiSi N-SSDNWMOS wafers, a low-energy As implant (4×10^{14} cm^{-2}/10 keV) was conducted without activation after spacer formation and prior to silicidation to introduce dopant segregation. Fig. 1(c) shows a cross-sectional TEM (XTEM) micrograph of a twin-SiNW device with wire sizes of approximately 5 nm (bottom) and

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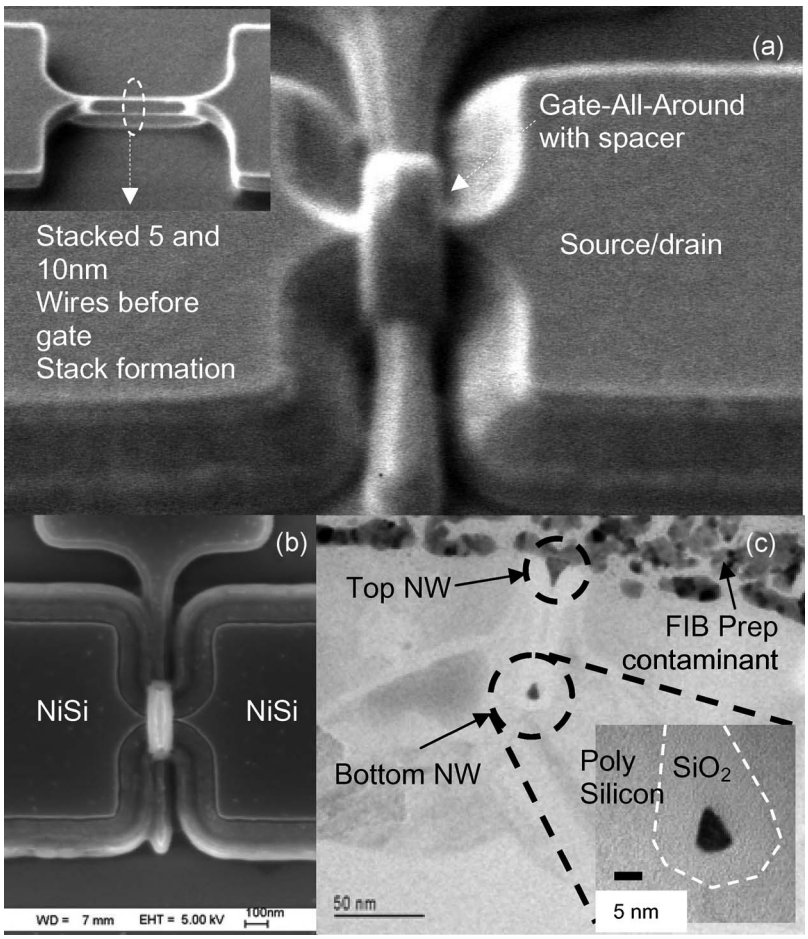

Fig. 1. (a) Tilted-view SEM of a GAA NiSi SBNWFET with $L_g = 120$ nm before silicidation. The inset shows the tilted-view SEM of a twin-SiNW channel device after oxidation (top, 8 nm; bottom, 5 nm). (b) Top-view SEM of a device with $L_g = 105$ nm after Ni-silicidation. (c) XTEM of the SiNW device in (b), which shows the stacked twin SiNWs. The inset shows a high-magnification XTEM micrograph of the bottom SiNW.

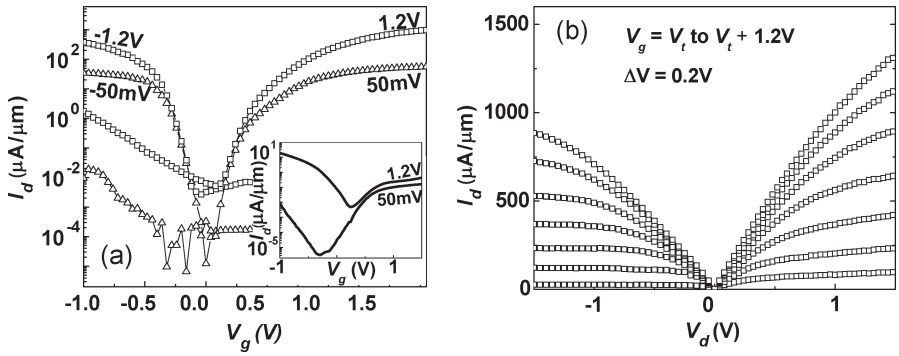

Fig. 2. (a) I_d-V_g and (b) I_d-V_d of a GAA NiSi complementary SBNWFET with $L_g = 90$ nm. The inset of (a) shows the I_d-V_g of a GAA NiSi N-SBNWFET without S/D implantation.

8 nm (top). The inset of Fig. 1(c) shows a high-magnification XTEM micrograph of the bottom nanowire surrounded by the thermally grown SiO_2 gate dielectric.

III. Results and Discussion

Fig. 2 shows the I_d-V_g and I_d-V_d characteristics of a GAA NiSi complementary SBNWFET with $L_g = 90$ nm. We normalized the current to the width of the SiNW, which was determined to be $\sim$5 nm + 8 nm from the TEM micrograph in Fig. 1(c). Clearly, a complementary transistor action is observed with high/low current in the positive V_g region and low/high current in the negative V_g region for the N-SBNWFET/ P-SBNWFET, respectively. In addition, the I_d-V_g curves are almost symmetrical, which indicates the possibility of using a single metal for the S/D silicide formation, greatly simplifying device processing. Gate-induced drain leakage (GIDL)-like reverse current characteristics are observed [15]. However, this behavior is due to the reverse current of SBMOSs, i.e., ambipolar behavior. This is due to the electron/hole current for

TABLE I

KEY ELECTRICAL PERFORMANCE INDEXES FOR SELECTED SBMOS DEVICES. $I_{\rm off}$ WAS MEASURED AT $V_g = V_t \pm 0.6$ V, WHEREAS $I_{\rm on}$ WAS MEASURED AT $V_g = V_t \pm 0.6$ V. FH: FIN HEIGHT; FW: FIN WIDTH; DS: DOPANT SEGREGATION; $*$: MEASURED AT $L_g \sim 80$ nm

	S/D	Channel	L_g (nm)	T_{ox} (nm)	V_d (V)	I_{on} (μA/μm)	I_{off} (μA/μm)	I_{on}/I_{off}	SS (mV/dec)	DIBL (mV/V)	Ref.
N-SBNWMOS	NiSi	wire, ~6nm	90	9	1.2	399	5.2 X 10^{-3}	2.3 X 10^5	~60	13	This work
P-SBNWMOS	NiSi	wire, ~6nm	90	9	-1.2	513	5.2 X 10^{-3}	1.5 X 10^5	~60	10	
N-SBMOS	NiSi DS	FinFET, FH = 50nm, FW = 15nm	15	1.3	1	1000	5 X 10^{-2}	2 X 10^4	~65*	-	3
P-SBMOS	NiSi DS	FinFET, FH = 50nm, FW = 15nm	15	1.3	-1	500	8 X 10^{-2}	6.3 X 10^3	~80*	-	
N-SBMOS	NiSi DS	FinFET, FH = 40nm, FW = 60nm	49	4	1	167	8.4 X 10^{-6}	2 X 10^7	94	-	10
P-SBMOS	NiSi DS	FinFET, FH = 40nm, FW = 60nm	49	4	-1	84	1.7 X 10^{-7}	5 X 10^8	71	-	

the P-SBNWFET/N-SBNWFET when a reverse V_g is applied ($+V_g$ for the P-SBNWFET and $-V_g$ for the N-SBNWFET).

The inset of Fig. 2(a) shows the $I_d{-}V_g$ characteristics of a NiSi N-SBNWFET ($L_g = 90$ nm) without the As implantation step. A higher current in the negative arm compared to the positive arm is observed due to the lower Schottky barrier height ϕ_b to holes of NiSi/p-Si compared to ϕ_b to electrons of NiSi/n-Si ($\sim$0.43 versus $\sim$0.67 eV) [12]. Therefore, in order for NiSi to effectively function as an N-SBMOS, As segregation must be employed to reduce the effective ϕ_b to electrons, i.e., to reduce the Schottky barrier thickness [4], [5].

The extracted SBNWFET performance indexes, together with selected Schottky barrier FinFETs from published results, are summarized in Table I. As can be observed, the extracted transistor parameters are comparable or better than the reported NiSi-based SBMOS [3]–[10], although barrier modification techniques were not used (for the P-SBNWFET). Examination of the SBNWFET SS shows that it is comparable, if not lower, than the lowest SS values reported in NiSi Schottky barrier FinFETs incorporating modified Schottky barriers by dopant segregation [3], [16].

It should be mentioned that the application of dopant segregation to the NiSi/Si interface in SBMOSs result in SS close to the thermal limit [4], [5], [10]. This is achieved as the Schottky barrier is thinned due to the high dopant concentration at the NiSi/Si interface, resulting in the carrier flow being determined by the channel potential similar to a conventional MOSFET [4]–[6], [10], [16].

It is believed that the SBNWFET (with an $\sim$5-nm-wide MS junction) exhibit thinning of the Schottky barrier, resulting in near-ideal SS. However, the barrier thinning mechanism is different from dopant segregation. As an MS junction is scaled, electrostatics due to the metal charge on nanometer-sized Si channel contacts affect the Schottky barrier shape, i.e., the Schottky barrier is thinner as the MS junction size is reduced [17]. The thinner Schottky barrier results in enhanced carrier injection and has been theoretically [17], [18] and empirically [17]–[19] shown by various groups.

The $I_d{-}V_d$ characteristics of the same device show the absence of an upwardly sloping sublinear turn-on, which is an indication of low effective ϕ_b [20]. For the P-SBNWFET, there is a clear presence of linear and saturation regions for all V_g biases, indicating that the channel pinchoff has been reached. It also shows the absence of short-channel effects. On the other hand, the N-SBNWFET does not show a clear saturation region at higher V_g biases due to the higher ϕ_b to electrons.

Fig. 3 shows the $I_{\rm on}/I_{\rm off}$ characteristics of NiSi complementary SBNWFETs with L_g ranging from 105 to 85 nm. The experimental fit of the slope shows that the $I_{\rm on}/I_{\rm off}$ ratios for both the N- and P-SBNWFETs are slightly higher than $\sim 10^5$. A comparison of $I_{\rm on}/I_{\rm off}$ ratios of the complementary SBNWFET with a NiSi SBMOS on an SOI ($t_{\rm SOI} = 25{-}50$ nm) without dopant segregation [4], [5] shows that the ratio has increased by more than 15 and 7 times for the N- and P-SBMOSs, respectively. In addition, Fig. 3 plots the $I_{\rm on}/I_{\rm off}$ characteristics of published SBMOS results [3]–[10], all of which employ some form of barrier modification technique. In Fig. 3 and Table I, it can be seen that SBNWFET $I_{\rm on}$ and $I_{\rm off}$ currents are comparable with published SBMOS results. It should be noted that for the NiSi P-SBNWFET, no barrier modification technique was used in our experiments. Thus, the improvements are due to the device architecture, i.e., the superior electrostatic gate control of the GAA channel [13], and the nanoscale MS junction.

IV. CONCLUSION

We have fabricated high-performance GAA NiSi complementary SBNWFETs with high $I_{\rm on}/I_{\rm off}$ ratio, near-ideal SS ($\sim$60 mV/decade), and low DIBL ($\sim$10 mV/V) characteristics. In particular, the P-SBNWFET transistor characteristics can be achieved without the use of barrier modification techniques. Thus, the improvements in performance are due to the superior gate control of the GAA structure and the Schottky barrier thinning in a scaled nanosized MS junction.

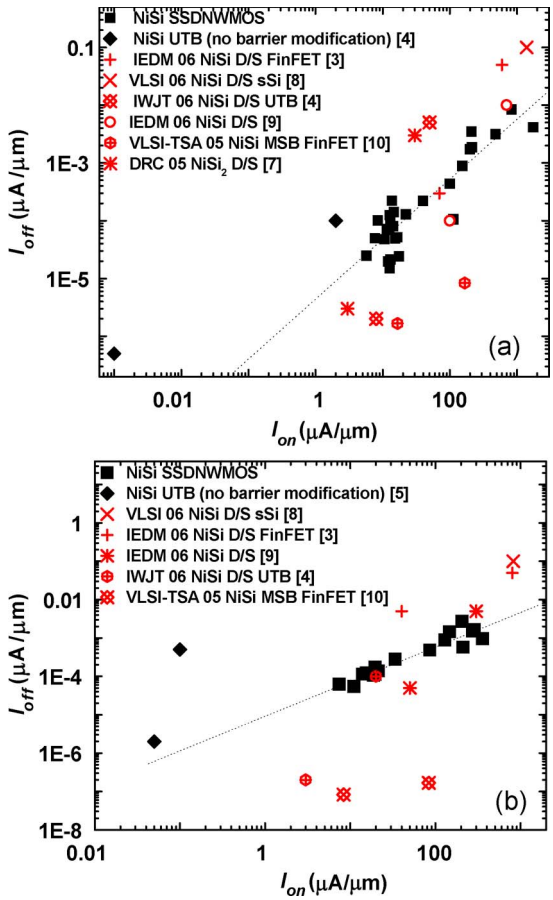

Fig. 3. $I_{\rm on}/I_{\rm off}$ characteristics of the GAA NiSi (a) N-SBNWFET and (b) P-SBNWFET extracted from the $L_g = 105-85$ nm devices. $I_{\rm off}$ was measured at $V_t \pm 0.6$ V, whereas $I_{\rm on}$ was measured at $V_t \pm 0.6$ V, for $V_d = \pm 50$ mV and $\pm 1/\pm 1.2$ V.

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