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Dip Pen Nanolithography™ and its potential for nanoelectronics

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Abstract — Dip Pen Nanolithography (DPN™) is a patterning technique for nanoscale science and engineering based on scanning probe microscopy. Its main advantages are very high resolution, the unique capability to deposit many different materials directly onto a substrate and low cost of ownership. We present here new research and development efforts that demonstrate the potential of DPN as a tool to produce nanoelectronic devices and circuits. We show the direct deposition of electronic materials as well as the use of external accessories to accelerate the development phase of nanoelectronic components.

Index Terms — AFM, dip pen, DPN, nanoelectronics, nanolithography, nanotube, scanning probe, CMP.

I. INTRODUCTION

Since the 1980s, scanning probe microscopy methods (SPM) have played an increasingly important role in research and development of novel materials and nanoscopic structures. Based on the most prominent offspring of this family of tools, atomic force microscopy (AFM) [1], new lithography techniques have emerged in recent years.
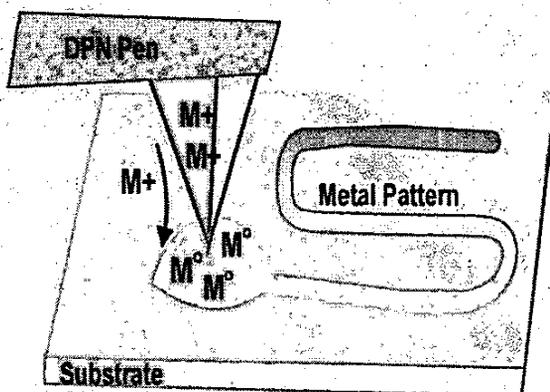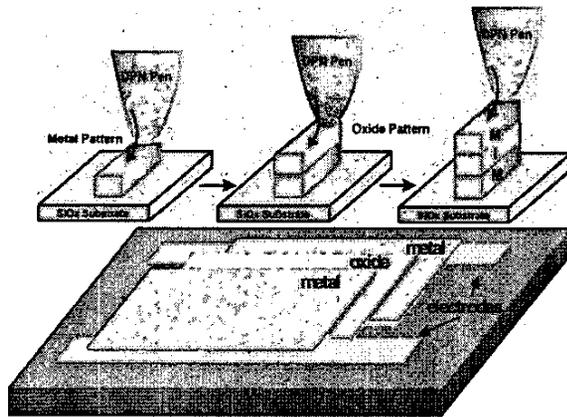

Figure 1: The concept of DPN for patterning metallic features

While there are many potential proximal probe patterning techniques, the most flexibility is achieved when using additive techniques. Here, the most versatile and well developed application is Dip Pen Nanolithography (DPN™) [2-4]. DPN uses the apex of a sharp microfabricated tip (or stylus) as a medium to deposit functional materials (the 'ink') onto a surface (see Figure 1). An advantage to the DPN process is in its generality for depositing both soft and hard material precursors. Soft materials include organic materials and biological molecules such as DNA and proteins but also functional polymers. Hard or "stiff" materials tend to be those typically found in the semiconductor industry whose Young's moduli are near and above 80 GPa. Hard materials such as inorganic oxides and metals often require a reduction step typically involving thermal, chemical, or electrochemical treatments after DPN deposition to become functional. The range of deposition height spans orders of magnitude from single molecular monolayers to tens of nanometers in height, depending on the ink used. Multiple deposition materials can be introduced on adjacent pens using microfluidic ink delivery. In order to parallelize fabrication, arrays of probes can be used to write simultaneously. Arrays of pens that allow individual engagement of pens on the surface, so called 'active pens', further increase patterning flexibility.

This new technology can address many of today's problems in micro- and nanofabrication: As device size continues to decrease and the useful limits of silicon and other solid-state material's physical properties are approached, an inevitable search for new materials has emerged. Novel molecular devices such as nanotubes, nanowires nanospheres and other nanoscience inventions, as well as biological nanostructures, promise to continue Moore's law of increasing transistor density for decreasing chip size while they also offer the possibility of introducing entire new classes of functionality. Challenges arise in their production: simple fabrication of nanodevices and their shape control is to date limited and such rapid prototyping of basic devices and shapes is virtually nonexistent. An equally important challenge exists where these devices are interfaced with their surroundings in terms of electronic packaging. For example, many kinds of nanoscale particles that are of interest cannot be patterned reliably on surfaces. Instead, they are often

scattered randomly on a substrate. When electrical connectivity is required, few appropriate methods exist today that can be applied. Often times a random grid of contact lines is produced before the particles are present in the hope that some objects position near the contact lines. DPN can help here in two ways. For one, templates can be created that direct positioning of nanoparticles such as carbon nanotubes. Furthermore, since DPN is inherently paired with a powerful inspection tool, AFM, it is possible to inspect the nanoparticle landscape and in-situ pattern conductive lines either of metal or conductive polymers as

be converted to metallic films at relatively low annealing temperatures.

Figure 3: A metallic line deposited via DPN. It is 2 micron wide (2-D color coded height scan on top) and 6 nm high (line scan below).
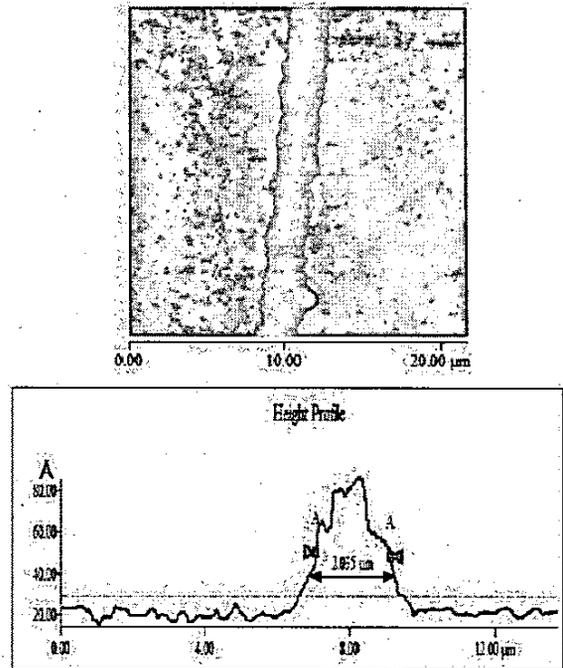

Figure 2: Potential nanofabrication scheme for generic layered metal-insulator-metal nanostructures via direct deposition DPN.

interconnects. Such conductive structures can also be used as nanoscale electrodes [5] or, together with dielectric structures, as a substitute for nanoelectronic devices (see Figure 2). Because DPN can pattern many different materials, it can also directly pattern sensor materials [6] such as metal oxides and metals that act as catalysts to address the local synthesis of sensor material.

As the first and enabling step, we investigate here the performance of a number of metal precursor ink systems as building blocks for nanoscale low-resistivity interconnects. The processing of metals can be difficult and operating at the nanoscale can further aggravate problems. Many metallization methods are limited to micron level manufacturing and require electrochemical biases or very high temperatures. The investigated precursor inks can be patterned using DPN under ambient environmental conditions. These inks can then

It is a particular challenge to pattern nanoscale lines that are nonetheless continuous with acceptable line resistance. A 5 micron wide version of the trace shown in Figure 3 exhibited a resistivity of only 4.3 microohm*cm, making this ink formulation a good candidate for further studies into miniaturization.

To help nanoscale device fabrication and testing but also to accelerate the screening of potential inks and for general material property investigation, we developed a host structure capable of electrically interfacing at the nanometer scale while being accessible at the macroscale. This device is called the Nanoscale Experimenters Test System (NETS) and consists of three different modules for connection from the nanoscale to the macroscale. The smallest module (see Figure 5) is a processed silicon chip that contains many electrode pairs and triples with a narrow gap of two microns between single electrodes. The electrodes consist of one-micron thick gold traces on an oxide layer with silicon oxide also filling the areas between electrodes. The enabling feature is the chemical-

mechanical planarization step that yields a very smooth surface consisting of two very different materials. This planar substrate allows smooth patterning of films only a few nanometers thick without risking the loss of continuity due to surface roughness or discontinuities.

Figure 5: The NETS substrate layout showing many electrode pairs. At their termination point towards the center of the die, two-micron sized insulating gaps allow testing of electronically active materials.

We show here the physical properties of the NETS substrate and its compatibility with the DPN process as well as patterning with a large number of different metal and metal oxide materials.

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