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Analysis and Modeling of Internal State Variables for Dynamic Effects of Nonvolatile Memory Devices

Yang Shang, Student Member, IEEE, Wei Fei, Student Member, IEEE, and Hao Yu, Member, IEEE

Abstract—Hybrid integration of CMOS and nonvolatile memory (NVM) devices has become the foundation for emerging nonvolatile memory-based computing. The primary challenge to validate hybrid memory system with both CMOS and NVM devices is to develop a SPICE-like simulator that can simulate the dynamic behavior accurately and efficiently. Since memristor, spin-transfer-toque magnetic-tunneling-junction (STT-MTJ) and phase-change-memory (PCM) devices are the most promising candidates of next generation of NVM devices, it is under great interest in including these new devices in the standard CMOS design flow. The previous approaches either ignore dynamic effect without consideration of internal states for dynamic behavior, or need complex equivalent circuits to represent those devices. This paper proposes a new modified nodal analysis for NVM devices with identified internal state variables for dynamic behavior. As such, compact SPICE-like implementation can be derived for all three new NVM devices in the design of large-scale memory circuits. As demonstrated by a number of examples on hybrid memory circuits with both CMOS and NVM devices, our newly developed SPICE-like simulator can capture dynamic behaviors of memristor, STT-MTJ and PCM devices, and can also reduce CPU runtime by 20–69 times when compared to the previous equivalent circuit based approaches.

Index Terms—Internal state variable, memristor, nonvolatile memory (NVM) device, spin-transfer-toque magnetic-tunneling-junction (STT-MTJ), phase-change-memory (PCM), SPICE-like simulation.

I. INTRODUCTION

T
HE recent advance in nonvolatile memory (NVM) has introduced promising future for the development of memory-based-computing with a natural merge of processor and memory, which might break the bandwidth-bottleneck of the conventional von Neumann architecture. A range of NVM devices [1]–[3] such as memristor, phase-change RAM (PCRAM), magnetic RAM (MRAM) and resistive RAM (RRAM), have appeared to potentially replace both SRAM and DRAM for the memory hierarchy in the conventional computing system. More importantly, the nonvolatile property of new devices leads to fast access time, low energy and high integration density. For example, compared to the traditional memory devices, spin-toque-transfer (STT) magnetic-tunneling-junction (MTJ) based MRAM has a 3–4 times reduced cell size which is about 6–8 F² (F is the minimum technology dimension, ~0.4 μm) [4]. With the advance in nanotechnology, even higher integration density can be achieved by memristor based crossbar-array, which can be fabricated with pitch of 17 nm [5]. Such advantage can be further enhanced by 3-D stacking [6].

In the emerging NVM technologies, very often new devices cannot be fully described by the conventional circuit state variables which are nodal voltage and branch current. For instance, additional internal state variables have to be considered when describing the dynamic behavior of following NVM devices: magnetization for STT-MTJ, doping ratio for memristor, temperature and crystalline fraction for PCM. The previous approaches describe these NVM devices by equivalent circuit [7]–[11] with additional circuit components and hence increased complexity. The equivalent circuit approaches are limited to deal with internal state variables for dynamic because many additional circuit components are required to maintain high accuracy. One equivalent circuit may require dozens of extra circuit components to describe one NVM device, and hence results in huge overhead to model and simulate large-scale memory designs. As such, novel modeling and simulation techniques are needed to improve the computation efficiency for the memory circuit design with hybrid CMOS and NVM devices.

In order to consider the new nonvolatile memory devices similarly to how we dealt with CMOS devices by physics based model, one critical perspective is to identify and include the new state variable relevant for the new dynamic behavior of the nonvolatile devices [12]. Note that different from device parameters, a device state variable varies with time under given input signals. Here, we deploy the term “internal state variables” to represent those physics-based state variables which cannot be observed from external electric behavior, while the conventional state variables such as nodal voltage and branch current are called “external state variables.” Take STT-MTJ for instance, many variables can be extracted from the physics point of view, such as temperature, polarization, magnetization, etc. Variables like temperature and electron polarization are assumed to be constant and therefore called parameters, but the variable of magnetization is the state associated with STT-MTJ and can change with time similar to the states of nodal voltages and branch currents. As such, the angles to describe magnetization are identified as internal state variables for STT-MTJ devices.

In this paper, we have the following primary contributions: 1) internal state variables have been identified for the consideration of nonlinear dynamic models for memristor, STT-MTJ and PCM; and 2) a new modified nodal analysis (MNA) formulation has been developed to consider internal state variables of
nonvolatile memory devices within one SPICE-like simulator. Experiments show that our new MNA formulation with internal state variable can handle the simulation of timing, power, variation and detailed transient behavior for the hybrid design of CMOS and NVM devices at large scale, with results consistent with the measurement. More importantly, compared to equivalent circuit approaches that only consider the static behavior or with large overhead of additional nodes, the newly developed SPICE-like simulator can be used to study the dynamic behavior of NVM device and the CPU time can be reduced by 20–69 times.

The rest of this paper is organized in the following manner. We first introduce the general derivation of a new MNA formulation to consider internal state variables of nonvolatile memory devices in Section II. Then in Section III, the dynamic models of typical NVM devices: memristor, STT-MTJ and PCM device are briefly discussed. The SPICE implementation with the use of internal state variables in our simulator is also illustrated. Experimental results and discussion are presented in Section IV, and the paper is concluded in Section V.

II. MODIFIED NODAL ANALYSIS OF NVM DEVICES

The appearance of state variable of an electronic device could be the result of the interaction of numbers of physical phenomenon at different domains. In the traditional circuit analysis for electronic device, nodal voltage and branch current are employed to describe the device terminal change with time. However, for memory relevant devices such as memristor [13], the nonlinear dynamic with memory effect cannot be explicitly described by these two states and additional internal state variables have to be introduced [12]. These internal state variables can be represented by the external state variables from equivalent circuit point of view [7]–[11] but with increased circuit complexity for simulation. In order to directly include internal state variables, we have introduced a new modified nodal analysis (MNA) for internal state variables of NVM devices, which can provide compact physics-based description for internal states with high efficiency and accuracy. All the relevant variables used in this section are summarized in Table I.

### Table I

<table>
<thead>
<tr>
<th>Variables</th>
<th>Definitions</th>
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<tr>
<td>$s_m$</td>
<td>internal state variable for new MNA</td>
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<tr>
<td>$v_n, j_n$</td>
<td>traditional state variables for MNA: nodal voltage and branch current</td>
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<tr>
<td>$v_s, j_s$</td>
<td>branch voltage, source current, and inductor current</td>
</tr>
<tr>
<td>$G, C, L$</td>
<td>traditional conductance, capacitance and inductance</td>
</tr>
<tr>
<td>$S$</td>
<td>new Jacobian as memductance</td>
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<tr>
<td>$K^c, K^f, K^r, K^i$</td>
<td>new Jacobians introduced by $s_m$</td>
</tr>
<tr>
<td>$E_c, E_g, E_I, E_i$</td>
<td>incident matrix for capacitor, resistor, inductor and current source</td>
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<tr>
<td>$E_m$</td>
<td>new incident matrix introduced for NVM devices</td>
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<tr>
<td>$f, g$</td>
<td>functions introduced by $s_m$ for new state equations</td>
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determined by the topology of circuits. Assuming $n$ nodes and $b$ branches, the incident matrix $E (\in \mathbb{R}^{n \times b})$ is defined by

$$v_{i,j} = \begin{cases} 1, & \text{if branch } j \text{ flows into node } i \\ -1, & \text{if branch } j \text{ flows out of node } i \\ 0, & \text{if branch } j \text{ is not included at node } i. \end{cases}$$

With $j_n, v_n$ and $v_m$ defined as in Table I, KCL and KVL can be described by

$$KCL : E j_t = 0 \quad KVL : E^T v_n = v_b.$$

Considering the presence of capacitor, inductor, resistor, and voltage controlled voltage source, the KCL and KVL become

$$\frac{d}{dt} F_c q \{ E^T v_n, t \} + E_g j (E^T v_n, t) + E_I j_I + E_i j_I = 0,$$

$$L_{j_i} \frac{d}{dt} j_i - E_{j_i} v_n = 0, \quad E_{j_i}^T v_n = 0.$$

Here the four incident matrices $[E_c, E_g, E_i, E_i]$ describe the topological connections of capacitive, conductive, inductive, and voltage-source elements. Matrix $L_{j_i}$ provides values for inductors in the circuit. Introducing the state variable $x = [v_n, j_t, j_I]^T$, the above MNA formulation can be denoted shortly by a differential-algebra-equation (DAE) as follows:

$$F(x, \dot{x}, t) = \frac{d}{dt} q(x, t) + j(x, t) = 0.$$ (1)

B. New MNA With Internal State Variables

In order to handle the dynamic models of NVM device with internal state variables, one needs to develop a new MNA by adding internal state variables into the traditional MNA (for CMOS devices). As shown in Fig. 1(a), these internal state variables, termed as $s_m$, determine the conductance of all nonvolatile memory devices, termed as memductance (memory conductance) here, and therefore can be categorized as one new device branch. Note that the simulation time is directly related to the total number of state variables generated for the circuit. Compared to the traditional approaches with complex equivalent circuits, the introduction of memductance adds much fewer state variables by including internal state variables to represent dynamic effect of NVM device. Take memristor for example, its equivalent circuit requires dozens of additional nodal voltages to characterize the circuit behavior, while only two nodal voltages and one internal state variable are required in our memductance approach. Therefore, the introduction of memductance greatly simplifies the model complexity and in turn largely reduces the verification and design cost.
One NVM device may require one or multiple internal state variables to accurately describe its dynamic behaviors. The corresponding incident matrix is termed as \( E_{m,n} \), with which the nonvolatile device branch current is obtained as \( \sum E_{m,j} E_{n,m} \). As Fig. 1(b) shows, combined with branch currents from the traditional CMOS devices, a new KCL equation is formed by

\[
\frac{d}{dt} E_{c,j} \left( E_{n,m} v_{n,m}, t \right) + \sum E_{m,j} \left( E_{n,m} v_{n,m}, s_m, t \right) + \sum E_{g,j} \left( E_{g,t} v_{n,m}, t \right) + E_{i,j} + E_{i,j} = 0
\]

\[
L_i \frac{dv_n}{dt} = E_{i,v}; \quad E_{i,v} = 0
\]

\[
f \left( E_{m,v}, s_m, t \right) + \frac{d}{dt} \left( E_{m,v}, s_m, t \right) = 0.
\]

(2)

Here functions \( f \) and \( g \) are the additional state equations for nonvolatile devices with \( s_m \). Moreover, with the new state variable vector \( X = [v_n, j, i, v_m, s_m] \), the above new MNA can still be described by the differential-algebra-equation (DAE) as (1).

We can further derive the Jacobian as general conductance \( G \), capacitance \( C \), and memductance \( S \). The additional term of memductance \( S \) is introduced to describe the conductance of nonvolatile devices for the induced current change under the change of internal state \( s_m \). At one biasing point \( X_0 \), the first-order derivative or Jacobian of the new DAE with respect to \( X \) are

\[
G = \left( E_g \frac{d}{dt} f \left( v_n^g, v_m^g, t \right) E_{g}^T \right)
\]

\[
C = \left( E_r \frac{d}{dt} g \left( v_n^r, v_m^r, t \right) E_{r}^T \right)
\]

\[
S = \left( E_m \frac{d}{dt} j \left( v_n^m, s_m, t \right) E_{m}^T \right)
\]

(3)

where \( v_n^g = E_g^T v_n, v_n^r = E_r^T v_n, v_n^m = E_m^T v_n \).

In addition, there are four additional Jacobian terms introduced from functions \( f \) and \( g \) due to the new state variable \( s_m \) for NVM device

\[
K_{e,v} = \left( E_m \frac{d}{ds_m} f \left( v_n^m, s_m, t \right) E_{m}^T \right)
\]

\[
K_{e,i} = \left( E_m \frac{d}{dsv_m} f \left( v_n^m, s_m, t \right) E_{m}^T \right)
\]

\[
K_{e,s} = \left( E_m \frac{d}{dv_m} g \left( v_n^m, s_m, t \right) E_{m}^T \right)
\]

\[
K_{e,i} = \left( E_m \frac{d}{ds_m} g \left( v_n^m, s_m, t \right) E_{m}^T \right)
\]

(4)

The subscripts \( v \) and \( s \) denote the derivatives to nonvolatile device branch voltage \( v_n^m \) and its internal state variable \( s_m \), respectively. The superscript \( F \) and \( G \) correspond to functions \( f \) and \( g \), which describe the additional state equation for the internal state variable \( s_m \).

In addition, with the new small-signal current introduced by \( s_m \), as shown in Fig. 1(c), the new linearized small-signal DAE becomes

\[
\mathcal{G} \cdot \delta v_n + C \cdot \delta \dot{v}_n + V_i \cdot \delta j_i + V_j \cdot \delta j_j + S \cdot \delta s_m
\]

\[
= -F \left( X_0, X_0, t \right)
\]

\[
K_{e,v} \cdot \delta \dot{v}_n = 0;
\]

\[
K_{e,i} \cdot \delta \dot{j}_i = 0;
\]

\[
K_{e,s} \cdot \delta \dot{s}_m + K_{e}^G \cdot \delta \dot{v}_n + K_{e}^G \cdot \delta \dot{s}_m = 0.
\]

(5)

Therefore, we have the following matrix form for linearized system equation with all Jacobian matrices \( \mathcal{G}, C, K_{e,v}, K_{e,i}, K_{e,s}, K_{e}^G, K_{e}^G \) and incident matrices \( E_i, E_{i,v}, E_{i,i}, E_{i,s}, E_{i}^G, E_{i}^G \):

\[
\begin{bmatrix}
\mathcal{G} & E_i & E_{i,v} & E_{i,i} & E_{i,s} & E_{i}^G & E_{i}^G \\
-E_i & 0 & 0 & 0 & 0 & 0 & 0 \\
-E_{i,v} & 0 & 0 & 0 & 0 & 0 & 0 \\
K_{e,v} & 0 & 0 & K_{e}^G & 0 & 0 & 0 \\
K_{e,i} & 0 & 0 & 0 & K_{e}^G & 0 & 0 \\
K_{e,s} & 0 & 0 & 0 & 0 & K_{e}^G & 0 \\
K_{e}^G & 0 & 0 & 0 & 0 & 0 & K_{e}^G
\end{bmatrix}
\begin{bmatrix}
\delta v_n \\
\delta j_i \\
\delta j_j \\
\delta s_m
\end{bmatrix}
\]

\[
= -F \left( X_0, X_0, t \right).
\]

(6)

Note that both large-signal and small-signal system equations can be obtained when introducing internal state variables. Its implementation for NVM devices is shown in the following section.

III. INTERNAL STATE VARIABLE OF NVM DEVICES

In this section, the internal state variables are identified from the dynamic operation of memristor, STT-MTJ and PCM devices separately. Then the application of new NMA is derived for each device in the SPICE-like simulator based on the modified nodal analysis in Section II. All the variables used in this section are summarized in Table II for memristor, Table III for STT-MTJ and Table IV for PCM, respectively.

### A. Memristor Device

The existence of memristor was first predicted by Chua in 1976 [13], but not until nearly 30 years later was it first discovered in nano-scale devices in HP lab [15]. A typical structure of memristor is illustrated in Fig. 2(a) with doping and undoping regions. The term doping ratio \( w \) is introduced to numerically...
represents the ratio of doping region \( W \) over the whole thickness of memristor film \( D \). As there is a large difference of resistivity in doping and undoping regions, the total resistance is changing with doping ratio. For instance, when \( w = 1 \) the memristor is at ON-state, where the resistance is a thousand times smaller than the resistance at OFF-state with \( w = 0 \).

The operating principle of memristor device can be summarized as: charge induced state (doping-ratio \( w \)) shifting. For instance, when the positive charge flows towards the right-hand side of memristor junction shown in Fig. 2(a), the doping ratio \( w \) increases and the resistance reduces accordingly, and vice versa for the charge flowing in the reverse direction. Traditionally, this mechanism can be described as generalized current-controlled memristive system [13] with the following equations:

\[
\begin{align*}
    v(t) &= R(w, v)i(t) \\
    \frac{dw(t)}{dt} &= f(w, v)
\end{align*}
\]

where \( R \) is the resistance of memristor and \( f \) is the explicit function of \( w \) and applied voltage \( v \); \( \frac{dw}{dt} \) is the normalized drift velocity determined by \( w \) and external voltage \( v \). Note that the complementary current-controlled memristive system can be defined similarly. We can easily see from (7) that, other than the voltage \( v \) and the current \( i \), the complete status of memristor is also dependent on the doping-ratio \( w \). Therefore, \( w \) is identified as the internal state variable for memristor.

The dynamic effect relevant to doping-factor \( w \) can be found in details from Appendix A. Considering charge-induced-drifting effect, slow-down effect and strong-electric-field effect as shown in Fig. 2(b), we can obtain a complete nonlinear dynamic memristor model from (10), (11) and (13):

\[
\begin{align*}
    v(t) &= R_{\text{eff}} - (R_{\text{on}} - R_{\text{off}})w(t) \\
    \frac{dw(t)}{dt} &= \mu E_0 \sin h \left( v(t) \frac{D}{D_0} F(w(t)) \right).
\end{align*}
\]

Equation (8) can be used to link internal state variable \( w(t) \) with the external state variables (nodal voltage and branch current). Accordingly, we can effectively determine the memductance of memristor when all state variables are determined.

Previous approaches by equivalent circuit [10], [16] require the use of many additional circuit components to capture dynamics and hence lead to large complexity for large-scale circuit simulation. For instance as depicted in Fig. 3 to implement an equivalent circuit of memristor shown in [10], many circuit components have to be added, including resistor, capacitor, diode and current-controlled-current-source, etc.

In the following, we first define the new state variable vector:

\[
X = [v_n, i_1, i_2, w_m]^T
\]

and then show how to obtain the Jacobian terms \( \mathcal{G}, \mathcal{S}, \mathcal{K}_\mathcal{G}^{F}, \mathcal{K}_\mathcal{S}^{F}, \mathcal{K}_\mathcal{G}^{I}, \mathcal{K}_\mathcal{S}^{I} \) in (6).

Applying (3) and (4) derived in last section to the memristor dynamic function described in (8), one can obtain the Jacobian terms:

\[
\mathcal{G} = \begin{bmatrix} G & -G \\ -G & G \end{bmatrix}, \quad \mathcal{S} = \begin{bmatrix} v_n \times \frac{dG}{dw_m} \\ -v_n \times \frac{dG}{dw_m} \end{bmatrix}, \quad \mathcal{C} = 0
\]

\[
\mathcal{K}_\mathcal{G}^{F} = \left[ -c_1 c_2 F(w_m) \cos h(c_2 v_n) \right], \quad \mathcal{K}_\mathcal{S}^{F} = \left[ -c_1 s_2 F(w_m) \cos h(c_2 v_n) \right], \quad \mathcal{K}_\mathcal{G}^{I} = 0, \quad \mathcal{K}_\mathcal{S}^{I} = 1
\]
where $G$ is the conductance and $(dG)/(dw_m)$ the internal state variable derivative of conductance, $c_1 = (\mu F_1)/(|D|)$, $c_2 = (1)/(|D|)$ are constants, and $F(u)$ is the window function. Recall that the other parameters are defined in Table II.

**B. STT-MTJ Device**

A typical STT-MTJ device structure appears as a sandwich with two ferromagnetic layers and one oxide barrier in between [11]–[13]. One STT-MTJ device has two stable states: parallel state (P) or anti-parallel state (AP), where the free layer magnetization is in the same or the opposite direction with respect to the hard axis (magnetization direction of fixed layer), respectively. One giant-magneto-resistance (GMR) at AP state is higher than the GMR at P state [17]. The GMR [18] can be expressed as:

$$G = \frac{\partial^2 G}{\partial w_m \partial w_n} = \frac{\partial^2 G}{\partial \theta \partial \phi}. \tag{9}$$

Note that angle $\theta$ is one magnetization angle between free-layer and hard-axis. It can be easily derived that: $R_{t=\theta} = R_L$ at P state and $R_{t=\phi} = R_H$ at AP state.

As depicted in Fig. 4, the operating principle of STT-MTJ device can be summarized as: the external current induced state (P or AP) change. STT-MTJ is switched from P to AP with sufficient forward biased current; and from AP to P with sufficient reverse biased current. The detailed dynamic effects required to describe the behavior of STT-MTJ is discussed in Appendix B. As discussed, we choose the azimuthal angles of normalized magnetization ($M$) of free layer in $x$–$y$ plane ($\theta$), and $y$ – $z$ plane ($\phi$) as internal state variables to describe the dynamic behavior of STT-MTJ device.

Considering the tunneling, spin-transfer-torque effect and arbitrary driving condition, the dynamics of one STT-MTJ device model can be constructed from (9), (14), (17), and (18), linking internal state variables $\theta$ and $\phi$ with the external state variables (nodal voltage and branch current).

Previous approaches by equivalent circuit [7]–[9] require the use of many additional circuit components to capture this dynamics and hence have large overhead for large-scale circuit simulation. For instance as depicted in Fig. 5, to implement an equivalent circuit of STT-MTJ shown in [9], at least ten more circuit elements have to be added, including current-control-current-source, capacitor, decision circuit and curve fitting circuit, etc. As a result, the circuit overhead of equivalent circuit approach can grow as the circuit size increases, which leads to huge amount of computation time.

Similar to memristor device, we can define the new state variable vector $X = [v_n, j_n, j_b, \theta_m, \phi_m, T]$, and then the Jacobian terms $G_s, S, K^F_s, K^F_v, K^F_s, K^G_v$ and $K^G_s$ in (6) for STT-MTJ.

Applying (3) and (4) derived in Section II to the STT-MTJ dynamic functions described in (9), (14), (17), and (18), we can easily obtain the Jacobian terms required as follows:

$$\begin{align*}
G &= \begin{bmatrix}
\frac{\partial^2 G}{\partial w_m \partial w_n} & \frac{\partial^2 G}{\partial \theta \partial \phi} \\
-\frac{\partial^2 G}{\partial \theta \partial \phi} & \frac{\partial^2 G}{\partial \theta \partial \phi}
\end{bmatrix} \\
H &= 0 \\
K^F_s &= \begin{bmatrix}
0 \\
0
\end{bmatrix} \\
K^F_v &= \begin{bmatrix}
1 \\
1
\end{bmatrix} \\
K^G_v &= 0 \\
K^G_s &= \begin{bmatrix}
0 & 0 \\
0 & 0
\end{bmatrix}
\end{align*}$$

Note that $G_s$ is the conductance of STT-MTJ, $S$ is the memductance of STT-MTJ, $f(\theta_m, \phi_m, t)$ is the function at the right hand side of (17), and $\omega_m$ is the angular movement speed of $\phi_m$. Recall that the other parameters are defined in Table III.

**C. PCM Device**

PCM device is based on the phase-changing technology of chalcogenide materials such as Ge$_2$SbTe$_5$ [19], of which the crystal structure can be thermally switched between two different stable states: crystalline and amorphous, and for the same PCM device, the resistance in amorphous state is one thousand times larger than that in crystalline state. Typically, PCM device has a mushroom structure as demonstrated in Fig. 6(a). This structure makes the heat dissipation rate at top surface much higher than that of bottom surface. As such, the thermal activation of phase changing always begins from the bottom side. Note that the resistance of PCM device is mainly determined by the active region shown in Fig. 6(a).
The operation of PCM device can be summarized as: thermal activated state (crystallizing and amorphousizing) change. As illustrated in Fig. 6(b), a narrow pulse of temperature surge above the melting temperature \( T_m \) will “RESET” the active region to the amorphous state; and a long pulse of temperature surge between melting temperature \( T_m \) and crystallization temperature \( T_X \) will “SET” the active region to the crystalline state. The dynamic effects required to describe the behavior of PCM device is discussed in Appendix C with details. As discussed, we choose crystallization ratio \( C_X \) and active region temperature \( T_m \) as internal state variables to describe the dynamic behavior of PCM device.

Considering the thermal effect and crystallization kinetics, we can describe dynamics of PCM device with (21), (22) and (23), linking internal state variables with the external state variables (nodal voltage and branch current).

Similar to memristor and STT-MTJ, the new state variable vector is introduced as \( \mathbf{x} \), and the Jacobian terms \( \mathbf{J} \) and \( \mathbf{K} \) in (6) for PCM device are then obtained by

\[
\mathbf{J} = \begin{bmatrix} G & G \\ -G & G \end{bmatrix}, \quad \mathbf{K} = \begin{bmatrix} C_X & C_X \\ -C_X & C_X \end{bmatrix}, \quad \mathbf{K}^T = \begin{bmatrix} G & G \\ -G & G \end{bmatrix}, \quad \mathbf{K}^G = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}, \quad \mathbf{K}^G = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}, \quad \mathbf{K}^G = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix},
\]

where \( G \) is the conductance, and \( (dG)/(dT) \) and \( (dG)/(dV) \) are the temperature and crystalline fraction derivatives; \( (dh(T_m, v_n, t))/(dn) \) and \( (dh(T_m, v_n, t))/(dT) \) are derived from (21) and (22), respectively. Note that \( h(T_m, v_n, t) \) is the function at the right-hand side of (21), and \( g(T_m, v_n, t) \) is the function at the right-hand side of (22). Recall that the other parameters are defined in Table IV.

IV. NUMERICAL EXPERIMENT

The SPICE-like transient simulator is implemented in MATLAB to consider both NVM and CMOS devices. With the use of the newly developed SPICE-like simulator considering the internal state variables of NVM devices, a number of numeric experiments are conducted for designs of hybrid CMOS and NVM circuits, mainly large-scale memories. Other than the accurate dynamic models of memristor, STT-MTJ, PCM, and CMOS devices, the SPICE-like simulator also contains the basic circuit elements such as BJT, capacitor, resistor, and voltage/current source. All numerical experiments are conducted on the same work station with Intel Core i5 CPU and 8G RAM. The efficiency of the proposed SPICE-like simulator is demonstrated by experiment results from three perspectives: modeling of NVM devices, capability of hybrid simulation with CMOS and NVM devices, and the scalability of for large-scale memory circuits.

A. Verification of Dynamic NVM Device Model With Internal State Variables

1) Memristor Model Verification: In order to consider the slow-down effect for the drift-velocity near the boundary, Joglekar window function [20] can be introduced for this purpose. The window function implemented in our developed simulator and the corresponding \( I-V \) curves under one sine-input are plotted in Fig. 8. The device parameters are: \( D = 10 \text{ nm}, R_{\text{on}} = 200 \Omega, R_{\text{off}} = 3800 \Omega \), the initial memristance \( M = 3790 \Omega, p = 2, \mu = 1 \times 10^{-17} \text{ m}^2/(\text{V.s}) \) and \( E_0 = 1 \text{ MV/cm} \). The dynamic behavior is investigated under the driving voltage of \( V(t) = -0.2 + \sin(200\pi t) \text{ V} \). As shown in Fig. 8, our dynamic model with Joglekar window function can capture the experiment results reported in [15].

Moreover, a Biolek window function [21] is also implemented in our simulator to show the impacts of different dynamic behaviors under different window functions: Biolek window function is asymmetric and Joglekar window function is symmetric. Two memristors with symmetric and asymmetric functions are investigated under sine voltage: \( V(t) = 0.5 \sin(200\pi t) \text{ V} \). As shown in Fig. 9, the asymmetric Biolek window function forces memristance to shift away from the boundary under the sine input. This has resulted in an oscillation around the center value regardless the initial value of memristor. On the other hand, Joglekar window function cannot show this behavior. Nevertheless, the difference between the symmetric dynamic and the asymmetric dynamic models obviously cannot be observed from a static device model.

2) STT-MTJ Model Verification: In order to validate our STT-MTJ model, the device-level simulation results are compared to the experiment verified modeling results from [22] under the same device parameters. The area of STT-MTJ cross-section is \( 130 \times 90 \text{ nm}^2 \), and the thickness of free layer...
is 2 nm. The saturation magnetization is 1000 emu/cm³, and the crystal anisotropy is 200e. The polarization efficiency is 0.57 with tunnel-magneto-resistance (TMR) around 100%. The damping parameter is 0.005. 500 Ω is assigned as the GMR at P state ($R_L$). The voltage-dependent tunneling conductance coefficient for P and AP states are set to 0.1 and 0.65 to fit the TMR voltage relationship. The same STT-MTJ model is used in the later experiments as well for consistency.

Fig. 10 shows the free-layer switching time versus STT-MTJ driving current. Our STT-MTJ model fits well with the results reported from [22]. Moreover, we can observe that the switching time increases very fast when the driving current approaches the critical current. As such, a huge current has to be applied when a very short switching time is required.

Under the constant current driving condition, the dynamic behavior of STT-MTJ device can be observed from Fig. 11, which shows the changes of resistance, voltage, and two internal state variables ($\theta$ and $\phi$) with respect to time. The STT-MTJ is initially at P state which has a smaller GMR ($R_L$). Upon applying a 600-μA driving current, it is switched to AP state in about 10 ns. $\phi$ increases continuously with a very high speed according to the large gyromagnetic ratio. At the same time, $\theta$ starts to deviate from the original value once the current is applied. Its maximum deviation increases exponentially with time before the reversal happens. Under the constant current condition, the voltage changes with the STT-MTJ resistance simultaneously, of which the fluctuation is observable after 5 ns and jumps to 850 Ω at 10 ns. This fluctuation decays very fast after reversal, and then STT-MTJ enters into the other stable state. Note that these dynamic behaviors of resistance fluctuation cannot be observed under the equivalent circuit-based STT-MTJ model in [9].

3) PCM Model Verification: To further validate the PCM model, the device level simulation results are compared to the experiment results shown in [11] under the same device parameters. The crystallization and melt temperature ($T_X$ and $T_m$) are 155 °C and 620 °C, respectively. The crystalline state resistance ($R_{SE1}$) is 10 KΩ and the amorphous state resistance ($R_{RESE1}$) is 1 MΩ. We select the activation energy ($E_a$) to be 2.24 eV for a typical chalcogenide material Ge$_2$Sb$_2$Te$_5$ [19], Avrami exponent ($n$) is 1.5 and the frequency factor is set to 1.2 e7.

Fig. 12 shows the resulting resistance of PCM device after a 300-ns current pulse, of which the amplitude is changed from 0.1 to 1 mA. We can see that our model fits well with the experiment results reported in [11]. Moreover, we can see the allowable current range for a 300-ns current pulse to change the PCM into crystalline state is between 0.3 and 0.6 mA. Out of this range the PCM remains in the amorphous state.

The dynamic responses of internal state variables: temperature and crystalline fraction of active region under SET and RESET operations are illustrated in Fig. 13. We can see that a 0.3-mA current pulse of 400 ns raises the temperature of active region well above the crystallization temperature.
Fig. 12. PCM device simulation: $R-I$ curve, which is consistent to the measured results reported in [11].

Fig. 13. Dynamic responses of internal state variables of PCM device under current driving SET and RESET operations.

and gradually changes PCM from amorphous to crystalline state. Then a 0.65-mA current pulse of 50-ns increases the temperature of active region higher than the melt temperature of $620^\circ C$, and then changes PCM back to amorphous state. Actually, the storage temperature of PCM device is limited by the crystallization temperature. If the PCM memory is placed in the environment higher than the crystallization temperature, all the data stored will be corrupted.

B. Simulation of Memory Circuits of Hybrid CMOS and NVM Devices

1) Memristor Based Crossbar Memory: We first demonstrate the use of dynamic model of memristor for crossbar-based memory circuit as shown in Fig. 14. Both memory and demux circuits are realized by memristors with different threshold voltages, and CMOS buffers are used to generate control signals.

Due to the slow-down effect of drift velocity near the boundary considered by the window function, the simulated access-time for a “Write”-operation is longer than the static model without the consideration of the window function. Recall the internal state variable here is doping-ratio ($w$). The two window functions by Joglekar model and Biolek model are compared with the static model in Table V. Up to 23% increase in rise-time ($t_r$) and 88.5% increase in fall-time ($t_f$) are observed (here rise/fall time is defined as time for the memristance, which can accumulate and eventually leads to an error such as “false-write” state, and hence can significantly affect the reliability for the memory design. To demonstrate this undesired dynamic result, a 4 × 4 crossbar memory is deployed here under a “Write-1”-operation. The driving voltage to the targeted memristor is 3 V while the applied voltages for the remaining memristors are only 1 V. The proposed dynamic model with Biolek’s window function ($p = 7$) is used. Here, we define the “error-free write time” ($t_{efw}$) as the total time required for the first “false-write” to happen, when one non-targeted memristor is unintentionally shifted across its middle resistance. And “error-free write cycle” ($t_{efwc}$) is defined as the

<table>
<thead>
<tr>
<th>Window function</th>
<th>Window function</th>
<th>$p$</th>
<th>Rise time (ns)</th>
<th>Fall time (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Model-1</td>
<td>NA</td>
<td>NA</td>
<td>6.02</td>
<td>4.36</td>
</tr>
<tr>
<td>Model-2</td>
<td>$f(x)=1-</td>
<td>x-a(1)</td>
<td>^2$</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>7</td>
<td>6.08 (1%)</td>
<td>4.85 (11%)</td>
</tr>
<tr>
<td>Model-3</td>
<td>$f(x)=1-(2x-1)^2$</td>
<td>2</td>
<td>7.39 (23%)</td>
<td>7.5 (72%)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>7</td>
<td>6.14 (2%)</td>
<td>6.25 (43%)</td>
</tr>
</tbody>
</table>
TABLE VI

<table>
<thead>
<tr>
<th>D (nm⁻¹)</th>
<th>Rise time (t₀, ns)</th>
<th>Error-free write time (tₑ₀, ns)</th>
<th>Error-free write cycle (tₑ₀/t₀)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1</td>
<td>474</td>
<td>2134</td>
<td>4</td>
</tr>
<tr>
<td>0.15</td>
<td>70.6</td>
<td>786</td>
<td>11</td>
</tr>
<tr>
<td>0.2</td>
<td>11.8</td>
<td>346</td>
<td>29</td>
</tr>
<tr>
<td>0.25</td>
<td>2.1</td>
<td>166</td>
<td>78</td>
</tr>
<tr>
<td>0.3</td>
<td>0.4</td>
<td>83.7</td>
<td>211</td>
</tr>
</tbody>
</table>

Fig. 15. Circuit diagrams of STT-MTJ memory cell: (a) simplified memory cell for write-1; (b) simplified memory cell for write-0; and (c) 16-bit STT-MTJ MRAM with 4 bit-lines and 4 word-lines.

number of write operation allowed in this period. Dynamic modeling parameter \( \frac{1}{D} \) (inverse of film thickness) in (10) is swept from 0.1 to 0.3 nm⁻¹, while \( \mu \) and \( E_{||} \) are kept the same. As shown in Table VI, although the rise time and the error-free write time both reduce with the film thickness, the number of error-free write cycle increases from 4 to 211. A detailed analysis shows a logarithm relationship between error-free write cycle and the inverse of film thickness: \( \frac{1}{D} \). Therefore, in order to increase the reliability, memristors need to have smaller \( D \).

2) STT-MTJ Based Memory: We further investigate the STT-MTJ dynamic behavior in the design of STT-MTJ based nonvolatile memory. A typical hybrid CMOS and STT-MTJ MRAM cell is shown in Fig. 15(a). In the “Write-1”-operation, WL is connected to VDD, and BL and SL are connected to VDD and GND, respectively. In the “Write-0”-operation shown in Fig. 15(b), the polarities of SL and BL line are interchanged. One NMOS is included to simulate the actual operation of STT-MTJ based memory cell. Here we choose VDD to be 1.2 V as a common biasing for 65-nm process for CMOS devices.

The dynamic model of STT-MTJ with NMOS is compared to the static model driving by constant current in the switching time of “write-1” operation. Note that the switching time with static model can also be obtained from (15). From the simulation results shown in Fig. 16, we can see that the switching time obtained by the static model with constant current [8] is over estimated for the change: AP to P, and is also under estimated for the change: P to AP. This is because the actual driving condition of STT-MTJ in NVM application is constant voltage instead of constant current. We can also observe that the actual switching time of “Write-1”-operation is 3 × smaller than that of the “Write-0”-operation. As such, the writing-pulse-width for 0 and 1 is not necessarily to be the same. Moreover, because the voltage is more than 1 V across the STT-MTJ device, the resistance stays at 550 \( \Omega \) after reversal from P to AP, and it will go back to 1000 \( \Omega \) once the applied voltage is removed.

3) PCM Based Memory: We also investigate the design of multilevel memory design based on PCM device similar to [11]. Note that the crystallization ratio increases with the time during SET-operation. As such, the resulting crystallization ratio is different for the pulse width. Therefore, it leads to different resistance levels in the same PCM to represent more than one bit of information. A 3-bit (8-resistance levels) memory design is used in this paper.

A simplified 4 × 4 PCM memory circuit shown in Fig. 17 is implemented in our simulator to demonstrate the multilevel storage with the use of our dynamic PCM device model. The current sources shown are only used for SET-operation. They are applied to drive the PCM devices once the controlling gates are triggered by the incoming pulses. The driving current is 0.3 mA and the different pulse widths selected are 22, 30, 40, 58, 88, 140, and 250 ns for different resistance levels \( R_{17} \) other than \( R_{\text{RESET}} \).

The dynamic responses of crystallization ratio and temperature are shown in Fig. 18. We can see that a longer temperature pulse width pushes crystallization ratio to a higher level, which will result in a lower resistance level of PCM device. Table VII presents the resulting resistance levels for different SET-pulses. Note that \( R_7 \) obtained from a SET-pulse of 250 ns is already very close to the \( R_{\text{SET}} \) value, which means 85% crystallization ratio is sufficient to SET a PCM device and not necessarily to be 100%.

We also implement the \( K^m \) function [11] in our simulator to further compare the dynamic crystallization processes modeled...
Fig. 17. Circuit diagrams of PCM memory cell in the application of multilevel storage.

Fig. 18. Comparison between the dynamic model (JMAK) and $Kt^n$ model in [11] for designs of PCM based memory: crystallization ratio and temperature for multilevel memory storage under SET-operation.

**TABLE VII**

<table>
<thead>
<tr>
<th>Storage Level</th>
<th>Crystallization Ratio (%)</th>
<th>Resistance (kΩ)</th>
<th>Pulse Width (ns)</th>
<th>JMAK (Our dynamic model)</th>
<th>$Kt^n$[11]</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{reset}$</td>
<td>0</td>
<td>1K</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$R_1$</td>
<td>0.98</td>
<td>528</td>
<td>22</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>$R_2$</td>
<td>3.0</td>
<td>259</td>
<td>30</td>
<td>40</td>
<td>40</td>
</tr>
<tr>
<td>$R_3$</td>
<td>6.4</td>
<td>141</td>
<td>40</td>
<td>65</td>
<td>65</td>
</tr>
<tr>
<td>$R_4$</td>
<td>13.9</td>
<td>70.2</td>
<td>58</td>
<td>108</td>
<td>108</td>
</tr>
<tr>
<td>$R_5$</td>
<td>27.8</td>
<td>36.5</td>
<td>88</td>
<td>170</td>
<td>170</td>
</tr>
<tr>
<td>$R_6$</td>
<td>52.1</td>
<td>19.8</td>
<td>140</td>
<td>260</td>
<td>260</td>
</tr>
<tr>
<td>$R_7$</td>
<td>85.2</td>
<td>12.2</td>
<td>250</td>
<td>360</td>
<td>360</td>
</tr>
</tbody>
</table>

by the JMAK function [23] in our model. The crystallization curve is also shown in Fig. 18. Note that $K = 1.25 \times 10^{-4}$ is a fitting parameter and the Avrami exponent $n = 1.5$ is the same as our JMAK model. We can see that the crystallization process of $Kt^n$ function is faster than the JMAK function in the beginning of SET-pulse-width (25 ns) and becomes slower afterwards. As such, the $Kt^n$ function that ignores the dynamic effect overestimates the dynamic effect, and has different resistance levels ($R_{2-7}$) as shown in Table VII. This further affects the PCM memory design specifications.

![Fig. 19. CPU runtime comparison between our method and equivalent circuit-based model [10] for memristor.](image)

**C. Runtime Scalability Comparison**

Finally, we evaluate the simulation efficiency of our developed simulator for NVM devices with dynamic models and internal state variable. The runtime scalability study is performed on size (bit) scaled memory designs with transient simulation of 10 time steps. Note that the equivalent circuits of memristor [10], STT-MTJ [9] and PCM [11] are also built in our SPICE-like simulator.

The CPU runtime comparisons are shown in Figs. 19, 20 and 21 for memristor, STT-MTJ, and PCM device, respectively. For a 4-bit memory simulation, the CPU time of our internal state variable based simulation is only half of equivalent circuit-based approach for all three devices. Note that the time reduction ratio obtained from experiment largely depends on the complexity of equivalent circuit and the memory circuit under study. With the increasing size of memory, the overall netlist complexity of equivalent circuit approach grows much faster than our approach. As such, this time reduction keeps increasing with the enlarged size of memory. For a 512-bit memory, compared to the equivalent circuit based simulation, the CPU time of our internal state variable-based simulation is 22 times smaller for memristor, 20 times smaller for STT-MTJ device, and 69 times smaller for PCM device.

**V. CONCLUSION**

In order to consider the nonlinear dynamic behavior of non-volatile memory (NVM) devices at nano-scale, internal state variables such as doping-ratio, magnetization orientation and crystallization ratio, active region temperature have been identified for memristor, STT-MTJ, and PCM devices, respectively. The corresponding modified nodal analysis considering internal state variables is developed inside one SPICE-like simulator to stamp all three NVM devices compactly together with CMOS devices. As such, one can perform efficient transient simulation for the design of large-scale memory circuits of hybrid CMOS and NVM devices. The experiment results show that our proposed method can accurately and efficiently simulate hybrid NVM circuits with up to 69 times CPU runtime speedup, when compared to the approaches using equivalent circuit models.
In addition, the nonlinear dynamic behaviors of NVM devices have shown significant impact on the performance.

**APPENDIX A**

**DYNAMIC EFFECT OF MEMRISTOR**

To fully describe the dynamic behavior of memristor, we need to consider several nonlinear effects of memristive system including: charge-induced-drifting effect, slow-down effect and strong-electric-field effect [15], [20], [21], [24].

As we have mentioned earlier, the basic operation principle of memristor is the charge-induced-shifting of doping level, which means the drifting velocity of memristor is a function of applied current. Together with the relationship between doping-ratio and memductance [15], (7) has the following piecewise linear form:

\[
\frac{dv(t)}{dt} = \begin{cases} 
\mu v(t), & \text{mode 1: normal operation} \\
0, & \text{mode 2: } w = 0 \text{ or } 1 \\
0, & \text{mode 3: } |v| < V_{th} 
\end{cases}
\]

where \( V_{th} \) is the threshold voltage for memory operations.

Moreover, slow-down effect of memristor is illustrated in Fig. 2(a), when \( w \) is approaching the boundaries where \( w = 0 \) or 1, the drift velocity drops quickly and is no longer a linear with the current applied [25]. This nonlinear dynamic effect can be characterized by either of the following window functions [20], [21]:

\[
P'(w) = 1 - (2w - 1)^{2p} \tag{11}
\]

\[
P'(w) = 1 - \left[w - u(-i(t))\right]^{2p} \tag{12}
\]

where \( p \in [0, 10] \) is a fitting parameter and \( u(-i(t)) \) equals to 1 when \( i(t) \) is positive, and equals to 0 when \( i(t) \) is negative. Note that the (11) is a symmetric window function, called Joglekar model [20]; while (12) is an asymmetric window function, called Biolek model [21].

In addition, strong-electric-field effect stands for the exponentially increase in the drift velocity under a strong electrical filed condition (>1 MV/cm). It usually happens in the nanoscale devices such as newly fabricated memristor [26] at scale of 20 nm. As illustrated in Fig. 2(b), the phenomenon can be approximated by a \( \sin \) function [24]:

\[
\frac{dv(t)}{dt} = \frac{\mu E_0}{D} \sin h \left( \frac{E}{E_0} \right) \tag{13}
\]

where \( E = (v(t))/(D) \) is the applied field strength, and definitions of remaining variables are shown in Table II.

**APPENDIX B**

**DYNAMIC EFFECT OF STT-MTJ**

Memory cell-based dynamic modeling with 1T1J structure (one transistor and one STT-MTJ) is proposed in [27]. However, to further make the STT-MTJ model usable at arbitrary circuit environment, we need to find the dynamic model of STT-MTJ separately. In order to model the operation mechanism of STT-MTJ device accurately, we need to look into two dominant dynamic effects: tunneling effect [28], and spin-transfer-torque effect [29].

Tunneling effect of STT-MTJ can be understood as a parabolic relationship between the junction conductance and the applied voltage [28]. This relationship is illustrated by line segments “ab” and “cd” in Fig. 4(b), which represents the change of normalized resistances with voltage at P and AP states, respectively. Tunneling effect normally becomes dominant when the applied voltage is relatively small such that it will not trigger the STT-MTJ to change state. This relation can be approximated by

\[
R_L(V) = \frac{R_L(V - 0)}{1 + k_a V^2} \quad R_H(V) = \frac{R_H(V - 0)}{1 + k_b V^2} \tag{14}
\]

where \( k_a \) and \( k_b \) are voltage-dependent coefficients for parallel (P) state and anti-parallel (AP) state, respectively.

Moreover, spin-transfer-torque effect becomes dominant when the current flowing through the STT-MTJ is larger than the critical value \( I_c \). This relationship is illustrated by line segments “bc” and “da” in Fig. 4(b). When the current at the junction is higher than the critical value \( I_c \), the resistance
will switch between \( R_H \) and \( R_L \) regions. This process is called *magnetization reversal*. However, magnetization reversal is not an instantaneous process. The switching time required \( (T_s) \) for magnetization reversal decreases exponentially with the current applied \( (I_c) \) \[8\]

\[ T_s = \tau_0 \exp \left( \Delta \left( 1 - \frac{I_0}{I_c} \right) \right) \]

where \( I_c = \frac{(2eA\alpha M_s)(H + I_H + 2\pi M_s)}{(\eta_0)} \), \( \tau_0 \) is the switching time at \( I_0 = I_c \), and the definitions of remaining variables are in Table III.

Note that \( \tau \) from (15) is the minimum pulse width requirement for certain \( I_0 \). For a particular write-operation in STT-MTJ device based memory, one must make sure that a constant current larger than \( I_c \) is applied within a period of \( T_s \).

A better understanding of \( T_s \) is important for modeling STT-MTJ devices. This requires the analysis for the dynamic behavior of STT-MTJ device under arbitrary driving condition. The Landau–Lifshitz–Gilbert equation (LLG) \[29\] is deployed for this purpose:

\[ \frac{dM}{dt} = -\gamma M \times \left[ H + \chi(M \times p) \right] + A \left( M \times \frac{dM}{dt} \right) \] \hspace{1cm} (16)

where \( \gamma \) is the pre-factor of the spin transfer term, \( p \) is the hard axis unit vector, and the definitions of remaining variables are shown in Table III.

The solution of (16) can be interpreted as the change of the normalized magnetization \( (M) \) of free layer over time. \( M \) can be expressed in spherical coordinates with variables \( \phi \) and \( \beta \) as shown in Fig. 22. \( \theta \) and \( \phi \) are the azimuthal angles of \( M \) in \( x - y \) plane and \( y - z \) plane, respectively, and \( \beta \) is the elevation angle of \( M \) from \( x - y \) plane. Note that for a very thin free layer, the value of \( \beta \) is rather small and will not affect the modeling of STT-MTJ device. So only \( \theta \) and \( \phi \) are associated with the state of STT-MTJ devices to describe the normalized magnetization direction. Note that \( \theta \) and \( \phi \) are calculated by \[29\]

\[ \theta = \theta_0 \exp \left( \frac{-t}{t_0} \right) \cdot \cos(\phi); \]

\[ \omega = \frac{d\phi}{dt} - k_e \sqrt{k_d - (\chi_{av1} \cdot k_t)^2} \]

where \( \theta_0 \) is the initial value of \( \theta \), which is slightly tilted from P or AP directions; \( t_0 \) is the precession time constant; and \( \omega \) is the angular speed of \( \phi \); \( k_e = \gamma_0 \cdot \gamma_M \) is product of gyromagnetic ratio and saturation magnetization; \( k_d \approx (H_K)/(M_s) \) is a function of anisotropy and applied field; \( \chi_{av1} \) is the critical pre-factor of spin transfer term, which is around half of the damping constant \( A \); \( k_t \) is the ratio between pre-factor of the spin transfer term and driving current. Definitions of remaining variables are shown in Table III.

**APPENDIX C**

**DYNAMIC EFFECT OF PCM**

Two dominant effects have to be considered to describe the dynamic behavior of PCM effects: thermal effect and crystallization kinetics \[23\].

Thermal effect can be subdivided into two different processes: heat generation and heat dissipation. The heat generation power is mainly contributed by Joule heat, which can be represented as

\[ W_j = I_M \times V_M \] \hspace{1cm} (19)

where \( I_M \) and \( V_M \) are current and voltage of one PCM device. The Joule heat generated will be dissipated through the surrounding media of active region. The heat dissipation power can be simplified as

\[ W_d = k_e \cdot \nabla T \] \hspace{1cm} (20)

where \( k_e \) is the effective thermal conductivity of surrounding material and \( \nabla T \) is the temperature gradient between active region and ambient environment. As such, the temperature of active region \( (T_M) \) will increase when \( W_j > W_d \); and will decrease when \( W_j < W_d \). This state of thermal effect can be represented by an integration function of the generated net-heat:

\[ T_M = \int \frac{W_j - W_d}{C \cdot V} \, dt \] \hspace{1cm} (21)

where \( C \) is the specific thermal capacity and \( V \) is the volume of active region.

Moreover, crystallization kinetics is actuated when the temperature of active region is above crystallization temperature \( (T_X) \). Such a state change can be described by the Johnson–Mehl–Avrami–Kolmogorov (JMAK) equations \[23\]

\[ C_X = 1 - \exp(-K t^n) \]

\[ K = K_0 \exp \left( \frac{E_a}{K B T_M} \right) \]

where \( C_X \) is the crystallization ratio, \( n \in [1, 4] \) is the Avrami exponent, and \( K \) is the effective crystallization rate determined by the temperature of active region \( (T_M) \). The definitions of remaining parameters are given in Table IV.

When the temperature of active region is higher than \( T_{wa} \), the chalcogenide material melts in the active region, and \( C_X \) is reset to zero. As such, the total active region resistance of PCM device \( (R_M) \) can be approximated as a function of \( C_X \):

\[ R_M = \begin{cases} \frac{R_{SEL}}{C_X} + \frac{R_{REL}}{C_X} \quad \text{when } V_M < V_{th} \\ \frac{R_{B}}{C_X} \quad \text{when } V_M \geq V_{th} \end{cases} \]

where \( R_{SEL} \) and \( R_{REL} \) are the PCM device resistance at crystalline and amorphous state, respectively. \( V_{th} \) is the
breakdown threshold voltage and $R_B$ is the break-down-state resistance.

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