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Low-voltage organic ferroelectric field effect transistors using Langmuir–Schaefer films of poly(vinylidene fluoride-trifluoroethylene)

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ABSTRACT

Langmuir–Schaefer transfer was used to fabricate ultrathin films of ferroelectric copolymer, poly(vinylidene fluoride-trifluoroethylene) (70–30 mol%), for non-volatile memory application at low operating voltage. Increasing the number of transferred monolayers up to 10 led to improved film crystallinity in the “in-plane” direction, which reduced surface roughness of the semicrystalline film. Treatment of the substrate surface by plasma results in different film coverage which was subsequently found to be governed by interaction of the deposited film and surface condition. Localized ferroelectric switching was substantially attained using piezo-force tip at 10 V on 10-monolayer films. Integrating this film as a dielectric layer into organic capacitor and field effect transistor yields a reasonably

good leakage current ($<10^{-7}$ A/cm²) with hysteresis in capacitance and drain current with ON/OFF ratio of 10^3 for organic ferroelectric memory application at significantly reduced operating voltage of |15| V.

Keywords:

Langmuir–Schaefer film; P(VDF-TrFE); Non-volatile memory

1. Introduction

Polyvinylidene fluoride (PVDF) and copolymer with trifluoroethylene P(VDF-TrFE) are well-known for their ferroelectric properties in crystalline forms [1,2]. The polymers have a vast application in sensors, actuators [3,4], and non-volatile memory [5–8]. These applications usually require a thin film fabricated by spin-coating or mechanical pressing. Crystallization of the polymer chains can be resulted from either post-process annealing or recrystallization from melting. Recently, a new method of forming P(VDF-TrFE) copolymer films has been reported using Langmuir–Schaefer transfer mechanism [9,10]. The method includes two main steps – first, compressing to form monolayer (ML) of compact polymer chains at the air-liquid interface and second, transferring the monolayer onto a substrate surface. Film thickness can be controlled by the number of transfers at a certain compressing pressure [11]. Film crystallinity can be enhanced by annealing at temperatures below melting point similar to those of spin-coated films [12]. In addition, Langmuir–Schaefer (LS) method has a potential for realizing a polymer monolayer by aligning and packing its molecular chains without anneal crystallization.

Forming and transferring the LS-films of P(VDF-TrFE) copolymer have been intensively performed by Nalwa [9]. Different properties and

characteristic of monolayer P(VDF-TrFE) can be observed including ferroelectricity, optical and energy band etc., as well as the proposed intrinsic switching polarization [9]. While Ducharme et al. have advocated for the intrinsic switching mechanism based on both experimental data and theoretical prediction [9], some other researchers have been expressing concerns regarding to the theoretical conditions of the data interpretation. Recent experimental works by Kliem et al. revealed that the switching process below a certain critical thickness could not be sufficiently explained by either intrinsic or extrinsic model alone [13]. Especially, Naber et al. have been able to obtain the experimental evidence of ferroelectric switching with bulk characteristics for ultrathin films with thickness ranging from 3 to 10 nm [14]. They have attributed this observation to the improved surface interfacing between the metal electrodes and the ultrathin ferroelectric polymer film. The intrinsic switching mechanism in the PVDF nanostructures and ultrathin films is beyond the scope of this report. However, it can be seen that various important properties of ferroelectric materials remain to be explored in spite of the tremendous efforts and achievements have been obtained in the field.

The application of LS-transfer P(VDF-TrFE) for non-volatile memory using hybrid device with Si-technology has been shown but limited to rather thick film of 100 ML [10]. A unique feature of the LS-transfer film is being strongly governed by the interfacial interaction with substrate that leads to formation of different nanostructures by simple annealing process [15]. It has been well postulated that the nucleation in ferroelectrics substantially occurs at defects or crystal boundaries. For the mesa nanostructures or ultrathin films, the domain-wall motion is in the film plane due to the highly anisotropic dimensions. It hence allows

more precise control of nucleation locations and domain-wall motion direction in the switching process. With the lateral size in the range of less than 200 nm, a group of these separately and accurately positioned nanostructures can serve as an equivalent memory element (1 bit) that can improve the storage density as well as reduce cross-talk noise between bits. These understandings are potentially useful for memory application in terms of enhanced device density and performance [10]. To date, demonstration of non-volatile memory behavior of thin LS-transfer films (<100 ML) has been lacking and the memory functionality of the ultrathin P(VDF-TrFE) is not fully explored. Furthermore, realization of organic ferroelectric field effect transistors (FeFET) with LS-transfer film has not yet been reported.

In this paper, we investigate the crystallization of the polymers upon annealing in the paraelectric phase, as a function of the number of transferred layers. We attained localized area switching using piezo-force microscopy and demonstrate a low voltage ferroelectric memory (<15 V) using 10 ML of the LS-transfer P(VDF-TrFE) film as dielectric layer in capacitors and ferroelectric field effect transistors. The electrical behavior and memory functionality is correlated to polarization properties of the LS-transfer films.

2. Experimental

P(VDF-TrFE) (70–30 mol%) was purchased from Solvay and used without purification. Copolymer pellets were dissolved in methyl ethyl ketone (MEK) at concentration of 0.1 mg/cc. The solution was then filtered by using 0.2 μm pore-size Teflon filter and promptly used for deposition to maintain a consistent concentration. N-type Silicon wafer was used as

transfer substrates. The wafers were cleaned with Piranha solution ($1\text{H}_2\text{O}_2:2\text{H}_2\text{SO}_4$), SC2 solution ($1\text{NH}_4\text{OH}:1\text{HCl}:10\text{H}_2\text{O}$), followed by acetone, methanol and DI water and blow-dried by N_2 gas. Plasma treatment was done on cleaned substrates with ambient medium for 2 min.

LS-transfer film fabrication was done using Langmuir KSV5000 trough. Ultra-purified water with resistivity of $18.2\text{ M}\Omega\text{ cm}$ was used as subphase medium. The copolymer solution was manually spread onto the subphase surface between the two automatically moving barriers with surface pressure measured by a platinum Wilhelmy plate. The monolayers were manually transferred onto substrates horizontally at $25\text{ }^\circ\text{C}$ and surface pressure of 5 mN/m . All transferred samples were then annealed in the ambient at $120\text{ }^\circ\text{C}$ for 1 h using a slow ramping oven ($1\text{ }^\circ\text{C/min}$). Film crystallinity was determined by Rigaku X-ray diffractometer (XRD) (40 KV , 30 mA) with an incident angle of 0.5° and step of 0.02 . The surface morphology of all layers was characterized by atomic force microscopy (AFM) (digital instruments) in tapping mode using nonconductive tip.

Polarization switching of the transferred films was observed by piezo-force microscopy (PFM) with conductive Si tip in contact mode. The closed circuit of sample and PFM equipment was made through the contact from the conductive tip to the LS-film surface and the back of the Si-wafer substrate using silver paste to reduce contact resistance. The surface morphology was first scanned with $10 \times 10\text{ }\mu\text{m}^2$ dimensions. Next a voltage of $+10\text{ V}$ was applied to an area of $6 \times 6\text{ }\mu\text{m}^2$ and a reversed voltage of -10 V was lastly applied to area of $2 \times 2\text{ }\mu\text{m}^2$ as shown in Fig. 2. The metal-ferroelectric-semiconductor (M-F-S) capacitor devices were fabricated by thermal evaporation of gold (99.9%

purity) through a shadow mask (diameter of 300 μm) onto annealed film samples. The leakage current was measured by Keithley 4200 analyzer and capacitance data was obtained by using HP4284 LCR meter (AC signal of 50 mV and 1 kHz). Ferroelectric field effect transistor (FeFET) was fabricated using Si-wafer with 5 nm thick thermal oxide. The transistor was formed by evaporation of pentacene on top of the transferred P(VDF-TrFE) layers in vacuum (5×10^{-7} torr) at 1–2 $\text{\AA}/\text{s}$ rate. It was then followed by evaporation of gold electrodes for source and drain formation using shadow mask. The transistor operation was then characterized by the Keithley analyzer in dark vacuum ambient.

3. Results and discussion

To examine the formation of continuous thin film by LS-transfer method, multiple monolayers were transferred onto cleaned Si-wafer followed by annealing as described. Fig. 1 presents the surface morphology and crystalline structure of films with thickness from 2 to 10 ML. After annealing, it can be seen that nano-mesas and nanowells were formed for 2 and 6 ML thick film, respectively, as well as fully covered film for 10 ML thick sample. Final thickness of the nano-mesa and nanowell samples is below 20 nm while that of the 10 ML sample is in the range of 20 ± 2 nm as determined by AFM line-profiling. Both the nanostructure formations and dimensions are in agreement with the previously reported data (1.8 nm per mono-layer) especially in the case of fully covered film of 10 ML layer [16]. The small variation in thickness suggests the crystallization of P(VDF-TrFE) copolymer occurred in a planar manner with crystallinity increasing with more transferred layers. While the 6 ML-film appears with vertical holes through the film thickness, no specific grain formation is observed on the covered regions

by the copolymer. On the other hand, grain formation can be seen on the fully covered 10 ML film. The film surface mainly consists of small and round-shaped grains, which results in roughness value (RMS) less than 9 nm. Besides, occasional appearance of rod-like crystals is also observed as shown in Fig. 1c. At the locations of the rod-like grain, the vertical dimension can eventually reach up to 50 nm indicating the crystallization propagates along the normal direction to the film only after the substrate surface had been fully covered. The rod-like grains with polymer lamellas packing along the grain direction appears as vertical walls which intercept each others leading to rough topography and deep valleys usually found on thicker film fabricated by spin-coating [17]. Formation of the 10 ML thin film (10 ML) with limited rod-like grain and good crystallinity (Fig. 1) is anticipated to improve the quality of multilayer ferroelectric memory device.

The XRD data (Fig. 1d) of 2, 6 and 10 ML samples show that both ferroelectric and paraelectric phases coexist [1,2]. Previous report [18] suggested that formation of nanostructures had only taken place in the copolymer paraelectric phase. The observation of ferroelectric phase here is hence believed to be due to the slow cooling process after annealing that resulted in paraelectric–ferroelectric phase transition even in the nanostructures. Measurement to confirm polarization properties was hence done by PFM method on all the samples shown in Fig. 1. It was found that only fully covered sample with 10 ML transferred possessed switchable regions under the tip bias application while it was unable to capture any responsive signals from samples with nanostructures (2 and 6 ML). We attribute this to the limitation of applied voltage in the PFM system (maximum applied voltage of $|10|$ V) as compared to the much higher value of intrinsic coercive field (~ 0.5 GV/m) which has been

estimated for ultrathin (<15 nm) Langmuir–Blodgett film [19]. Polarization switching examined in a 10-ML sample on Si-wafer substrate by the d_{33} coefficient an phase images are presented in Fig. 2. The experiment was performed in two steps – first, $6 \times 6 \mu\text{m}^2$ (dotted box) scan with +10 V that registered “down” dipoles (point towards substrate) appearing as dark contrast, and then $2 \times 2 \mu\text{m}^2$ scan (dashed box) that reversed the polarization to “up” dipoles (pointing away from substrate) appears as different contrast in Fig. 2b. The bright contrast in the dashed box of Fig. 2a clearly indicates the strong dipolar response which could only be resulted from the orientation switching as compared to the outer areas where polarization was not disturbed. The stable existence of the switched region ($2 \times 2 \mu\text{m}^2$ box) after continuous scanning enables the storing of information in an ultrathin film device without the adverse effects by depolarization.

Non-volatile memory behavior was studied using M-F-S device with 10 ML thick P(VDF-TrFE) film as a dielectric layer. Fig. 3a shows the leakage current profile which is reasonably low (less than 10^{-7} A/cm^2) for device application with the inset showing a typical diode behavior. It can be seen the current is asymmetric across the vertical axis but has the minimum value at 0 V. The asymmetric shape of the current curve is believed to be caused by different barrier heights at P(VDF-TrFE)/Au and P(VDF-TrFE)/Si interfaces. With potential applied at the bottom electrode to the silicon substrate, higher current obtained by positive biases means the apparent barrier height of charge injection at the top electrode (Au) is lower than that at bottom one (Si). The minimum current at 0 V possibly indicates the absence of detrapping current by charges existing near the interfacial regions. The memory function is hence mainly resulted from the switching polarization of the P(VDF-TrFE) dipoles as explained by the capacitance hysteresis below.

Fig. 3b presents the capacitance hysteresis data obtained by different sweeping voltages with the first curve (-5 V to $+2\text{ V}$) as reference curve. As voltage was swept in the reversed direction ($+2\text{ V}$ to -5 V , dash curve), a capacitance hysteresis was obtained with a shift in flat-band voltage of 0.7 V to the negative potential. This can be explained from the direction of dipole vectors. The positive bias ($+2\text{ V}$) at the top metal electrode caused the dipole pointing down towards the Si substrate and led to accumulation in Si. As the voltage was swept to negative bias (-5 V), the field across the device must overcome the dipolar coercive field to revert the dipole direction. As a result the charges were accumulated in the Si until coercive field was reached and led to depletion as displayed in the insets of Fig. 3b. The charge accumulation and depletion in the semiconductor can be treated as ON and OFF state, respectively, for the non-volatile memory. An estimation of the switching field for this device including voltage of $|1|\text{ V}$ over thickness of 18 nm yields a value of $|56|\text{ MV/m}$ similar to previous report [2] for spin-coated films. Furthermore, Fig. 3b also displays variability of flat-band voltage shift or memory window of the device with the application of different voltage amplitudes. When the “writing” voltage was increased to $+4\text{ V}$, the voltage shift could be extended up to 1.3 V (dot curve). To bring the device back to the original state, an “erasing” voltage was applied at -6 V (dash-dot curve). To read the data in the device, a small “reading” voltage should be used e.g. -0.5 V without destroying or reversing the polarization state, which will result in a capacitance difference of up to 40 pF for $+4\text{ V}$ “writing” voltage. Hence this proves the versatility and applicability of thin ferroelectric polymer for low voltage non-volatile memory application.

It can be seen that the accumulation in the M-F-S device is unstable

which coincides with the high leakage current in the device (Fig. 3). In order to improve the device stability during accumulation for field effect transistor, the semiconducting layer of Si is replaced with pentacene which is an organic p-type semiconductor with lower charge carrier concentration ($\sim 3 \times 10^{17} \text{ cm}^{-3}$ [20]) while the n-type Si-wafer serves as an electrode. Surface morphology of the evaporated pentacene layer (50 nm thick) on spin-coated and LS-transfer (10 ML) films are shown for comparison in Fig. 4. The surface roughness of the spin-coated P(VDF-TrFE) film is about 17–20 nm as previously reported [6]. For the 10-ML LS-transfer film, pre-scans of surface morphology by AFM were performed to select regions with minimal appearance of the rod-crystallite. As a result, the effective surface roughness of the LS-film was maintained below 10 nm. The average size of pentacene grains is found from the AFM profile to be around 100 nm for both types of P(VDF-TrFE) films. However the pentacene grain-growth is seen to follow the morphology of the rod-like grains on the spin-coated film (Fig. 4c), which limits the intergrain connection in the thin (~ 50 nm) semiconductor layer. This resulted in weak semiconducting behavior of the pentacene film and negligible transistor device characteristics. In the contrary, pentacene grains on the LS-transfer film (Fig. 4d) are generally in circular shape and unaffected by the underneath surface morphology. The average small grain size is probably due to the low surface energy of the P(VDF-TrFE) copolymer [21,22].

The electrical characteristics (I_D-V_D , I_D-V_G) of the FeFET device fabricated on the LS-transfer film are shown in Fig. 5. Both of drain and gate voltages were applied in ascending order for I_D-V_D . The mobility is calculated in the saturation regime from Fig. 5a yielding value of $0.003 \text{ cm}^2/\text{Vs}$ for device with an effective capacitance of $3.1 \times 10^{-7} \text{ F/cm}^2$ and

channel length and width of 75 and 4000 μm , respectively. The value of mobility is likely affected by the smaller grain size [23] and the lower dielectric constant of SiO_2 ($\kappa = 3.9$ as compared to $\kappa = 13$ of P(VDF-TrFE)) in the composite insulating layer. The transfer characteristic shows hysteresis in drain current (ON/ OFF ratio around 2×10^3 at zero gate bias) which follows the polarization switching of the copolymer dipoles and is in agreement with previously reported devices fabricated by spin-coating P(VDF-TrFE) film [5,6]. As switching current peaks seen from the inset of Fig. 5b are around $V_G = |5| \text{ V}$, a sweeping gate voltage of $|15| \text{ V}$ is hence sufficient to induce saturated polarization in the ferroelectric layer. One of the clear advantages is hence the saturating of polarization at low bias ($\sim|15| \text{ V}$) which results in low voltage application device.

The formation of nanostructures from the first few monolayers is governed by both of the elastic and surface energy density [18]. We attempted to improve the contact formation between the LS-transferred film and the substrate surface by briefly subjecting the Si surface to ambient plasma for 2 min. The obtained result was a more hydrophilic surface (with smaller contact angle of 7.72° as compared to 25.27° of normally cleaned Si-wafer). The higher surface energy led to pattern coarsening to minimize the interface area during annealing in paraelectric phase [18]. Examination by AFM of annealed 1 ML sample on both types of treated surfaces shows different nano-structure formation. While separating nano-islands were seen on the normally cleaned sample, percolating nano-mesa with larger coverage of substrate surface was obtained for the plasma-modified sample as previously described [15]. FeFET device with 10 ML film transferred onto the plasma-modified surface shows similar drain current hysteresis and carrier

mobility in the semiconductor channel as the ones on normally cleaned substrate (Fig 5b). However the ON/OFF ratio is reduced to 350 due to lower current retention at zero gate bias. It is possibly resulted from the defects generated during plasma-modification. The plasma ion bombardment partially removed the topmost oxygen-bonding layer and left unsaturated bonds on the Si surface that makes it more susceptible to trapping of mobile charges during the transfer of first few layers. The existence of trapped charges between the SiO₂ and the P(VDF-TrFE) layer subsequently caused the non-switching polarization which induced higher drain current during strong accumulation but did not retain the current as gate voltage drop to 0 V [6]. It is hence required further improvement in the engineering of interface between substrate and the transferred films to obtain denser dielectric layer of ultrathin thickness.

4. Conclusion

We have demonstrated the fabrication of good quality ultrathin Langmuir–Schaefer films for the application in non-volatile memory device. Study of crystallinity evolution and surface morphology in the process of film formation indicates planar crystallization occurring in the LS-film with transferring of up to 10 ML. The good coverage of this film with high crystallinity of small flat grains allows the demonstration of non-volatile memory devices. The memory behavior was presented in MFS capacitor as well as FET with the retention by the dipolar polarization. Different states of data storing and erasing was demonstrated with operation voltages less than 15 V. One of the detrimental defects has been identified as mobile charge trapping at the interface that worsens the current retention when the substrate is plasma treated to improve the LS-film coverage. This hence prompt for more attention in

optimizing the crystallization of the LS-film and the engineering of the surface morphology. In spite of those shortcomings, the LS-transfer method offers the advantages of simple processing conditions and small volume of consumed material. The ferroelectric LS-film is proven to be versatile and applicable for device application that requires low operation voltages.

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List of Figures

- Fig. 1 Changes in surface morphology and crystallinity of the LS-transfer P(VDF-TrFE) films as thicknesses were increased (a), (b) and (c) 2, 6, and 10 ML, (d) XRD data of all the three films.
- Fig. 2 PFM images of 10 ML LS-transfer sample (a) d_{33} coefficient image and (b) phase image. The dashed and dotted boxes in (a) indicate the scanning areas of different voltage application and the contrast difference in (a) and (b) represents the polarization switching.
- Fig. 3 Electrical characteristic of 10 ML M-F-S capacitor device (a) leakage current J - V curve. The electrode area is $7.07 \times 10^{-4} \text{ cm}^2$. The inset shows the linear plot. (b) Capacitance hysteresis C - V curves. Two insets present the device structure with hysteresis mechanism.
- Fig. 4 Comparison of surface morphology of (a) spin-coated film (200 nm thick) and (b) 10 ML (~20 nm thick) LS-transfer film. Morphology of pentacene layers grown on both films are shown in (c) and (d), respectively.
- Fig. 5 Device characteristics of pentacene transistors with 10 ML transferred dielectric layer on normally cleaned and plasma-modified Si substrates (a) I_D - V_D (device on normally cleaned Si substrate). (b) I_D - V_G measured at $V_D = -5 \text{ V}$. The inset shows the gate current I_G - V_G of device on normally cleaned Si substrate.

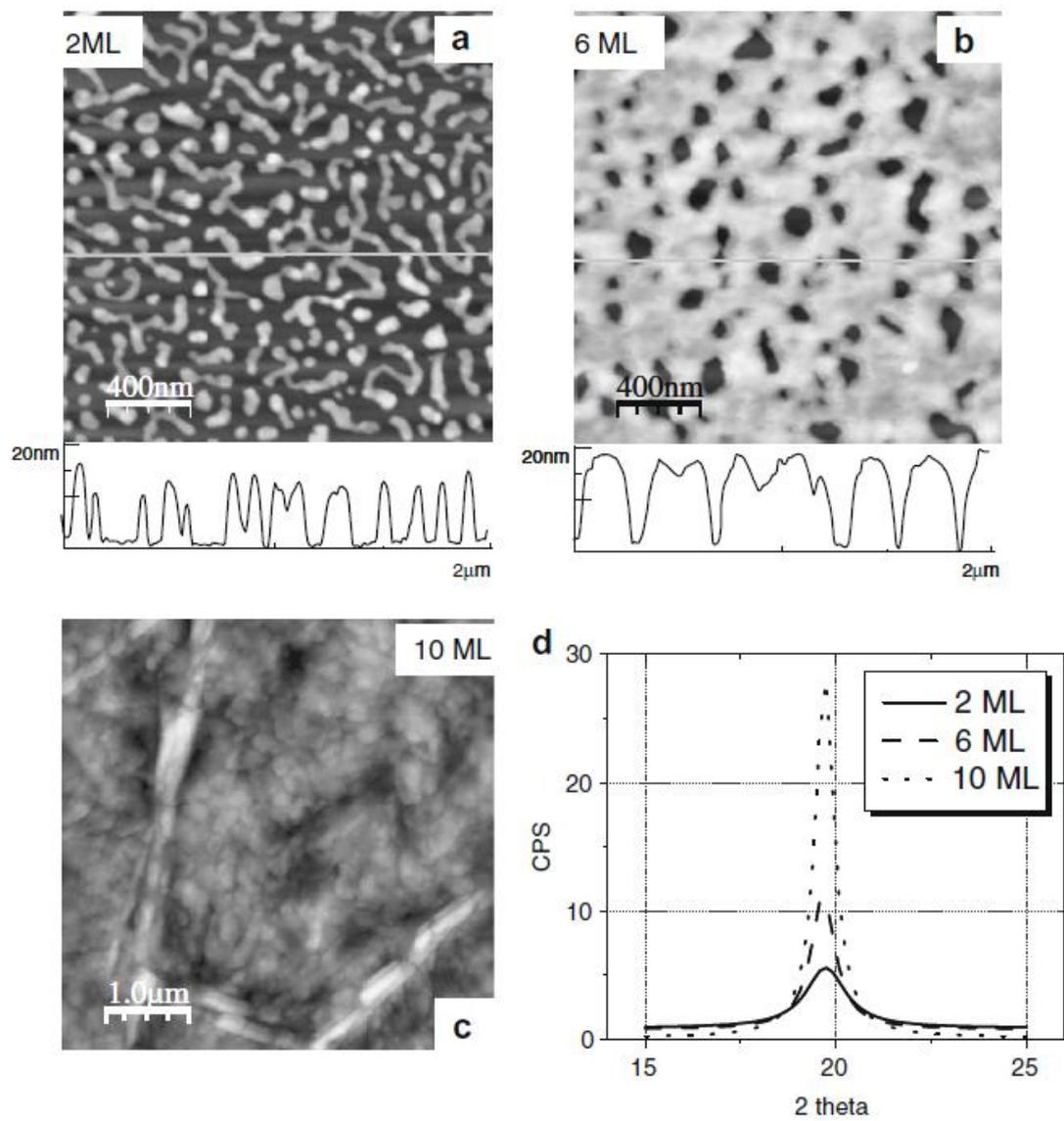


Fig. 1

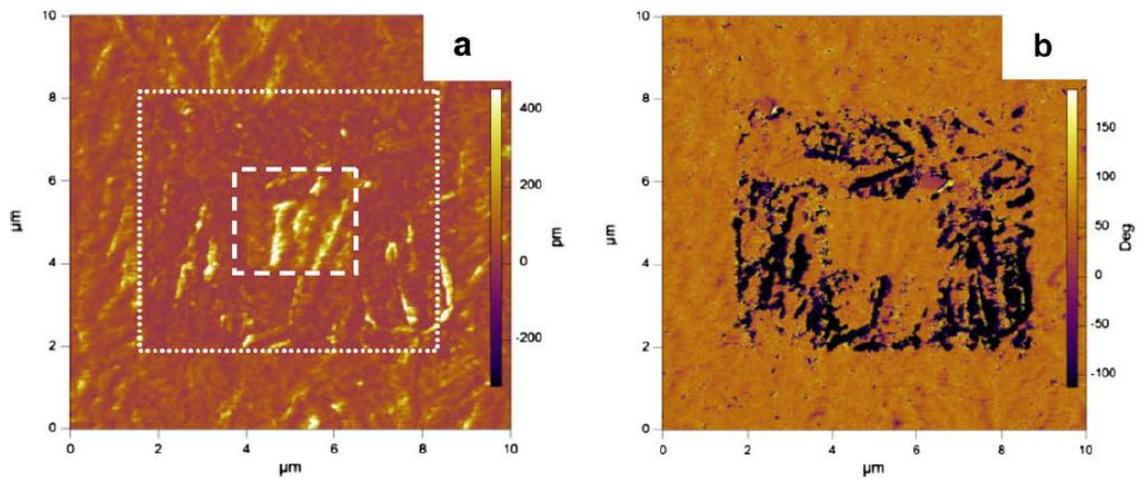


Fig. 2

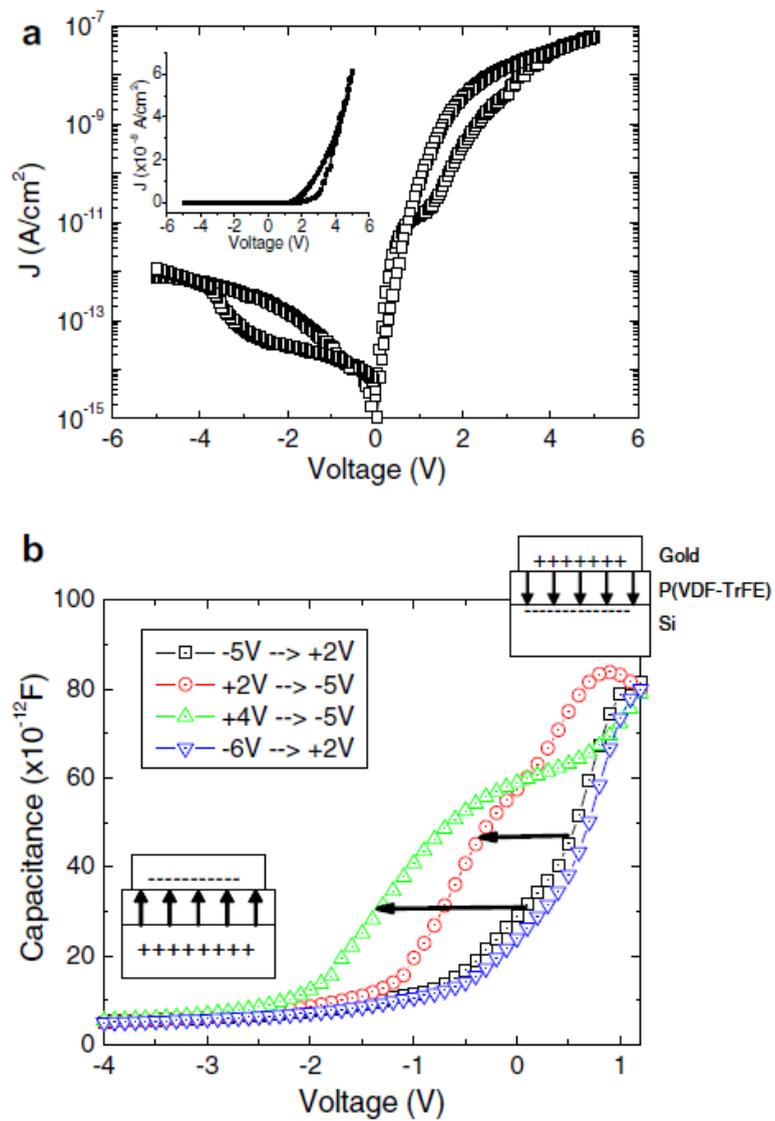


Fig. 3

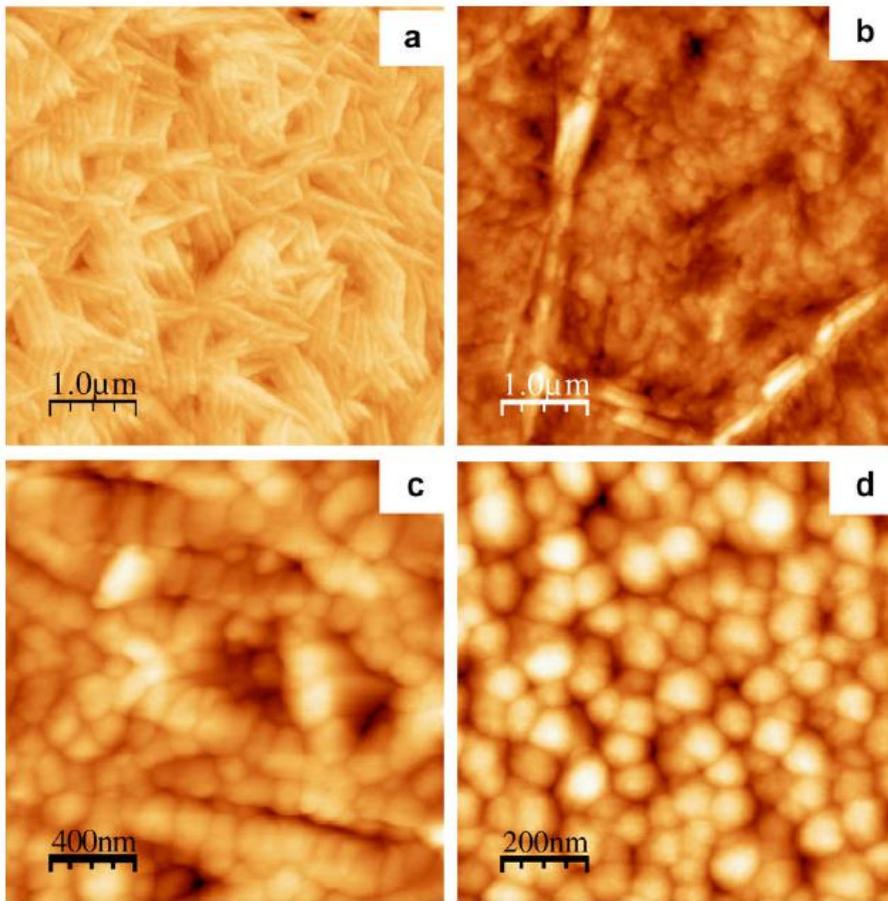


Fig. 4

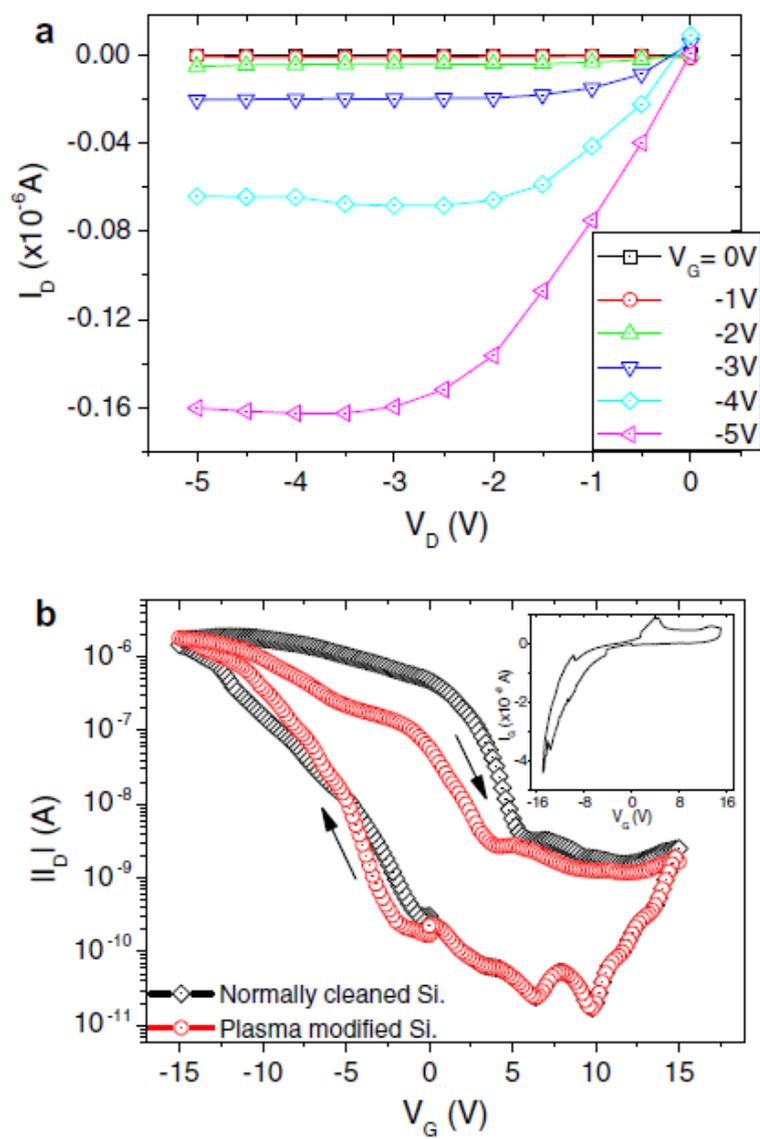


Fig. 5