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Resistive switching in a GaO$_x$-NiO$_x$ p-n heterojunction

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We report a unidirectional bipolar resistive switching in an n-type GaO$_x$/p-type NiO$_x$ heterojunction fabricated by magnetron sputtering at room temperature. The resistive switching behavior coincides with the switching between Ohmic conduction (low resistance) and rectifying behavior (high resistance) of the heterojunction diode. Under external electric field, electromigrated intrinsic defects, such as oxygen vacancies and oxygen ions, accumulate at the pn junction interface and modify the interface barrier, forming or rupturing the filamentary paths between n-GaO$_x$ and p-NiO$_x$, leading to the switching between Ohmic and diode characteristics of the device. The device shows good endurance, retention performance, and scaling capability, signaling the potential of a diode-structured resistive switching device for non-volatile memory applications. © 2012 American Institute of Physics.

Resistive switching random access memory (RRAM) has attracted much interest with great potential in non-volatile data storage. Various RRAM devices have been reported thus far based on transition metal oxide (TMO) film sandwiched by two metal electrodes, such as TiO$_2$, NiO, CuO, ZrO, ZnO, etc. Based on this basic metal/insulator/metal (MIM) structure, several mechanisms have been proposed to explain the origin of resistive switching (RS). To avoid the thermal disadvantages of unipolar RS (usually related with a filamentary path), recently more attention have focused on bipolar RS, which mainly attribute to the interface engineering in MIM structure. It is generally accepted that the RS occurs mainly at interface between oxide and electrode rather than in the bulk, and the interface-type RS usually originates from the redox process based on migration of oxygen vacancies (or oxygen ions) and change in Schottky barrier height or width by trapping/detrapping effects near interface region. As for the Schottky barrier mode of RS, the electrons pass through the thinner barrier in low resistive states (LRS) via a tunneling process, while the thicker barrier in high resistive states (HRS) prevents the electrons from tunneling. Similar as barrier engineering in MIM based RRAM device, adjusting the interface between p-type and n-type oxide films in metal/insulator/metal (MIIM) structure could also result in RS phenomenon. According to the initial rectifying characteristic of p-n junction (HRS under reverse bias, LRS under forward bias), the reproducible resistance change could be obtained by an opposite operation; the proper soft breakdown under reverse bias could turn the device from HRS to LRS, whereas the forward bias will recover the device from LRS back to HRS (preferably in low voltage region).

Transition from stable rectifying behavior to RS behavior has been reported in MIM structure with a Schottky junction. However, there is little report on such transition for p-n junctions, although some early works had observed the resistance hysteresis in some perovskite oxide heterojunction. In this paper, we shall report a stable RS phenomenon in a p-n junction based on the GaO$_x$/NiO$_x$ heterostructure, which offers an alternative design of RRAM device. We shall show that migration of oxygen vacancies near interface of p-n junction play an important role in the switching process.

Commercial ITO glass was employed as the substrate with ITO as the bottom electrode in our device. A NiO$_x$ and GaO$_x$ film with a thickness of 90 nm and 70 nm respectively was deposited successively on the ITO substrate by rf magnetron sputtering. The sputtering process was carried out in an Ar ambient (6 × 10$^{-4}$ Torr) at room temperature. Finally, indium shots were used as a simple top electrode for test. The schematic structure of device is shown in the inset of Fig. 1(a). The I-V characteristics were measured by a semiconductor parameter analyzer in a diode I-V sweeping mode at room temperature. During the test, the bottom ITO electrode was always grounded while different biases were applied on top electrode (In).

Fig. 1(a) shows the current-voltage (IV) characteristics of the as-fabricated stack of In/GaO$_x$/NiO$_x$/ITO and stacks of In/GaO$_x$/In and ITO/NiO$_x$/ITO for comparison purpose. We can see a typical rectifying curve intrinsic to diode with a turn-on voltage of about −2 V for In/GaO$_x$/NiO$_x$/ITO stack. It is worth mentioning that the positive voltage applied on In cannot be too high; otherwise, the diode will run into RS state. For our In/GaO$_x$/NiO$_x$/ITO structure, the RS behavior
could happen in the following regions: the GaO\textsubscript{x} layer, the NiO\textsubscript{x} layer, the interface between GaO\textsubscript{x} and NiO\textsubscript{x}, and the interfaces of In/GaO\textsubscript{x} and NiO\textsubscript{x}/ITO. As shown in Fig. 1(a), the In/GaO\textsubscript{x}/In and ITO/NiO\textsubscript{x}/ITO structures show Ohmic behavior, and no resistive switching are triggered by applying bias with any polarity or intensity. Thus, we can exclude the possibility of RS in the semiconductor layer and their interfaces with electrodes. As reported previously, non-stoichiometric NiO\textsubscript{x} (x > 1) is a p-type semiconductor due to the excess oxygen ions (Ni-deficient) as acceptors for generating holes,\textsuperscript{11} and non-stoichiometric GaO\textsubscript{x} (x < 1.5) is an n-type semiconductor due to the oxygen vacancies (oxygendeficient) as donors for generating electrons.\textsuperscript{12} With Hall Effect measurement, we confirmed the carrier type for GaO\textsubscript{x} and NiO\textsubscript{x} and the sheet carrier concentration of GaO\textsubscript{x} and NiO\textsubscript{x} is $-8.603 \times 10^{11}/\text{cm}^2$ and $+2.012 \times 10^{12}/\text{cm}^2$, respectively. Accordingly, the as-prepared GaO\textsubscript{x} and NiO\textsubscript{x} layers in Ar ambient at room temperature were relatively conductive due to the existence of intrinsic defects (oxygen vacancies/oxygen ions). On the other hand, from the current curves in Fig. 1(a), the contact of NiO\textsubscript{x}/ITO and GaO\textsubscript{x}/In are close to ideal Ohmic; thus, there exist no Schottky barrier between the semiconductor and electrode. Concluded from the analysis above, the rectifying and RS behaviors should come from the p-n junction formed by GaO\textsubscript{x} and NiO\textsubscript{x}; under external excitation, the alteration of the potential barrier at the junction between n-type GaO\textsubscript{x} and p-type NiO\textsubscript{x} should be responsible.

Fig. 1(b) demonstrates a typical resistive switching behavior of the In/GaO\textsubscript{x}/NiO\textsubscript{x}/ITO stack. When a positive bias on In sweeps to a critical value of about 3 V, the current suddenly increases due to a restorable breakdown and the device is set from HRS to LRS. An Ohmic behavior is detected as the bias sweeps back to negative (within $-1$ V). When the negative voltage increases further, an abrupt decrease of current occurs and the device is reset from LRS to HRS. With further increase of the negative voltage, the current increases again, but it is not an Ohmic behavior. In fact, after reset process, the device returns to rectifying behavior again, and the HRS state just exists in a narrow negative voltage range. It is worth mentioning that the device could only be set by applying positive voltage and reset by applying negative voltage on In, which also provides the evidence that RS behavior originates from the n-p interface in metal/n-type semiconductor/p-type semiconductor/metal structure. Supposing the RS occurs from either the interface between In and n-type GaO\textsubscript{x} or p-type NiO\textsubscript{x} and ITO, the device should be set from HRS to LRS when negative voltage was applied on the In (reverse bias on In/n-type GaO\textsubscript{x}) or when positive voltage was applied on ITO (reverse bias on p-type NiO\textsubscript{x}/ITO). The inset of Fig. 1(b) shows the I-V curves of RS performance in 50 cycles, from which we can see that the set voltages distribute in a larger range compared to reset and the was randomly distributed for the 50 cycles below 5 V. As is widely accepted, the forming process and compliance current (CC) are two important factors for RS operation. In our measurement, there exists no apparent forming process. A CC of 5 mA was applied to the set operation to prevent the device from permanent breakdown. When the CC exceeds 15 mA, the repeatable RS behavior disappears and is replaced by permanent Ohmic behavior.

Fig. 2(a) shows the endurance characteristics of the In/GaO\textsubscript{x}/NiO\textsubscript{x}/ITO memory cell in DC sweep mode at room temperature. We can see that although there is a relatively larger fluctuation in HRS resistance in the first 30 cycles, the resistance ratio of HRS/LRS is $\sim10^5$ with little degradation, which is suitable for practical applications. After 30 cycles, the resistance of HRL becomes stable. The retention performance of our device under room temperature is shown in Fig. 2(b). Both resistance in HRS and LRS display little decay in $10^5$, showing very good non-volatility for RRAM applications.

To study the switching behavior of p-n heterojunction, the conduction property during whole resistive switching were investigated. As illustrated in Fig. 3, typical I-V curve of both set and reset were both redrawn in positive log-log scale. The device exhibits Ohmic behavior in LRS and represents the existing filamentary path as widely accepted.\textsuperscript{13} However, the case is more complicated in HRS region. Under low electric field, the device obeys the Ohmic behavior, while the I-V curve shows nonlinearity under higher electric field. Three main conduction models, including space charge limited conduction (SCLC), Schottky emission, and Poole-Frenkel emission (PF emission) were employed respectively to fit the nonlinear region. The slope in log-log curves was 3.18 in set process and 3.09 in reset process, which exclude the SCLC mechanism (slope should be around 2 according to Child’s Law) in our case. For Schottky emission, the relationship between current and voltage could be expressed as follows:\textsuperscript{14}
$I \propto T^2 \exp \left[ \frac{e \sqrt{eV}}{4 \pi \varepsilon_0 \varepsilon d} \right] \frac{1}{kT}$.

(1)

And PF emission can be depicted as:

$I/V \propto \exp \left[ \frac{e \sqrt{eV}}{\pi \varepsilon_0 \varepsilon d} \right] \frac{1}{kT}$.

(2)

where $I$ is the current, $V$ is the voltage, $e$ is the electron charge, $\varepsilon_0$ is the permittivity of free space, $\varepsilon$ is the dielectric constant, $d$ is the thickness of film, $k$ is the Boltzmann’s constant, and $T$ is the temperature. After comparison, the PF emission better fit the nonlinear curve than Schottky emission as shown in the inset of Figs. 3(a) and 3(b). The Schottky emission usually refers to electric-field-enhanced thermal excitation of electrons from defect-related trapped states into conduction band, and according to previous reports, it usually occurs at higher electric field region compared with Schottky emission in RS behavior. The PF model was also modified by Ieda et al. that at low electric field the current can follow Ohm’s law, while at high field it will obey the usual PF equation. Therefore, the transport characterization corresponds to filamentary property in LRS while it is dominated by PF emission in HRS in our device.

As for the RS mechanism, a controversy between the filament and interface models has lasted for a long period.

Unlike the irreconcilable discussion in early time, recently more people would like to believe that these two mechanisms can exist simultaneously and affect each other in some types of RS behaviors. Akinaga et al. also offered a unified model of RS based on such combination. Considering the conduction analysis above, the RS process in the p-n heterojunction could be illustrated with the energy band diagram as Fig. 4 shows. The process can be divided into four steps: (a)
When a positive bias is applied on the In top electrode, the p-n junction is reversely biased, external electric field will enlarge the depletion region and elevate the interface barrier, which suppresses the diffusion current passing through the junction as a usual diode behaves. The conductive paths at both sides were blocked by the interface barrier and the device is in HRS. (b) Oxygen vacancies ($V_{o}^{+}$) are known to be positively charged and mobile.\textsuperscript{19} Further increasing the positive bias leads to accumulation of positive oxygen vacancies (from inside GaO\textsubscript{x}) at the p-n junction on GaO\textsubscript{x} side, forming a high-doping region. At the same time, there also forms a negatively charged high-doping region on NiO\textsubscript{x} side near the interface due to the accumulation of negative oxygen ions ($O^{2-}$). Thus, a significant reduction of effective barrier height and depletion region width could be expected.\textsuperscript{19,20} Beyond a critical value, large amount of electrons tunnel through the narrower barrier between two high-doping regions and the filamentary paths are able to pass through the interface,\textsuperscript{21} which bring the device to LRS. The process corresponds to the so-called soft breakdown of insulator. (c) Due to the high density of defects (oxygen vacancies/oxygen ions) near the interface, the junction behaves like a resistor with high current and the LRS is non-volatile. Until a high enough negative bias on In electrode to repel these defects away from interface region, the barrier recovers back, cutting off the connected filaments. The device returns to HRS and the small drift current mainly due to the electron transport over the p-n barrier (like diode). (d) With further increase of negative bias, the height of barrier reduces and an increasing current could pass through the interface, tracing back the rectifying behavior of heterojunction. Summarizing from above description, the RS can be interpreted as a switching between rectifying and Ohmic behavior. The filaments in both NiO\textsubscript{x} and GaO\textsubscript{x} away from interface just serve as virtual cathode and anode, while the junction barrier engineered by defects migration controls the connection and rupture of filaments near interface, resulting in the RS behavior. There exists only a unidirectional bipolar RS in p-n heterojunction (set in reverse bias, reset in forward bias) due to the rectifying characteristics. And the HRS of the RRAM device exists at low voltage region when the p-n junction is in forward bias.

We also fabricate a 1-\textmu m testing cell with the same thickness of GaO\textsubscript{x} and NiO\textsubscript{x} to investigate the scaling property of p-n heterojunction RRAM. As presented in Fig. 5(a), the whole device was deposit by magnetron sputtering on silicon wafer and patterned by photolithography. Ti/W alloy instead of indium spots is employed as n-contact top electrode on GaO\textsubscript{x} film. Compared with previous device, an apparent decreasing of current (increasing of resistance) in both LRS and HRS was observed in the 1-\textmu m testing cell as Fig. 5(b) shows. According to the resistance dependence on cell area reported by many other works,\textsuperscript{2} the interface factor should play a significant role in the RS in the GaO\textsubscript{x}-NiO\textsubscript{x} heterojunction. The reducing cell area directly decreases the amount of conductive paths crossing over the interface and further increases the resistance.

In conclusion, a unidirectional bipolar RS was observed in the GaO\textsubscript{x}-NiO\textsubscript{x} heterostructure fabricated by magnetron sputtering at room temperature. The RS behavior could be concluded as the switching between rectifying and Ohmic behavior of the diode. The alteration of junction barrier due to the electric field and the migration of intrinsic defects (oxygen vacancies in GaO\textsubscript{x} and oxygen ions in NiO\textsubscript{x}) control the filamentary paths passing through the interface, which accounts for the RS behavior observed. The device shows good endurance and retention performance, manifesting the potential application of p-n junction structure in non-volatile memory.

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