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Citation	Yu, Q., Liu, Y., Chen, T., Yu, Y. F., Wong, J. I., & Yang, M. (2012). Modeling of lateral charge transfer in Si nanocrystals in SiO2 thin film. Journal of applied physics, 111(7).
Date	2012
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Citation: J. Appl. Phys. **111**, 073707 (2012); doi: 10.1063/1.3701577
View online: http://dx.doi.org/10.1063/1.3701577
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Modeling of lateral charge transfer in Si nanocrystals in SiO_2 thin film

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(Received 22 November 2011; accepted 28 February 2012; published online 6 April 2012)

In this work, lateral charge diffusion in Si nanocrystal (nc-Si) layer embedded in a SiO_2 thin film has been simulated with Silvaco-TCAD tool by monitoring the influence of the charging of the nanocrystal in one metal-oxide-semiconductor structure on its neighboring devices. With the existence of the nc-Si layer in the spacing regions between the charged device and a neighboring device, a flatband voltage shift can be observed in the neighboring device after a charging operation on the charged device. The phenomena are explained in terms of the lateral charge diffusion in the nc-Si layer. The lateral charge diffusion can cause the interference among the neighboring devices. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.3701577]

INTRODUCTION

Si nanocrystals (nc-Si) embedded in SiO_2 thin films have attracted extensive research due to their applications in light-emitting device[1–4] (LED), and nonvolatile memory.[5–8] For nonvolatile memory application, nc-Si is usually confined in a single layer as the charge storage element.[1–8] Due to its discrete nature, it was always assumed that there is negligible lateral charge diffusion between two neighboring devices. However, this assumption is not always true if the nc-Si density approaches such a high level that trapped charge can diffuse to neighboring nc-Si. A good understanding on this issue is necessary for the device applications because this will have impact on the charge retention capability of memory device. Furthermore, the lateral charge diffusion may lead to malfunction of the neighboring devices. Our previous study[9–12] was focused on the metal-oxide-semiconductor (MOS) structure of gate/nanocrystal embedded dielectric layer/Si substrate, which is more relevant to transport of charge in vertical direction. In this work, investigation on the lateral charge diffusion of nc-Si in the oxide has been carried out by simulation. It is observed that with the existence of the nc-Si layer in the spacing regions between the charged device and a neighboring device, a flatband voltage shift can be observed in the neighboring device after a voltage operation on the charged device.

SIMULATION AND DISCUSSION

The process and device simulations were carried out using Silvaco-TCAD tool. MOS capacitor device models are generated with oxide layer embedded with Si nanocrystals using a 2D process in the module of Athena as following. A 15 nm SiO_2 thin film is grown on a *p*-type (100) Si wafer with the resistivity of 5.3 Ωcm. Si nanocrystals having a size of 5 nm are embedded in the oxide at the depth 5 nm underneath the oxide surface. A nc-Si layer is formed with a uniform distance of 9 nm between two neighboring nanocrystals. MOS capacitors are formed by depositing Al film of 250 nm on the SiO_2 surface. Two types of samples (i.e., Sample 1 and Sample 2) were modeled, as shown in Fig. 1. Both samples have identical MOS capacitors A, B, and C. In Sample 1, Device A is not isolated from Device B due to the existence of the continuous nc-Si layer embedded in the oxide in the spacing region between A and B; in contrast, in Sample 2, the nc-Si/oxide layer in the spacing region is completely removed by etching process. The device characteristics were simulated with the module of Atlas. A set of models including Shockley Read Hall (SRH) recombination model, Lombardi surface mobility model, self-consistent Fowler-Nordheim tunneling model for electrons, self-consistent Fowler-Nordheim tunneling model for holes, and oxide charge transport model are used for simulation. The capacitance-voltage (C-V) simulations were carried out at 1 MHz.

Figure 2(a) and 2(b) show the *C-V* characteristics before and after the charging operation for Devices A and B in Sample 1, respectively. The charging operation is carried out by applying +20 V for 2 s on the gate of Device A. The distance between Devices A and B is 25 nm. As shown in Fig. 2(a), Device A has a positive ΔV_{FB} of ~+5.30 V, while Device B has a positive ΔV_{FB} of +0.36 V as depicted by Fig. 2(b). The flatband voltage shift in Device A indicates that a significant amount of negative charges have been trapped in the nc-Si in the oxide. This is due to the simultaneous occurrence under the positive charging voltage of electron injection from the *p*-Si substrate and electron tunneling from the nc-Si to the gate electrode. ΔV_{FB} of ~ 0.14 V in Device B means that there is a small amount of charges that are trapped in the nc-Si of Device B. As discussed later, the charge trapping in Device B is attributed to lateral charge diffusion from Device A to Device B via the nc-Si layer.

Figure 3(a) and 3(b) show the C-V characteristics before and after the charging operation for Devices A and B in Sample 2, respectively. The charging operation is carried out by applying +20 V for 2 s to the gate of Device A. The

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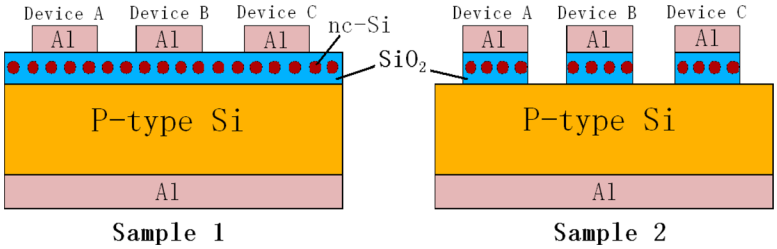

FIG. 1. Schematic illustration of the device structures with (Sample 1) and without (Sample 2) the nc-Si layer in the spacing region between the devices.

distance between Device A and B is 25 nm. In Sample 2, the charging at Device A causes a positive ΔV_{FB} of $\sim$ 6.10 V in Device A; however, there is no obvious flatband voltage shift observed in Device B, showing insignificant charge trapping in Device B caused by the charging at Device A.

It should be noted that the difference in the sample structure leads to slight deviation in C-V characteristics between Sample 1 and Sample 2. As shown in Fig. 2(a) and Fig. 3(a), both C-V characteristics before and after charging show different behaviors between Sample 1 and Sample 2. As the nc-Si layer in the spacing regions between two neighboring devices is cut in Sample 2, the electric field distribution should be slightly changed and thus resulting in different behaviors in C-V characteristics.

For Sample 1, as the charging voltage of +20 V is applied to the gate of Device A, electrons are injected from the silicon substrate and some of them are trapped in the nc-Si of Device A. Therefore, a large positive flatband voltage shift is observed in Device A. The electrons in Device A can move along the nc-Si layer to Device B due to the charge diffusion; thus, a positive flatband voltage shift is also observed in Device B. As the amount of charges that diffuse to Device is small, only a small flatband voltage shift can be observed, as shown in Fig. 2(b). In contrast, for Sample 2, the charging operation causes almost no charge trapping in nc-Si layer of Device B, leading to no flatband voltage shift observed. The results in Figs. 2 and 3 clearly show that the nc-Si in Device B can be charged by the charging operation in Device A if there is a continuous nc-Si layer in the spacing region. On the other hand, if the spacing region is cutoff, there is no charge diffusion between Device A and Device B, and thus there is no flatband voltage shift in Device B can be observed.

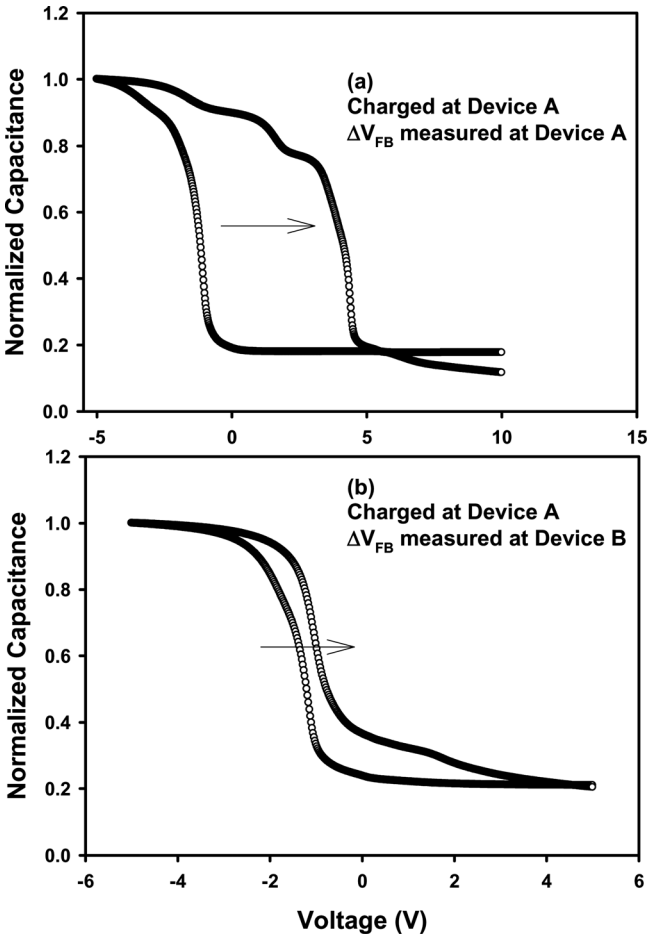

FIG. 2. Influence of the positive-voltage charging at device A on the C-V characteristics of Devices A (a) and B (b) in Sample 1. The charging operation is carried out by applying +20 V to the gate electrode of Device A for 2 s.

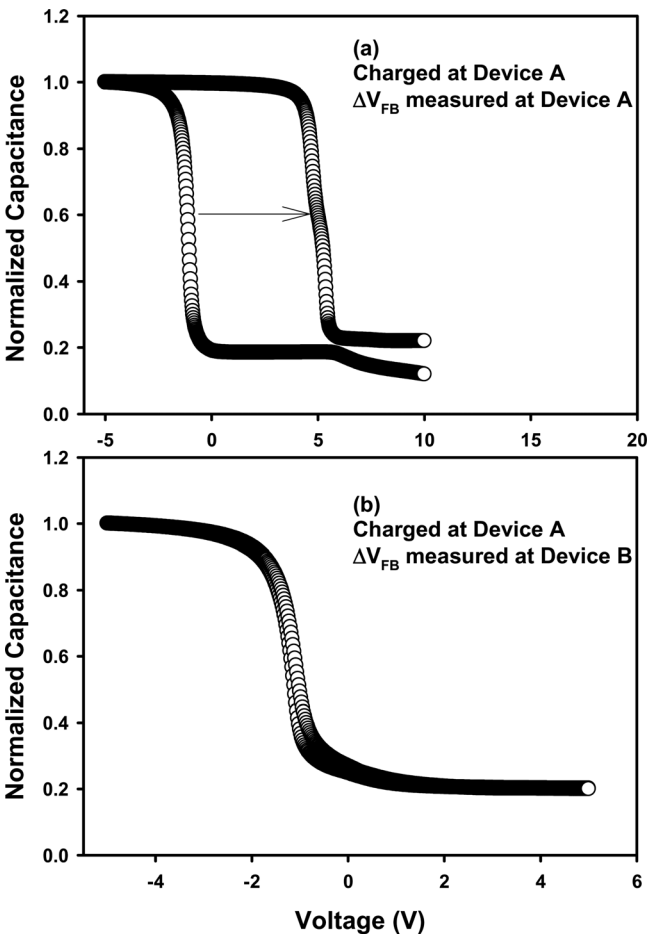

FIG. 3. Influence of the positive-voltage charging at Device A on the C-V characteristics of Devices A (a) and B (b) in Sample 2. The charging operation is carried out by applying +20 V to the gate electrode of Device A for 2 s.

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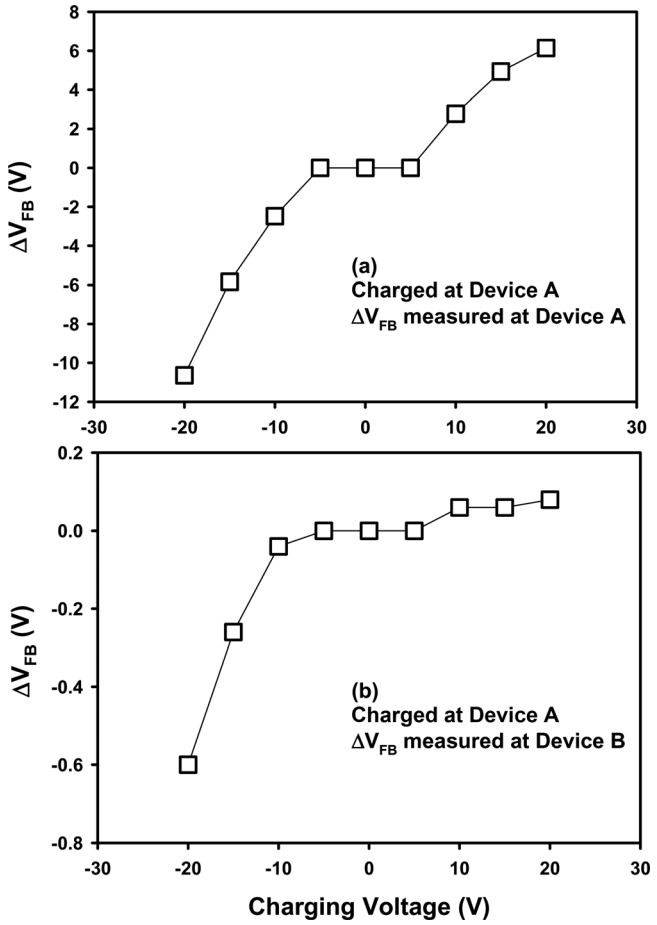

FIG. 4. Flatband voltage shifts of Device A (a) and Device B (b) caused by the charging operation at Device A in Sample 1 as a function of the charging voltage. The charging operation is carried out by applying a charging voltage to the gate electrode of Device A for 2 s.

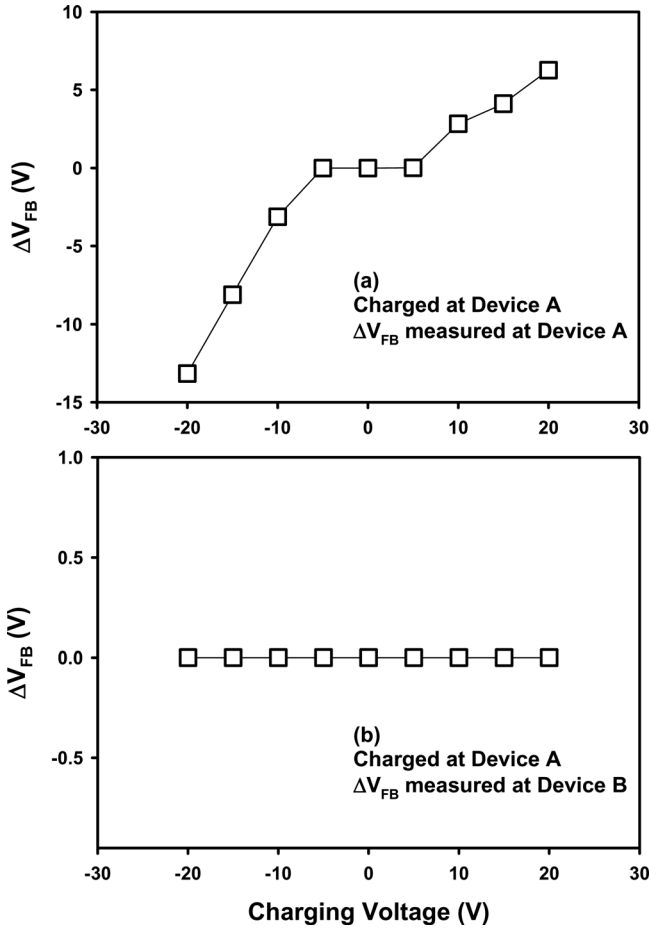

FIG. 5. Flatband voltage shifts of Device A (a) and Device B (b) caused by the charging operation at Device A in Sample 2 as a function of the charging voltage. The charging operation is carried out by applying a charging voltage to the gate electrode of Device A for 2 s.

The effect of the charge diffusion in the nc-Si layer has been systematically investigated, by monitoring the flatband voltages of Devices A and B when Device A is charged by various positive or negative voltages. For Sample 1, all the charging operations are carried out at Device A for 2 s under various charging voltages. The distance between Device A and Device B is 45 nm. Figure 4(a) shows ΔV_{FB} measured at Device A and Fig. 4(b) presents ΔV_{FB} measured at Device B. When a positive charging voltage is applied to the gate of Device A, electron trapping occurs in the nc-Si of Device A due to electron injection from the substrate. As a result, Device A exhibits a positive ΔV_{FB} under positive bias, and ΔV_{FB} increases with the voltage magnitude also. On the other hand, a negative charging voltage leads to hole trapping in the nc-Si of Device A due to hole injection from the substrate. Thus Device A exhibits a negative ΔV_{FB} under a negative charging voltage. Due to the charge diffusion from Device A, there is charge trapping in the nc-Si of Device B with the same charge sign as in Device A. As the amount of charges diffusing to Device B is small, Device B has a smaller ΔV_{FB}, as shown in Fig. 4(b).

For Samples 2, the charging operations are conducted on Device A at various charging voltages for 2 s. The distance between Device A and Device B is set to 45 nm. Figure 5(a) and 5(b) show the ΔV_{FB} measured at Device A and Device B, respectively. Device A exhibits a positive and negative ΔV_{FB} under a positive and negative charging voltage, respectively, as shown in Fig. 5(a). However, Device B exhibits no charge trapping due to no charge diffusion from Device A as a result of the lack of the nc-Si layer in the spacing region between Device A and Device B.

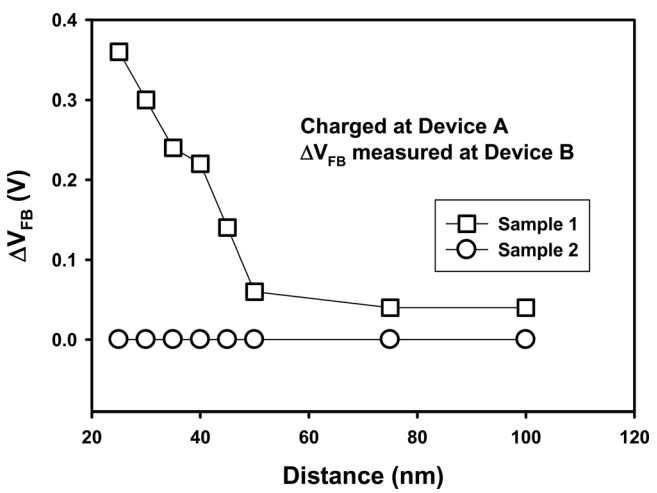

FIG. 6. Flatband voltage shift of Device B as a function of the distance between Devices A and B in Samples 1 and 2 after the charging operation at Device A under +20 V for 2 s.

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Figure 6 shows the flatband voltage shift of Device B as a function of the distance between Devices A and B in Sample 1 and Sample 2. In Sample 1, due to the charge diffusion from Device A to Device B, Device B exhibits a ΔV_{FB}. As the charge diffusion becomes weak with the increase in the distance between the two devices, ΔV_{FB} decreases, as can be seen in Fig. 6. On the other hand, for Sample 2, Device B shows no flatband voltage shift as the nc-Si layer in the spacing region is cutoff.

CONCLUSION

In conclusion, lateral charge diffusion in nc-Si embedded in a SiO_2 thin film has been modeled with Silvaco-TCAD tool. An flatband voltage shift can be observed in the neighboring device after a charging operation on the charged device with the existence of the nc-Si layer in the spacing regions between the two devices. The lateral charge diffusion can cause the interference among the neighboring devices.

ACKNOWLEDGMENTS

This work has been financially supported by NSFC under project No. 60806040, the Fundamental Research Funds for the Central Universities under project No. ZYGX2009X006, the Young Scholar Fund of Sichuan under project No. 2011JQ0002 and National Research Foundation of Singapore (NRF-G-CRP 2007-01).

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