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Characterization of epitaxial GaAs MOS capacitors using atomic layer-deposited TiO$_2$/Al$_2$O$_3$ gate stack: study of Ge auto-doping and p-type Zn doping

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Abstract

Electrical and physical properties of a metal-oxide-semiconductor (MOS) structure using atomic layer-deposited high-$k$ dielectrics (TiO$_2$/Al$_2$O$_3$) and epitaxial GaAs [epi-GaAs] grown on Ge(100) substrates have been investigated. The epi-GaAs, either undoped or Zn-doped, was grown using metal-organic chemical vapor deposition method at 620°C to 650°C. The diffusion of Ge atoms into epi-GaAs resulted in auto-doping, and therefore, an n-MOS behavior was observed for undoped and Zn-doped epi-GaAs with the doping concentration up to approximately $10^{17}$ cm$^{-3}$. This is attributed to the diffusion of a significant amount of Ge atoms from the Ge substrate as confirmed by the simulation using SILVACO software and also from the secondary ion mass spectrometry analyses. The Zn-doped epi-GaAs with a doping concentration of approximately $10^{18}$ cm$^{-3}$ converts the epi-GaAs layer into p-type since the Zn doping is relatively higher than the out-diffused Ge concentration. The capacitance-voltage characteristics show similar frequency dispersion and leakage current for n-type and p-type epi-GaAs layers with very low hysteresis voltage (approximately 10 mV).

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Keywords: epitaxial-GaAs, Ge out-diffusion and auto-doping, ALD, high-$k$ dielectrics.

Introduction

In recent years, there had been increasing interest in the introduction of III-V semiconductors as high-mobility channel materials in nanoscale silicon-based [Si-based] complementary-metal-oxide-semiconductor [CMOS] devices [1-7]. This migration from the present strained Si channels is due to two reasons: First, with the replacement of silicon oxide [SiO$_2$] and silicon oxynitride (SiO$_x$N$_y$) by high-permittivity [high-$k$] dielectrics as the gate insulator [1-8], the choice of a channel material is no longer restricted to Si. Second, the incorporation of appropriate stressors, such as silicon nitride, can enhance both electron and hole mobilities in sub-90-nm devices; there could be scaling limits to such approaches. An inversion n-channel GaAs field effect transistor [FET] with a metal gate high-$k$ dielectric was fabricated on GaAs wafers by de Souza et al. [4]. Ye et al. [5] characterized the Al$_2$O$_3$/GaAs metal-oxide-semiconductor field effect transistor [MOSFET] and found a very high drain current and a relatively high transconductance. Also, the studies on the effect of the atomic layer-deposited [ALD] Al$_2$O$_3$ blocking layer indicates that it can suppress the growth of an interfacial layer and that the ALD Al$_2$O$_3$ could reduce the formation of native arsenic oxides to below the detection level of X-ray photoelectron spectroscopy [6].

For high-volume manufacturing, it is of great interest to develop epitaxial III-V high-mobility channel materials on a silicon platform to realize CMOS devices with...
increased carrier mobility and device flexibility [9-11]. Convergence of the Si and compound semiconductor industries promises the best of both worlds for device manufacturers due to the high performance, flexibility, and enhanced functionality of III-V compounds coupled with the low manufacturing cost and sheer scale of the Si process. In particular, GaAs has received much attention due to its lower effective mass and, hence, an intrinsic superior transport property than Si. Moreover, it is possible to grow epitaxial GaAs [epi-GaAs] on a Si-based CMOS technology-compatible Ge substrate since the lattice parameter of GaAs (0.5653 nm) is almost identical to that of Ge (0.5658 nm), and both have similar thermal conductivity [9]. In addition, Ge has the added advantage of having a high hole mobility of 1,900 cm² V⁻¹ s⁻¹ at 300 K which is about four times higher than that of Si [12]. This suggests the possibility of a heterogeneous integration of GaAs n-channel FETs with Ge p-channel FETs on a common Si platform.

One of the key considerations in fabricating a surface channel MOSFET using epi-GaAs is to achieve a good interface quality between the epi-GaAs substrate and gate oxide, which is vital for the device performance [13]. Fortunately, atomic layer deposition provides a unique opportunity to integrate high-quality gate dielectrics on bulk and epi-GaAs [2,14,15]. It was observed that ALD Al₂O₃ provides a better interface with GaAs interface compared with other ALD high-k dielectrics [6,8]. Although, by continuing effort on surface passivation, it is possible to grow a high-quality interface with low defect density, the hysteresis voltage for ALD high-k/GaAs gate stack is still high [2,7,15]. There are some attempts to achieve low hysteresis voltage using ALD SiO₂, directly deposited titanium oxide [TiO₂], and Si passivation on GaAs substrates [16-19]. On the other hand, GaAs grown at its optimum temperature on Ge will result in high Ge contamination, such as auto-doping and formation of Ge-based complexes, as significant Ge atoms will diffuse into the GaAs epilayer during growth. Chia et al. [20] suggested that a thin 10-nm AlAs interfacial layer is sufficient to effectively block the out-diffusion of Ge atoms at a high growth temperature of 650°C, eliminating Ge-based complexes and auto-doping effects in the GaAs layer. It is highly desirable to grow p-type epi-GaAs with good structural and electronic qualities for n-MOSFET device applications. However, to the best of our knowledge, there is no report of a metal-oxide-semiconductor [MOS] capacitor using p-type epi-GaAs grown on Ge substrates. TiO₂ [17,18] gate dielectric provides low hysteresis voltage, and thin ALD Al₂O₃ is a promising gate dielectric for surface passivation [6,7] as well as improved interface quality. In this paper, we demonstrate ALD TiO₂/Al₂O₃ gate stack on undoped (which is n-type) and Zn-doped (p-type) epi-GaAs grown by metallorganic chemical vapor deposition [MOCVD] technique. The epi-GaAs device characteristics are compared with that of undoped and Zn-doped epi-GaAs for different concentrations. Further, we have identified the minimum Zn dopant concentration required for p-type epi-GaAs substrates. Electrical and physical analyses and simulation using SILVACO software (SILVACO, Inc., Santa Clara, CA, USA) have also been performed to understand the impact of the material and processing conditions for a high-quality gate stack on epi-GaAs substrates and the impact of Ge diffusion on the performance of MOS characteristics. The surface topography of epi-GaAs and high-k/epi-GaAs surfaces was examined via atomic force microscopy [AFM]. Interfacial reaction of high-k/epi-GaAs and Ge out-diffusion was studied by time of flight secondary ion mass spectrometry [ToFSIMS] for all the structures. Capacitance-voltage [C-V] and current-voltage [I-V] characteristics were measured using an Agilent 4284A LCR (Agilent Technologies Inc., Santa Clara, CA, USA) and a Hewlett-Packard 4140B semiconductor parameter analyzer (Hewlett-Packard Company, Palo Alto, CA, USA), respectively.

**Experiment**

MOS capacitors were fabricated on epi-GaAs substrates. The epi-GaAs substrates were grown at 620°C to 650°C by MOCVD technique. Vicinal Ge (100) substrates with 6° offcut toward the (111) plane were used to ensure that the epitaxial GaAs grown on Ge is free from APD defects. Prior to the growth of GaAs layers, the Ge substrate was heated up to and kept at 650°C for 5 min under H₂ environment to remove the native oxide layer. Tertiarybutylarsine and trimethylgallium were introduced into the reactor for the growth of the Zn-doped 300-nm-thick GaAs layer at 620°C. For undoped epi-GaAs, the GaAs substrate was grown on Ge(100) samples with an AlAs interfacial layer at 650°C by MOCVD technique. The details of the film growth and their properties are reported elsewhere [20]. The as-grown wafers were then degreased using isopropanol, cleaned in HF solution (1%) for 3 min to remove the native oxide, and then dipped in NH₄OH solution for 10 min. A thin layer of Al₂O₃ was deposited on epi-GaAs using trimethylaluminium (SAFC Hitech, Havermall, MA, USA; 99.9%) and H₂O as the precursors in a viscous flow-type (0.6 Torr working pressure) atomic layer deposition equipment (fXALD ALD equipment, Azimuth Technologies Pte Ltd., Singapore) with a N₂ flow rate of 50 sccm at 170°C. After that, TiO₂ films were deposited under similar conditions. Vapors of TiCl₄ (Merck & Co., Inc., Whitehouse Station, NJ, USA; 99%) and H₂O precursors were sequentially introduced into the chamber with an exposure time of 0.1 s and purged by 50-sccm
N_{2} flow for 10 s between the two exposures. Post-deposition annealing was carried out in a N_{2} ambient at 500°C for 1 min by rapid thermal annealing technique. The Au metal, deposited by sputtering, was used as the gate electrode (area, 7.8 \times 10^{-3} \text{ cm}^{2}). Finally, a low-resistance ohmic back contact was formed by depositing Ti/Pt/Au alloy on the p-GaAs substrate, AuGeNi alloy on the n-GaAs substrate, and Au on the Ge substrate.

Results and discussion

The surface roughness of epi-GaAs and bulk p-GaAs was measured using AFM. Figure 1 shows the surface topology of epi-GaAs on a scale bar of 10 \times 10 \, \mu \text{m}^{2}, and a distinct triangular feature is observed. The root-mean-square [rms] surface roughness is high, and it is measured to be 4.0 nm over this scale. These triangular features are typical of epi-GaAs grown on Ge(100) substrates with 6° offcut toward the [111] direction [21]. The rms values for Zn-doped epi-GaAs ranges from 4.4 to 4.7 nm. The ALD high-\textit{k} dielectric stack follows the epi-GaAs topography as observed in the AFM image. The rms value increased slightly to 4.2 nm with ALD coated undoped epi-GaAs after rapid thermal annealing at 500°C in a N_{2} ambient.

Figure 2 presents the ToF-SIMS profile of the epitaxial GaAs/Ge interface for undoped and Zn-doped epi-GaAs with ALD coated TiO_{2}/Al_{2}O_{3} gate stack. The Zn-doped epi-GaAs (without AlAs) was grown at a relatively low temperature (620°C) to suppress Ge out-diffusion. The epi-GaAs thickness is 300 nm. The Ge atoms were diffused up to approximately 100 nm from the GaAs/Ge interface. However, for epi-GaAs films grown at 650°C, Ge is diffused up to 270 nm from the GaAs/Ge interface [20]. It is apparent from the SIMS depth profiles of Ga, As, Ti, Al, and Ge atoms for Zn-doped and undoped epi-GaAs that except for Ge, all other atoms hardly interdiffuse at the heterointerface between GaAs and the Ge substrate. This indicates that Ge is diffused into the epi-GaAs layer, resulting in a strong asymmetry between the two sides of the interface. It is worthy to note that from the SIMS depth profile images, it appeared that diffusion of the Ge atom is of random nature and is independent of Zn concentration. Ge diffusion into the GaAs film is much more pronounced than As/Ga.

Figure 1 AFM images \((10 \times 10 \, \mu \text{m}^{2})\) for epitaxial GaAs on Ge structures. (a) Undoped epi-GaAs and Zn-doped epi-GaAs with doping densities of (b) \(1 \times 10^{17} \, \text{cm}^{-3}\), (c) \(1 \times 10^{18} \, \text{cm}^{-3}\), and (d) \(1 \times 10^{19} \, \text{cm}^{-3}\). The rms surface roughness of the structures determined from AFM is (a) 4.0 nm, (b) 4.7 nm, (c) 4.4 nm, and (d) 4.6 nm.
diffusion into the Ge substrate without any diffusion barrier. However, after introducing the AlAs barrier layer, Ge diffusion was mainly confined to the barrier layer. After AlAs interfacial layer insertion, it shows abrupt heterointerfaces, and no significant compositional diffusion of Al and Ge atoms into the GaAs epilayer was observed at a high growth temperature. Since Zn dopant concentration is beyond the SIMS detection limit, it is difficult to see the Zn profile for epi-GaAs.

In order to examine the elemental distribution with superior sensitivity and depth resolution, ToF-SIMS measurements on the ALD TiO$_2$/Al$_2$O$_3$ on epi-GaAs substrates were performed. Figure 3 shows the SIMS depth profile from the surface of the ALD TiO$_2$/Al$_2$O$_3$ to the epi-GaAs layer. The transition region of the TiO$_2$/Al$_2$O$_3$/epi-GaAs interface is clearly shown in the Figure 3. A gallium-rich region was observed above the interface. From the gradient of Ti and Al intensity at the TiO$_2$/Al$_2$O$_3$ interface, it is evident that interdiffusion of Ti into Al$_2$O$_3$ is higher compared to that of Al into TiO$_2$. These profiles can be divided into three different sections: In the first region, a decreasing intensity of Ti-, TiO-, and O-related signals is observed. The second region in the ToF-SIMS profile presents Ti and TiO double bumps at the TiO$_2$/Al$_2$O$_3$ interface which exhibit different distributions of Ti inside the layer, i.e., that the stoichiometry is strongly changing with depth. It is important to note that the Al or AIO signal intensity does not vary with depth. This suggests almost constant stoichiometry throughout the Al$_2$O$_3$ interlayer thickness and aluminum enrichment of the interface. The As and Ga intensity demonstrated a decreasing intensity from the epi-GaAs/high-$k$ interface, and no further increase in intensity was observed corresponding to the reduced interfacial As-O or Ga-O layer. The above observation may be explained using the intermixing model proposed by Kamata and Kita et al. [22,23], whereby it is possible that TiO$_2$/Al$_2$O$_3$ was able to mix with residual GaO$_x$ or...
out-diffused elemental As such that the TiO$_2$/Al$_2$O$_3$/epi-GaAs stack has an interfacial layer like Ti/Al-GaAsO$_x$ after annealing.

High-frequency C-V measurements were carried out to evaluate the epi-GaAs substrate doping and electrical properties of the TiO$_2$/Al$_2$O$_3$/epi-GaAs structure. It is known that Ge is an n-type dopant and Zn is a p-type dopant in GaAs. Figure 4 shows the C-V characteristics of TiO$_2$/Al$_2$O$_3$/epi-GaAs for undoped and Zn-doped epi-GaAs. The C-V characteristics of epi-GaAs without doping (undoped) and Zn-doped epi-GaAs with a doping concentration of $10^{17}$ cm$^{-3}$ exhibit an n-type behavior since accumulation is achieved at positive gate biases. This is due to the auto-doping of out-diffused Ge atoms in GaAs. On the other hand, epi-GaAs with a Zn dopant concentration of $10^{18}$ cm$^{-3}$ shows a p-type C-V behavior, which suggests that the concentration of Zn dopant is higher than that of the out-diffused Ge atoms. According to Figure 4, the accumulation capacitance is different for n-type and p-type epi-GaAs substrates. This suggests that the interfacial layer thickness between the high-$k$ and semiconductor depends on the nature of the substrate dopants [2]. It is also reported that, in the case of HfO$_2$ on Ge substrates, the interface growth kinetics depends on the dopant type [24]. Although, the epi-GaAs MOS capacitor for the Zn-doped epi-GaAs with $10^{18}$ cm$^{-3}$ shows a p-type C-V behavior, the C-V curves stretched along the voltage axis. This is due to the presence of defects at the interface. It is not surprising since the structural defects formed near the substrate surface due to the impurity diffusion, particularly when the impurity concentration is high (approximately $1 \times 10^{18}$ cm$^{-3}$).

It was observed from the SIMS analysis of the epi-GaAs layer grown at 620°C that a significant amount of Ge was diffused into the epi-GaAs thereby converting it to n-type due to auto-doping of Ge to GaAs. By introducing a high density of Zn, it is possible to convert the n-type epi-GaAs to p-type. It is worth noting that although, from SIMS analysis, there was Ge atom diffusion in the epi-GaAs layer up to 20 nm with an AlAs interlayer and up to 100 nm without the AlAs interlayer, however, for both the cases, the epi-GaAs layer shows an n-type behavior. This suggests that although AlAs effectively reduced the Ge atom diffusion into GaAs, there is still some Ge which could possibly be below the SIMS detection limit. From the simulation of Ge diffusion and C-V characteristics, it was also observed that Ge atoms were present in the epi-GaAs even for the AlAs barrier layer, but the concentration is very low (approximately $10^{15}$ cm$^{-3}$). The hysteresis voltage for ALD TiO$_2$/Al$_2$O$_3$ gate stack was very low (approximately 10 mV) as shown in the inset of Figure 4.

Figure 5 shows the plots of C-V characteristics of the ALD TiO$_2$/Al$_2$O$_3$ gate stack on Zn-doped epi-GaAs with two different doping concentrations of $10^{17}$ cm$^{-3}$ (Figure 5a) and $10^{18}$ cm$^{-3}$ (Figure 5b). The measured C-V characteristics were also simulated for all the frequencies considered for a similar structure using SILVACO, a commercially available software package. It is observed that the simulated curves match well with the experimental data. A significant amount of dispersion in the accumulation region of the C-V curves in the frequency range of 60 to 100 kHz is observed which is attributed to the presence of an interfacial layer with lossy dielectrics. The frequency dispersion for the Zn-doped epi-GaAs with doping concentrations of $10^{18}$ cm$^{-3}$ and $10^{17}$ cm$^{-3}$ is almost similar, and the values are measured to be $\Delta C_{60-100 k}$ which are approximately 15% and 12%, respectively. It is apparent from the ToF-SIMS elemental depth profiles (Figure 3) where a significant amount of interdiffusion of TiO, AlO, O, Ga, and As was noticed. As a result of such interdiffusion, a lossy dielectric layer at the interface has been formed. To account for this, an interfacial layer thickness of 2.6 to 3.0 nm with a dielectric constant of 6 was incorporated during simulation in between the Al$_2$O$_3$/GaAs layer. The fixed oxide charge densities ($Q_F$) of $4 \times 10^{13}$ and $1 \times 10^{13}$ cm$^{-2}$ needed to be incorporated to match the flat band voltage. It should be noted that the flat band voltage is negative for the Zn-doped devices with a doping concentration of $10^{18}$ cm$^{-3}$, whereas it is positive for $10^{17}$ cm$^{-3}$ doping.

The leakage current vs. applied voltage [$I$-$V$] characteristics of different MOS capacitors exhibits a leakage
current of approximately $10^{-3}$ A at flat band voltage, $V_{fb}$ ± 1 V, as shown in Figure 6. It was observed that the leakage current increases sharply with applied voltage and then nearly saturates. Poole-Frenkel [PF] emission was first considered to be the possible conduction mechanism for the leakage current across the gate stack [25]. To clarify whether the leakage current is due to the PF emission, the logarithm of the current density over the electric field was plotted against the square root of electric field as shown in Figure 6b. If the leakage current is governed by the PF emission, such a plot will show a straight line, and from the slope of the straight line, the extracted values of the dynamic dielectric constant are found to be very low compared to the reported results [26,27]. Therefore, we assumed the current conduction in the small electric field is not a pure PF emission, indicating that different conduction mechanisms contribute to the leakage current. Fowler-Nordheim [F-N] tunneling due to the narrowed oxide energy barrier width is also considered as a possible...
current transport mechanism in the Al_2O_3/epi-GaAs heterostructure because the gate leakage mechanism was well fitted by the F-N tunneling model [25,28]. From the slope of the curve, the tunneling barrier heights were found to be 2.1 eV (undoped epi-GaAs) and 1.18 to 1.2 eV (for doped epi-GaAs). The large bandgap of interfacial Al_2O_3 and the high-quality oxide film are responsible for this because the F-N tunneling conduction requires sufficient band offsets and a low density of oxide traps [29].

Conclusions

In summary, epi-GaAs MOS capacitors were fabricated and characterized using electrical and physical analysis. Atomic layer-deposited TiO_2/Al_2O_3 gate stack is used to fabricate epi-GaAs MOS capacitors on a Ge substrate for III-V CMOS applications. The epi-GaAs MOS capacitor shows an nMOS behavior for undoped and even for Zn-doped epi-GaAs with low concentration due to Ge auto-doping, which is confirmed by the SIMS analysis and simulation. Zn-doped epi-GaAs with a high concentration > 10^{18} cm^{-3} converts epi-GaAs into p-type. Interfacial reaction mechanisms between epi-GaAs and ALD TiO_2/Al_2O_3 have been discussed through SIMS analysis and capacitance-voltage characteristics. Although the simulated and experimentally obtained C-V result showed frequency dispersion due to the presence of the interfacial lossy dielectric layer between Al_2O_3 and epi-GaAs, the hysteresis voltage for epi-MOS device is very small for the ALD Al_2O_3/TiO_2 gate stack. Therefore, using suitable surface passivation with ALD TiO_2/Al_2O_3 on epi-GaAs can pave the way for the next generation of Si-based CMOS technology for ultra-high-speed devices or multifunctional devices on a Si platform.

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Authors' contributions

GKD was involved with the design and planning of the manuscript as well as with the growth and characterization of the ALD TiO_2/Al_2O_3 gate stack on epi-GaAs. TRSV was involved with the surface characterization and participated in the drafting of the manuscript. AFM and electrical measurements were done by XL. CKM was involved with the MOOCV growth of epi-GaAs. Simulation of C-V characteristics and Ge diffusion was done by AD and SC. CM and CKM were involved with the electrical characterization of the epi-GaAs MOS capacitors. SIMS measurements and analysis were done by HLS. ALD TiO_2/Al_2O_3 was deposited by HG and MKK. DZC was participated in the characterization of the epi-GaAs MOS capacitors. All authors read and approved the final manuscript.

Competing interests

The authors declare that they have no competing interests.

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