Title	Electron trap transformation under positive-bias temperature stressing
Author(s)	Gao, Yuan; Ang, Diing Shenp; Bersuker, G.; Young, C. D.
Citation	Gao, Y., Ang, D. S., Bersuker, G., & Young, C. D. (2013). Electron Trap Transformation under Positive-Bias Temperature Stressing. IEEE Electron Device Letters, 34(3), 351-353.
Date	2013
URL	http://hdl.handle.net/10220/9977
Rights	© 2013 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works. The published version is available at: [http://dx.doi.org/10.1109/LED.2013.2242041].

Electron Trap Transformation Under Positive-Bias Temperature Stressing

Y. Gao, D. S. Ang, G. Bersuker, and C. D. Young

Abstract—**Electron detrapping in the TiN/HfO$_2$ gate n-MOSFET under dynamic positive-bias temperature instability (PBTI) is examined. Similar to hole detrapping under dynamic negative-bias temperature instability (NBTI), electron detrapping per relaxation cycle is a constant under a low oxide stress field ($\sim$5.5 MV/cm), independent of the number of times the transistor is stressed and relaxed, and it progressively decreases with the number of stress/relaxation cycles at a higher oxide stress field ($\sim$7 MV/cm). Analysis shows that the decrease is due to a portion of the electron trap states being transformed into deeper levels, thereby increasing the emission time of the trapped electrons. However, unlike hole detrapping, the decrease in electron detrapping is not accompanied by a correlated increase in the stress-induced leakage current, and it can be reversed with a moderate negative gate voltage. These differences from NBTI suggest that distinct defects are active under PBTI.**

Index Terms—**Bias temperature instability (BTI), electron traps, high-k/metal gate stack, oxide-trapped charge.**

I. Introduction

POSITIVE-bias temperature instability (PBTI) is a serious problem of the high-k gate n-MOSFET [1]–[6]. Under a positive gate voltage (V_g), defects in the high-k oxide capture electrons from the channel and are negatively charged, causing the threshold voltage (V_t) to increase. It has been implicitly assumed in most analyses that defect characteristics, such as physical configuration, energy state, etc., are predetermined by material properties and processing and are not altered by the electrical stress applied. In this letter, we show that such an assumption may not be valid in general, even under a moderate oxide field. Evidence of a time-dependent oxide-field-driven shallow-to-deep electron trap transformation under PBTI stressing is discussed. Similarities and differences with the recently reported hole detrapping under dynamic negative-bias temperature instability (DNBTI) [7]–[12] are highlighted.

Y. Gao and D. S. Ang are with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798 (e-mail: edsang@ntu.edu.sg).

G. Bersuker is with SEMATECH, Austin, TX 78741 USA.

C. D. Young was with SEMATECH, Austin, TX 78741 USA. He is now with the Department of Materials Science and Engineering, The University of Texas at Dallas, Richardson, TX 75080 USA.
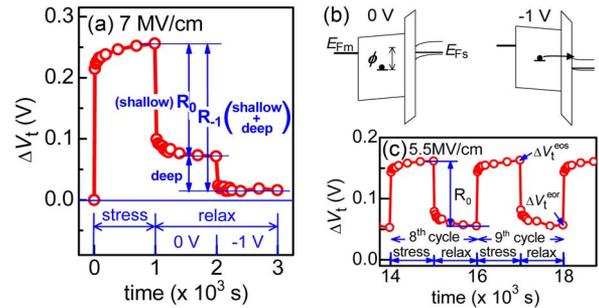
Fig. 1. (a) Evolution of threshold voltage shift ΔV_t during a cycle of PBTI stress and relaxation. (b) Schematic energy band diagram for the TiN/HfO$_2$/Si structure showing 1) a detrapping barrier ϕ of a deep electron trap under $V_g = 0$ V and 2) lowering of the barrier by a negative gate bias. (c) Typical evolution of ΔV_t under stress/relaxation ($V_g = 0$ V) cycling.

II. Experimental Details

The test devices were n-MOSFETs with 0.25 and 10 μm drawn channel length and width, respectively. The gate stack consists of a 3-nm atomic-layer-deposited HfO$_2$ and a $\sim$0.9-nm SiO$_x$ interfacial layer. The equivalent oxide thickness (EOT) is 1.4 nm. The devices were subjected to alternating PBTI stress and relaxation phases, each lasting 1×10^3 s. A stress phase and the consecutive relaxation phase are defined as one dynamic PBTI (DPBTI) cycle. During stressing, the oxide stress field (defined as $(V_g - V_{t0})$/EOT; V_{t0} is prestress V_t) was set at either 5.5 or 7 MV/cm, whereas the relaxation was performed at $V_g = 0$ or -1 V. The temperature was fixed at 100 °C throughout. At certain time intervals, the linear transfer curve was measured by an ultrafast switching method, with a drain-current resolution of 1 μA and a delay time of 60 ns [13]. V_t shift was extracted by the constant subthreshold current (15-μA) method. Gate current was measured before the first and after the last DPBTI cycle to monitor bulk trap generation.

III. Results and Discussion

Fig. 1(a) depicts the variation of ΔV_t in a typical DPBTI cycle. After the ΔV_t recovery has reached a "plateau" under $V_g = 0$ V, a change in V_g to -1 V is seen to trigger another abrupt ΔV_t reduction. This gate-polarity-dependent ΔV_t recovery implies that a fraction of the trapped electrons are situated at relatively deep trap states. A long time is needed for an electron at a deep trap to be emitted under $V_g = 0$ V, due to the barrier between the trap level and the Si conduction band edge E_C [see Fig. 1(b)]. The emission time is, however, drastically reduced when the trap state is "raised" toward E_C by a negative V_g, which explains the sudden decrease in ΔV_t after $V_g = -1$ V
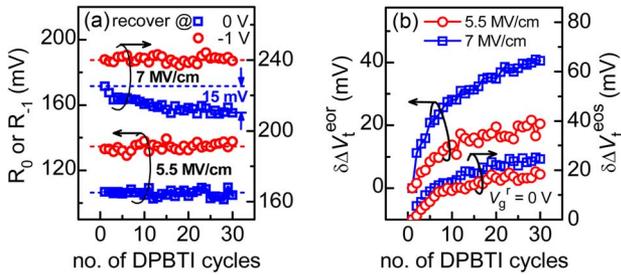
Fig. 2. (a) Evolution of ΔV_t recovery per cycle under a 0 V (R_0) and -1 V (R_{-1}) gate relaxation voltage as a function of the number of DPBTI cycles. (b) Increase in ΔV_t^{eos} (or $\delta\Delta V_t^{\text{eos}}$) with respect to the ΔV_t^{eos} of the first cycle, i.e., $\delta\Delta V_t^{\text{eos}} = \Delta V_t^{\text{eos}}$ (nth cycle) $- \Delta V_t^{\text{eos}}$(first cycle), as a function of the number of DPBTI cycles. A similar definition applies to $\delta\Delta V_t^{\text{eor}}$.

is applied [see Fig. 1(a)]. The remnant ΔV_t is ~ 0, implying that impact of stress-induced interface state generation is far less than electron trapping at preexisting defects [3], [4]. This agrees with the unchanged peak transconductance of the device after stress (not shown).

The evolution of ΔV_t under multiple stress and relaxation ($V_g = 0$) cycles is depicted in Fig. 1(c). The ΔV_t recovery per cycle or R_0 can be regarded as a measure of electrons emitted, within the given relaxation interval, from a spectrum of relatively shallow traps [cf., Fig. 1(a)]. When the oxide stress field is 5.5 MV/cm, R_0 can be observed to remain approximately constant, independent of the number of DPBTI cycles [see Fig. 2(a)]. This result implies that it is the similar group of preexisting oxide traps that are charged and discharged, respectively, under a given stress and relaxation condition. However, when a higher oxide stress field (7 MV/cm) is applied, a *progressive decrease* in R_0 is observed. When the oxide field is further increased to 8.5 MV/cm, a greater but also gradual decrease in R_0 is obtained (not shown). The results in Fig. 2(a) also show that the R_0 decrease depends mainly on the applied oxide stress field, i.e., electron trapping alone does not induce the reduction in R_0.

To probe the reason for the gradual reduction in R_0, we examine, in Fig. 2(b), the increase in ΔV_t^{eos} and ΔV_t^{eor} in subsequent DPBTI cycles, which was measured with reference to the respective ΔV_t^{eos} and ΔV_t^{eor} of the first DPBTI cycle. ΔV_t^{eos} is the V_t shift at the end of each stress phase, just before the onset of relaxation [see Fig. 1(c)] and is a measure of the *total* electron trapping in the gate stack. On the other hand, ΔV_t^{eor} is the V_t shift at the end of each relaxation phase and is a measure of the remaining trapped electrons, which could not be emitted within the given relaxation interval, i.e., electrons trapped at deeper oxide traps. For the 5.5-MV/cm stress, although R_0 is constant, ΔV_t^{eor} (and ΔV_t^{eos}) still increase with the number of DPBTI cycles. This increase in ΔV_t^{eor} may be attributed mainly to the filling of originally deep oxide traps,[1] which could not be detrapped within the given relaxation interval [contribution of stress-induced interface states is minor,

[1]Electron trapping at an oxide trap with energy state $E_t < E_F$ (Fermi energy of the tunneling electrons) may not happen instantaneously during stressing. The trapping barrier controlling the electron capture time is determined by a complex interplay of the nature of the defect and the neighboring oxide network (e.g., [14]). Therefore, it may take longer times to fill deep traps as compared to some shallow traps in resonance with the tunneling electrons.
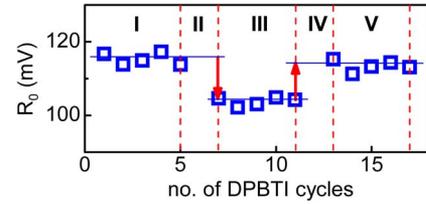

Fig. 3. Phase I: A fresh n-MOSFET was subjected to PBTI stress (at 5.5 MV/cm) and recovery (at 0 V) for five cycles and R_0 for each cycle noted; Phase II: The device was then subjected to PBTI stress (at 7 MV/cm) and recovery (at 0 V) for 30 cycles [evolution of R_0 in this case is not shown; cf., Fig. 2(a)]; Phase III: A repeat of phase I gave a smaller R_0; Phase IV: The device was relaxed under $V_g = -1$ V; Phase V: A repeat of phase I saw a restoration of R_0.

since transconductance degrades $< 5\%$ after 30 DPBTI cycles (not shown)]. The constant R_0 implies that all shallow oxide traps within a certain energy range are always filled and that the filling of these traps is not affected by the filling of deep oxide traps, i.e., the oxide traps do not interact. For the 7-MV/cm stress, the increase in the ΔV_t^{eos} per cycle is comparable with that of the 5.5-MV/cm stress, but the increase in the ΔV_t^{eor} per cycle is much larger. The former implies that the incremental electron trapping per cycle at originally deep oxide traps is similar for both oxide stress fields. The latter implies that the remaining electrons trapped at deep oxide traps after each $V_g = 0$ V relaxation phase increase more quickly under the 7-MV/cm stress. As only electrons captured at relatively shallow oxide traps could be emitted over a given relaxation interval, this observation implies that the fraction of electrons trapped at deep oxide traps increases more quickly under the 7-MV/cm stress. Given that the incremental electron trapping per cycle at originally deep oxide traps is similar for both oxide stress fields, the results thus imply that the gradual reduction in R_0 under the 7-MV/cm stress is due to some of the formerly shallow oxide traps being transformed into deeper traps after every stress phase. We speculate that such transformation may involve the transition from a metastable shallow trap state to a deeper trap state [15], facilitated by oxide-field-induced lowering of the energy barrier.

To check our inference, a negative V_g of -1 V instead of 0 V was applied during relaxation. The evolution of R_{-1} (ΔV_t recovery per cycle under $V_g = -1$ V) is examined as a function of DPBTI cycles [see Fig. 2(a)]. Clearly, R_{-1} is larger than R_0 because electrons trapped at deep oxide traps could be also emitted, in addition to those emitted from shallow oxide traps under $V_g = 0$ V. More interestingly, the decrease in R_0 (seen under the 7-MV/cm stress) is no longer observed for R_{-1}. Since a negative V_g could detrap most of the electrons trapped at deep oxide traps [cf., Fig. 1(a)], almost the entire spectrum of oxide traps is sensed, regardless if some shallow oxide traps have been transformed into deeper traps. This result supports our inference that the decrease in R_0 stems from shallow-to-deep oxide trap transformation.

Further evidence, which supports our inference, is given in Fig. 3. One would expect that once a shallow oxide trap has transited to a deeper level, it would be rendered inactive and no longer participate in DPBTI. This is indeed observed in Fig. 3. An n-MOSFET was first stressed at 5.5-MV/cm oxide field and relaxed at $V_g = 0$ V repeatedly for five cycles, and R_0 was
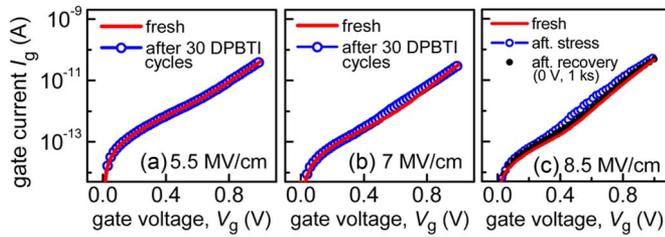
Fig. 4. No generation of SILC or bulk traps can be observed (a) when R_0 is constant and (b) when it is decreased. (c) Increase in the gate current remains very marginal even after *continuous* stressing at a much higher oxide field (8.5 MV/cm) for 5×10^3 s.

recorded. The device was then stressed at 7-MV/cm oxide field and relaxed at $V_g = 0$ V for 30 cycles. During this test, the ΔV_t recovery per cycle gradually decreased with the DPBTI cycles, similar to the result shown in Fig. 2(a). The DPBTI test at 5.5-MV/cm oxide field and $V_g = 0$ V relaxation was then repeated. R_0 is now smaller (by $\sim$15 mV), indicating that some of the shallow oxide traps are no longer active after the DPBTI test at 7-MV/cm oxide field.

It is also shown in Fig. 3 that shallow oxide traps that had transformed into deeper traps could be reactivated after a negative V_g relaxation. After a $V_g = -1$ V relaxation, the device was again subjected to the DPBTI test at 5.5 MV/cm oxide field. Evidently, R_0 is now back to almost the same level as that of the pristine device when it was first subjected to the same 5.5 MV/cm DPBTI test, indicating that the shallow-to-deep oxide trap transformation is reversible.

While the evolution of electron detrapping under low and high PBTI stress fields is similar to that of hole detrapping of DNBTI [7]–[12], some differences should be noted. For DNBTI, the decrease in hole detrapping is not suppressed by a positive gate relaxation voltage [7, Fig. 8], i.e., the decrease is largely irreversible. This is contrary to DPBTI, where the decrease in electron detrapping is almost entirely eliminated under a negative relaxation V_g [see Fig. 2(a)]. Moreover, the decrease in hole detrapping under DNBTI correlates with the growth of stress-induced leakage current (SILC), which reflects on the bulk trap density [10]–[12]. The SILC increase is found to be rather permanent (i.e., no apparent recovery under an opposite-polarity V_g sweep and after an extended relaxation period). On the other hand, no apparent SILC growth is observed in our devices when the electron detrapping under DPBTI is decreased (see Fig. 4). One might expect that different defects are active in NBTI and PBTI and understanding the difference in the evolution of hole and electron detrapping under these two stresses needs to be further investigated.

IV. SUMMARY

Repetitive stress/relaxation experiments have shown that electron detrapping under DPBTI is gradually reduced with the number of stress/relaxation cycles, implying that the emission time of the trapped electrons are slowly increased under the

PBTI stress. A greater decrease in the electron detrapping is observed under a higher oxide stress field. The observation can be interpreted in terms of an increase in the electron detrapping barrier, which may be related to an oxide-field-driven relaxation of the electron trap, into a deeper energy level, as verified by recovery study involving a negative V_g. This letter implies that characteristics of defects in the high-k oxide can be altered, even under moderate electrical stressing. Thus, the general assumption that defect properties are stress invariant may have to be reviewed.

REFERENCES

[1] H. C. H. Wang, C. W. Tsai, S. J. Chen, C. T. Chan, H. J. Lin, Y. Jin, H. J. Tao, S. C. Chen, C. H. Diaz, T. Ong, A. S. Oates, M. S. Liang, and M. H. Chi, "Reliability of HfSiON as gate dielectric for advanced CMOS technology," in *VLSI Symp. Tech. Dig.*, 2005, pp. 170–171.

[2] G. Bersuker, J. H. Sim, C. S. Park, C. D. Young, S. V. Nadkarni, R. Choi, and B. H. Lee, "Mechanism of electron trapping and characteristics of traps in HfO$_2$ gate stacks," *IEEE Trans. Device Mater. Rel.*, vol. 7, no. 1, pp. 138–145, Mar. 2007.

[3] S. Pae, M. Agostinelli, M. Brazier, R. Chau, G. Dewey, T. Ghani, M. Hattendorf, J. Hicks, J. Kavalieros, K. Kuhn, M. Kuhn, J. Maiz, M. Metz, K. Mistry, C. Prasad, S. Ramey, A. Roskowski, J. Sandford, C. Thomas, J. Thomas, C. Wiegand, and J. Wiedemer, "BTI reliability of 45 nm high-K + metal-gate process technology," in *Proc. IRPS*, 2008, pp. 352–357.

[4] A. Kerber, K. Maitra, A. Majumdar, M. Hargrove, R. J. Cater, and E. A. Cartier, "Characterization of fast relaxation during BTI stress in conventional and advanced CMOS devices with HfO$_2$/TiN gate stacks," *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 3175–3183, Nov. 2008.

[5] K. Zhao, J. H. Stathis, A. Kerber, and E. Cartier, "PBTI relaxation dynamics after ac vs. dc stress in high-k/metal gate stacks," in *Proc. IRPS*, 2010, pp. 50–54.

[6] E. Cartier, A. Kerber, T. Ando, M. M. Frank, K. Choi, S. Krishnan, B. Linder, K. Zhao, F. Monsieur, J. Stathis, and V. Narayanan, "Fundamental aspects of HfO$_2$-based high-k metal gate stack reliability and implications on t$_{inv}$-scaling," in *IEDM Tech. Dig.*, 2011, pp. 18.4.1–18.4.4.

[7] Y. Gao, A. A. Boo, Z. Q. Teo, and D. S. Ang, "On the evolution of the recoverable component of the SiON, HfSiON and HfO$_2$ P-MOSFETs under dynamic NBTI," in *Proc. IPRS*, 2011, pp. XT.8.1–XT.8.6.

[8] Y. Gao, D. S. Ang, A. A. Boo, and Z. Q. Teo, "On the dynamic NBTI of the metal/high-κ gate stack p-MOSFET," *Microelectron. Eng.*, vol. 88, no. 7, pp. 1392–1395, Jul. 2011.

[9] T. Grasser, P. J. Wagner, H. Reisinger, T. Aichinger, G. Pobegen, M. Nelhiebel, and B. Kaczer, "Analytic modeling of the bias temperature instability using capture/emission time maps," in *IEDM Tech. Dig.*, 2011, pp. 27.4.1–27.4.4.

[10] Y. Gao, D. S. Ang, C. D. Young, and G. Bersuker, "Evidence for the transformation of switching hole traps into permanent bulk traps under negative-bias temperature stressing of high-k gate P-MOSFETs," in *Proc. IRPS*, 2012, pp. 5A.5.1–5A.5.5.

[11] A. A. Boo, D. S. Ang, Z. Q. Teo, and K. C. Leong, "Correlation between oxide trap generation and negative-bias temperature instability," *IEEE Electron Device Lett.*, vol. 33, no. 4, pp. 486–488, Apr. 2012.

[12] A. A. Boo and D. S. Ang, "Evolution of hole trapping in the oxynitride gate P-MOSFET subjected to negative-bias temperature stressing," *IEEE Trans. Electron Devices*, vol. 59, no. 11, pp. 3133–3136, Nov. 2012.

[13] G. A. Du, D. S. Ang, Z. Q. Teo, and Y. Z. Hu, "Ultrafast measurement on NBTI," *IEEE Electron Device Lett.*, vol. 30, no. 3, pp. 275–277, Mar. 2009.

[14] G. Bersuker, D. Heh, C. D. Young, L. Morassi, A. Padovani, L. Larcher, K. S. Yew, Y. C. Ong, D. S. Ang, K. L. Pey, and W. L. Taylor, "Mechanism of high-k dielectric-induced breakdown of the interfacial SiO$_2$ layer," in *Proc. IRPS*, 2010, pp. 373–378.

[15] T. Grasser, "On the frequency dependence of the bias temperature instability," in *Proc. IRPS*, 2012, pp. XT.8.1–XT.8.7.