Investigating the Electromigration Reliability of Copper Interconnects

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Abstract

With changing materials systems and interconnect architectures from Al based metallization to Cu dual damascene based metallization, electromigration (EM) continues to be a major reliability concern. The objectives of this research are to investigate EM behavior of Cu interconnects, develop an in-depth understanding of the EM-induced voiding mechanisms, and lastly to suggest methodologies to improve the reliability of dual damascene Cu interconnects.

Via-fed Cu interconnects that represent the dual damascene architecture were investigated using package level electromigration tests and failure analysis techniques. Effect of reservoirs at the Cu via regions on electromigration performance was studied in these structures. Based on experimental data and finite element analysis (FEA) based calculations, a critical dimension of 60 nm via extension was identified beyond which increasing extension lengths ceases to prolong electromigration lifetimes. Previous studies have provided support for the notion that the Cu/dielectric-cap interface provides the fastest EM diffusion path. Microstructural observations with focused ion beam (FIB) and electron microscopy indicated the preferential accumulation of voids at the $Cu/SiN_x/Ta$ edges thus indicating that the Cu/dielectric-cap/liner edges would serve as the dominant diffusion path under electromigration stressing.

Improvement in EM failure times was observed in pulse-plated Cu interconnects which were characterised by a smooth Cu/SiN_x interface and even Cu grain boundaries. Poorer EM performance of DC-plated and multistep plated Cu interconnects was attributed to the poor quality of the Cu/SiN_x interface and grain boundaries connected with surface defects. It was also observed that the Cu grain size at M1 end below the cathode via decreases possibly due to recrystallization caused by high temperature exposures aided by electromigration induced high compressive stresses.

Electromigration-induced voiding mechanisms simulated by means of a simple dynamic model based on Monte Carlo methodologies. Two parameters, electron wind force, and bonding energy, were considered. The preferential role of the $Cu/SiN_x/Ta$ edge, the effects of microstructure and interface conditions on voids behaviour under electron wind force, in combination with EM failure mechanisms were analyzed and explained qualitatively by these simplified, novel Monte Carlo simulations.

Chapter One: Introduction

1.1 Background

Modern microelectronics continues to evolve being driven incessantly by system demands of higher functionality, sophistication, and reliability in less space and lower cost. As the complexity of multilayer metallization increases, reliability continues to be a significant concern in integrated circuit (IC) technology. One of the most important reliability problems of thin film metallurgy in ultra large scale integration (ULSI) is electromigration (EM) induced open circuit failures in interconnects. Electromigration was first identified as a serious reliability concern in the Al-based circuits in 1967 [1]. At high current densities the ballistic impact between the electrons and the Cu ions causes the Cu ions to accumulate at the anode end causing metal extrusions leading to electrical short circuits, and causing voiding at the cathode end leading to electrical open circuits. This phenomenon referred to as electromigration, after more than thirty years of investigations, remains a dominant reliability concern for the modern ICs due to the aggressive decrease of interconnect dimensions and the comparably aggressive increase of current densities required during operation [2].

Since late 1990's, copper has been increasingly used as the conductor material for interconnect metallization of advanced ULSI circuits. In comparison with aluminium, copper with a lower resistance value, yields a lower Resistance- Capacitance (RC) delay and is also expected to be more robust against electromigration failure due to the strong Cu-Cu bonds as indicated by its higher melting temperature. Copper has the second lowest resistivity of any non-superconductor, with only about 5% of difference in

resistivity from silver (Table1.1) [3-7].

Table1.1 Properties of metal for interconnects [3-7].

Material	Resistivity (μΩ·cm)	Melting Point(K)	RC Delay (ps/mm)	EM Resistance	Diffusivity (in SiO_2)
Cu	1. 67	1356	2.3	High	Very High
Ag	1.59	1235	2.2	Very low	High
Au	2.35	1337	3.2	Very high	Very high
Al	2.66	933	3.7	Low	Low
W	5.65	3660	7.8	Very high	Low

With low resistivity as compared to the widely used conductor material aluminium, higher average currents are possible using copper for a given voltage. Higher currents are desirable from a performance standpoint. Since Cu has a much higher melting temperature (1356 K) than Al (933 K), a better electromigration performance is also expected. Major considerations with Cu are its extremely high diffusivity in silica glass or polymer dielectrics, and its proneness to corrosion.

Electromigration occurs when diffusing metal atoms are bombarded by conductive electrons and effectively pushed in the direction of electron flow. Since metal atom diffusion is thought to be the root cause of electromigration failure, whatever impacts diffusion correspondingly impacts electromigration [8]. Three kinds of atomic diffusion routes in metal thin films are: surface diffusion, grain boundary diffusion and lattice diffusion. Table 1.2 gives the different diffusion activation energy (E_a) of metal thin films.

Table1.2 Different Activation energy of metal thin films [3-7].

Metal	Interface diffusion (eV)	Surface diffusion (eV)	Grain boundary diffusion (eV)	Lattice diffusion (eV)
Cu	0.9-1.2	0.7	1.2	2.2
Al-5%Cu	0.9-1.2	NA	0.6-0.7	1.2
Al	NA	0.31	0.55	1.4
Ag	0.73	NA	0.88	1.8

In addition to its high tendency to diffuse along the dielectric silica glass interface, unlike Al, Cu is very prone to diffusing into the silica dielectric [8]. Therefore, the Si devices must be protected from Cu atoms diffusing into the single crystal Si. This must be accomplished either through preparation of the dielectric layers between the metallization and the Si and by introduction of a diffusion barrier. Often a refractory metal such as Ta, TaN, Ti or their combination such as Ti/W is used for this purpose. These barrier layers serve as prevention for Cu diffusion at temperatures below 873 K [9, 10].

1.2 Motivation for the Present Research Investigation

Al or Al-based interconnects is an established and mature technology with an advanced level of research and understanding of electromigration and other reliability mechanisms [11-14]. In comparison, Cu interconnects are relative newcomers; they are not as well understood as Al interconnects either in integration or reliability issues. With the introduction of low dielectric constant (low-*k*) materials as insulators, the interconnect reliability challenges have intensified. An understanding of how copper will perform in the new surrounding environment needs to be urgently addressed. The varying reliability concerns between Al and Cu interconnects stem from two areas: the differences in the

material properties and in the integration scheme. The integration scheme is ultimately determined by the material properties and manufacturing cost. These differences render that experiences in Al interconnect reliability were not totally applicable to Cu interconnects, thus necessitating further inquiry into systematic reliability studies in these materials and interconnect architectures [15].

This study will address the effects of interconnect structure, microstructure, and interfacial conditions on electromigration. The impact of electromigration on Cu surface evolution and interconnect microstructural change would also be taken into account.

1.2.1 Dependence of interconnect structure on electromigration

Continuous downscaling of the interconnect feature size of devices has been driven by faster circuit speed, high chip functionality, and lower per-function cost. This downscaling is pushing current density upward on the order of at least 10^6 A/cm^2, which has greatly increased the attention towards the electromigration reliability issue [16, 17]. To reduce the impact of high current density and minimize the chip size, some studies considering the effect of interconnect structure in dual damascene architecture on Cu reliability were reported [18-22]. The design of single via and narrow lines with cathode and/or anode extension is commonly used in real Cu metallization. Schematic of a dual damascene via-fed Cu interconnect structure used in most studies is illustrated in Figure 1.1. However, few experimental studies of the effect of this interconnect structure especially the line extension on electromigration behavior in Cu interconnects have been reported so far. A detailed understanding of this effect on electromigration reliability is required for effective operation of these devices.

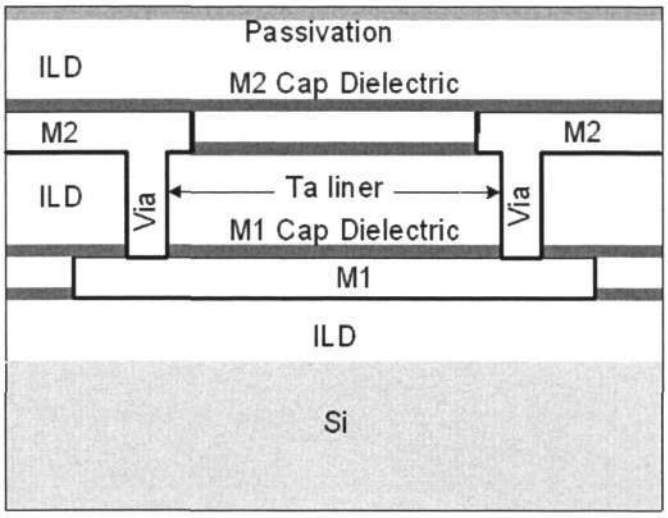


Figure1.1 Dual damascene Cu interconnects schematic structure.

1.2.2 Effects of surface engineering and Cu microstructure on EM

Cu interconnects have the lowest activation energy for interface diffusion, with the interface between the dielectric cap and the Cu conductive line serving as the fast diffusion path [15, 23]. Efforts on Cu surface modification include surface treatments after and/or surface coating before dielectric cap deposition and the use of different dielectric-cap layers such as SiN_x, SiNC and variants thereof [24-29]. Although some initial efforts in this field are emerging in electromigration, the effects of these changes and a change of dielectric cap composition on electromigration are still of great importance.

In case the Cu/dielectric-cap interface conditions are improved to some extent the microstructure of Cu interconnect will play an important role in impacting electromigration behavior. In advanced backend-of-line (BEOL) manufacturing processs used for Cu interconnects, bamboo or near-bamboo-like microstructure became the main

microstructure style in Cu interconnects to decrease the number of Cu grain boundaries hence to escape Cu from grain boundary diffusion [30-34]. However, the percentage of Cu grain boundaries to the volume of the whole interconnects has few changes [35-37]. Thus Cu grain boundary effect on the reliability of interconnects turned out to be more important in microstructure effect study.

This study will execute the effects of surface engineering and microstructure on electromigration reliability of Cu interconnects and will compare them with electromigration results available from related studies in Nanyang Technological University (NTU), *Singapore* and Advanced Micro Device (AMD), *Dresden, Germany*.

1.2.3 Impact of EM on surface morphology and bulk microstructure

Electromigration refers to the motion of atoms induced by the electron flow. The resulting atomic transport leads to the redistribution of atoms and vacancies, and eventually the reconstruct of Cu surface morphology and bulk microstructure along with the formation of voids or metal extrusions. Surface and microstructure morphology evolution in Cu interconnects takes place to reduce the total free energy that may include the interfacial energy and bulk electrostatic energy under applied electrical field [38]. Since the complexity and nonlinear nature of surface and microstructure evolution, numerical instead of experimental approaches [39, 40] are often employed to deal with the observation of surface and microstructure morphology change under electromigration stressing.

The studies of the influence of microstructure and surface morphology on electromigration reliability have been carried out from several perspectives in recent years. However, the great impacts of electromigration on the change of morphological and

microstructural evolution in Cu interconnect are relatively lack of consideration by support of experiments. In this study, the surface morphology and bulk microstructure evolution as the direct and indirect results of electromigration stress would be studied in detail.

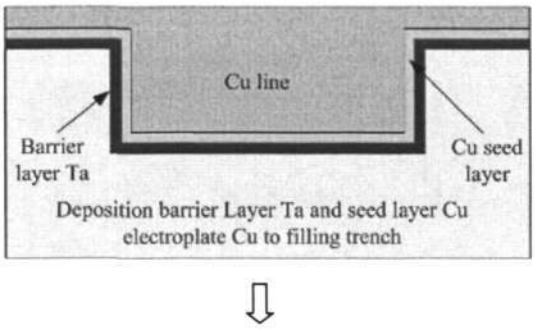
1.3 Objectives

1) Study the influence of interconnects structure on electromigration behavior of dual damascene Cu interconnects. In particular the study will focus on the understanding of the reservoir effect and investigate the mechanism that impacts electromigration reliability related to interconnect design.
2) Investigate the influence of surface treatment and bulk microstructure on the electromigration reliability of Cu interconnects. In particular, effect of surface treatments and the impact varied Cu microstructures created by different electroplating techniques were investigated.
3) Study the impact of electromigration stressing on the change of Cu surface morphology and bulk microstructure in Cu interconnects and approach the further understanding for the process of Cu atom and vacancy redistribution.
4) To develop a novel simplified Monte Carlo simulation methodology to comprehend the contribution of the above factors to electromigration.

Chapter Two: Literature Review

2.1 Cu damascene interconnects

As ULSI devices shrink in size and high levels of integration become the norm, Cu is expected to replace Al in ULSI interconnects for continued improvements in IC performance. The dual damascene fabrication process is presently recognized as a standard Cu interconnect technique. In this technique, metallic barrier layers and Cu seed layers are deposited inside walls of via holes or trenches using sputtering, physical vapour deposition (PVD), and Cu interconnects are then embedded into the via holes or trenches using an electrochemical deposition method (ECD) or electroplating method [41]. Then chemical-mechanical polishing (CMP) is used to remove the excess Cu and metal liner. Blanket dielectric was deposited for the next level in succession. As for the scale increasing seek, the multiple levels of interconnects are required in deep submicron metallization, the global planarization at each interconnect level is critical. It facilitates deep submicron lithography within a small depth-of-focus. A uniform interconnect height at each level simplifies via etching with the same depth. In the multilevel interconnect structures, successive levels of interconnects are connected by vias. This processing can be illustrated using Figure 2.1 [42].



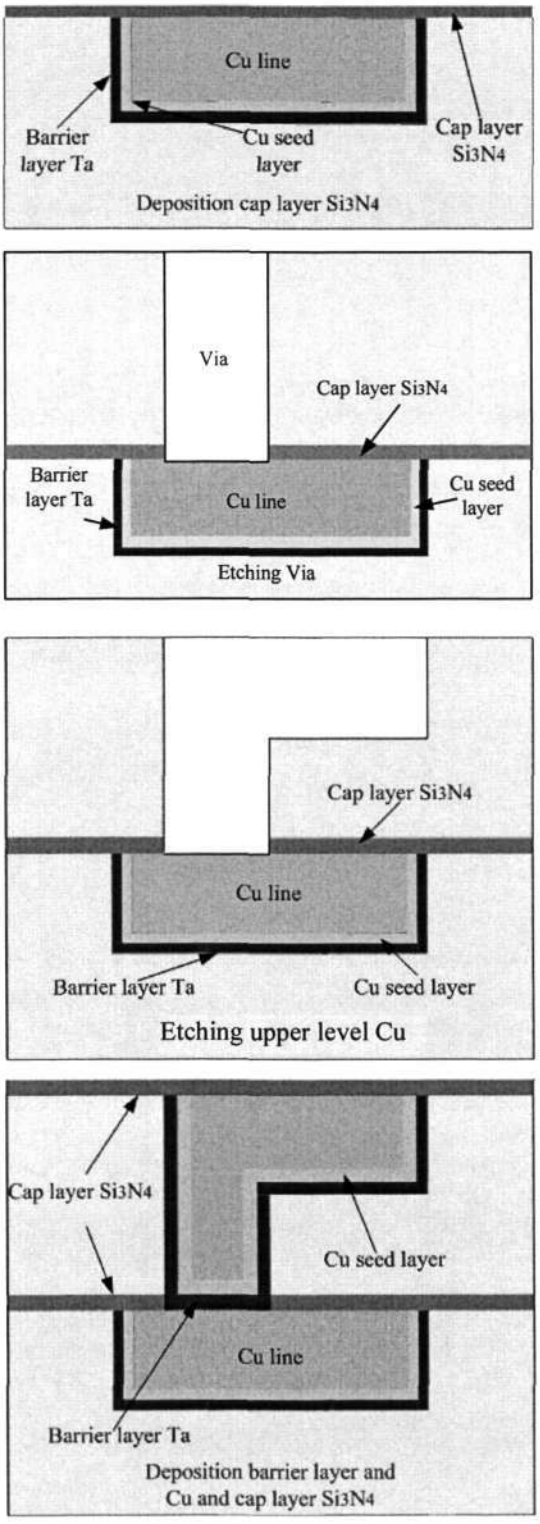


Figure 2.1 Illustration of Cu dual damascene processes.

2.2 Electromigration fundamentals

2.2.1 Basic physics of electromigration

Electromigration is widely accepted as the description as the mass transport of metal ions in a conductor as a result of momentum transfer from electrons traveling under the influence of an applied electrical field [43]. It is basically a diffusion process of bulk and surface atoms under the influence of a driving force. The electron wind action, as one of the electromigration driving force is given by Equation 2.1.

$$\vec{F}_{wd} = Z^{*} \cdot e \cdot \rho \cdot \vec{j} \tag{2.1}$$

The driving force has two major components. One is the direct electrostatic interaction between the applied field and the atoms. The other one, denoted as the "wind force" and believed to be dominant, is due to momentum transfer from the conduction electrons impinging upon the atomic cores [44]. The electromigration force can be given by

$$\vec{F}_{EM} = \vec{F}_{wd} + \vec{F}_{d} \tag{2.2}$$

Where $\vec{F}_{wd}$ and $\vec{F}_{d}$ is electron wind force and direct force respectively. In addition to atoms diffusion, there is another force, which has the opposite direction of electron flow, called back stress force. This force is related to the stress gradient induced by atomic motion to cathode end along the interconnects. As a result, atomic flux during electromigration is the combination of these two forces, which is given by [1]

$$J_{a} = \frac{DC_{a}}{k_{B}T}\left(\rho \cdot \vec{j} \cdot q \cdot Z^{*} - \Omega \frac{\partial \sigma}{\partial x}\right) \tag{2.3}$$

Where D is effective diffusion coefficient, C_{a} is atomic concentration, k_{B} is

Boltzmann's constant, Z^* is effective charge number, ρ is interconnects resistivity, $\vec{j}$ is current density applied , Ω is atomic volume and $\frac{\partial \sigma}{\partial x}$ is stress gradient along the line, respectively.

Because electromigration drift velocity under applied electron field can be expressed by

$$\vec{v}_d = \frac{D\vec{F}_{EM}}{k_B T} \tag{2.4}$$

Where D is the atomic diffusion coefficient of conductive material, which is given by Equation 2.5 as the function of temperature.

$$D = D_0 \exp\left(\frac{-E_a}{k_B T}\right) \tag{2.5}$$

Where D_0 is diffusion constant. Therefore, as modified to consider back stress force, the electromigration drift velocity can be revised to be

$$\vec{v} = \frac{D_o}{k_B T}.\exp\left(\frac{-E_a}{k_B T}\right).\left(e.Z^*.\rho.j - \frac{\Delta\sigma}{\partial x}\Omega\right) \tag{2.6}$$

Electromigration is transport phenomenon under the influence of applied electric field and indeed a diffusion phenomenon. The diffusivity is a weighted sum of the atomic diffusivities of all diffusion path in the interconnects. Because Cu interconnects process is referred to as dual damascene when the trench and via are processed together, see Figure 2.2, the resulting set of primary diffusion paths in this interconnect system is: bulk, metal/liner, interface, metal/inter-level diffusion barrier interface, and grain boundary.

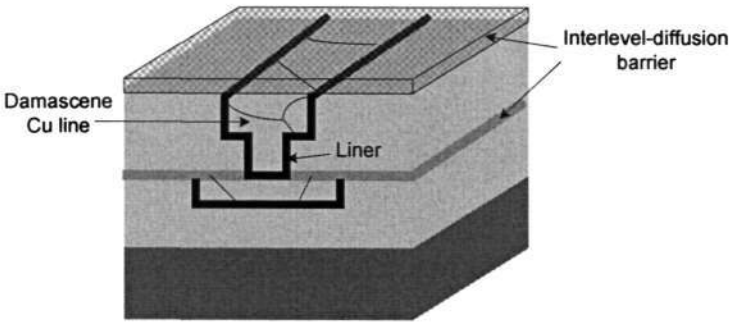


Figure 2.2 Schematic cross section of dual damascene interconnects system.

An expression for the product of Z^* and D for a damascene structure can be written using Equation 2.7 as a weighted sum of all diffusion paths in this interconnects system [45]:

$$Z^*D = Z_L^* n_L D_L + Z_I^* D_I \delta_I \left(2/w + 1/h\right) + Z_S^* D_S \delta_S / h + Z_{GB}^* \sum_j^n D_{GB} \left(\delta_{GB}/d\right) \tag{2.7}$$

where the subscripts L, I, S, and GB refer to the lattice, metal/liner interface, metal/inter-level diffusion barrier surface, and grain boundary, respectively; δ_I, δ_S, and δ_{GB} are the width of the interface, surface and grain boundary, respectively; d is the grain size, w is the line width, h is the line thickness, and n_L, $\delta_I\left(2/w + 1/h\right)$, δ_S/h, and $\left(\delta_{GB}/d\right)$ are the fraction of atoms diffusing through the bulk lattice, interface, surface, and grain boundary of the line, respectively.

2.2.2 Electromigration characterization

There are several methods to characterize electromigration such as low frequency noise measurement [46], ratio of resistance or resistometric [47], internal friction method [48], temperature-ramp resistance analysis (TRACE) [49, 50] as well as wafer-level fast tests like standard wafer-level electromigration accelerated test(SWEAT) [51], breakdown

energy of metal (BEM) method [52, 53] and wafer-level isothermal joule-heated electromigration test (WIJET) [54] are reported. Drift velocity method is another important technique which was invented by Blech [55] and is very elegant method to study electromigration mass transport. In this report the resistometric test will be used to study electromigration. In this test, the resistance change is monitored as a function of time with the test being carried out at temperatures in excess of 300 ^{o}C and in the presence of current densities in excess of 1.2 MA/cm^2.

2.2.3 Time to failure (TTF) in electromigration

Generally lognormal distribution is employed for electromigration time-to- failure statistics, although a few reports have suggested other distributions [56]. The two parameter form has parameters σ = the shape parameter and t_{50} = the median (a scale parameter). The lognormal probability distribution function (PDF) is defined as [57, 58],

$$f(t)=\frac{1}{t\sigma\sqrt{2\Pi}}\exp\left[-\frac{(\ln t-\mu)^2}{2\sigma^2}\right] \tag{2.8}$$

t_f, has a lognormal distribution, then the (natural) logarithm of time-to-failure(TTF) has a normal distribution with mean μ = ln t_{50} (t_{50} is the median of time -to-failure of lognormal distribution) and standard deviation (σ).The lognormal cumulative probability (or failure) distribution function (CDF), which gives the cumulative probability of failure prior to t, is as follows.

$$F(t)=\int_0^t\frac{1}{t\sigma\sqrt{2\Pi}}\exp\left[-\frac{(\ln t-\ln t_{50})^2}{2\sigma^2}\right].dt=\phi\left(\frac{\ln t-\ln t_{50}}{\sigma}\right) \tag{2.9}$$

Where, $\phi(z)$ denotes the standard normal CDF.

The TTF failure data is generally analyzed using probability plots, which is a simple visual method for performing goodness-of-fit (GOF) analysis and also obtaining estimates of the mean and standard deviation of the data. It consists of analyzing reliability data by plotting CDF estimates against time. Lognormal CDF can be re-rewritten as

$$\ln t = \sigma\phi^{-1}\{F(t)\} + \ln t_{50} \tag{2.10}$$

Where ϕ^{-1} denotes the inverse function for the standard normal distribution. If we let $y = t$ and $x = \phi^{-1}\{F(t)\}$, then ln y is linear in x with slope σ and intercept (when $F(t) = 0.5$) of $\ln t_{50}$. If the data are consistent with a lognormal model, the resulting plot will have points that line up roughly on a straight line with slope σ and intercept t_{50} on the y-axis.

The electronic industry uses the Median time to failure (MTF) analysis to predict the life time of a device. In 1969, Black provided the following empirical equation to analyze failure in Al interconnects caused by electromigration [24]:

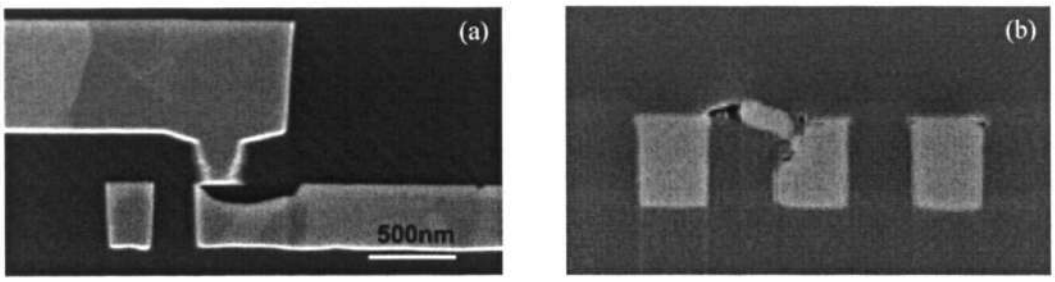
$$MTF = A \cdot j^{-n} \cdot \exp\left(\frac{E_a}{k_B T}\right) \tag{2.11}$$

Where A is an empirical-determined constant, j is the current density, n is the current density exponent, E_a is the activation energy to electromigration failure, and k_B and T have been previously defined. The derivation of the equation was based on an estimate of the rate of forming a void across Al interconnects. The most interesting feature of the equation is the dependence of MTF on the square power of current density, i. e., the current density exponent n=1, 2, or a large number has been controversial, especially

when the effect of Joule Heating is taken in to account.

2.2.4 Electromigration failure modes

The electric field applied across interconnects causes the net motion of metallic atoms in the direction of the electron flow (i.e. from cathode to anode). This net flux of atoms caused by electromigration is a reliability concern because it can lead to interconnect failure at sites of atomic flux divergence. At sites where there is a net depletion of atoms, local stresses become increasingly tensile, which can eventually lead to voiding in the interconnect once a critical tensile stress value σ_{crit} is reached [59] and can subsequently lead to failure by open circuit (see Figure 2.3 (a)). At sites where there is a net accumulation of atoms, the local stresses become increasingly compressive, which can lead to the formation of metallic extrusions (see Figure 2.3 (b)). A failure by short circuit may result if the extruded metal touches a neighbouring interconnect or via.



(a) EM induced void at cathode [60]. (b) EM induced extrusion at anode [61].

Figure 2.3 Examples of electromigration induced failure in interconnects.

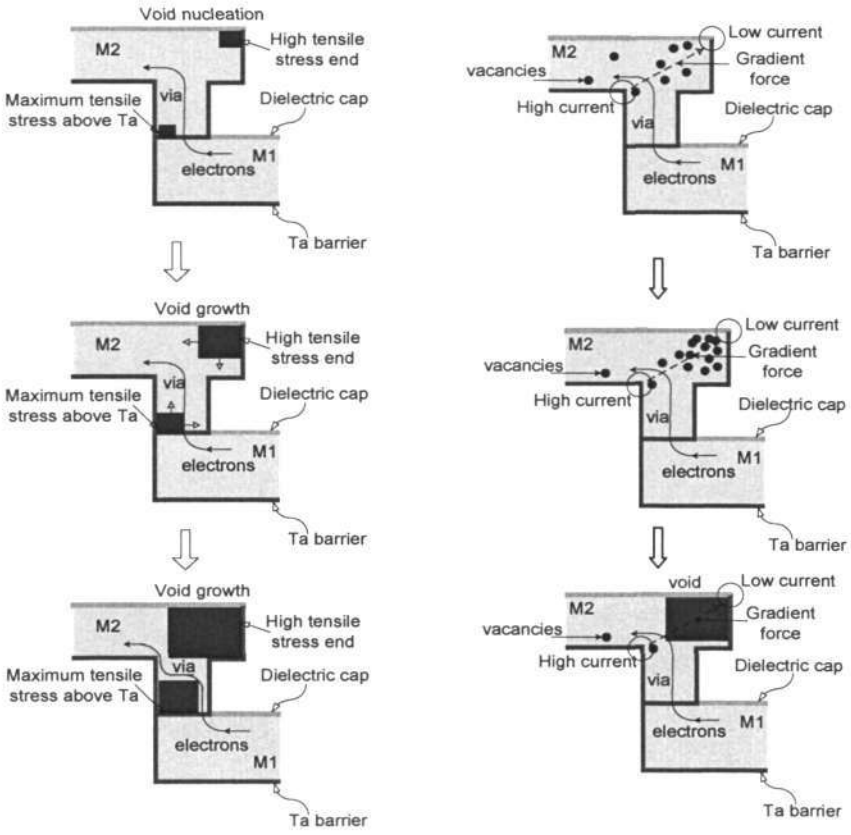
Electromigration induced voids have various modalities and locations due to the different effective factors, such as metal line level, dielectric type, and via component and

position. For example, in M2 test structures, voids initially formed at the interface between Cu and cap and at the top of via, then extended along the M2 line. Whereas in M1 structures, voids were found to be below the via. The voids seem to propagate along the Cu/dielectric cap interface [62].

2.2.5 Current understanding of electromigration failure mechanism

Currently, there are two common understanding of EM mechanism. One is tensile stress theory which proposes that a tensile stress develops at the cathode end of the via during electromigration, where the Ta liner forms a blocking boundary to the diffusing Cu. When the critical tensile stress for void nucleation is reached, a void forms [63]. In M2 interconnects, the maximum tensile stress is reached at the base of the via. Figure 2.4 (a) illustrates the tensile stress theory.

Another theory was proposed for explaining voids formed in the low current density region such as reservoirs. This current crowding theory explained that due to current density gradient induced vacancy drift [64], there should be vacancy accumulation and super-saturation in the upper corner of M2 line extension [24]. According to this theory, there is a current density gradient between lower corner to extension in M2 line above the via, which may induce a flux of vacancies to accumulate at the upper corner, which is illustrated in Figure 2.4 (b). A void will nucleate, grow, and eventually deplete the entire cathode end of the strip. Both of these theories propose that void should nucleate at the cathode via region and subsequently coalesce and grow. Neither of these theories explains recent in-situ electromigration observations that demonstrate that voids nucleate heterogeneously at the Cu/SiN_x interface and migrate towards the cathode end to cause failures [65].



(a) (b)

Figure2.4 Current understanding of electromigration mechanisms (a) Illustration of Tensile stress theory; (b) Illustration of current crowding theory.

2.3 Factors that affect electromigration

Electromigration has been identified as a major failure mode in metallic interconnects of microelectronic integrated circuits for over three decades. The problem of electromigration has been extensively investigated both experimentally and theoretically. The factors that effect electromigration are believed to be as follows:

2.3.1 Interconnects structure

Due to miniaturization of integrated circuits, thin-film metallic interconnects are subjected to increasingly high current densities. It is therefore of great technological importance to understand the impact of interconnect geometrical design on electromigration lifetimes [66-70]. A number of investigations have been carried out on the effect of interconnects length and width on electromigration in Cu damascene interconnects [71-73]. It was reported that due to the sufficient back flow stress gradient in the interconnect, a critical length effect is present impacting electromigration lifetime, which addresses a key interconnect reliability and design concern [74]. Assuming a linear dependence between the interconnect line stress and length, the one-dimensional EM drift equation explains how certain line lengths are less prone to EM induced interconnect failure due to compensating back flow stress and is commonly written as [75]:

$$v_d(j,L)=\frac{D_{eff}}{k_B T}\left[Z^*_{eff} e\rho j-\Omega\Delta\sigma/L\right] \tag{2.12}$$

where v_d is the average drift velocity of Cu ions, D_{eff} is an effective diffusivity, $Z^*_{eff}e$ is the effective charge, ρ is the electrical resistivity, j is the current density, Ω is the atomic volume, $\Delta\sigma$ is the stress difference between anode and cathode end, and L is the line length. Besides, the critical length effect on electromigration is also thought to depend on temperature and process defects [20].

2.3.2 Cu/dielectric-cap interface morphology

The interface of interconnects and dielectric cap provides easy migration paths for ions because of the high diffusion coefficient associated to the low surface migration

activation energy, especially in Cu dual damascene interconnects. The self diffusion activation energies of interconnect materials can be referred to Table 1.2. It can be known that for Cu interconnects, which has the lowest activation energy for interface diffusion, the interface between the dielectric cap and the Cu conductive line serves as the fast diffusion path during electromigration stressing.

These suggest that the reliability of Cu interconnects can be improved through the suppression of interfacial diffusion, so that the condition of the top interface of the Cu plays a key role on electromigration reliability. If the Cu/dielectric-cap interface could be altered or modified appropriately, the trends towards increase reliability of future generation of Cu chip may be gained [76, 77]. In order to suppress this fatal interface diffusion in Cu damascene interconnects, a great deal of effects have been adopted. For example, as an effectual method to enhance Cu/dielectric-cap bonding strength, post-CMP Cu surface treatment was adopted to strengthen interface adhesion [26].

2.3.3 Bulk microstructure in interconnect

It has been recognized for a long time that electromigration lifetime is strongly correlated to the geometry and microstructure of the metal lines. A number of early studies have been carried out to investigate the effect of microstructure on electromigration lifetime. The increase of electromigration lifetime with increasing grain size has been reported in A1 conductors with a width exceeding several micrometers [78, 79]. The extent of improvement was found to increase approximately linearly with grain size. **A** subsequent study showed that such an improvement is limited by the ultimate grain size that can be reached by means of primary grain growth [80]. The effects of grain size and grain morphology on electromigration lifetime in Al-Cu fine lines have been

investigated [81]. The electromigration lifetime was found to depend upon the grain size as well as on the grain morphology in metal lines of less than 2 μm wide. By annealing 2.0 μm wide Al-Cu lines at elevated temperatures to induce grain growth, the electromigration lifetime was found to increase until grain growth was constrained by the metal line thickness. The dependence of the electromigration lifetime on grain size in 2.0 μm wide Al-Cu lines is plotted in Figure 2.5.

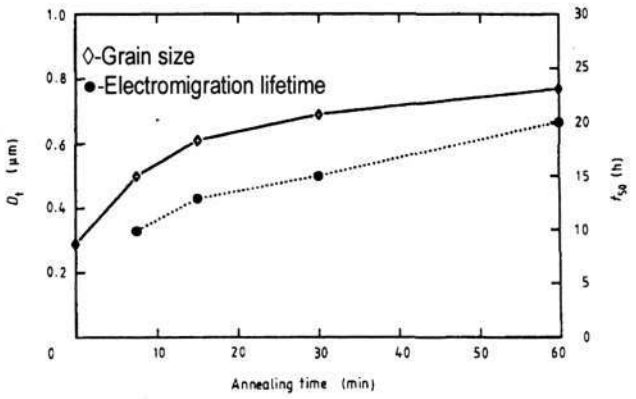


Figure 2.5 EM lifetime as a function of grain size of a 2.0 μm wide Al-Cu line [81].

Electromigration in Cu conductors differs from that in Al or Al alloys in that the mass transport mechanism, at typical integrated circuit operational use conditions, is almost exclusively interfacial diffusion as opposed to grain boundary diffusion [82-84]. As a result, Cu electromigration is relatively insensitive to grain sizes as compared to Al-based interconnects and is more a function of the nature of the interfaces available for mass transport.

In most of the advanced backend-of-line manufacturing process in new technology, owing to the demand of scaling-down of Cu interconnects, bamboo or near-bamboo-like microstructure became the main microstructure morphology in Cu interconnects. Figure

2.6 showed the typical bamboo-like microstructure in damascene Cu interconnects [26]. Bamboo-like microstructure decreases the number of Cu grain boundaries and thereby reduces the grain boundary diffusion of Cu [85, 86]. The ratio of Cu grain boundaries to the volume of the whole interconnects does not change much although the line width and aspect ratio is reducing [87]. Therefore, the effect of Cu grain boundary on the reliability of interconnects could still be important to investigate deeply especially with the developing Cu/dielectric-cap interface conditions.

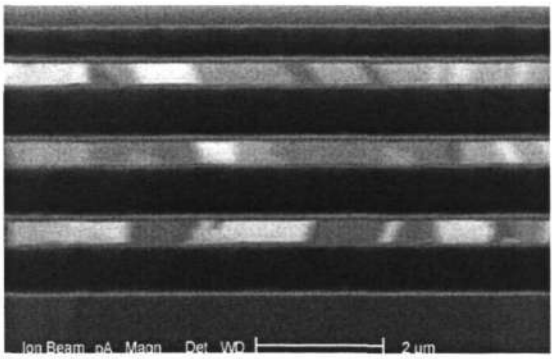


Figure 2.6 FIB cutting SEM image showing bamboo-like grain structure in Cu damascene interconnects [26].

2.4 Impact of EM on surface morphology and bulk microstructure in Cu line

Electromigration is a process in which metal atoms drift as a result of electron impact when an electrical current passes through a metal thin film interconnect. The Cu atoms at Cu/dielectric-cap interface and bulk are activated by electrons and redistribute to reconstruct Cu surface and bulk microstructure in combination with the

electromigration-induced voiding process. This course reduces the interfacial and bulk free energy in Cu interconnects [37].

The impact of electron wind force on surface evolution in Cu interconnects exposed to electromigration and surface diffusion became more interesting in microelectronics technology recently. Cu surface evolution caused by the formation of electromigration-induced voids has been numerically simulated [88-90]. As a matter of fact, Cu surface evolution could be the result impacted both directly and indirectly by electromigration stressing. Electromigration-induced degradation as well as the sample preparation exposed to failure analysis both could contribute to the surface profile change after electromigration stressing. However, there are relatively few reports focusing on the experimental study of the Cu surface morphology change and the root cause behind.

It has been reported that the surface voids induced by electromigration stressing may nucleate at defect sites in the middle of the Cu interconnects, as illustrated in Figure 2.7. Then driven by the electron wind force, the voids may coalesce with other voids, temporarily stop at defects such as grain boundary (GB) triple junctions, detach from these triple junctions, migrate further to reach the cathode via, and finally grow to large enough sizes leading to eventual open circuit failures. As a result, the grain boundaries features in the bulk in Cu interconnect could be changed after atoms and vacancies migration. Thus, migration and coalescence of voids as well as their interactions with grain boundaries in the presence of the electric wind force is crucial for understanding the failure mechanism in Cu interconnects.

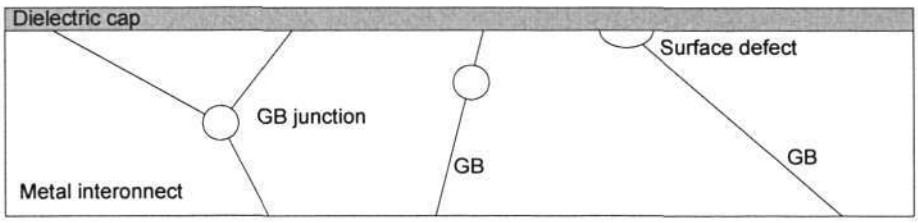


Figure 2.7 Possible cases of void location at interconnect/dielectric cap interface.

2.5 Methods to improve EM behaviour in Cu interconnects

One of the goals in studying electromigration in thin-film conductors is to devise methods to improve the electromigration resistance of interconnects. As seen from the discussion of the electromigration-induced damage formation process, it is clear that the basic requirement for reducing damage is to minimize the local divergence of the atomic flux. This can be accomplished, in principle, by reducing the magnitude of the atomic flux and/or the inhomogeneity of the parameters controlling the mass transport. Since the damage formation process is complex in nature, methods found to be effective often incorporate several factors for reducing the flux divergence.

2.5.1 Interconnect structure design

Although to reduce the flux divergence by modifying the conductive interconnect structures always confronts the limitation from devices scaling down, the risk of high current density, the study of the interconnect structures with an overhang or reservoir region has been recently reported [91-94]. It is thought that the extension of the interconnect could serve as a reservoir for void growth, thus prolonging the median time to failure. Recently, the reservoir effect in Al-Cu interconnect with W vias was reported

[95], where voids are generally initiated at the W/Al interface by large Al atomic flux divergence. It is reported the four times enhancement in electromigration life time was gained by increasing the extension, which is few current area at cathode, from 40 nm to 300 nm in Al-0.5%Cu interconnects [93]. Lower levels of stress and vacancy concentration in the longer reservoir was proposed to contribute to better electromigration reliability of interconnects. However, the reservoir mechanism in dual-damascene Cu interconnects is clearly different than with the W/Al via structures since voids nucleate at the Cu/dielectric-cap interface far from the cathode end and move along the interface towards the cathode end. Because of the technological importance of dual-damascene Cu interconnects, it is necessary to understand how extension lengths impact electromigration lifetimes. Our group recently published some achievement of reservoir effect in Cu interconnects using overlap structure by increasing the reservoir length from 0 to 120 nm [92] and by interconnect tree structure [91, 96]. The influence of extension length on electromigration lifetime in combination with the FEA calculated critical length will be discussed in detail in the results and discussion chapter in this thesis.

2.5.2 Surface engineering effect on electromigration reliability

As the Cu/dielectric-cap interface is the most dominant electromigration path, especially for sub-micron line-width Cu damascene interconnects with bamboo-like grain structure, this interface should be made more electromigration resistant. One kind of the effective methods is surface modification including Cu surface treatment and surface coating. SiH_4 and H_2 plasma surface treatment after Cu CMP was reported to enhance the electromigration reliability of Cu interconnect by the formation the Cu-silicide which may led the higher bonding strength between Cu and dielectric SiN_x cap [27]. A technique is

reported to suppress the electromigration at Cu/dielectric-cap interface [97]. A two-orders-of-magnitude improvement in Cu electromigration lifetime was reported recently when comparing Cu lines coated with a 10-nm-thick, electroless CoWP film to lines with a 35-nm-thick SiC*x*H*y* surface film [97-100]. Besides, the thin (10-20nm) electroless CoSnP, or Pd, with selectively electroless plating [97, 101, 102] were also employed to retard the interface diffusion of Cu interconnects. Figure 2.8 presents this significant intermixing layer of about 2 nm thickness with a high degree of disorder in the interface structure [100]. It is experimentally approved that this intermixing layer consolidated the bonding strength between Cu and dielectric cap and thereby increase the electromigration reliability of Cu interconnects. A significant reduction in electromigration was observed for the coated samples. Although this is a promising technique to effectively suppress electromigration, selective electroless deposition is hindered with problems such as deposition controllability and film quality [101].

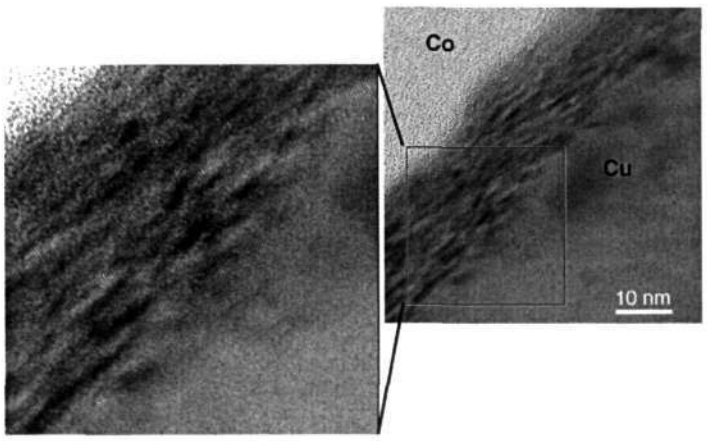


Figure 2.8 TEM bright field image of a Cu/CoWP interface [100].

Other method involving Cu surface passivation by Cu silicide passivation was previously reported [103]. In this study higher lifetime was observed for passivated

interconnects, but the activation energy was lower. Also, improvement due to NH_3 treatment after CMP is suggested [104]. In reference [105] a novel self-assembled ZrN cap technology to replace dielectric-cap layer is reported. Interesting property of thin (<10nm) ZrN films was observed- these films were found to be metallic when formed on metal under-layer and insulator when formed on dielectric. But similar electromigration activation energies were found for single damascene test structures with and without ZrN cap layer. Also significant improvement in lifetimes was not observed. For early failures (<50% of CDF), lifetimes were almost similar and longer life times were observed only for late failures in case of ZrN capped interconnects.

In recent days the research of using Self Assembled Monolayer (SAM) to improve the reliability of Cu interconnects either in terms of sealing the interface diffusion pathways or in sealing the pores opened by plasma exposure of ultra-low-k materials are paid more attention by researchers [106, 107]. A molecule which is essentially an alkane chain, is given a head group with a strong preferential adsorption to the substrate used. The thiol molecules adsorb readily from solution onto the Cu, creating a dense monolayer with the tail group pointing outwards from the surface. By using thiol molecules with different tail groups, the resulting chemical surface of Cu and dielectric IMD can be optimized to a high bonding strength.

2.5.3 Microstructure optimizing for conductive interconnect

To reduce the atomic flux, the choice is to reduce the driving force and/or the diffusivity. To reduce the driving force has some basic difficulties since it requires either a change in the scattering process responsible for the effective charge or a reduction in the current density. To achieve the reduction of grain boundary diffusivity, the most common

approach is by solute addition although it should be emphasized that solute addition can contribute to the improvement by other effects, e.g. grain structure modification, and is not confined only to the reduction in diffusivity [108]. Doping of Al with Cu was found to retard electromigration in Al [109, 110] and Al alloy is widely used later on for better electromigration performance of interconnects. Similarly, various dopants like Mg, Al, Sn, Zr are being investigated for reducing electromigration in Cu interconnects [111]. Some of these dopants are used during Cu seed layer deposition and have shown to improve Cu/diffusion barrier metal interface [112]. But actually not the Cu/diffusion barrier metal interface but Cu/dielectric cap interface is important for electromigration. Various other techniques which attempt to optimize the microstructure are also being tried [113]. But with bamboo-like grain structure in sub-micron line-width damascene interconnects and interfaces being the electromigration path, microstructure is not a major concern.

Alloying of Cu interconnects with Mg can be of particular interest for interfacial electromigration. Recently, integration of Cu-Mg alloys in interconnects was demonstrated [114, 115]. Mg doping was used to improve adhesion of Cu with dielectrics. It is important to note from this study that Mg diffuses through Cu to surface and being highly reactive with oxygen, nitrogen and carbon, which are typical constituents of dielectric-cap layer, will form compounds such as MgO or MgF to alter interface. Formation of such an MgO layer at Cu surface is reported in reference [116]. Thus Mg can improve the adhesion between Cu and the dielectric-cap layer. Better adhesion will lead to reduced electromigration according to recently proposed relationship between adhesion and electromigration activation energy [117]. Similarly, Sn was thought to retard surface electromigration in Cu by means of strengthening interface adhesion [118].

2.6 Simulation and modeling techniques in EM study

Two main computation methods that are used commonly in numerical analysis of micro-electronics experimental data include finite element analysis (FEA) and Monte Carlo based calculations. FEA describes a standard model and utilizes a solid geometrical model of the interconnects and imposes structural, thermal, or current distribution based boundary conditions to generate a solution based on the finite element theory. Monte Carlo based simulations on the other hand simulate the atomic movements based on statistical random jumps or atomic movements under the influence of an externally applied gradient such as current flow or stress.

2.6.1 Finite element analysis

Finite Element Analysis (FEA) uses a complex system of nodes to make a mesh. This mesh is programmed to contain the material and structural properties which define how the structure will react to certain loading conditions. Nodes are assigned at a certain density throughout the material depending on the anticipated stress levels of a particular area. Regions which will receive large amounts of stress usually have a higher node density than those which experience little or no stress [119]. FEA methodology is being used generally to solve the local electrical, thermal, and mechanical analyzing based on certain algorithm in a plain finite element model in the interconnect structures [120-124]. In the previous research work of our group, we presented some results dealing with the current density distribution in the extension of overlap structures [92], and thermal-mechanical stress distribution and stress induced failure in a finite element model in via-fed Cu interconnects [125].

2.6.2 Monte Carlo dynamic simulations

Another powerful methodology being used in electromigration behavior study is Monte Carlo dynamic simulations. Monte Carlo methods are stochastic techniques, meaning they are based on the use of random numbers and probability statistics to investigate problems. A majority of these simulation techniques have employed continuum approach to solve the problem of mass transport along the surfaces of interconnects [126-134]. Each of these approaches have considered a sub-set of three principle modes of atomic migration – mass flux due to electromigration, surface curvature, and stress driven mass transport. Simulations for various different scenarios were carried out. These include simulation of voids in perfect lattice, near an external surface, near other voids leading to coalesce of voids, slit-like void evolution in Al interconnects and simulation of surface evolution along a single crystal and across grain boundary.

Monte Carlo approach is used in statistical mechanics, which is a tool to study systems that consist of a large number of interacting elements, like the atoms of a crystalline solid. Monte Carlo simulations have allowed researchers to successfully study a variety of relevant aspects of electromigration degradation as: damage patterns, the distribution of the time to failures, early stage resistance change in the presence of compositional effects, Black's law, and so on [135-140]. General Monte Carlo simulations are carried out according to the following flowchart shown in Figure 2.9.

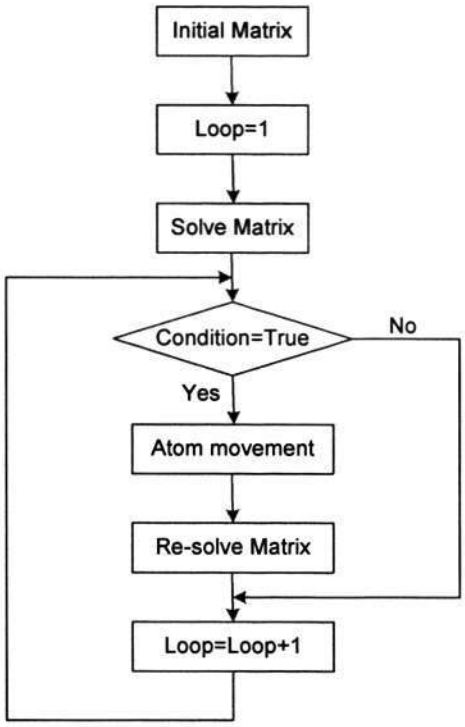


Figure 2.9 Flowchart of general Monte Carlo simulation.

Almost all of the electromigration simulation techniques developed so far are formulated as the continuum or mass transport level rather than the atomic level. Very few attempts are made to develop atomic level electromigration simulation. An atomistic model of void nucleation and growth was developed [135, 136] and a model to simulate void nucleation and evolution was demonstrated by Robert Roy Atkinson and co-workers [137]. Monte-Carlo methods were employed for simulation of atomic transport in these research works.

When Monte Carlo techniques are employed in study of atoms behavior in a two or three-dimensional crystal metal bulk, the objective metals generally exist in a fixed crystalline lattice which defines the location of atoms. The use of statistical mechanism here is to define the motion of an atom through the lattice. The combination of Monte

Carlo selection of atoms and statistical mechanics result in a method to track the motion of atoms in a material under environmental forces resulting from various fields such as electric current, stress gradient, surface tension, grain boundary interface etc. Metropolis algorithm for atomic jumps is generally employed in such Monte Carlo approach. The Metropolis algorithm states that an atomic movement is successful if there is a reduction in the total energy of the system. However, a movement that raises the total energy of the system is still possible but has a finite probability, as explain below:

$$A(\mu \to \nu) = \{1...if E_\mu - E_\nu < 0$$

$$= \left\{ \exp\left[\frac{E_\mu - E_\nu}{kT} \right] ...if E_\mu - E_\nu > 0 \right. \tag{2.13}$$

Where, $A(\mu \to \nu)$ is the probability of system change form state μ to state υ and E represents the system energy.

2.7 Novelty of this research work

- ✓ Cu damascene technology is relatively new and electromigration failure mechanisms in dual-damascene interconnects are still under intense investigations. A detailed characterization of electromigration in upper and lower layer dual-damascene structures with various extension lengths was carried out. Recently, the reservoir effect in Al-Cu interconnect with W vias was reported [95, 141], where voids are generally initiated at the W/Al interface by large Al atomic flux divergence. However, the reservoir mechanism in dual-damascene Cu interconnects is clearly different than with W/Al via structures since voids nucleate at the Cu/SiN_x interface far from the cathode and move along the interface [142-144]. Due to the technological importance of dual-damascene Cu interconnects, it is necessary to understand how extension

lengths impact electromigration lifetimes. In this research work, the reservoir effect and the role of low current density regions on electromigration lifetimes in Cu dual-damascene interconnects were investigated.

✓ Initial part of this study suggested that the peculiar electromigration behavior is due to Cu/dielectric-cap interface acting as vacancy sink and preferable nucleation site. Electromigration performance of damascene Cu interconnects can be improved by suppressing the interfacial diffusion along the dominant Cu/dielectric-cap interface path. In this study, an attempt is made to modify Cu/SiN_x dielectric-cap interface by different surface treatments after CMP of Cu and improve the electromigration performance in via-fed two-layer Cu structures fabricated by 0.28 μm technology. TEM/EELS is employed to achieve the element analysis in detail.

✓ The evolution of a surface morphology subjected to electromigration and surface diffusion are areas of great interest because they may have a direct impact in extending electromigration lifetimes are nevertheless less understood. Cu surface evolution due to the formation of electromigration voids has been numerically simulated [145-147]. Practically, Cu surface evolution has been suggested to be influenced directly and indirectly by electromigration stressing. However, there are relatively few reports focusing on the experimental study of the Cu surface evolution and the root cause behind it. In this research work, the Cu surface morphology evolution was experimentally and theoretically investigated with special attention being paid to the Cu/SiN_x interface and the Cu/SiN_x/Ta edges.

- ✓ Although most of the studies on electromigration in Cu damascene interconnects have shown that the Cu/dielectric-cap interface is the dominant electromigration path [148-151], some have reported grain boundary diffusion to be dominant [152] and have interpreted electromigration in Cu interconnects by coupling grain boundary and interface diffusion [153]. Others have indicated that the Cu/liner interface is the fast electromigration path [154]. Heterogeneous void nucleation followed by migration towards the cathode end has been directly observed using cross-sectional *in situ* SEM observations and interaction of the voids with grain boundaries and triple junctions has also been numerically simulated [96, 155-157]. However, the relative contributions of the Cu/dielectric interface as opposed to the Cu/cap/liner edges have not been studied. It is important to investigate the course of electromigration-induced voiding process and to clearly understand the dominant diffusion path for electromigration in Cu interconnects so as to extend the reliability lifetimes of these devices. In this research work, the process of electromigration-induced voiding was experimentally and theoretically investigated with special attention being paid to the Cu/dielectric-cap interface and the Cu/cap/liner edge so as to identify the dominant electromigration path in Cu damascene interconnects.

- ✓ Electrochemical plating (ECP) is generally used as a method for the fabrication of current Cu interconnects metallization in integrated circuit manufacturing due to its high filling capability and low cost [158-160]. Cu electrochemical plating impacts both the microstructure features and Cu/dielectric-cap interface conditions in the conductive lines, which in turn has a great influence on the reliability of Cu damascene interconnects [161, 162]. Number of studies have been carried out on the

microstructure evolution in electroplated Al interconnects and Cu thin films. However, it is not as clear how this microstructure features and interface conditions affect Cu interconnects electromigration reliability in advanced dual damascene interconnects [163, 164]. Therefore, the effect of different electroplating methodologies on Cu microstructure and ultimately the electromigration lifetimes form an important part of this study.

✓ Statistical properties of electromigration phenomena have been studied extensively as a function of applied current density and temperature [130, 131, 165]. These approaches provide a useful characterization of the interconnect performance and reliability. However, they do not yield much insight into the fundamental processes that give rise to electromigration. Electromigration is not driven by a single atomic diffusion process, but is a complex phenomenon that involves temperature and stress effects, and depends on the microstructure features of the interconnect. Studies of dominant electromigration at the atomic and nanometer scales may provide much insight into the fundamental electromigration-induced processes. A simplified model is developed, which was implemented using random atomic jumps based on the Monte Carlo method, to understand electromigration-induced voiding observations revealed during this research work. Now, equipped with FIB and TEM observations of electromigration-induced void evolution in this research work, an attempt is made to investigate the dominant electromigration path and the effects of Cu grain boundaries on electromigration. Incentive Monte Carlo model was created in Professor Gusak and his co-workers to study semi-quantitatively the void evolutions in several conditions [156]. Here the author refers to a simplified Monte Carlo model that

enables the researchers to get the simulation results qualitatively and much faster. The novelty and the practicability of our simplified Monte Carlo model are as followed.

- This is a simplified model in which we only consider the most contributive factors only to reduce the calculations. We are pursuing the qualitative understanding of voiding process here. By this simplification, the simulation results of voiding process may not be misled because the trend of vacancies and voids motion are always led by the most impacted factors that we have considered in our model.
- Our model has a high versatility. We can change or add effective factors easily into the programs at any time. The study of voiding process at grain boundaries, interface and edges can be implemented if we change the program slightly.
- The computing time is saved a lot for the decrease in calculations in our simplified models. It takes only 2 or 3 days for one simulation to get the final results with the support of MatLab.

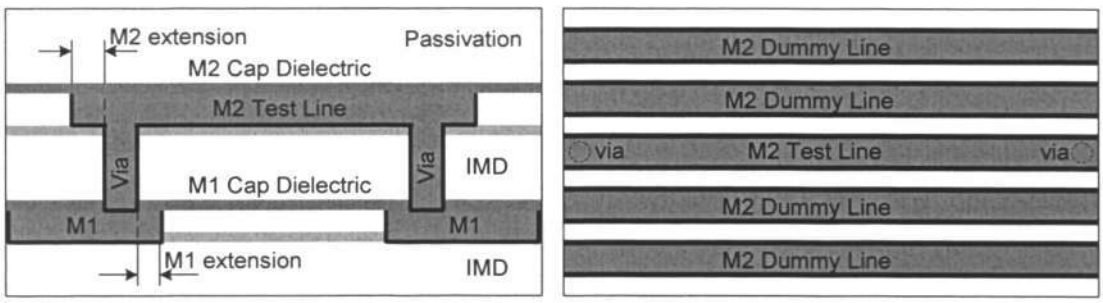
The electromigration-induced void evolutions in Cu damascene structures revealed during this work as well as experimental results reported by various other researchers can be understood well based on our Monte Carlo model.

Chapter Three: Experimental Procedures

3.1 Test structure fabrication

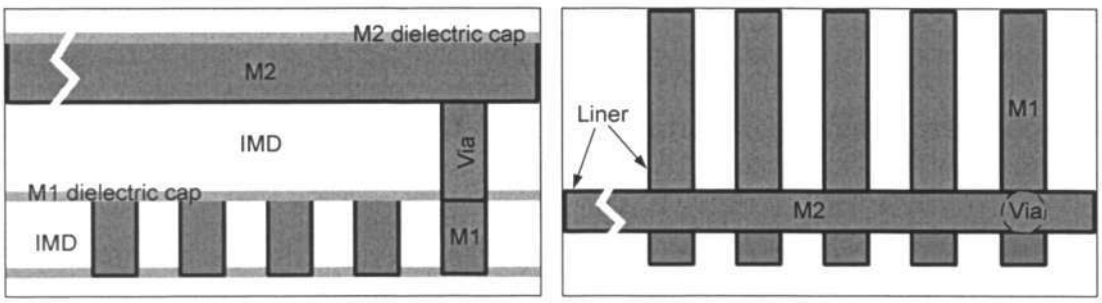
3.1.1 Overlap extension test structures

Studies on the effects of interconnect geometry design on electromigration reliability can be carried out using overlap structure with different M2 or M1 extension. Figure 3.1 shows the schematic of test structure. Studies on the dominant diffusion path for electromigration can be carried out using lower layer test structures with fixed M2 and M1 extension structure, as shown in Figure 3.2.



(a) Cross-section scheme of test structure (b) Plane-view scheme of test structure

Figure 3.1 M2 overlap schematic test structure.



(a) Cross-section scheme of test structure (b) Plane-view scheme of test structure

Figure 3.2 M1 overlap schematic test structure.

The test structures subjected in this study are capsulated by a barrier liner at bottom and sidewalls and a dielectric cap on the top, and fabricated in a Cu/oxide dual damascene process stack, indicated in Figure 3.3. The test structures were fabricated with 0.18 μm Cu/Oxide damascene technology developed at Institute of Microelectronics (IME), Singapore. The test line is the upper layer (metal layer-2, M1) trench and it is connected to a lower layer (metal layer-1, M1) trench by a single via at both the ends. The first inter-metal dielectric (IMD1) consists of plasma enhanced chemical vapour deposited (PECVD) layers of 50nm SiN_x and 800nm undoped silicate glass (USG). The USG layer was etched using a standard fluorine chemistry based dry etch process after metal 1 trench was patterned. Photoresist stripping and wet clean followed the etch process to remove polymer. Cu metallization in these trenches involved depositing a stack of 25 nm Ta barrier, 150nm physical vapour deposited (PVD) Cu seed and 0.6 μm electrochemical plated (ECP) Cu layers. Three kinds of Cu ECP techniques were employed in the study of Cu plating effect: standard DC-plating, multistep DC-plating, and pulse-plating. A cap of 50nm SiN_x was deposited after Cu chemical mechanical polishing (CMP) process. USG (0.8 μm), SiN_x (50 nm) and USG (0.5 μm) were then sequentially deposited as IMD2. The SiN_x layer served as the trench 2 etch stop layer. M2 trench and via were then formed by a via-first dual damascene process. The M2 metallization stack was the same as that of M1 and is 350 nm thick with a via diameter of 260 nm. The lines connecting the pads were short and wide so that voids would be formed in the narrow and long test line between the vias. The test lines were 500 μm long and 280 nm wide.

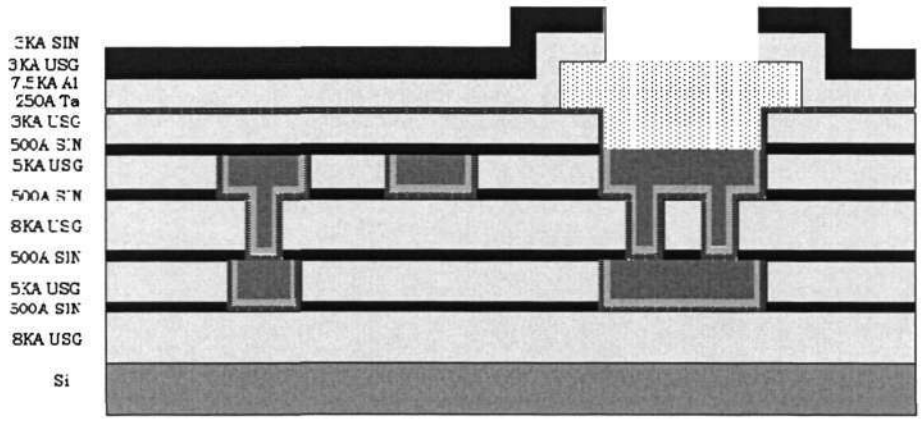


Figure 3.3 Schematic of cross section of Cu/oxide dual damascene stack.

Table 3.1 shows the dimensions of test structures employed in this study. To study the reservoir effect on electromigration, the three different reservoir lengths in M2 and M1 were considered: no extension, 60 nm and 120 nm.

Table 3.1 Dimensions of the overlap test structures in M1 and M2.

Metal level	M1 extension (nm)	M2 extension (nm)
M1	0, 60	0
M2	0	0, 60, 120
M1	120	120

3.1.2 Structures with surface treatment

Different surface treatments as listed in Table 3.2 were performed on wafers from the same bath immediately after Cu CMP prior to SiN_x dielectric cap deposition. An identical set of samples without surface treatment (control wafers) was also fabricated for comparison purposes.

Table 3.2 Surface treatments performed after Cu CMP.

Surface Treatment Samples	Description
Control samples	No surface treatment
NH_3 treatment	In-situ NH_3 flush before SiNx cap deposition
H_2 treatment	Remote H_2 plasma treatment
SiH_4 treatment	In-situ SiH_4 flush before SiNx cap deposition

3.1.3 Structures fabricated by different electrochemical plating

The microstructure features of Cu interconnect shows a dependence on interconnect electroplating techniques following Cu seed layer deposition [166]. In light for the study of the microstructure effects on electromigration behaviour, three kinds of electrochemical plating for Cu interconnects fabrication were employed in this research work: Standard DC-plating, multistep DC-plating, and pulse-plating. After electrochemical plating, the wafers were annealed at 200 °C in a pure N_2 ambient.

- **Standard DC-plating**

  In standard DC-plating process, Cu was electrochemically plated from purged solutions of 0.05 M $CuSO_4$ in H_2SO_4 supporting electrolyte liquid at pH = 1. Films were deposited under constant potential conditions at voltages between -0.6 V and -0.2 V versus Ag/AgCl electrodes at room temperature. Phosphorized Cu anodes were used as a Cu replenishment source. The plating was performed in the plating cell (Figure 3.4) with air agitation.

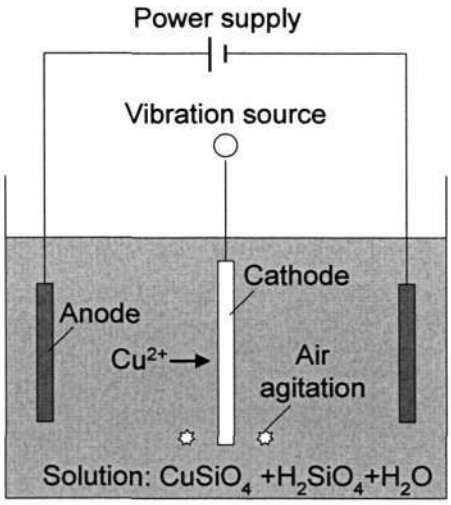


Figure 3.4 Schematic diagram for the electrochemical plating setup.

- **Multistep DC-plating**

Multistep DC-plating was performed in a Novellus Sabre which contained a standard electrolyte and proprietary organic additives from Shipley, comprising of 17 g/l Cu, 170 g/l H_2SO_4 , 50 ppm chloride ions, 1 ml/l accelerator, and 25 ml/l suppressor, at 25 °C for the patterned wafers [167]. The wafers were prepared by depositing 150 nm Cu seed/25 nm Ta barrier/500 nm SiO_2 on 8 in (100)-oriented *p*-type Si substrates. They were then electroplated using the recipes to a nominal thickness of 1.0 mm Cu.

- **Pulse-plating**

Pulse-plating is similar to DC-plating but it has a square-wave current along with a periodic reverse current [168, 169]. The change of reverse current and the selective desorption of additives cause the change in polarization [170], resulting in high throwing power. Typical pulse plating uses square wave currents, alternating between forward and reverse. The duty cycle of the wave form depends on the forward current on-time and the reverse current on-time. The plating program was performed by an Elgar switching amplifier. An acid Cu sulphate bath which contained Cu sulphate

($CuSO_4 \cdot 5H_2O$), sulphate acid (H_2SO_4), chloride ion (Cl^-), organic additives and a carrier was employed in this study.

3.2 Experimental plan

3.2.1 Interconnect structure effect

For studying the geometry design effects on the reliability of Cu dual damascene interconnects, 4 overlap structures were employed in electromigration test. Table 3.3 listed these structures. On accelerated tests of electromigration in Cu interconnects, results gathered above 300 °C are inaccurate since the mass transport will have a large contribution of grain boundary diffusion, which is irrelevant to electromigration failure in real device induced by surface diffusion [24]. Thus, 300 °C was set as the test temperature for electromigration tests.

Table 3.3 Experiments to determine the effect of M-2 extension on electromigration.

Test conditions		Test structures		
Current Density (MA/cm^2)	Temperature (°C)	Metal level	M2 extension (nm)	M1 extension (nm)
1.2	300	M2	0	0
		M2	60	0
		M2	120	0
		M1	0	60

Electromigration characterization was performed by the life-time test method using a package level reliability test system in which 12 test structures were tested at one time.

The wafers were diced into dies containing the test structure, followed by die attach to 24-pin ceramic package and wire-bonding for electrical connection to the test structure. The wire-bonding process was established using a 1.2 mil gold wire and the wire-bonding parameters are shown in Table 3.4.

Table 3.4 Wire bonding parameters.

Wire	Gold wire (1.2mil)
Temperature	200°C
Impact force	150mN
Bond force	100mN
Time	17msec
Ultrasonic Power	23%

3.2.2 Cu surface morphology and electromigration

The study of surface treatment effect on electromigration behavior was performed by electromigration test utilizing the dual damascene Cu interconnects with NH_3, H_2, and SiH_4 treatment respectively after Cu CMP. Subsequent TEM/EELS and XPS analysis were employed to achieve the root cause of electromigration life time variation and pursue the in-depth understanding of electromigration failure mechanisms.

Electromigration-induced voiding process along Cu/SiN_x interface and more significantly along $Cu/SiN_x/Ta$ edges were observed by transversal FIB and TEM tracking along the electromigration stressed line. This preferential accumulation of the voids towards the $Cu/SiN_x/Ta$ edge is analyzed and explained by the means of a simplified Monte Carlo simulation.

The impact of electron wind force on Cu surface morphology evolution at Cu/SiN_x

interface in test structures would be investigated based on samples exposed to electromigration stresses followed with surface characterization. Overlap extension structures, utilized for the study of geometry effect, were employed in this study. The interest area is the interface between Cu surface and SiN_x dielectric cap. For sample preparation, the tested structure was subjected to buffered hydrofluoric acid (12% HF) etching to remove the SiN_x dielectric-cap and SiO_2 passivation. The etching time period is about 5 minutes, depending on the properties of test structures. Failure analysis would be used for the study of interface morphology change following electromigration test by supporting of FESEM and TEM observation.

3.2.3 Cu Microstructure and electromigration

Cu interconnects subjected to this study are fabricated using a dual damascene process in which trenches are filled with Cu by standard DC-plating, multistep DC-plating, and pulse-plating. The details in Cu electrochemical plating subjected to this study were presented in section 3.1.3. The microstructure features of Cu interconnect shows a dependence on interconnect electroplating techniques following Cu seed layer deposition. Overlap structures with two M2 extensions, 0 and 60 nm, were used in this study using electromigration test conditions of 1.2 MA/cm^2 at 300 ^oC.

The bulk microstructure change in Cu interconnects subjected to electromigration test would be investigated by comparing of Cu grain boundaries, grain size change (based on counting the number of grains in a small region) before and after electromigration stressing. The finding of Cu grain boundaries concaving connected to Cu/SiN_x interface, and grain size decreasing at the end of M1 under cathode via would be discussed by supporting of cross-sectional TEM observation, plan-view FESEM observation, and

Monte Carlo simulations.

3.3 Electromigration Characterization

Electromigration test was carried out using MICRO Instruments Co ™, a package level electromigration reliability test system. It consists of an oven that is maintained at a constant temperature and boards with electrical connections onto which the packages are mounted. During electromigration stressing in package level electromigration system, a constant current was forced through each test structure and its resistance was continuously monitored by measuring voltage across the test structure.

Electromigration failure time is demarcated as the point when the resistance increased more than the pre-defined failure criteria of 10%-20% and cumulative failure distribution was plotted. A statistical analysis tool was used to plot lognormal distribution and obtain median time to failure (MTF), which was based on Persson and Rootzen method for analysis of lognormal data [171].

3.4 Microstructure analysis of samples subjected to EM tests

3.4.1 Focused Ion Beam (FIB) Microscopy

Cross sectional samples were prepared by Focused Ion Beam (FIB) cutting. FIB systems are similar to that of scanning electron microscopes in that they involve rastering a beam of focused ions (rather than electrons) over a sample. The ions are field extracted from a liquid metal ion source that consists of a tungsten needle with a radius of curvature of 1 μm that is wetted by a liquid metal. The application of an electric field ($>10^8$ cm/V) to the wetted tip results in the formation of a Taylor's cone with a radius of

curvature of 10 nm from which the ions are field extracted. The most commonly used liquid metal is Ga since it is liquid almost at room temperature. Other metals, which have been used include In while alloy sources such as Co/Nd, Au/Si or Pd/As/B have also been used in conjunction with a mass separator in the ion column. The extracted ions are accelerated, collimated and focused by a series of apertures and electrostatic lenses. Typically the accelerating voltage used ranges from 5 to 30 keV and, depending on the size of the aperture and the strength of the lenses, beam currents from 1 pA to 20 nA with corresponding spot sizes of approximately 10 nm to 500 nm are possible. On penetrating a solid an accelerated ion transfers energy to the solid which can result in the formation of collision cascades and, for events close to the surface of the solid, the emission of ions, atoms and electrons. The emitted electrons or ions can be collected to form an image, as the ion beam is rastered over the surface of the solid. Depending on the material being imaged and the spot size of the beam the resolution of a typical system for the electron or secondary ion imaging modes can be 10 nm and 100 nm, respectively.

The position of the ion beam can be controlled by electrostatic deflector plates and depending on the dwell time, i.e. the dose, at each pixel a system can be used to either implant or sputter away material in user defined areas. The capability of removing material in user-defined areas makes FIB very useful for failure analysis.

The FIB tool was used in this study for cross-sectioning to detect the location of the void. FIB sections were subsequently used in transmission electron microscopy studies.

3.4.2 Transmission Electron Microscopy (TEM)

Microstructure observation and analysis was done using JEOL-JEM-2010, a 200kV ultrahigh resolution analytical Transmission Electronic Microscopy (TEM). The TEM is

an electron-optical microscope that uses electromagnetic lenses to focus and direct an electron beam. Data is collected from the beam after it passes through the sample. Various electron signal and characterized spectrums are shown in Figure 3.5. The resolution and magnification of a microscope are related to the wavelength and the energy of the radiation. In general, the shorter the wavelength, the better the resolution is [172].

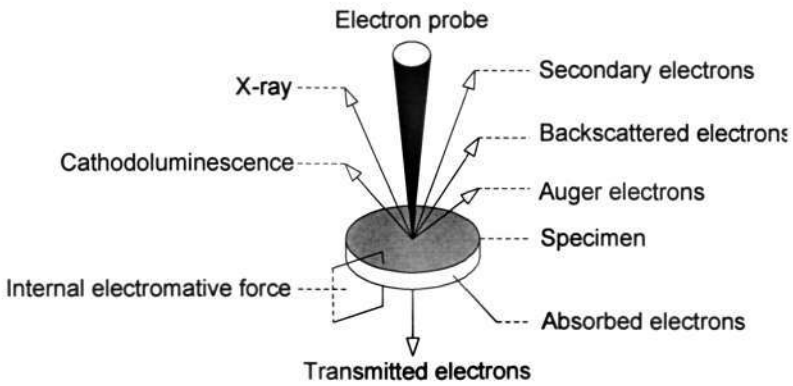


Figure 3.5 Signals from specimens.

Electrons can be diffracted when passing through thin crystals and that is the principle to obtain diffraction patterns. Electron diffraction is an indispensable part of TEM and is arguably the most useful aspect of TEM in materials science. From diffraction patterns, we can get information on the crystal structure, lattice repeat distance, and specimen shape, as well as being a most striking pattern [173]. Normally, if we see spots, the specimen is at least partly crystalline. When the specimen is polycrystalline, the diffraction pattern should be a series of spiccato rings. A series of rings is obtained if the specimen is amorphous. The ability to determine crystallographic orientations locally (down to the nm level) gives the TEM great advantage over visible-light microscopes.

3.5 Monte Carlo simulations

3.5.1 Simulation model setup

To estimate the process of vacancy collection and void migration, an numerical simulation model was created using random atomic jumps based on the statistical Monte-Carlo method, to understand electromigration-induced voiding observations revealed by the *in-situ* characterizations from our previous results. The locations of simulation area are only small region covered several couples of nanometers in Cu segment, which are being modeled are shown in Figure 3.6.

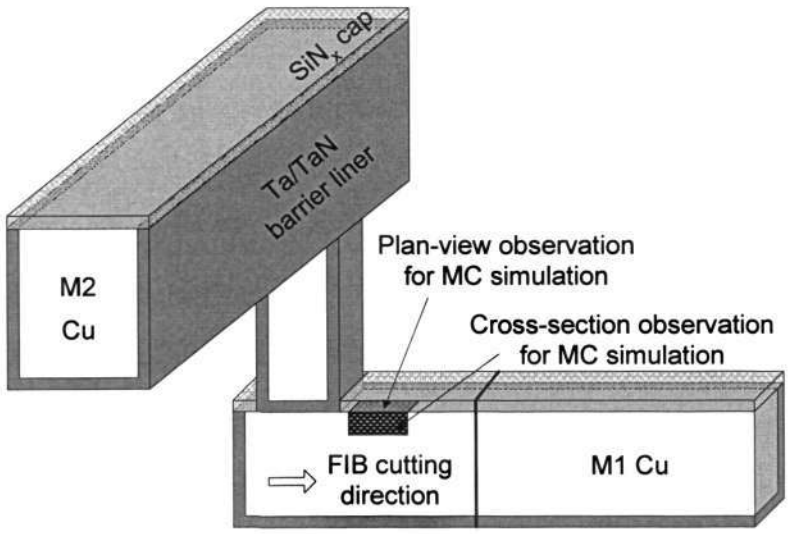


Figure 3.6 Schematic structure of MC simulation region in M1 Cu line.

Atomic displacements in the frame of a statistical Monte Carlo method, with probability of displacement that depends on the difference in system energy, are analysed based on the following considerations:

(1) The region of Cu line is modelled at an atomic level in a framework. For simplification, square lattices (15 sites × 150 sites) were employed to represent the possible position of Cu atoms or vacancies.

(2) The energy of an atom consists of the effective energy of an ion in the field of electron wind force $Z_{ef}eU$ (U is the electric potential) plus the sum of pair interactions zE (z is the number of the nearest neighbors for the randomly selected atom).

(3) The field of the electric potential U is determined in a framework based on the electron flow direction used in our model. The bonding energy at Cu/dielectric-cap interface region was set one third lower than that in Cu bulk in calculations.

(4) We distinguish lattice sites between atoms and vacancies by setting [1] and [0] in the framework. Several vacancies clusters are assigned primarily to implement the defect density gradient at the Cu/dielectric-cap interface and Cu/liner interface.

(5) Vacancies in the bulk and at the Cu/dielectric-cap interface were considered in the Monte Carlo model. The percentage of vacancies used in the model was based on estimates published in the literature of 0.25% [174] at the Cu/dielectric-cap interface and a value of 0.01% [175] in Cu bulk. These numbers *qualitatively* express the different vacancy concentrations at the surface and the bulk; with higher concentrations of vacancies at the surface thought to be resulting from CMP, plasma, process, and growth stresses.

(6) The probability of displacement depends on the difference in system energy of the randomly selected atom and its neighbour vacancy. Redistribution of the interactions is recalculated for the actual configuration before and after the displacement.

(7) Displacement direction is chosen according to the possible jumps of atoms in empty sites.

Note that the simulation areas are only small regions which cover couples of nanometers in the Cu interconnect. It should also be noted that for *visualization* purposes, the vacancies represent a concentration of 2.5% and 0.1%. This simplified Monte Carlo simulation takes into account only two parameters such as electron wind force and bonding energy; and this methodology is being used in this investigation to explain the experimental observations *qualitatively* only. For a rigorous, 3-D solution, one may refer to other published methodologies in the literature including our work published elsewhere [165]. The Monte-Carlo algorithm steps are explained in Figure 3.7. Complete code for the simulations was written in MatLab in *Appendix I*.

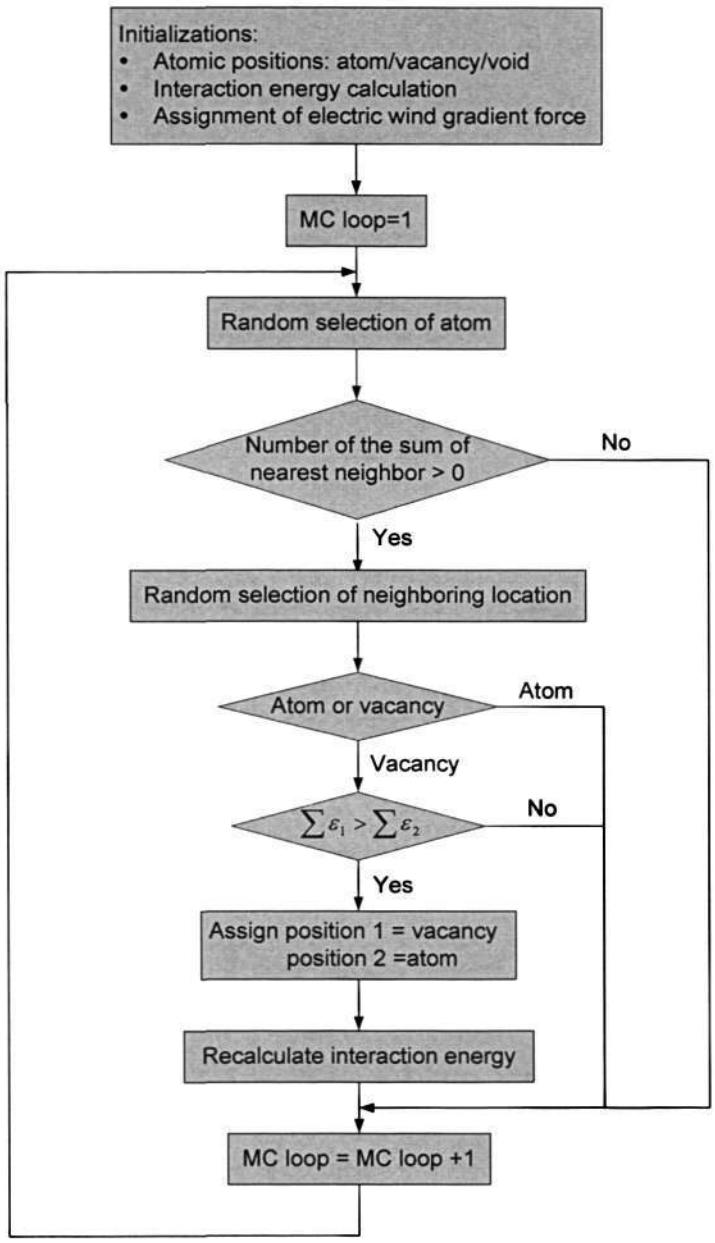


Figure 3.7 Flow chart of Monte Carlo algorithm.

3.5.2 Voiding at Cu/dielectric-cap interface

Vacancy and void behavior in a region of Cu interconnects under electromigration stressing was simulated with the initial conditions. Some vacancy concentration in

random and pre-existing initial tiny voids at Cu/dielectric-cap interface and in the bulk as well, representing the defects owing to some damages during CMP, dielectric cap deposition and Cu electroplating during Cu interconnects fabrication. The Monte Carlo simulation model in the cross-section observation used in this study is shown in Figure 3.8. Lower vacancy percentage was employed to exhibit the less vacancy density in bulk of Cu interconnect.

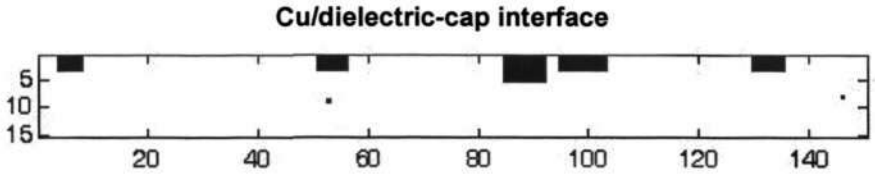


Figure 3.8 Monte Carlo model for study of voiding at Cu/dielectric-cap interface.

Low bonding energy was introduced at the interface in the case of simulation of electromigration in Cu interconnects, which represents highly disordered and weak Cu/dielectric-cap interface bonding strength. The primary results indicate that initial pre-existed surface voids will remain at the Cu/dielectric-cap interface and capture surrounding vacancies to merge into these surface voids, while other pre-existed voids in the bulk will capture surrounding vacancies along with merging into Cu/dielectric-cap interface. Note that this is a simulation of a region at the interface, which is only a small section along of the whole interconnect line. However, this phenomenon will occur through out the entire length of the Cu interconnect line. It can be inferred that these vacancies will move along this interface in a direction opposite to electron flow direction leading to void nucleation at the Cu/dielectric-cap interface at the cathode region. This observation is consistent with our previous *in-situ* SEM observations of voids only at the Cu/dielectric-cap interface at the cathode end of the line [124, 152, 154] and 'preferential

void nucleation at Cu/dielectric cap interface' reported in Cu electromigration studies by other researchers [15, 23, 76]. It is clear from these results that the peculiar electromigration voiding mechanism in Cu interconnects is due to Cu/dielectric-cap interface acting as vacancy sink.

3.5.3 Voiding at Cu/cap/liner edge

Experimental observations have established that Cu is prone to diffuse along the interface of Cu and SiN_x based dielectric cap under electromigration test because of the weak bonding strength between Cu and capping layer. As a matter of fact, the Cu/cap/liner edge is also an area of weakness due to low adhesion and bonding strengths, exacerbated by residual mechanical and growth stresses at Cu/SiN_x/Ta edges. During electromigration, atoms and vacancies redistribute under the electron wind force and the direct force, which leads to vacancies capture at the Cu/dielectric cap interface and more significantly at Cu/cap/liner edges. It is important to investigate the course of voiding process and what is the dominant diffusion path for electromigration in Cu interconnects to understand the electromigration failure mechanism. In this simulation of electromigration in Cu interconnects from plane-view observation, low bonding energy was introduced at Cu/cap/liner edges (i. e. the upper and lower edges in the plan-view observed model shown in Figure 3.9), which represents highly disordered and weak Cu/cap/liner interface bonding strength. Random vacancies and several little pre-existed voids at Cu/dielectric-cap interface were assigned to simulate the contamination and surface defects induced by CMP and followed dielectric cap deposition during metallization process. Primary simulation on the voiding process exhibited the proneness of vacancies collection and merge into voids towards Cu/cap/liner edges. These results fit

the experimental observations based on a TEM investigation in this research that Cu/cap/liner played a dominant role in electromigration-induced diffusion along Cu/dielectric-cap interface in an opposite direction of electron flow.

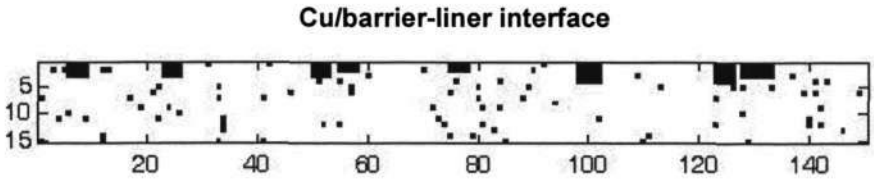


Figure 3.9 Monte Carlo model for study of voiding at Cu/cap/liner edge.

The results explained so far are consistent of our experimental results and serve to validate the applicability of such a model to investigate the electromigration-induced voiding mechanism, and to explain electromigration degradation and eventually interconnect failure.

3.5.4 Effects of grain boundaries

Since grain boundaries seem to play an important role in void migration, the model constructed herein consists of several grains and grain boundaries, which are introduced artificially, by prescribing different values of interaction energies to atoms that make up the grain boundary [153]. That means the interaction energy of atoms within each grain is identical, but the interaction energy of the atoms contained in grain boundaries is different. The simulations for grain boundary effect include two kinds of random high angle Cu grain boundary: the grain boundary connected or disconnected to a defect at Cu surface. Since most of the microstructure profile in recent Cu metallization is bamboo or bamboo-like Cu grains with the grain boundaries cross through the whole line, the

rectangular grain boundaries were employed in priority in this case for ease in programming. The frame networks used in this case were consistent of that utilizing in the above 2 sections (i. e. the model for study voiding at Cu/dielectric-cap interface from cross-section observation and voiding at Cu/cap/liner edges from plane-view observation).

The model can qualitatively explain electromigration-induced voiding observed during experimental *in-situ* SEM characterizations in our previous work as well as in various other reported electromigration studies. Based on this model, it can be inferred that peculiar electromigration-induced void evolution in Cu interconnect structures is mainly due to weak interfaces like *Cu/dielectric-cap interface acting as vacancy sink* and due to redistribution of atoms at interface. However, this model is relatively simple with many approximations. Therefore, it can provide only a qualitative explanation of voiding during the initial stage of electromigration. These findings warrant the need to re-investigate electromigration mechanisms by developing rigorous models based on similar concepts, considering other important parameters such as microstructure, current density distribution, stress and temperature gradients, and introducing diffusivities for different atomic transport paths using Dynamic Monte Carlo [153, 176, 177] and finite element methods [178-185]. Such approaches will provide quantitative information and further in-depth understating of electromigration-induced voiding in damascene Cu interconnect structures.

Chapter Four: Results

4.1 Effect of interconnects structure

4.1.1 Interconnects structure effect on EM behavior

The cumulative distribution of failure times for three different extensions of 280 nm wide M2 test structures are shown in Figure 4.1. Test condition was 300 ^{o}C of temperature and 1.2 MA/cm^2 of current density. A sample size of 12 and a failure criterion of 10% resistance increase were employed for each of the experiment. Median time to failure (MTF) was obtained from a best-fit straight line drawn through data points in the lognormal plot of time of failure, which is given by the intercept at the 50% cumulative failure point (t_{50}) [186, 187].

The distributions were relatively well behaved with approximately similar slope, which means these structures have the same failure mode. The dependence of electromigration lifetime on the M2 extension length for smaller extension range (0 to 120 nm) is obtained in Figure 4.1 (a). This phenomenon is called reservoir effect by some investigation as well. As the M2 extension was increased from 0 to 120 nm, the electromigration lifetime was improved correspondingly. For samples with no extension part in M2 Cu interconnect, the MTF was about 56 hours, whereas MTF was about 112 hours in case of M2 extension equal to 60 nm and 126 hours in 120 nm reservoir. However, to some extent, it seems that the electromigration lifetime does not continue to increment by same amount as the extension length is increased further. When the extension length was increase from no extension to 60 nm, MTF increased by ~100%, but as the extension length was further increased from 60 nm to 120 nm, there was

improvement of only ~10%. At the same time, we found M1 extension may not affect electromigration lifetime so much, as shown in Figure 4.1 (b). Samples with 0 and 60 nm M1 extension showed approximately the same MTF.

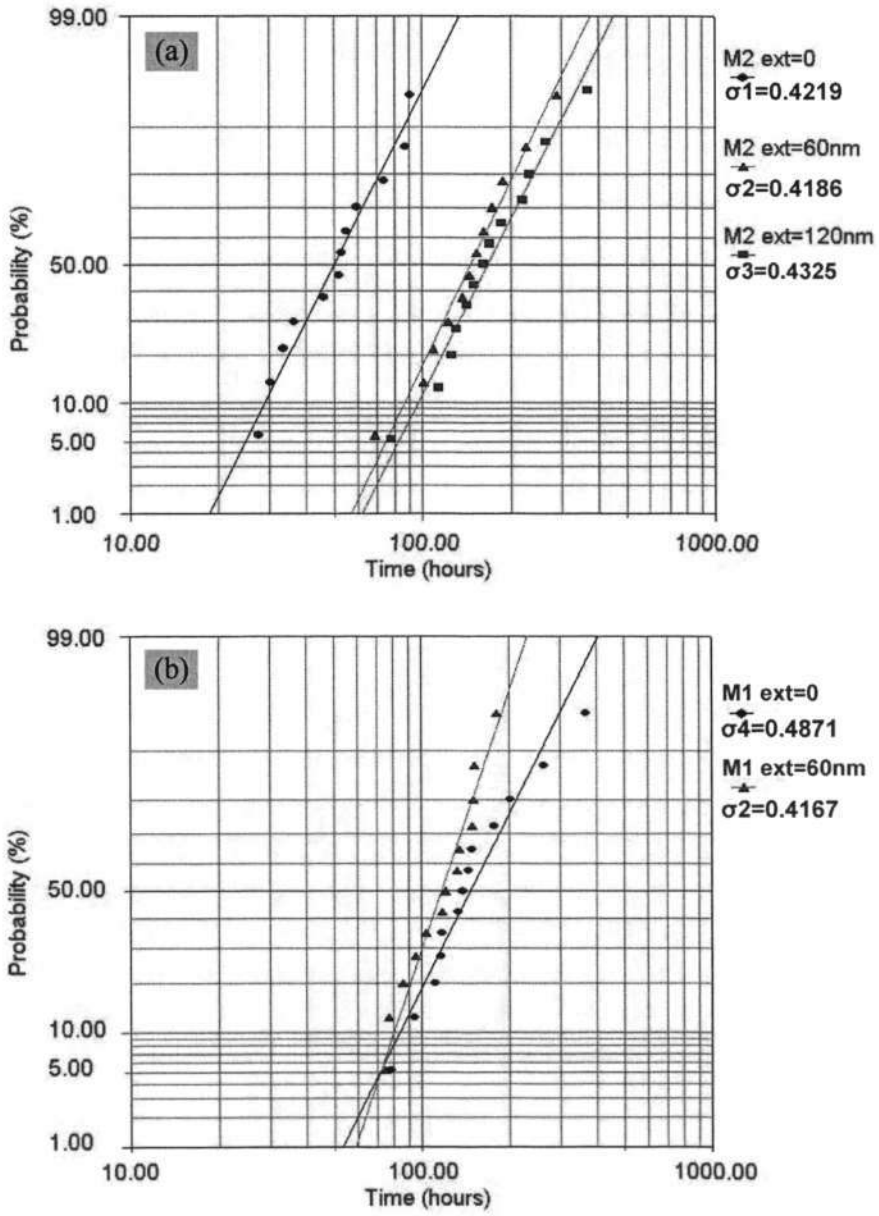


Figure 4.1 Probability plot for failure of Cu interconnects with (a) three different M2 extensions and (b) two different M1 extensions.

4.1.2 Failure analysis on overlap structures subjected to EM

Cross-sectional FIB photographs around cathode via and line extension after electromigration test is shown in Figure 4.2 (with 10% resistance increase). This specimen has 120 nm extension in M2 Cu line at cathode and anode regions respectively. From this image it can be clearly seen that the in M2 structure initial electromigration void nucleation take place preferentially at the interface of Cu/dielectric-cap interface in the M2 line, away from the cathode via. It is interesting to note that the extension part in M2 Cu line was integral without any void.

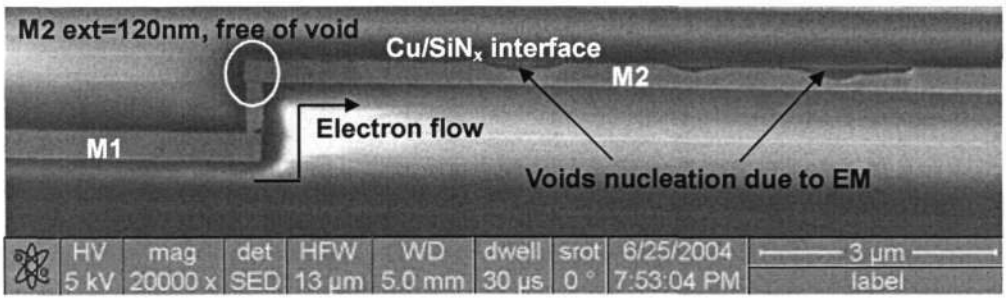


Figure 4.2 Cross-sectional FIB image after 10% resistance increase induced by EM.

At the 30% failure criterion, a cross-sectional FIB photograph around cathode via with 120 nm M2 extension of electromigration structure is shown in Figure 4.3. It can be seen that at 30% resistance increase, the electromigration induced void located at the end of the M2 test line around cathode end and above the via. At the same time, there were some voids at the interface of Cu line and SiN_x dielectric cap as well. It can be inferred from these observations that, the electromigration induced voids nucleate preferentially at the Cu/dielectric-cap interface in the M2 line away from the via, then move/grow along the Cu/dielectric-cap interface of the M2 trench against the electron flow direction and

finally agglomerate at the cathode via / extension region.

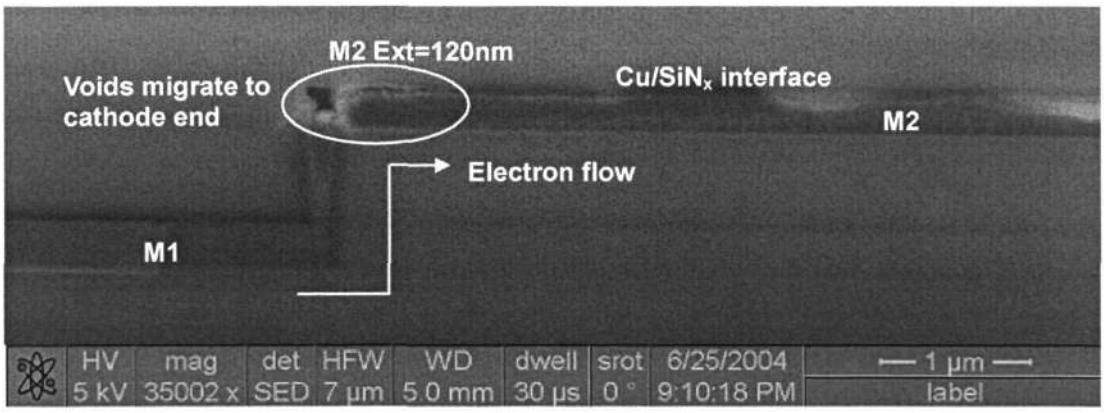


Figure 4.3 Cross-sectional FIB image after 30% resistance increase induced by EM.

Once the voids agglomerate at the cathode via region, the via region is blocked which can cause very high current densities in the via region leading to via burn-out. The agglomerated voids at the Cu/dielectric-cap interface at cathode via region may also migrate along the Cu/Ta interfaces in the via leading to via bottom opening. Such electromigration induced open-circuit failure is shown in Figure 4.4. Electromigration induced voids were seen both at the cathode end of M2 line and the via bottom.

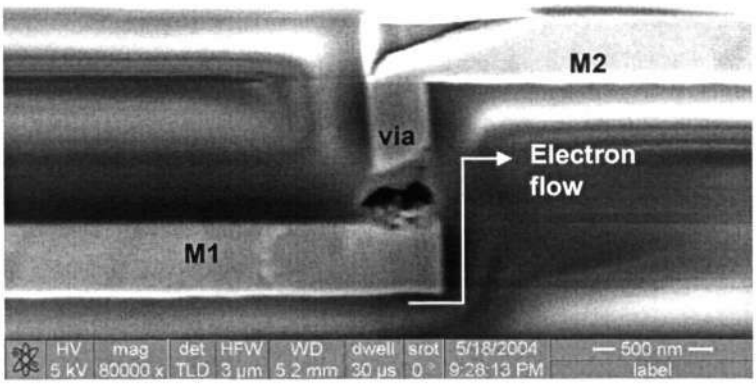


Figure 4.4 Cross-sectional FIB image after open circuit failure induced by EM.

To investigate microstructural changes during electromigration of Cu interconnects, TEM analysis was conducted on test structures after temperature and current stressing. In order to minimize the contribution from the adjacent amorphous oxide and Cu line during TEM imaging, the smallest selected area aperture was used. A cross sectional TEM micrograph around cathode via of M2 structure (with 120 nm extension) after 30% resistance increase is shown in Figure 4.5. It can be seen that at the last failure stage, the electromigration induced void located at the end of the M2 test line around cathode end. At the same time, there are still some voids along the Cu/SiN_x dielectric cap.

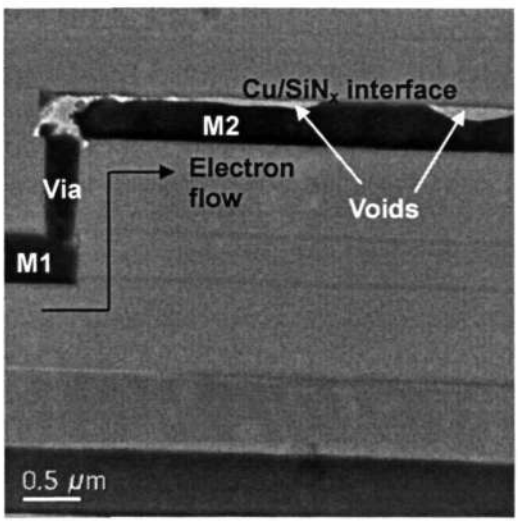


Figure 4.5 Cross-sectional TEM image after 30% resistance increasing induced by EM.

During the electromigration-induced interconnect degradation process, several phases can be distinguished [100, 188]: void formation by vacancies accumulation, void migration at interfaces, void growth to a volume that causes significant resistance increase, and void growth that causes further resistance increase leading to electromigration failure. In the first two phases (i. e. in figure 4.3 and 4.5), agglomerations of vacancies and voids are formed at interfaces and grain boundaries. Depending on the interface bonding energy,

voids apparently move along weak interfaces, most of them, eventually, towards the cathode end of the line. Subsequently, the voids grow and merge into a larger void which eventually migrate along Cu/Ta-liner inter face into the cathode via. It can be seen from Figure 4.6 that electromigration void had grown down into the cathode via. Void evolution depends strongly on both interfaces (i. e. Cu/dielectric-cap interface and Cu/barrier-liner interface) bonding of the inlaid Cu structures.

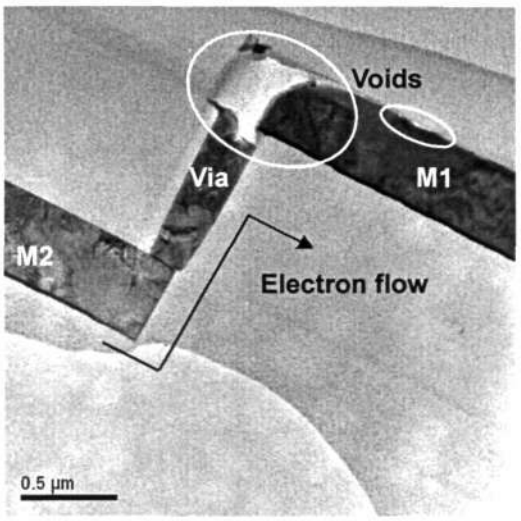
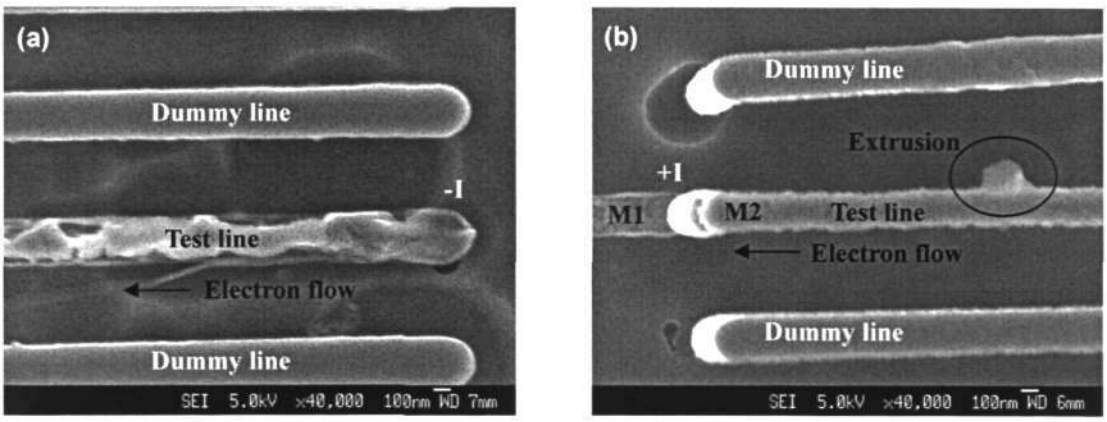


Figure 4.6 Cross-sectional TEM image about EM void migrating into via.

Before EM voids nucleation, Cu/dielectric cap interface was clear and smooth. After electromigration stressing, plan-view FESEM image of the top Cu metal structure (Metal 2) is presented in Figure 4.7 (a). For sample preparation, the tested structure had 10% resistance change and was subjected to buffered hydrofluoric acid (HF) etching to remove the SiN_x cap and SiO_2 passivation. The significant uneven surface of the tested line is found in comparing with surrounding dummy lines. At the cathode end of tested line, it is also clearly observed that the Cu may have detached or grooved along the Cu/cap/liner edge by the formation of electromigration-induced voids. Furthermore, extrusion near the

anode end was also observed from the top view of specimen (Figure 4.7 (b)).



(a) Voids at cathode end. (b) Extrusion at anode end.

Figure 4.7 FESEM plan-view images of Cu interconnects after electromigration.

4.1.3 Microstructure observation on Cu interconnect

Cu interconnects had bamboo-like microstructure and smooth interface of Cu/SiN_x dielectric cap and Cu/Ta barrier before electromigration stressing as shown in Figure 4.8 (a). Diffraction Pattern from zone axis [011] through tilting specimen is shown in Figure 4.8 (b). Single crystal spot transmission electron diffraction pattern for the Cu F. C. C. crystal structure was labelled. The mean grain size was 0.5 to 1 μm, which was calculated by counting the number of grains in a certain region along the Cu line. The value of the mean grain size is larger than the width of interconnects (280 nm). Grain boundary can be seen across the Cu interconnect.

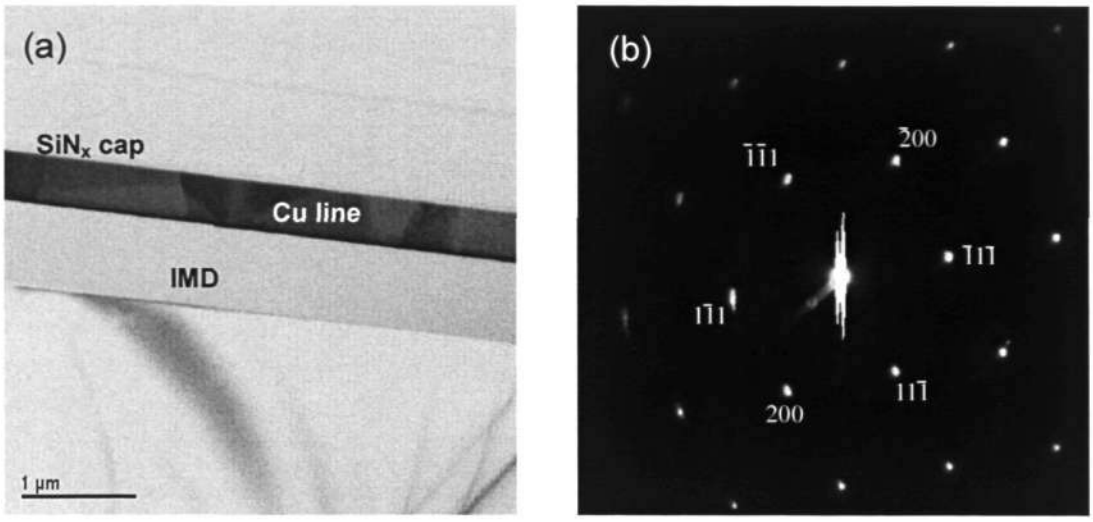
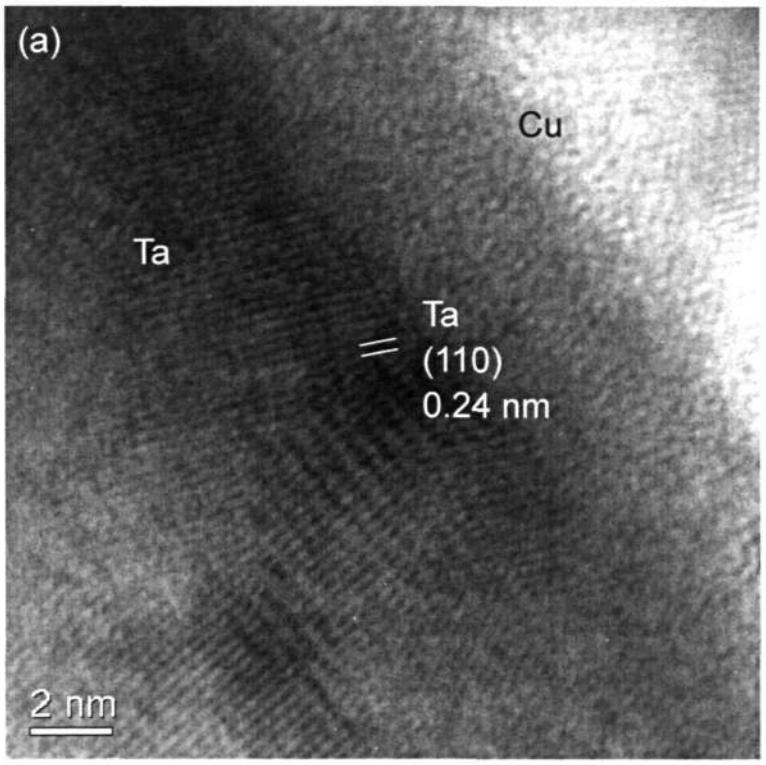
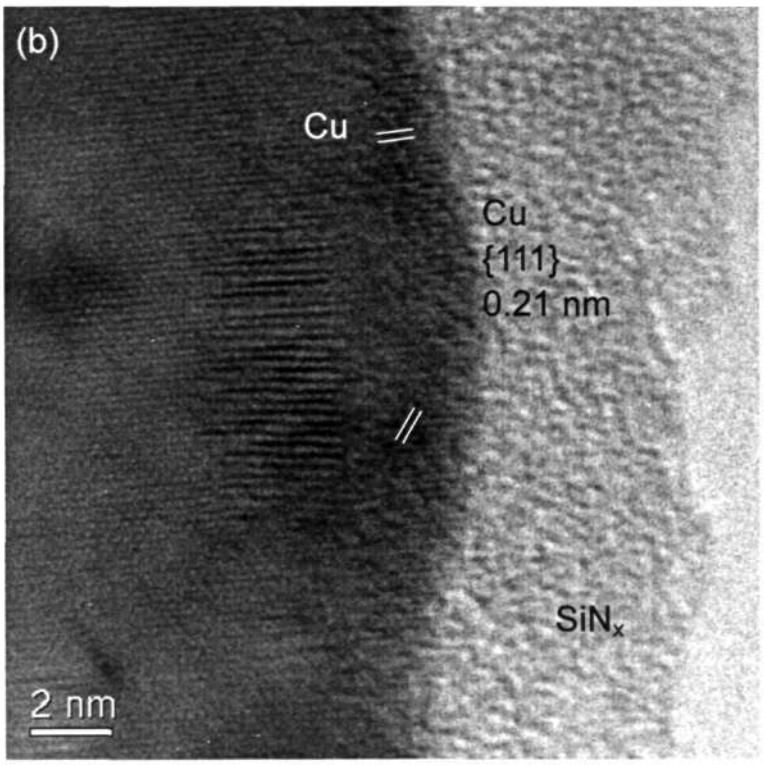


Figure 4.8 Cross-sectional TEM image of Cu interconnect before EM with diffraction pattern from zone axis=[011] through tilting specimen.

High resolution cross sectional TEM images of the Cu/Si_3N_4 and Cu/Ta interface are shown in Figure 4.9 (a) and (b) respectively. Interface observation was carried out using blanket sample. The orientation of Cu grain is labelled in Figure 4.9 as (100) from plan view direction along the Cu thin film surface. The interface between Cu and Ta seems to be demonstrated good structural integrity. Adhesion of Cu and dielectric cap on the line top surface is a key issue in reliability of interconnects during electromigration. Poor interfacial structure may lead to vacancy concentration and void nucleation during electromigration or stress migration.



(a) Cu/Ta liner interface.



(b) Cu/SiN_x interface.

Figure 4.9 HR-TEM images on blanket thin films deposited on Si wafers.

4.2 Surface engineering effect on electromigration

4.2.1 Cu surface treatment effect on electromigration behavior

The lognormal plot of failure times of electromigration test structures with different surface treatments are shown in Figure 4.10. Significant improvement was observed for hydrogen plasma and silane treatment structures. The Cu surface treated with reactive SiH_4 gas and plasma H_2 immediately after chemical mechanical polishing (CMP), but prior to SiN_x dielectric cap deposition was reported to ameliorate electromigration reliability significantly as the formation of Cu silicide prior to nitride formation could improve EM lifetime appreciably.

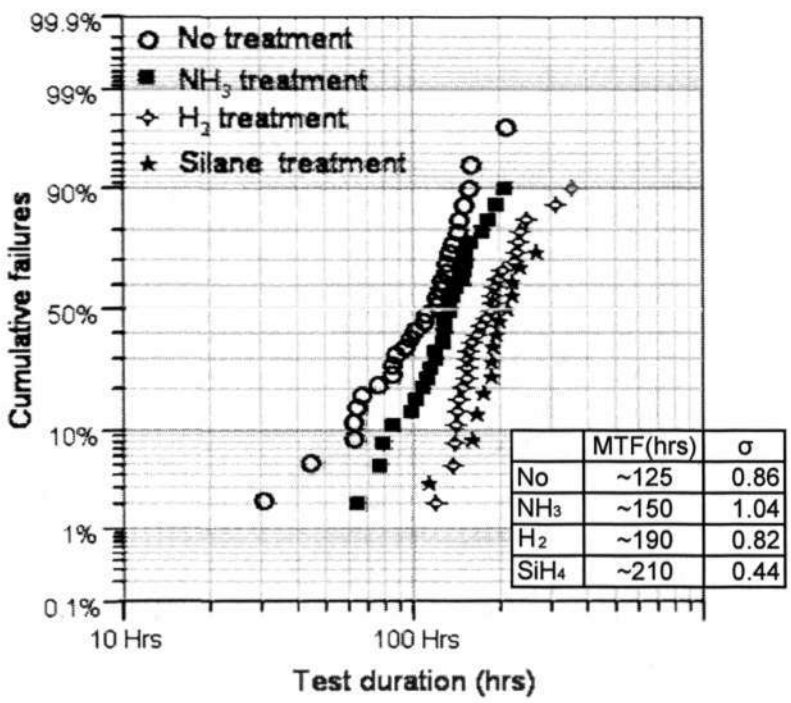


Figure 4.10 Lognormal plot of failure times of M2 Cu line with surface treatments.

4.2.2 Characterization on structures with surface treatments

In this study, TEM bright field imaging, EELS analysis, and XPS elements survey were employed for material characterization to pursue an in-depth investigation on the function of Cu surface treatment on electromigration. Figure 4.11 is the cross-sectional TEM images before EM which indicated the copper silicide formation at the Cu/dielectric-cap interface in initial structures for both H_2 and silane treated specimens.

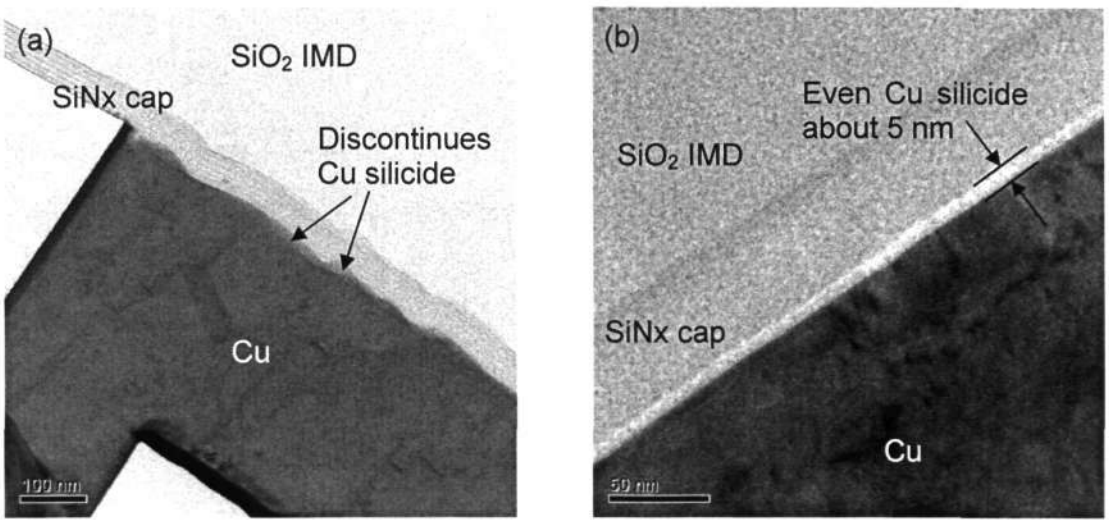


Figure 4.11 Cross-section TEM indicating the Cu silicide formation at the Cu/dielectric-cap interface for (a) H_2 treated and (b) silane treated specimen.

TEM/EELS (Electron Energy-Loss Spectroscopy) analysis was employed for the light element detection between Cu and the upper SiN_x cap layer. Figure 4.12 shows the TEM bright field and imaging and element mapping on the interlayer, which demonstrates the chemical element in the interlayer between Cu and SiN_x dielectric cap. Element of Cu, N, Si, and O were found, which provided the basic chemical component of Cu silicide. It should be noted that Cu distribution in the interlay is not uniform.

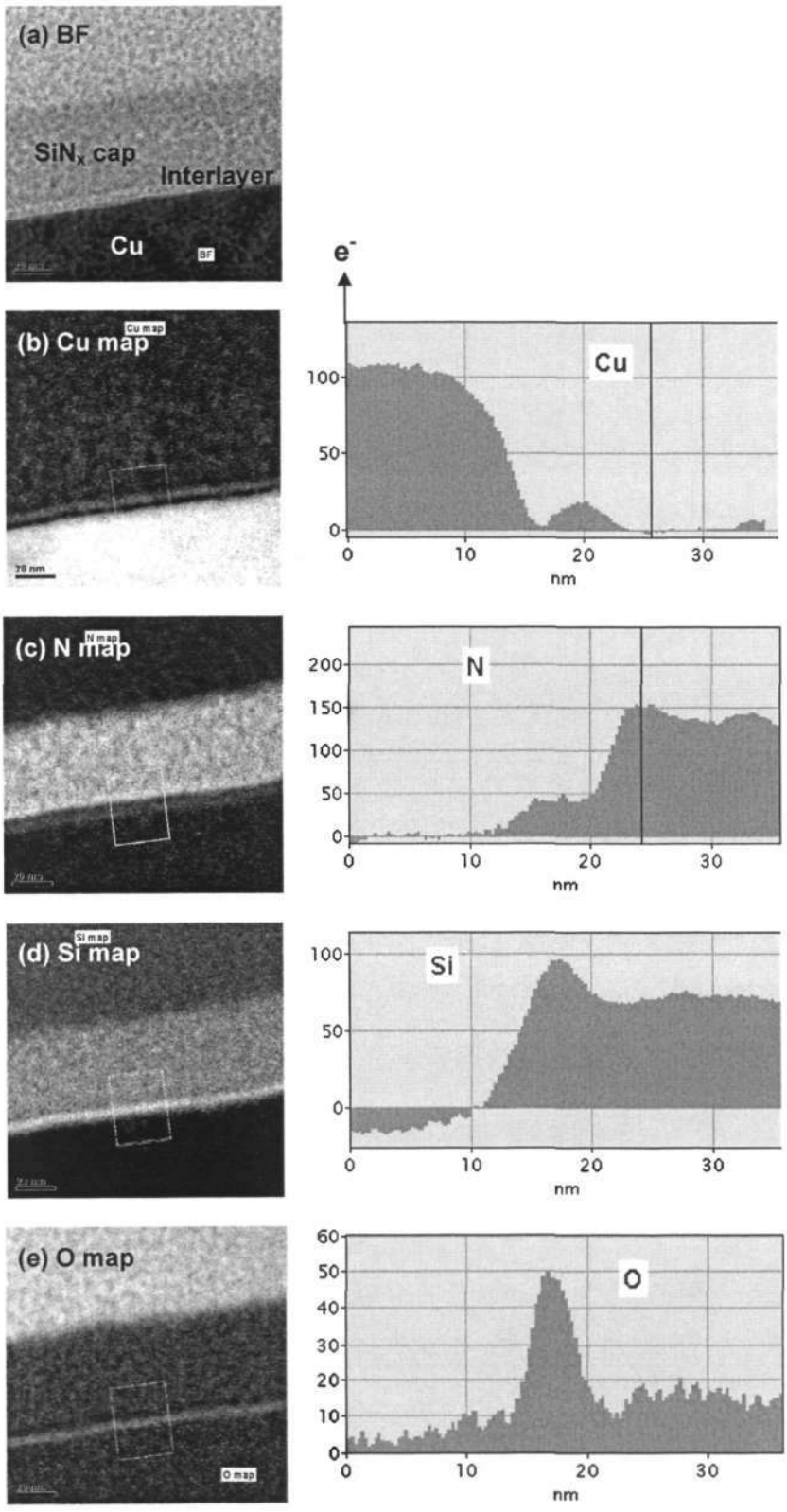
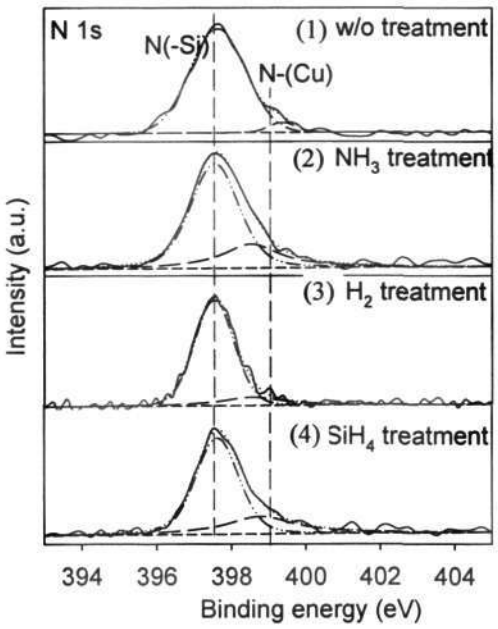


Figure 4.12 TEM/EELS analysis on interlayer indicating the formation of Cu silicide.

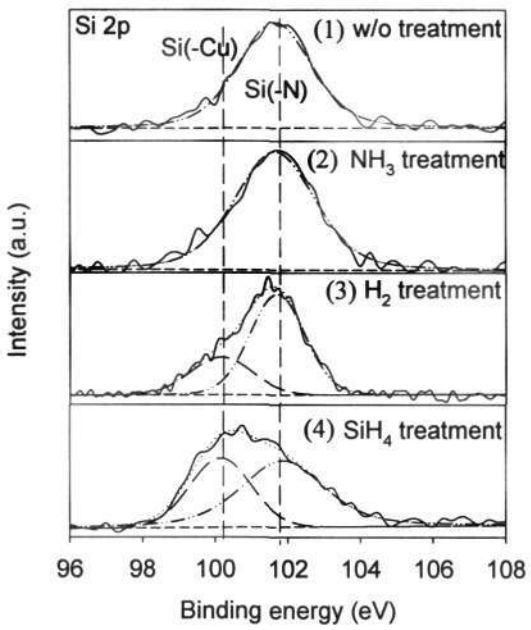
To further examine the effect of different treatments on the interface bond formation, Figure 4.13 compare the spectra deconvolution of N 1s, Si 2p and Cu $2p_{3/2}$ for four surface treatment cases respectively. In Figure 4.13 (a) the N 1s core level spectra of the Cu/SiN_x interface can be disassembled into two peak components at the binding energies of 397.9 and 399.4 eV, associated with the N-Si bond in SiN_x [189] and the N-Cu complex [190], respectively. Similar amount of nitrogen atoms are bonded to Cu for the SiH_4 treated specimens. On the other hand, the Cu-N bonds are much less for pristine and H_2-treated specimens. A detailed discussion will be given later in Discussion Chapter.

Figure 4.13 (b) shows the cases with H_2 and SiH_4 treatment. The Si 2p core level spectra can be disassembled into two peaks at the binding energies at 100.2 eV and 101.8 eV, assigned to Si-Cu and Si-N bonds, respectively. However, for the cases without treatment and with NH_3 treatment, the peak corresponding to Si-Cu bond disappear, indicating that no Si-Cu bonds form at the interface or its content is under the detectable limit.

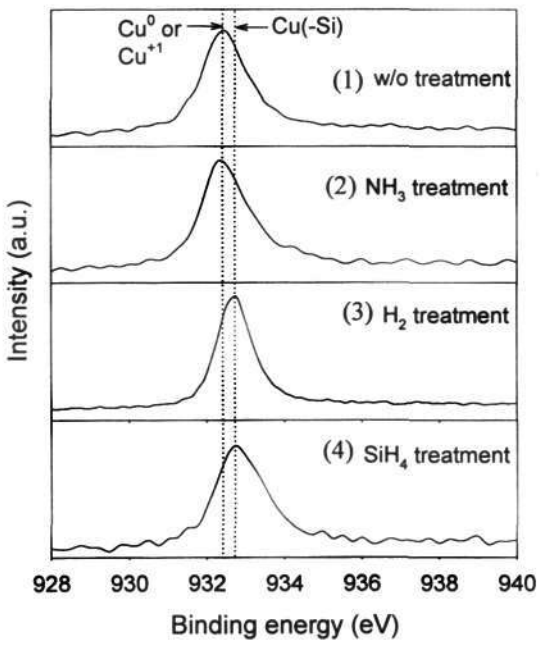
Figure 4.13 (c) clearly indicates that the Cu $2p_{3/2}$ peak is centered at 932.5 eV, which could be assigned to Cu^0 or Cu_2O (i.e., Cu^+) for the control specimen and the one with NH_3 treatment. However, when the specimens are subject to H_2 or SiH_4 treatments, the Cu $2p_{3/2}$ peak shifts to 932.9 eV, corresponding to the Cu-Si bond [191]. This observation agrees well with Figure 4.13 (b) in the formation of Cu-Si bond.



(a) N 1s spectra.



(b) Si 2p spectra.

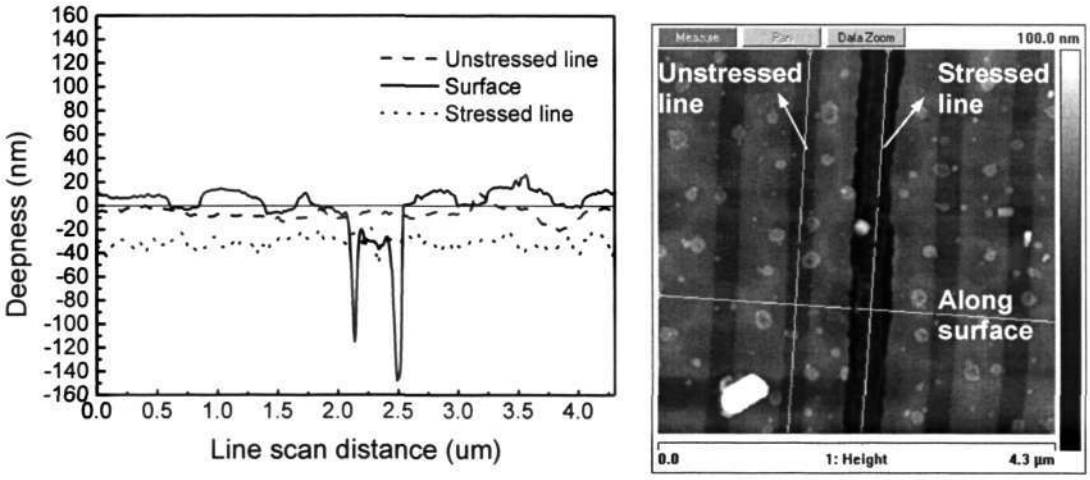


(c) Cu $2p_{3/2}$ spectra

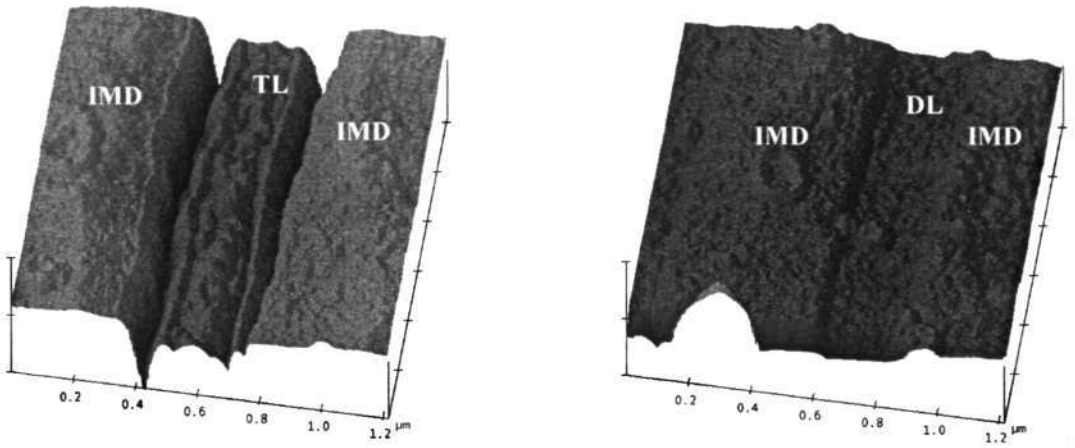
Figure 4.13 XPS spectra of (a) N 1s spectra, (b) Si 2p spectra, and (c) Cu $2p_{3/2}$ spectra for samples with (1) none, (2) NH_3, (3) H_2, and (3) SiH_4 treatments.

4.3 Cu surface roughness change subjected to EM

The impact of electron wind force on Cu surface morphology evolution in Cu interconnects was investigated based on samples exposed to electromigration stresses followed by microstructural and morphological examinations. The top surface of Cu below the dielectric cap (SiN_x under study) was observed in electromigration stressed interconnects. For sample preparation, the tested structure was subjected to buffered hydrofluoric acid (HF) etching to remove the SiN_x cap and SiO_2 passivation. AFM measurements were employed to study the morphology and contours of the Cu surface on the samples expose to HF etching. The AFM line-scan surface images in tapping mode along the top Cu surface of tested structures were shown in Figure 4.14 (a), (b) and (c) respectively. The length of the scan region is about 5 μm along the M2 cathode end. The deepening of the tested line is clearly observed (Figure 4.14 (a)). The top surface of the electromigration tested line is about 30 nm deeper than that the dummy lines in its vicinity. There is no apparent difference in the depth of the dummy lines with respect to the surrounding SiO_2 inter-metal dielectric. Line scans along the tested line shows a much higher surface roughness / amplitude in comparison with the surrounding dummy lines. It is also clearly observed that the Cu may have detached or grooved along the $Cu/SiN_x/Ta$ edge. A depth of up to 60 nm was observed between the sidewall of the tested Cu line and adjacent SiO_2 inter-metal dielectric (Figure 4.14 (b)). The A total of 8 samples were studied in AFM and the observations in all these samples supported these observations.



(a) AFM line-scan measurement.



(b) Surface topography in tested line (TL). (c) Surface topography in dummy line (DL).

Figure 4.14 AFM line-scan on samples subjected to passivation removal with HF.

To investigate Cu/SiN_x/Ta edges further, transversal cross-sectional TEM studies of the test structures in the cathode region with and without HF etching were studied. In HF etched samples, it can be seen clearly that the SiN_x cap on top of the tested line is totally etched out while there is a thin layer of SiN_x remnant on top of the adjacent dummy line (Figure 4.15). Besides the SiN_x cap, the SiO_2 inter-metal dielectric adjacent to Cu/SiN_x/Ta edges in the stressed line was etched out to the depth of more than 60-90 nm. In contrast,

the SiN_x cap was intact on the unstressed dummy lines and the SiO_2 inter-metal dielectric was also unaffected by the HF etching solution.

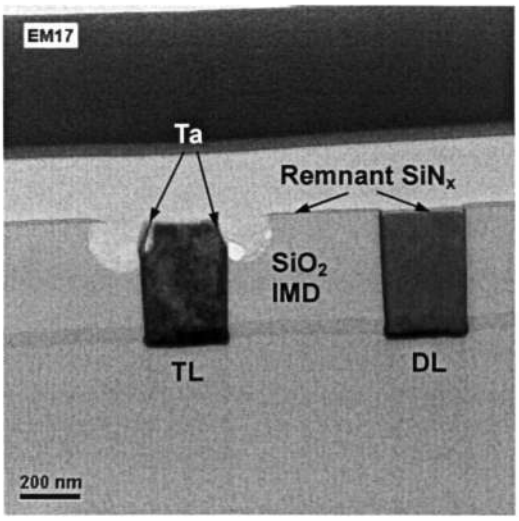
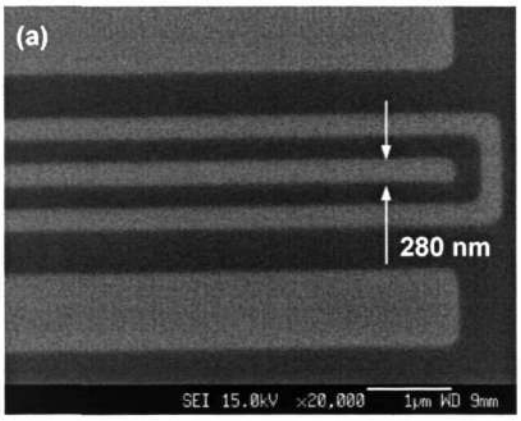


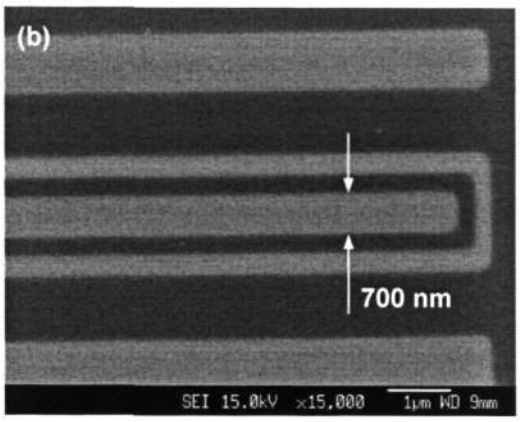
Figure 4.15 Transversal TEM image of Cu/SiN_x interface after buffered HF etching.

It is important to take an observation on the SiN_x cap before any etching to understand the primary stage of Cu surface roughness change under the cover of SiN_x cap layer. To further investigate this phenomena, specimens with a thin (about 50 nm) layer of SiN_x cap only (without passivation layer on top of chip) were fabricated followed the same process flow used for other wafers in this research work. Electromigration test in the same test conditions (1.2 MA/cm^2 and 300 ^oC) was adopted to make results comparable. The plan-view FESEM images about the surface roughness change in structures without suffering HF etching are exhibited in Figure 4. 16. In comparing the stressed (Figure 4.16 (c) & (d)) and un-stressed lines (Figure 4.16 (a) & (b)), it is apparent that the surface roughness of stressed Cu interconnect in the cathode region has been increased at the upper void surface below the SiN_x cap. Crystal on the surface of tested structures were from the contamination by conductive glue during sample preparation, which can not

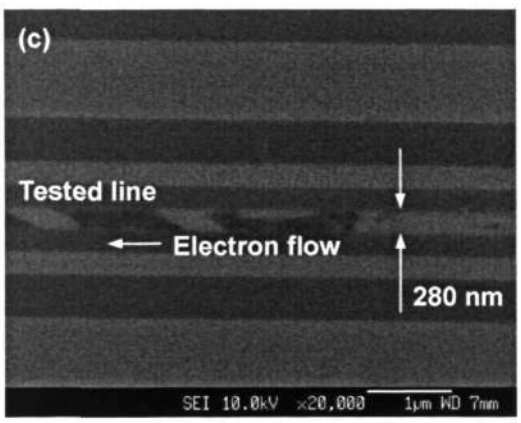
impact the test results but prove the presence of the protection of SiN_x cap. Nevertheless, the unevenness of the Cu surface both in electromigration tested narrow line as well as the wide line is unmistakable.



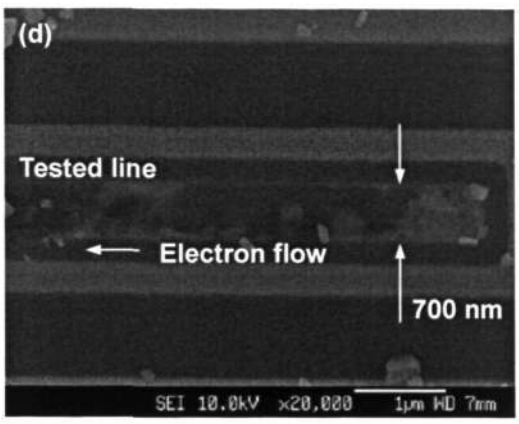
(a) Width=280 nm, before EM.



(b) Width=700 nm, before EM.



(a) Width=280 nm, after EM.



(b) Width=700 nm, after EM.

Figure 4.16 Plan-view FESEM images about surface roughness change in Cu interconnects with width of 280 nm ((a), (c)), and 700 nm ((b), (d)) before and after EM.

4.4 Cu/SiN_x/Ta Edge as the dominant electromigration path

Plan-view FESEM image of the top Cu metal structure (Metal 2) is presented in Figure 4.17. For sample preparation, the tested structure had 10% resistance change and was subjected to buffered hydrofluoric acid etching to remove the SiN_x cap and SiO_2 passivation. The significant grooving surface of the tested line is found in comparing with surrounding dummy lines. At the cathode region of tested line, it is also clearly observed that the Cu may have detached or grooved along the Cu/cap/liner edge by the formation of electromigration-induced voids.

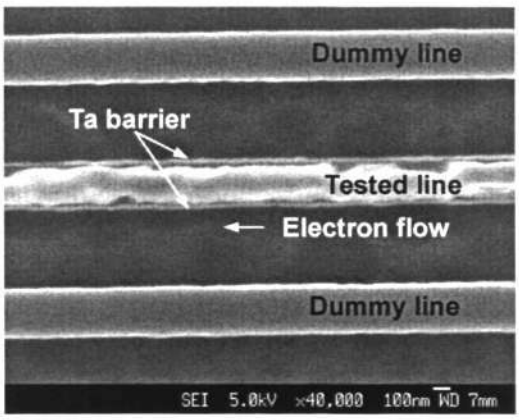


Figure 4.17 FESEM plan-view image at the cathode region of electromigration tested Cu line and surrounding dummy lines subjected to buffered HF etching.

It was proposed that the primary stage of electromigration-induced voiding occurred at Cu/dielectric-cap interface and more significantly at Cu/cap/liner edges. In order to investigate the electromigration-induced degradation along the Cu/cap interface, a series of transversal FIB images were acquired The samples subjected to this study are from *AMD, Germany*. The area of FIB examination is schematically represented in Fig. 3.6 and the FIB transversal images are presented in Fig. 4.18. The first four frames in this

sequence, Figure 4.18 (a) to (d), are taken from near the center of the via to the edge of the via and the frames Figure 4.18 (e) to (f) are taken from the edge of the via to approximately 500 nm inside the interconnect line. Figure 4.18 (a) to (d) show an increasing size of the void that spans most of the width of the line. As we move towards frame (e), the void size decreases and it is clearly observed that the void does not span the width of the line and is more or less confined towards the Cu/cap/liner edge. Figure 4.18 (e) and (f) show the void towards the left hand Cu/SiN_x/Ta edge whereas the voids are seen on the right hand side edge in Figure 4.18 (g) and (f).

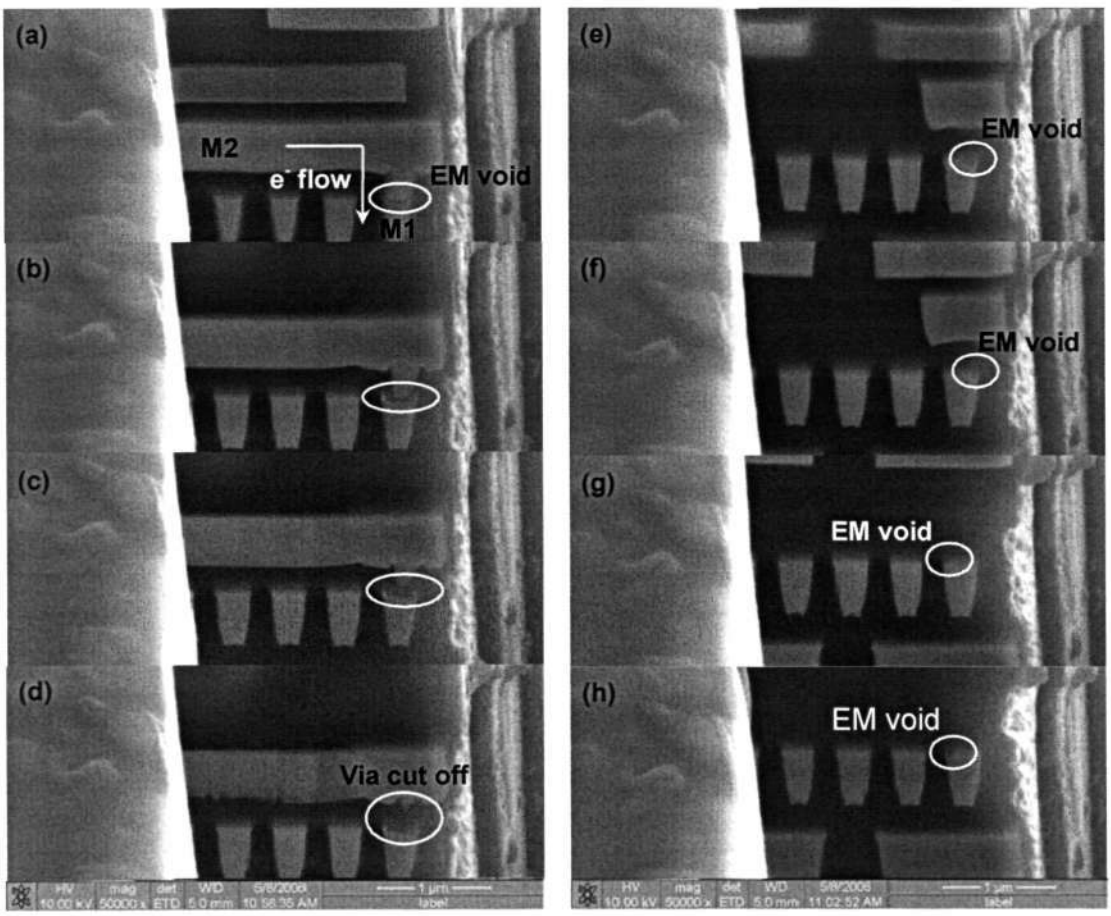


Figure 4.18 Transversal FIB images of EM-induced voiding at the Cu/cap/liner interface.

In order to comprehend of the exact position of electromigration-induced voids in a clearer view, TEM transversal observation was employed (Figure 4.19) utilizing the same sample subjected to FIB observation. In comparing the stressed and unstressed lines, an apparent triangular electromigration-induced void was observed at Cu/cap/liner edge near cathode region in stressed line. The top surface of the stressed Cu line is thinning from one of the Cu/cap/liner edge towards the center of stressed line. The thinning velocities at Cu/dielectric-cap and Cu/liner interface are thought to be similar since the dimensions of the triangular void has the approximate borders in Cu/cap interface and Cu/liner interface.

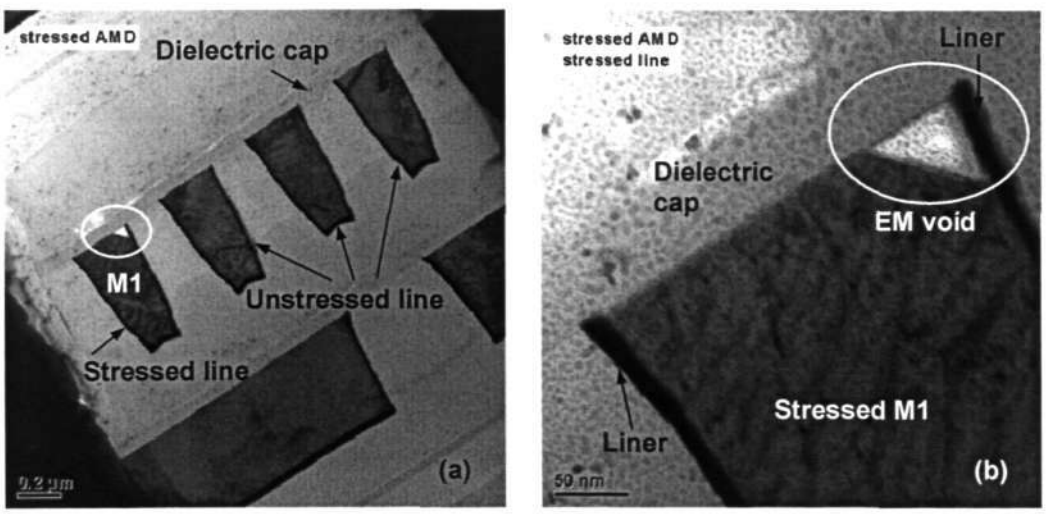


Figure 4.19 Transversal TEM image of EM voiding at Cu/cap/liner interface.

The FIB and TEM observations presented here suggest that the Cu/SiN_x/Ta edge near cathode region plays a significant role in the electromigration induced void migration in Cu interconnects.

4.5 Cu bulk microstructure effect on electromigration

4.5.1 Cu electrochemical plating effect on EM behaviour

Cu interconnects subjected to this study are fabricated using a dual damascene process in which trenches are filled with Cu by electrochemical plating (ECP). Standard DC-plating, multistep DC-plating, and pulse-plating were adopted as the trench-fill in this study. Both multistep DC-plating and pulse-plating are currently employed for ULSI applications. In this study, we focus on the influence of CU ECP techniques and the followed microstructure characterization of electroplated Cu interconnects obtained using these ECP methods.

For packaged level electromigration test specimens, a Median Time to Failure (MTF) and a standard deviation were calculated assuming a lognormal distribution, as shown in Figure 4.20. The Failure criteria of 10% resistance increase for cumulative percentage was employed in this study.

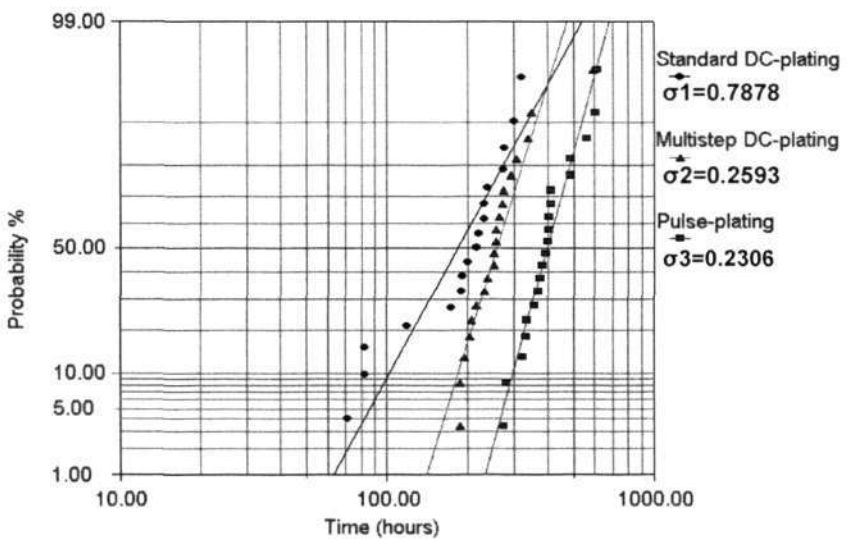


Figure 4.20 Probability plot of failure of Cu interconnects with different ECP.

Table 4.1 The MTF and sigma of test structures with different ECP.

ECP for Cu interconnects	MTF (hrs)	Sigma
Standard DC-plating	200	0.79
Multistep DC-plating	256	0.26
Pulsed-plating	347	0.23

The relative resistance change in two test structures as the function of time during electromigration stressing is shown in Figure 4.21. Abrupt resistance change profile was observed in pulse-plated Cu line while gradual profile was observed in standard DC-plated Cu line. The difference in the profile of structure resistance change indicates the variation in failure modes of test structures obtained by various ECP techniques.

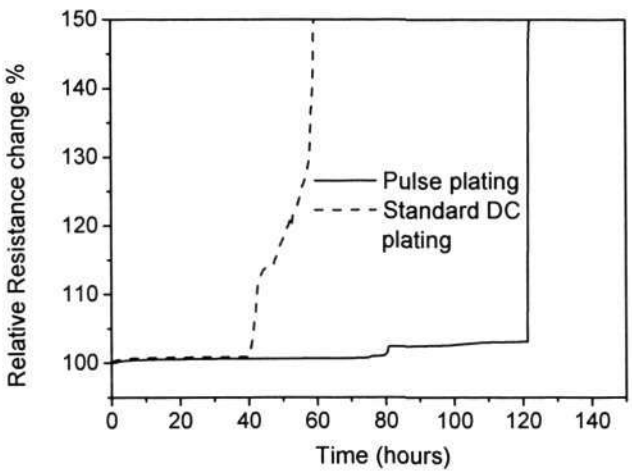


Figure 4.21 Relative resistance changes with time for different ECP Cu interconnect.

4.5.2 Characterization on Cu microstructure due to ECP

The microstructure features of Cu interconnect shows a dependence on interconnect electrochemical plating techniques following Cu seed layer deposition. Three kinds of Cu electrochemical plating techniques were adopted in this study: standard DC-plating, multistep DC-plating, and pulse-plating. The difference in Cu grain boundaries and

surface defects caused by the variation of Cu electrochemical plating would be discussed as the parameters considered in this study. To investigate microstructure variation induced by different electroplating techniques and microstructure changes during electromigration in Cu interconnects, TEM analysis was conducted on test structures before and after electromigration test. A series of cross sectional TEM micrographs around Cu/SiN_x interface before electromigration test are shown in Figure 4.22.

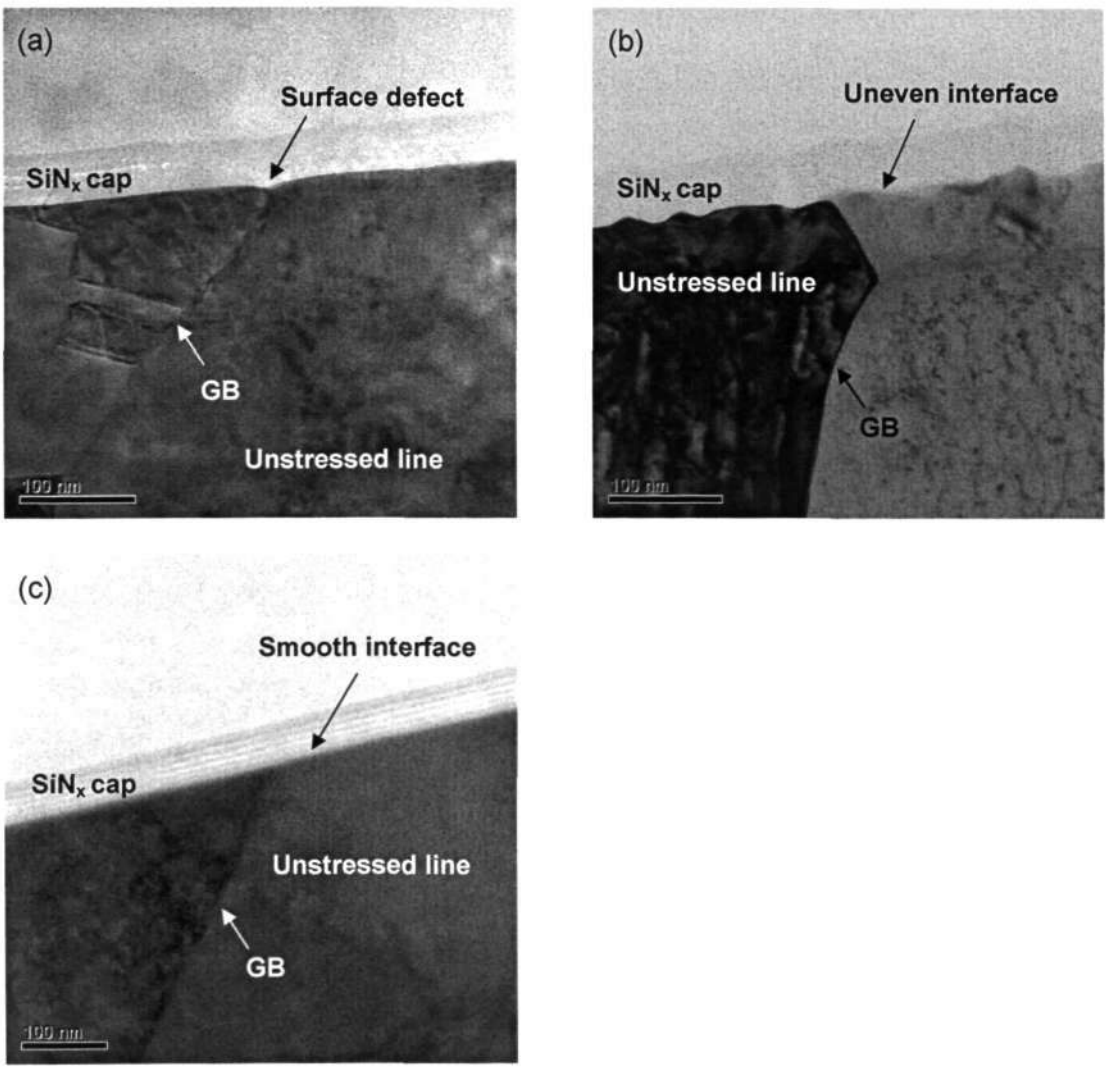
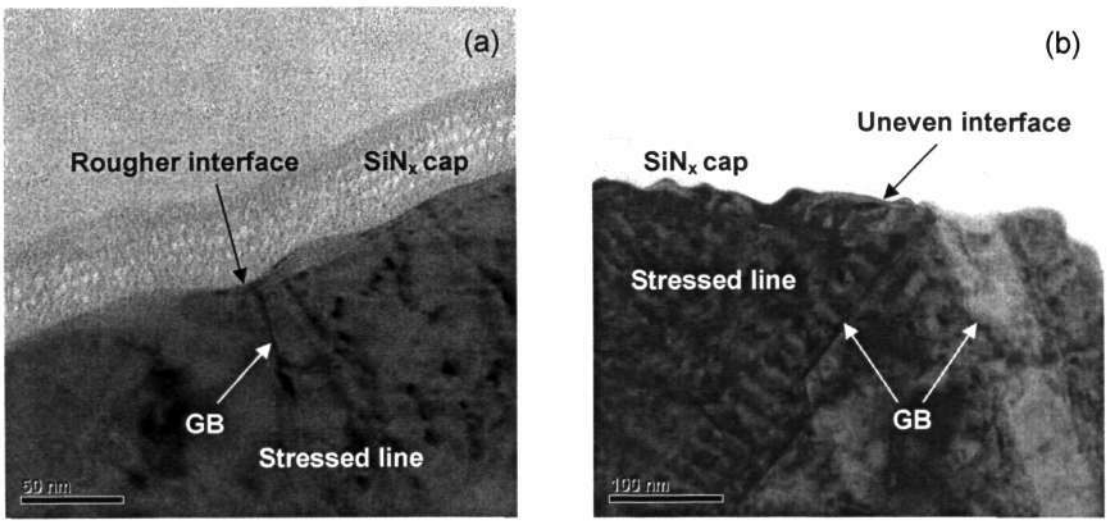


Figure 4.22 Cross-sectional TEM images at Cu/SiN_x interface in initial Cu interconnects fabricated by (a) DC-plating; (b) multistep DC-plating and (c) pulse-plating.

It can be seen clearly that pulse-plated Cu interconnects have very smooth Cu/SiN_x interface with rarely few concave and interface defect connected to Cu grain boundary. Although multi-step DC-plating makes Cu/SiN_x interface much rougher, it should be noticed that Cu grain boundary is disconnected to concave and interface vacancy. Whereas DC-plated Cu interconnect does not have perfect Cu/SiN_x interface since interface defect can be seen to connected to Cu grain boundary.

After electromigration stressing, Cu interconnects showed some changes in microstructure profile, as shown in Figure 4.23. Cu surface roughness was believed to be increased with evident concavity observed at Cu grain boundary after electromigration test in DC-plated interconnects. There are not significant changes in microstructure profile and interface condition in Cu interconnects fabricated with multistep DC-plating and pulse-plating.



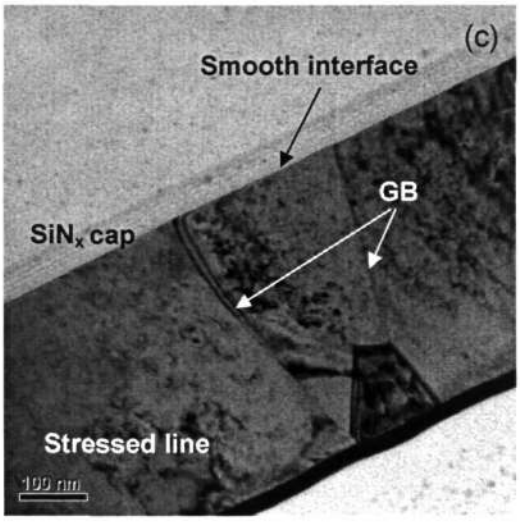
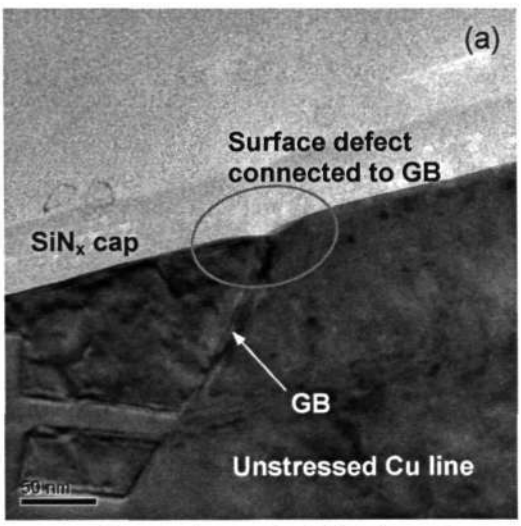


Figure 4.23 Cross-sectional TEM images at Cu/SiN_x interface in EM tested interconnects fabricated with (a) DC-plating; (b) multistep DC-plating and (c) pulse-plating.

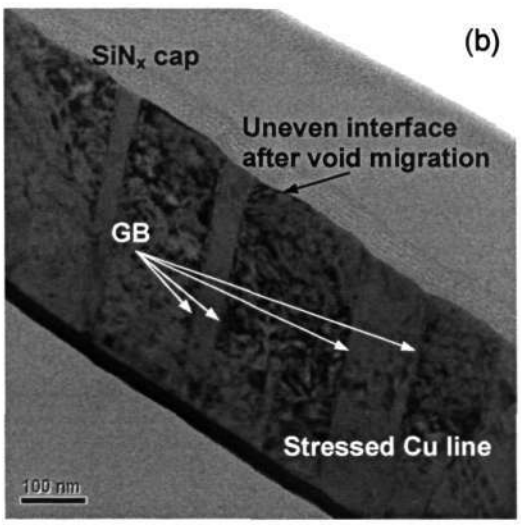
4.5.3 Role of Cu grain boundary

Although interface diffusion is believed to be the dominant failure mechanism in electromigration-induced degradation in advanced Cu interconnects with bamboo microstructure, grain boundary also plays an important role during void movement. In case the interface and adhesion between Cu and dielectric cap are improved, the importance of Cu grain boundary could be noticeable. Figure 4.24 describes the different phases of electromigration-induced void formation at Cu/dielectric-cap with the combination of grain boundary effect utilizing standard DC-plating specimens. Before electromigration stressing, surface defect connected to Cu grain boundary was found at Cu/SiN_x interface (Figure 2.24 (a)). The surface defects or impurities might be introduced by Cu CMP and/or the following dielectric deposition, and might be introduced by Cu grain growth during annealing as well. These surface defects and impurities would serve

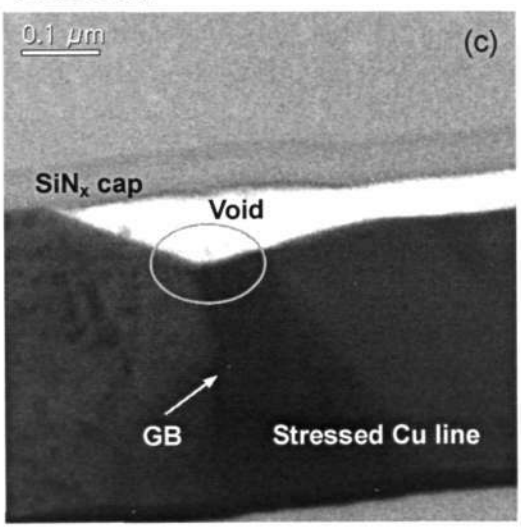
as the vacancy source during the course of void nucleation. Followed voids migration along the Cu/SiN_x interface, Cu atom construction led the Cu/SiN_x interface uneven with evident concavity at Cu grain boundaries (Figure 2.24 (b)). Electromigration-induced void along the Cu/SiN_x interface had approximately a triangular shape with one point at the Cu grain boundary (Figure 2.24 (c)).



(a) Surface defect at Cu/SiN_x interface before EM.



(b) Unevenness at Cu/SiN_x interface and GBs after void migration.



(c) Triangle EM void with one point at Cu GB.

Figure 4.24 Electromigration voiding at Cu/cap interface connected to GBs.

4.6 Grain size change at M1 end subjected to EM

Before electromigration test, bamboo like microstructure in Cu interconnects was observed both in M1 and M2 line. Grain boundary crosses the M1 and M2 line with the grain size from 0.5 – 2 μm, which is shown in Figure 4.25.

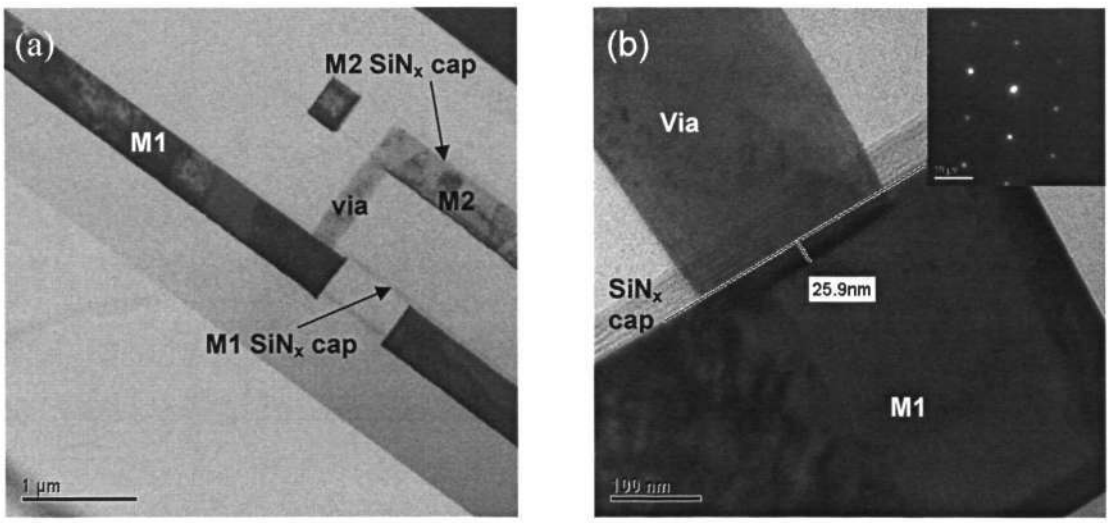
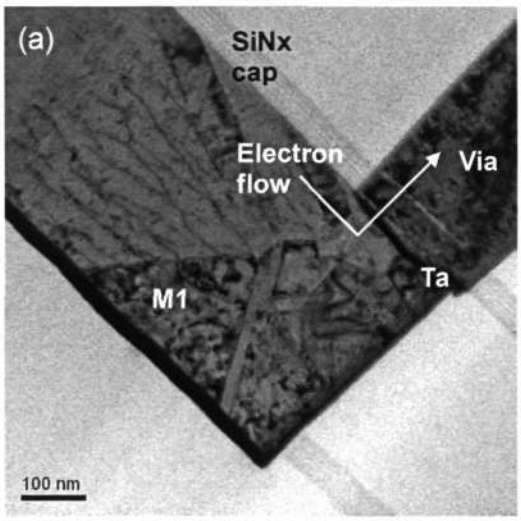
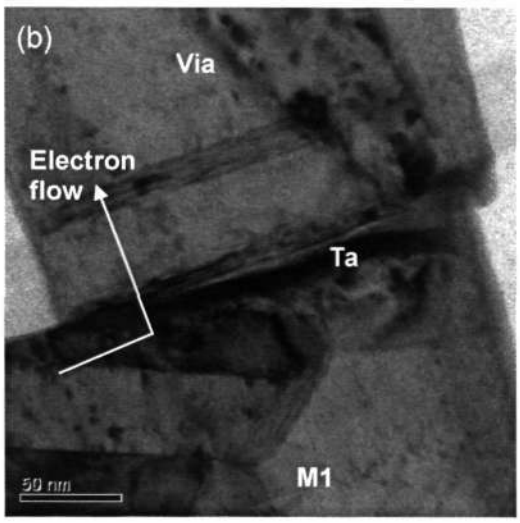


Figure 4.25 Microstructure in Cu M1 and M2 before EM stressing.

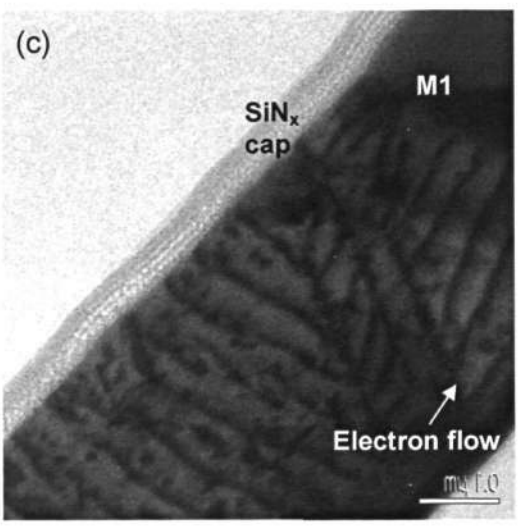
After electromigration stressing, Cu interconnects showed some changes in microstructure. Firstly, grain size of Cu interconnects below the cathode via was observed to be decreased as shown in Figure 4.26 (a). The diffraction pattern of TEM image shows this grain size decreasing as there appears a series of concentric rings (see Figure 4.26 (b)), whereas, large crystal structure should exhibit spot patterns [172].



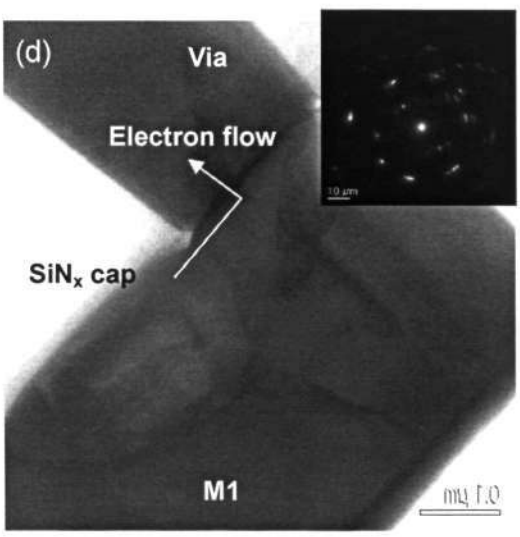
(a) Dislocations and smaller grains at M1 end under cathode via.



(b) Higher Magnification on the smaller grains and GBs.



(d) Dislocations near M1 end under cathode via.



(d) Smaller grains and GBs with diffraction pattern.

Figure 4.26 TEM image about dislocations and Cu grain size change after EM.

Chapter Five: Simulation and Modeling

5.1 Finite element analysis for reservoir effect

The observations of the improvement in electromigration life time by introducing an extension at cathode region as reservoir of atoms, described in section 4.1.1, leads further support the following sequence of events: a) voids form heterogeneously at the Cu/SiN_x interface and away from the cathode, b) migrate through interfacial diffusion paths at this interface into the extension part driven by the electron wind force, c) accumulate near the cathode, and d) grow to the edge of zero current and eventually lead to opening circuit failure. To understand the void accumulation and growth process into extension, three-dimensional finite element analysis (FEA) was evaluated to calculate the localized current density at the via and M2 extension region. Figure 5.1 shows the contours of current density (in color, unit: MA/cm^2) around the M2 extension/via region for three extension lengths. Table 5.1 listed the material propertied used in this analysis [192-195].

Table 5.1 Material properties for the thermal-electrical analysis [192-195].

Materials	Electrical R (μΩ·cm)	Thermal conductivity (W/m·K)	Specific heat capacity (J/kg·K)	Density (kg/m^3)
SiO_2	1E34	16	680	2270
SiN_x	1E34	20	700	3110
Cu	1.67	400	385	8920
Ta	13.5	57	140	16650

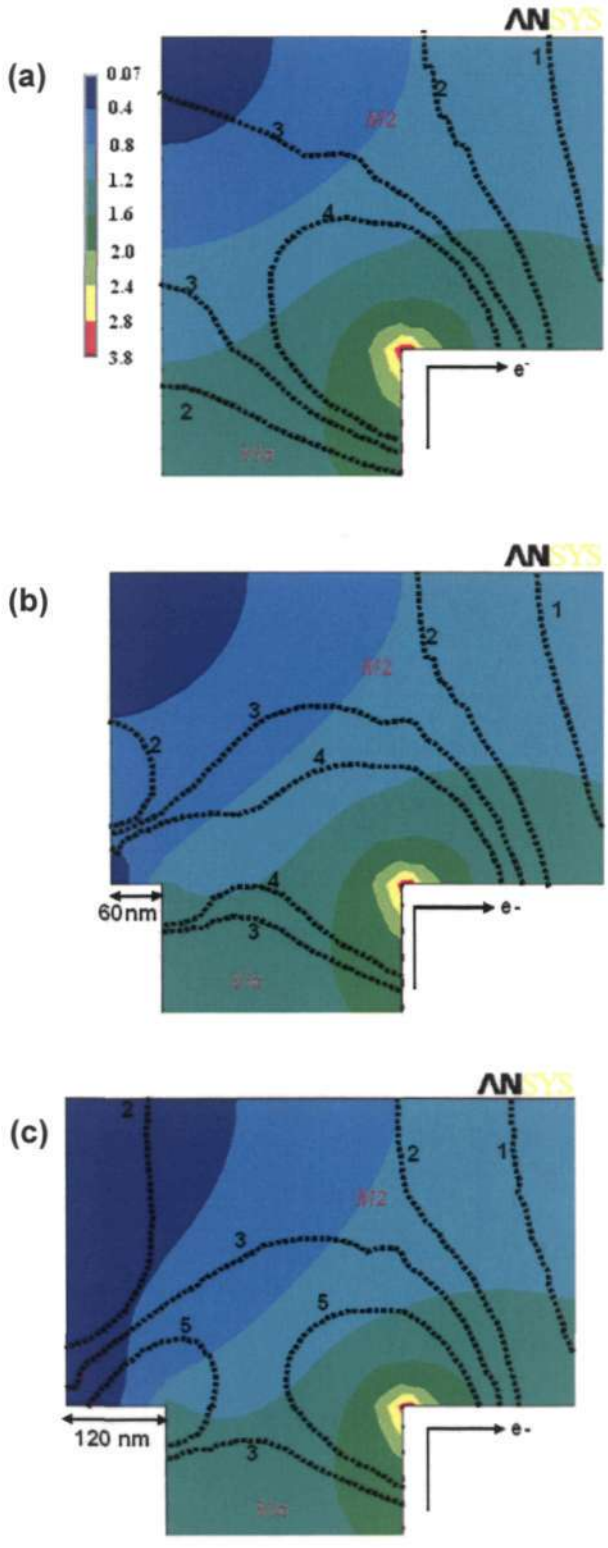


Figure 5.1 Contours of current density (in color, MA/cm^2) and current gradient (dotted curves, 10^{10}A/cm^3) around the M2 extension (a) =0, (b) =60 nm, and (c) 120 nm.

The contours of current density gradient (dotted curves, untie: 10^{10}A/cm^3) have been overlaid on the current density contours. After the interfacial void is generated in the Cu/SiN_x interface away from the cathode end in M2 (Figure 4.2), where the current is uniform and parallel to the interface, the void migration along current direction is driven by the electron wind force (i.e., $\boldsymbol{F}_c$).

$$F_c = -Z^* e \rho j \tag{5.1}$$

where Z^* is the effective charge number of the diffusing Cu atom, ρ is the resistivity of Cu, and j is the current density. The void velocity v is related to the current density by the following equation:

$$v = \left(-\Omega A \frac{3ND_s}{kTa} \right) * F_c \tag{5.2}$$

where N is atomic density, Ω is the atomic volume, k is the Boltzmann constant, T is the temperature, a is the radius of the void, D_s is the diffusion constant, and A is a factor related to the void location.

Another driving force due to current-density gradient (i.e., F_g) may also influence the void migration.

$$F_g = -\frac{dP}{dr} \tag{5.3}$$

$$P = q_v |j| S_c * \Delta R_v \tag{5.4}$$

Where P is the potential energy of an excess vacancy driven by the current density j, q_v is the charge of the vacancy, S_c is the scattering cross section of the vacancy, ΔR_v is the resistance of the excess vacancy.

However, analyzing Equation (5.1) and (5.3) using the following material parameters [196]: $q_v = Z^*e = 4e$; $S_c = 1\times10^{-15}$ cm^2; $\Delta R_v = 1\times10^4$ Ω; $\rho = 1.67\times10^{-6}$ Ω·cm,

leads to the inference that F_g is at least one order of magnitude lower than F_c for the location along the M2/SiN_x interface as well as at the current density contours (e.g. 0.4 MA/ cm^2), where the values of $\left|\frac{dj}{dr}\right|$ are between 2×10^{10} to 3×10^{10} A/cm^3. Therefore, the effect of current density gradient (F_g) could be ignored in the present study.

We propose that there exists a low current density region (dead-zone) bounded by a critical low current density (j_{crit}) around the corner of extension (upper-left corner in Figure 5.2) that highly retards the movement of the incoming voids and may prevent or *resist* void entry into the M2 extension. Figure 5.2, derived from Figure 5.1, presents current density contours of j = 0.4 MA/cm^2 for extensions of 0 nm to 120 nm. It should be noted that the current density contours for different extensions have been overlaid along with the M2/via geometry so as to provide a direct comparison of the change in contours as a function of extension lengths. It may be envisaged that the incoming voids are retarded near a j_{crit} boundary, slowing down or even possibly blocking their further progress into the low current density regions located at the far corners of the reservoirs. Only a certain part of the extension volume may effectively serve as a reservoir for accumulation.

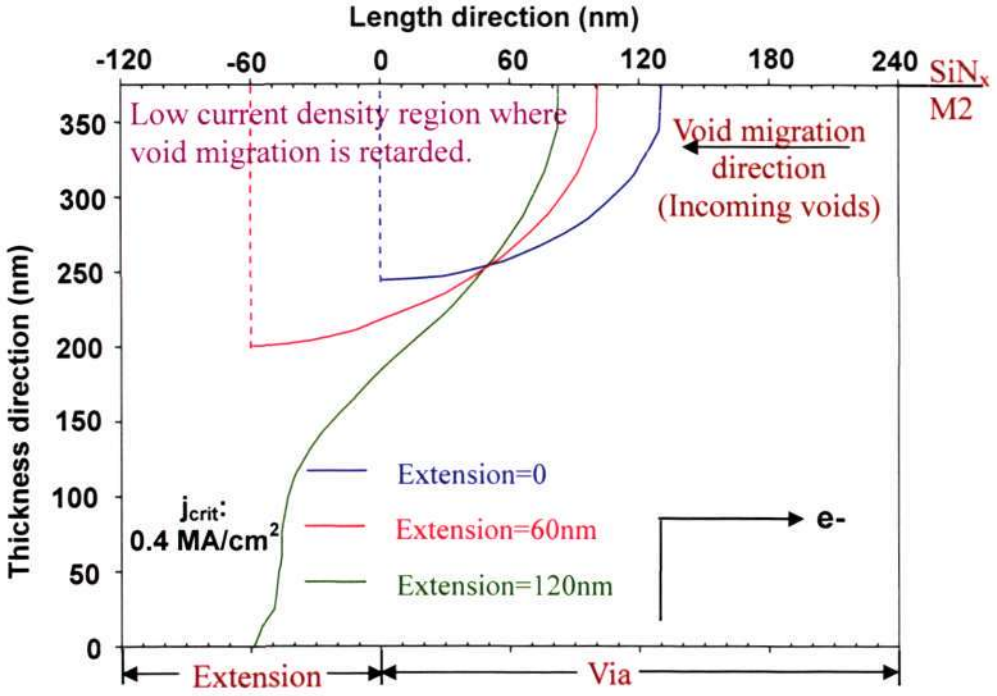


Figure 5.2 Overlaid contour lines around the extension region corresponding to 0.4 MA/cm^2 for varied M2 extensions.

It is observed in Figure 5.2 that the low current density zone changes in shape and shifts slightly to the left with varying M2 extensions. It is thus instructive to compare the "effective reservoir volume" above the cathode via in M2 extension, which is defined here as the overall geometrical volume above the via subtracted by the low current density volume. We use the effective reservoir volume of 0-extension as an internal standard to normalize all three cases with varied extension length. The normalized effective reservoir volumes for current densities of 0.3 to 0.5 MA/cm^2 are plotted with respect to the extension length in Figure 5.3. It can be seen that for 0 and 60 nm M2 extensions, the effective volume serving as void accumulation reservoir increases with increasing extension lengths at all current densities. However, this trend may change for the 120 nm extension because of current crowding around the via region evident in Figure 5.3. It may thus be summarized that increasing extension length from 0 to 60 nm

increases effective reservoir volume thus increasing the void volume that leads to via opening and improving EM lifetimes. However, further increase in M2 extension to 120 nm does not increase this effective reservoir volume and does not significantly improve EM lifetimes any further. This concept of effective reservoir volume successfully explains the experimental observations that MTF was doubled with extension increase from 0 to 60 nm, whereas there was arguably a ~5 to 10% enhancement on MTF as the extension length was further increased from 60 nm to 120 nm. The data analysis thus indicates that 60 nm may be the critical extension length beyond which increasing extension sizes have no effect on electromigration lifetimes. The effective reservoir volume plotted in Figure 5.3 also suggests that the critical current density below which significant void migration does not take place may be of the order of 0.4 MA/cm^2 in this study.

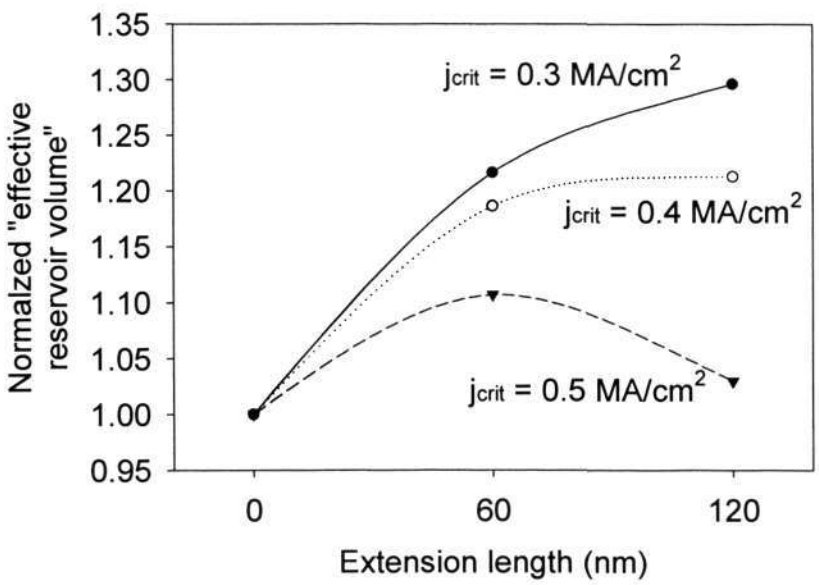


Figure 5.3 Normalized "effective reservoir volume" in terms of extension length.

5.2 Monte Carlo simulations

5.2.1 Development of Monte Carlo based EM simulation tool

The understanding of heterogeneous thermal gradient distribution in Cu interconnect give a guide for the study on the course of vacancy migration and capture at the Cu/dielectric-cap and Cu/barrier-liner interfaces. An analytical model was created using random atomic jumps based on the kinetic Monte-Carlo method. The evolution of several nano-scaled voids in a region, under electric current, at the confined Cu/dielectric-cap interface and in the bulk was governed by three forces: (a) the bonding strength from nearest neighbour ions that tries to tension and makes it stabilized, and (b) the electron wind force that pushes and eventually redistributes the surface atoms. Besides the electron wind force and the interaction form the neighbor atoms, the motion of voids is also influenced by some other parameters such as the low bonding energy at Cu/cap/liner edges, temperature induced stress gradient [153], high defects density at Cu/dielectric-cap interface and Cu/cap/liner edges due to the peculiar Cu in-laid process.

Thermal energy per atom at the site of high temperature (higher than Debye temperature) is *3kT* (*1.5kT* for kinetic energy of vibrations and *1.5kT* for potential energy of vibration deviations). Therefore the thermal energy difference between neighboring positions is *(3kT)*a*, where *a* is inter-atomic space. If we calculate this difference using the following properties: $gradT=3\times10^{3}$ *K/m*, $k=1.38\times10^{-23}$ *J/K*, and $a=3\times10^{-10}$ *m*, then the difference in thermal energy is about 3.7×10^{-29} *J*.

The void migration along current direction is driven by the electron wind force. The energy of one atom due to electron force is:

$$\varepsilon_e = F_c * a = \rho j Z_{ef} e a \tag{5.6}$$

Where Z^* is the effective charge number of the diffusing Cu atom, ρ is the resistivity of Cu, and $\boldsymbol{j}$ is the current density. In this study $j=1.2\times10^{10}\ A/m^2$. If we take $Z_{ef}e=30\times1.6\times10^{-19}\ C$ and Cu resistivity $\rho=1.7\times10\text{-}8\ \Omega\bullet m$, then the electron force during one atom jump is approximately $2.5\times10^{-29}\ J$. Therefore, the function of thermal gradient is at least four orders of magnitude lower than that of electron wind force. For simplification, we omitted the thermal gradient effects in this simulation.

Monte Carlo scheme is governed by calculation of change of energies for deciding success of an atomic jump between randomly selected neighboring atomic positions. The energy of an atom consists of the effective energy of an ion in the field of electron wind force $Z_{ef}e\vec{U}$ ($\vec{U}$ is the electric potential) plus the sum of pair interactions $z\vec{E}$ (z is the number of the nearest neighbors for the randomly selected atom).

$$\varepsilon_{at} = Z_{ef}e\vec{U} + z\vec{E} \tag{5.7}$$

The probability of atom displacement/jumping in the frame of a stochastic Monte Carlo model depends exponentially on the difference of vector of energies between connected atom and one of the nearest neighbor vacancies. Complete code for the simulations was written in MatLab and listed in *Appendix I*. A square lattice is employed for ease in programming and atomic jumps to eight neighboring atomic positions are considered. For random selection of atoms, only an atomic position with at least one neighboring vacancy was considered to save computational time. Pair interaction energies were re-calculated only after atom jump between an atomic location filled with an atom and a location with a vacancy. The force due to electron wind force was simulated by introducing a linear force gradient from one end of the line to another. The interaction energy was considered to be relatively higher than the gradient due to the electromigration wind force.

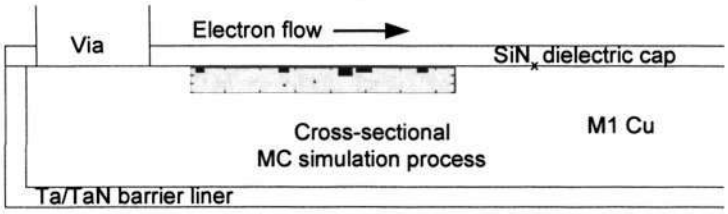
5.2.2 EM-induced voiding at Cu/dielectric-cap interface

To understand the course of vacancy migration and capture at the Cu/SiN_x interface, an analytical model was created using random atomic jumps based on the statistic Monte-Carlo method. The irreversible voiding processes have been proposed by combining electrical, thermal and mechanical forces on atomic diffusion. The phenomenological equations for atom flux could be expressed as [156]:

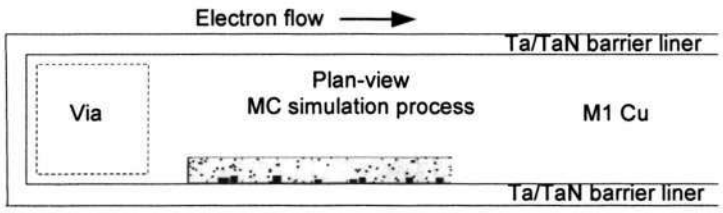
$$J_{at} = \frac{C_s D_s}{k_B T}\left(Z_{ef} e E_s - \Omega \frac{\partial W}{\partial x} \right) \tag{5.8}$$

where C_s is the atomic concentration of mobile surface atoms, D_s is the corresponding diffusivity, Z_{ef} is the effective charge of jumping ions, e is the elementary charge, E_s is the tangential component of electric field, Ω is the atomic volume, W is the sum of pair interactions from the unbroken nearest neighbor ions, and $\frac{\partial W}{\partial x}$ is the directional derivative along Cu/SiN_x interface.

The probability of atom displacement/jumping in the frame of a stochastic Monte Carlo model depends exponentially on the difference of energies between connected atom and one of the nearest neighbor vacancies. The simulation region covering couples of nanometers in the Cu segment from cross-sectional and plan-view observation was shown in Figure 5.4. The process of vacancy and void behavior in a region of Cu segment under electron field is shown in cross-sectional observation in Figure 5.5.



(a) Cross-section observation



(b) Plan-view observation

Figure 5.4 Illustration of Monte Carlo simulation regions.

Pre-existed little voids were assigned in this model to simulate the interface diffusion as the main electromigration path. The size of these pre-existed voids is small as the cluster of several vacancies. The percentage of vacancy was set as 2.5% in Cu/dielectric-cap interface while 0.1% in Cu bulk to *qualitatively* express the different vacancy concentrations at the surface and the bulk. Higher concentrations of vacancies at the surface are thought to be resulting from CMP, plasma, process, and growth stresses. In all the Monte Carlo dynamic models built in this study, the direction of electron flow is from left to right. Note that the simulation region is only several nanometers including hundreds of Cu atoms.

It can be inferred that these vacancies would collect and move from the bulk towards Cu/dielectric-cap interface (the top surface in this model) in a direction opposite to the electron flow. This observation is consistent with FIB and TEM observation of voids formation and migration at the cathode region of the line in Figure 4.2, 4.3, and 4.5.

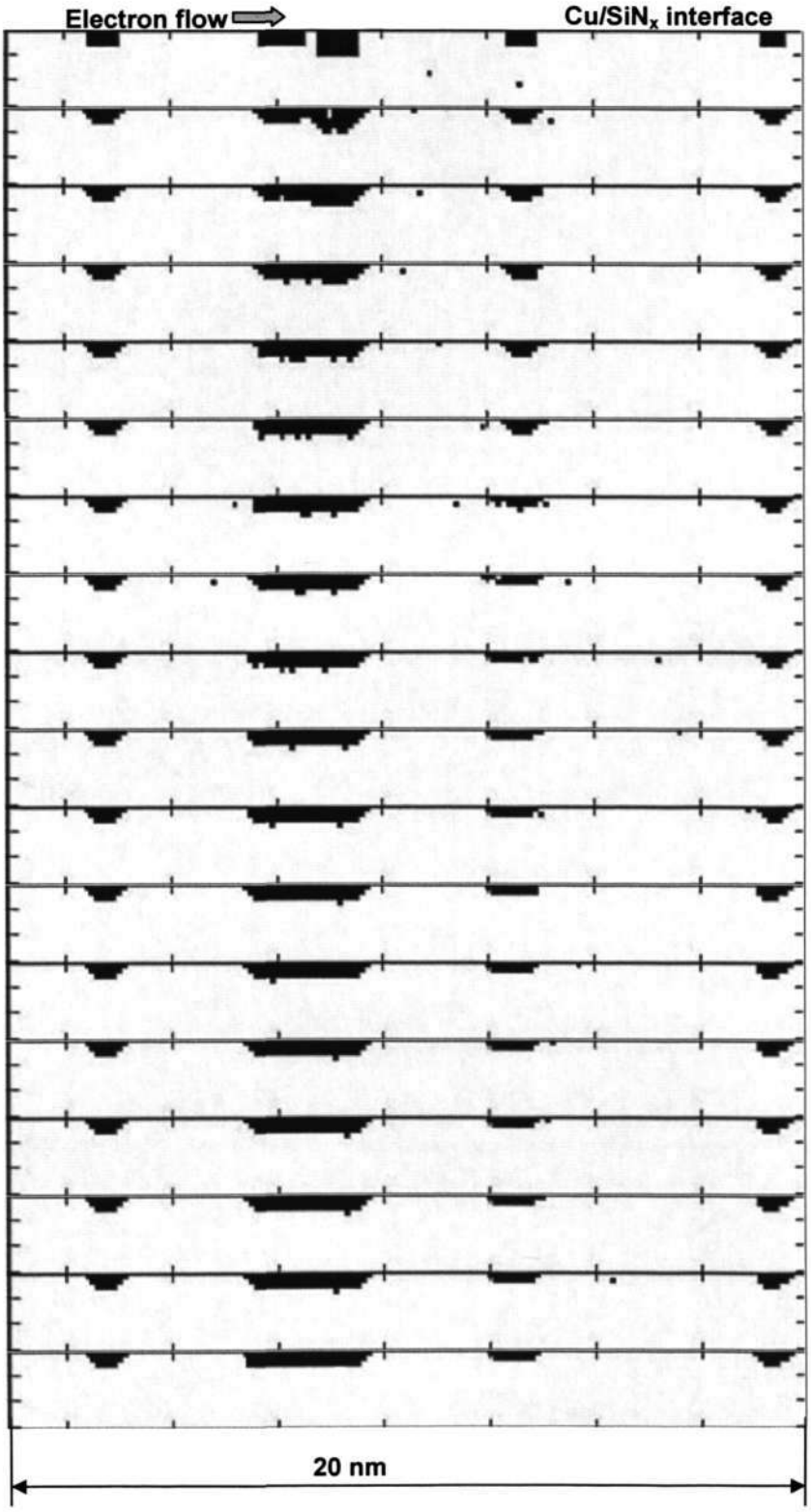


Figure 5.5 Monte Carlo simulation process of vacancies cumulative at top Cu/dielectric-cap interface from cross-sectional observation.

5.2.3 EM-induced voiding at Cu/cap/liner edges

The primary electromigration-induced voids at both of the Cu/cap/liner edges below the dielectric cap were observed in electromigration stressed interconnects as observed by FESEM (Figure 4.16), FIB (Figure 4.17), and TEM (Figure 4.17). The surface was grooved at Cu/cap/liner edges in stressed lines as compared with unstressed lines owing to the slit-like voids formation along Cu/cap/liner edges. It is proposed that the Cu/cap/liner edges at Cu interconnect served as the dominant electromigration-induced atom diffusion path driven by the electron wind force. In order to investigate the validation of this proposal, the observation of electromigration-induced void nucleation, migration, and coalescence on the top surface of Cu interconnects have been modeled by means of an analytical simulation from the plan-view observation.

In comparison with the central part of Cu/dielectric-cap interface, the condition of Cu/cap/liner edges are exacerbated more by residual mechanical and growth stresses besides low adhesion and bonding strength in this area. Besides, the percentage of surface defects and impurities introduced by wafer process at Cu/cap/liner edges were thought to be higher than that in other area in Cu interconnects [197]. Therefore, lower bonding energy was introduced at Cu/cap/liner edges, which represents the weak Cu/cap/liner bonding strength. On the other hand, several pre-existing small voids and more vacancies were assigned at Cu/dielectric-cap interface to denote the highly disorder and surface contaminations induced by Cu CMP and following dielectric cap deposition. Figure 5.6 exhibits the voiding process at Cu surface from the plan-view observation.

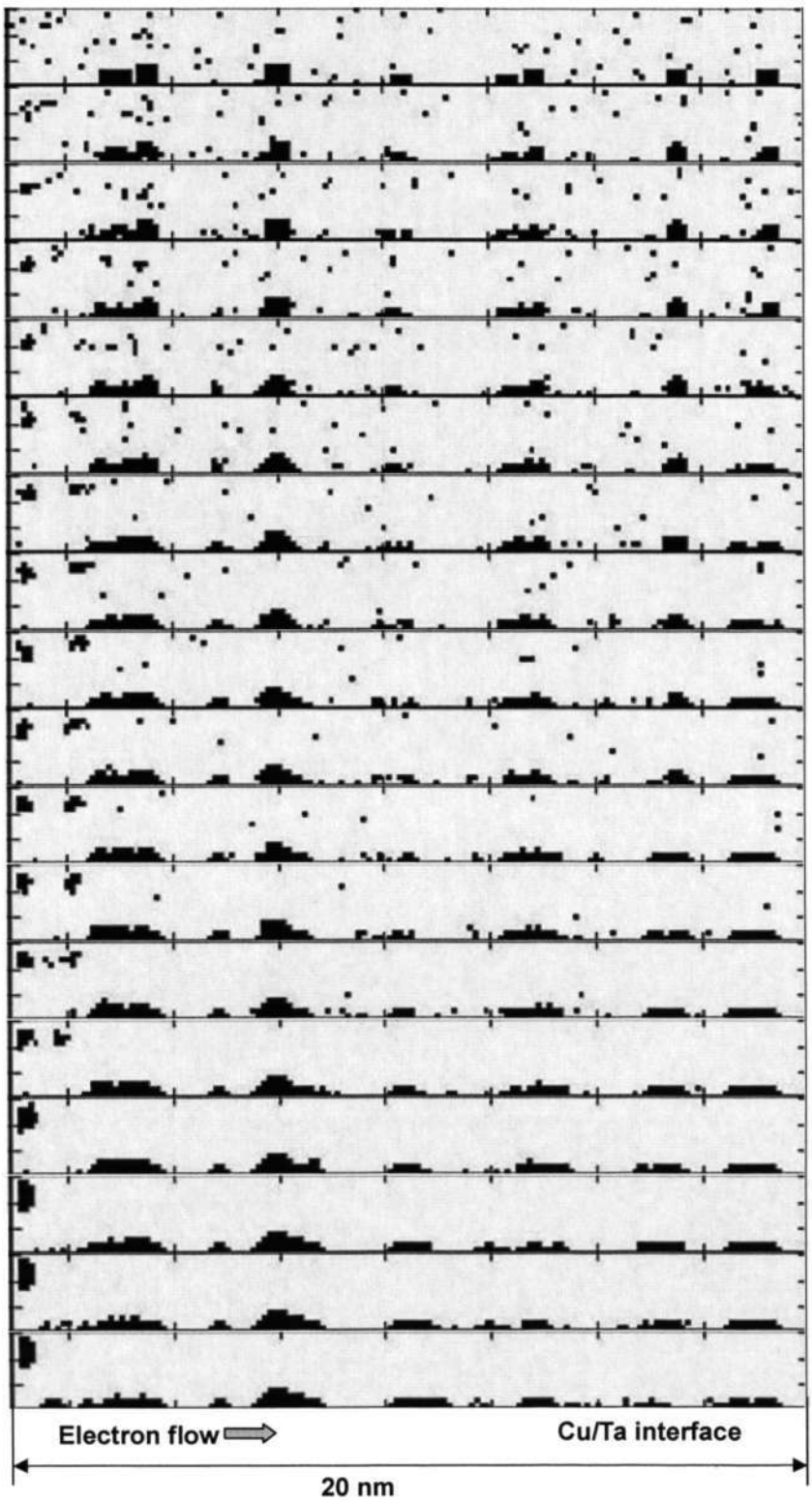


Figure 5.6 Monte Carlo simulation process of vacancies cumulative at Cu/cap/liner edges from plan-view observation.

Take note that the simulation area is only a small region in Cu interconnect, containing dozens of atoms in width and hundreds of atoms in length. Only one Cu/dielectric-cap/liner edge can be taken into account in our model. In spite of this, the trend of vacancies accumulation and void migration are clearly shown in this model.

It can be inferred from simulation results in Figure 5.6 that these vacancies would collect and move from the bulk towards Cu/cap/liner edges (the top and bottom edges in this model) in a direction opposite to the electron flow. This observation is consistent with FESEM, FIB, and TEM observation of voids formation and migration at the cathode region of the line in Figure 4.18, 4.19, and 4.20, and gives a clear idea about the void movement process to support the proposal of *Cu/cap/liner as the dominant electromigration path.*

5.2.4 Grain boundary effects on voiding process

The migration and coalescence of voids as well as their interactions with grain boundaries in the presence of the electric wind force is crucial for understanding the failure mechanism in Cu interconnects. From Prof. Gusak's simulation results [156], void trapping at GB is already known. In this study, the author is trying to complete the simulations on void nucleation combined with the effect of grain boundary as soon as possible. Two kinds of high angle grain boundaries would be taken into account. GB1 represents the grain boundary cross the line but disconnected to the surface defect or vacancy, while GB2 connected to a surface defect or void. To simplify, the grain boundaries were set to be vertical to the interface. The simulation processes are shown in cross-sectional observation in Figure 5.7, and in plan-view observation in Figure 5.8.

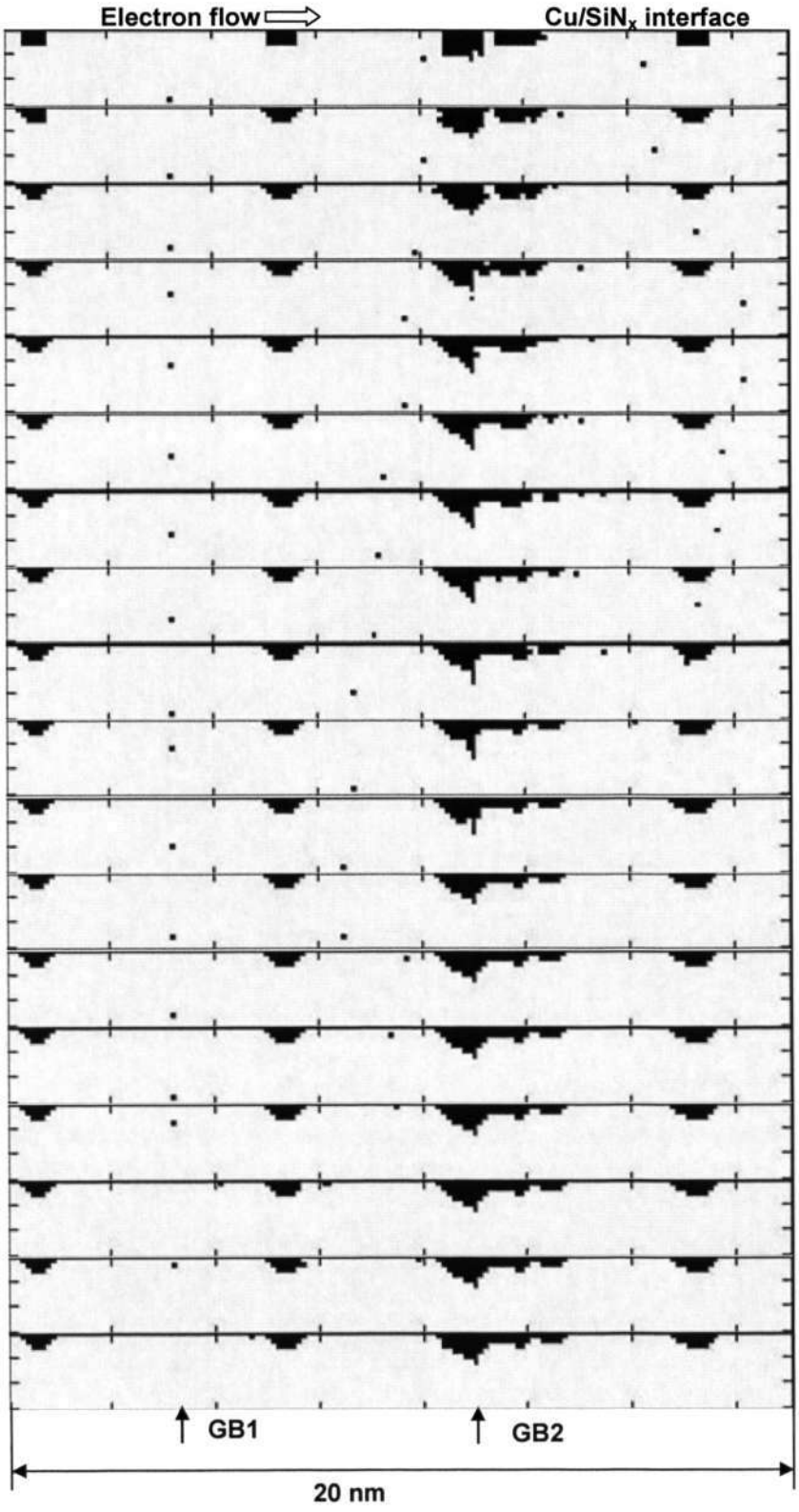


Figure 5.7 GB effects on voiding process from cross-sectional observation.

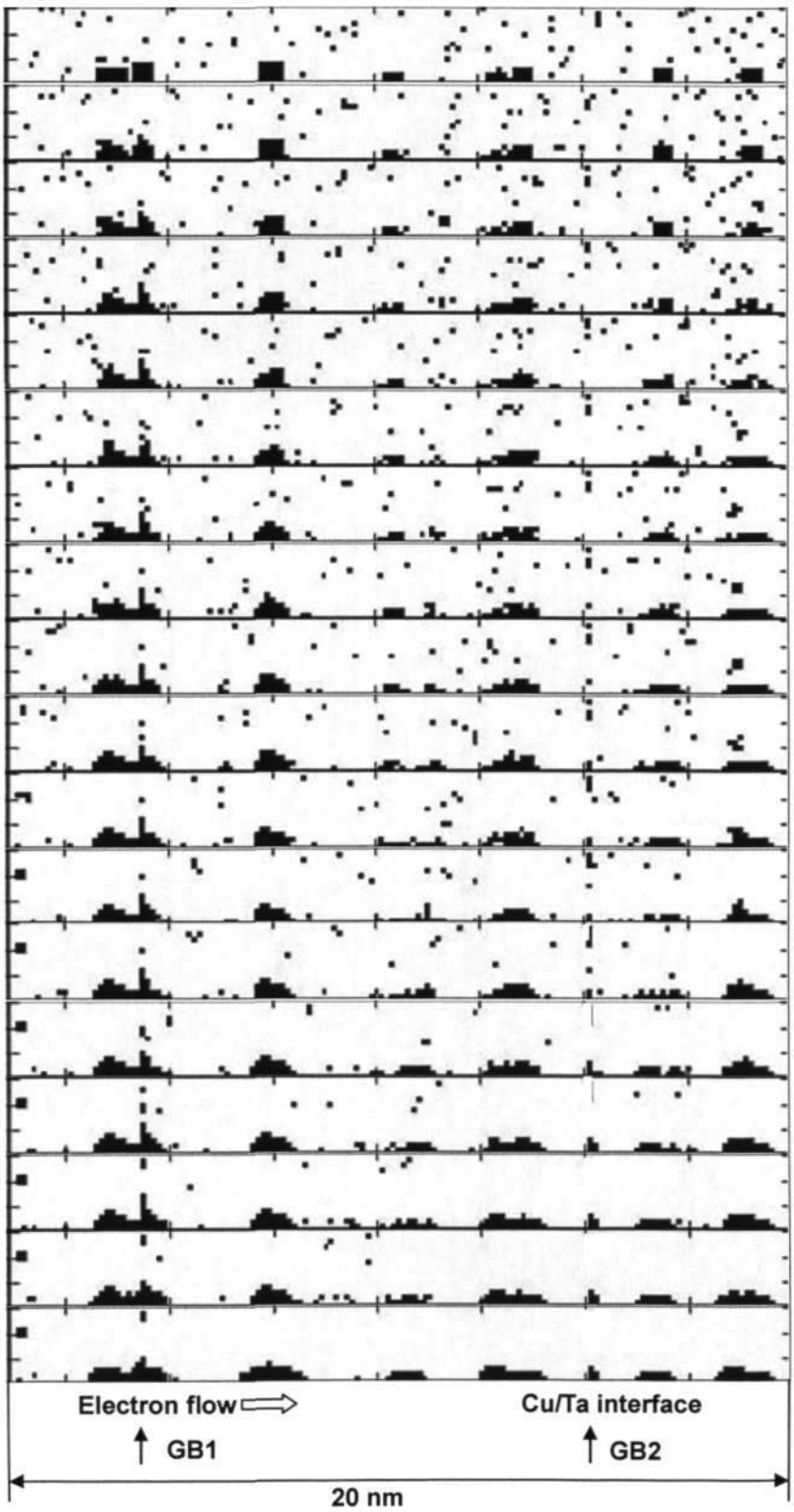


Figure 5.8 GB effects on voiding process from plan-view observation.

It can be inferred that these vacancies would move towards Cu/SiN_x interface from bulk and collect at Cu/dielectric-cap interface and more significantly at Cu/cap/liner edges to form voids. Besides, voids migrate and elongate along Cu/dielectric-cap interface in a direction opposite to electron flow. Voids can be trapped by grain boundaries with/without a pre-existed void connected to it. Simultaneously, vacancies collect and voids grow continuously inside grain boundary region. If an interface defect or void is present in grain boundary (i. e. GB2), trapping of voids towards grain boundary is easy because there in high vacancy density which leads voids growth in a fast rate to reach the critical size [153] and escape from the bound of grain boundary and move away and grow continuously [198]. If there is no interface defect or void present in grain boundary (i. e. in GB1), voids would hold on in this grain boundary in a longer time. We thus expect that the grain boundary connected to an interface defect would facilitate void growth and migration, whereas the grain boundary disconnected to interface defect would hold void for a longer time as a hampering site.

In summary, the models built in this research work can qualitatively explain electromigration-induced voiding process observed during experiments and characterizations as well as in various other reported electromigration studies. Based on these models, it can be inferred that peculiar electromigration-induced void evolution in Cu interconnect structures is mainly due to weak interfaces like Cu/dielectric-cap interface and Cu/cap/liner edges which act as vacancy sink and due to reconstruction of atoms at interface. However, this model is relatively simple with many approximations. Therefore, it can provide only a qualitative explanation of voiding process during the initial stage of electromigration-induced degradation in Cu interconnects. These findings warrant the need to re-investigate electromigration mechanisms by developing rigorous

models based on similar concepts, considering other important parameters such as microstructure, current density distribution, stress and temperature gradients, and introducing diffusivities for different atomic transport paths using kinetic Monte-Carlo and finite-element methods. Such approaches will provide quantitative information and further in-depth understating of electromigration-induced voiding in damascene Cu interconnect structures.

Chapter Six: Discussion

6.1 Reservoir effect on electromigration

Current understanding of tensile stress theory states the high tensile stress develops at the cathode end of the via during electromigration, where the Ta liner forms a blocking boundary to the diffusing Cu atoms, and it serves as the electromigration void nucleation site. If the critical tensile stress for void nucleation is reached, a void forms [34]. In M2 Cu interconnects, the maximum tensile stress is reached at the base of the via above the Ta barrier liner.

Another theory was proposed for explaining voids formed in the low current density region such as reservoirs based on current crowding [23]. This current crowding theory explained that due to current density gradient induced vacancy drift [199, 200], there should be vacancy accumulation and super-saturation in the upper corner of M2 line extension [24]. According to this theory, there is a current density gradient between lower corner to extension in M2 line above the via, which may induce a flux of vacancies to accumulate at the upper corner. A void will nucleate, grow, and eventually deplete the entire cathode end of the strip. Both of these theories propose that void should nucleate at the cathode via region and subsequently coalesce and grow.

However, our observations indicate that voids are heterogeneously nucleated at the Cu/SiN_x interface away from the via. Sites for heterogeneous nucleation may include grain boundaries and other structural imperfections. FIB image (Figure 4.2) shows voids along the Cu/SiN_x interface that may well extend in to the M2 extension area. Due to electron wind force of electromigration, atoms are driven along the direction of electron

flow along the surface of the void, so the voids are driven to move towards the cathode end against the electron flow direction.

This electromigration induced void movement mechanism is illustrated by Figure 6.1, revealed during in-situ electromigration characterizations of similar structures have been published [65, 154]. Void agglomeration eventually at the cathode end creates a void large enough to block current flow through the via, finally leading to open circuit failures.

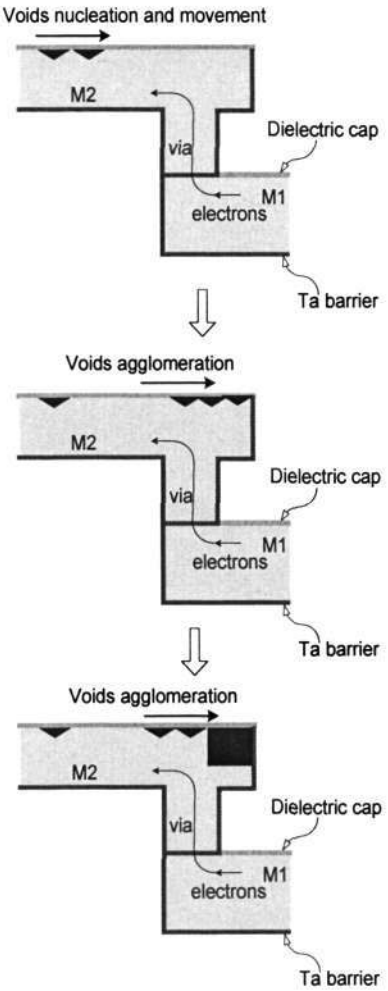


Figure 6.1 Proposed electromigration failure mechanism in M2 structure with extension.

The observed reservoir effect may be explained by void migration and agglomeration mechanism [154]. Voids are heterogeneously nucleated at the Cu/dielectric interface in the M2 line, which migrate in a direction opposite to electron flow. These voids finally reach the cathode end via and agglomerate to form a void which leads to resistance increase and eventual open circuit failure. If a reservoir is present at the cathode via, the voids will agglomerate at the reservoir and the formation of a large void that blocks current flow in the via region is delayed. This may explain why MTF increased significantly as the reservoir length was increase to 60 nm as compared with the samples without extension and thus without any form of a reservoir. Further increase in the reservoir lengths from 60 nm to 120 nm did not result in any further increase in MTFs (Figure 4.1 (a)). This may be postulated to be partly contributed by the statistical nature of the failures. It may also be potentially be due to the fact that the area of the extension has very low current densities and the driving force to move the voids further into the areas of the extension is much reduced. According to the calculation in section 5.1, the 60 nm may be the critical extension length beyond which increasing extension sizes have no effect on electromigration lifetimes. The effective reservoir volume plotted in Figure 5.3 also indicates that the critical current density below which significant void migration does not take place may be of the order of 0.4 MA/cm^2 in this study.

6.2 Cu surface treatment effect on electromigration

The improvement of electromigration life time in Cu interconnects by introducing Cu surface treatment, as a surface modification after CMP, have been reported [26, 62, 201]. It is suggested that the surface treatments modify the Cu/dielectric-cap interface leading to change in adhesion between Cu and dielectric cap, which in turn influences the

Cu/dielectric-cap interface dominated electromigration. Plasma H_2 and SiH_4 treatments were found to yield the best improvement in electromigration performance.

NH_3 treatment is reported to cause the reduction of Cu oxide as well as formation of CuN leading to a better Cu/SiN_x interface [202]. This is also supported by the present XPS analysis (Figure 4.13). Hydrogen plasma treatment is known to form hydride on the Cu surface with no change in microstructure [203-208] and to clean the Cu surface [202] providing better adhesion between Cu and subsequently deposited silicon nitride dielectric-cap layer. Improvement in electromigration performance due to hydrogen has also been attributed to interfacial segregation of hydrogen and the reduction of defects by athermal annealing [209, 210]. Thus the observed improvement in H_2 treated samples may have been contributed by formation of hydrides or reduction of Cu oxide with consequent better adhesion. The present XPS analysis in Figure 4.13 indicated that the H_2 plasma treatment also facilitates the formation of both Cu-N and Cu-Si bonds at the interface, (also can be seen in Figure 4.11 (a)) which directly improve the electromigration performance. Improvement due to SiH_4 treatment may be attributed to silicide formation on the Cu surface [211]. The change in the Cu/dielectric-cap interface due to surface treatments is supported by the XPS data in Figure 4.13 which showed large portion of Si-Cu bond in the Si 2p and shift in the Cu 2p spectra for SiH_4 treated samples as compared to control sample with no surface treatment and NH_3 treated samples. Cross-sectional TEM image before EM tests (Figure 4.11) and TEM/EELS analysis (Figure 4.12) also indicated the Cu silicide formation in the interlayer between Cu and SiN_x dielectric cap for SiH_4 and H_2 treated specimens. It should be noted that the TEM/EELS analysis on Cu mapping indicated the inhomogenous distribution of Cu in the interlayer. The density of Cu is higher in the upper part (i. e. near SiN_x cap) that that in the

lower layer (i. e. near Cu line). Amorphous N-based diffusion barrier was commonly used in Cu metallization due to its higher thermal stability against Cu diffusion and ability to offer lower resistivity [212, 213]. In this study, the diffusion of Cu atoms in the interlayer can be retarded effectively by the SiN_x dielectric cap during the course of annealing. More Cu atoms would accumulate at the upper boundary between the interlayer and SiN_x dielectric cap, which in turn increase the density of Cu composition in this point.

Terrace-ledge-kink (TLK) model has been put forward to explain the surface diffusion phenomena [214], where a continuous flux of adatoms on the surface is necessary (Figure 6.2). The kink sites are believed to be the source of the adatom flux since at the kink sites the transition to an adatom involves the breaking of the smallest number of bonds. Therefore, the key to stop or retard the surface/interface electromigration in Cu interconnects is to reduce the number of kink sites or to increase the energy needed to dissociate Cu atoms from the kink sites. In the present study, the formation of Cu-N and Cu-Si bonds can both passivate the kink sites. However, it is expected that Cu-Si bond is much stronger than the Cu-N bond. From thermodynamic point of view, Cu-Si has a bond formation enthalpy around -220 kJ/mol [215], whereas that for the Cu-N bond is around -30 kJ/mol [216]. Therefore, it is the formation of Cu silicide that will enhance the EM lifetime more, which is the case for H_2 and SiH_4 treated specimens. The contribution of Cu nitride to EM reliability is much less appreciable than that of Cu silicide.

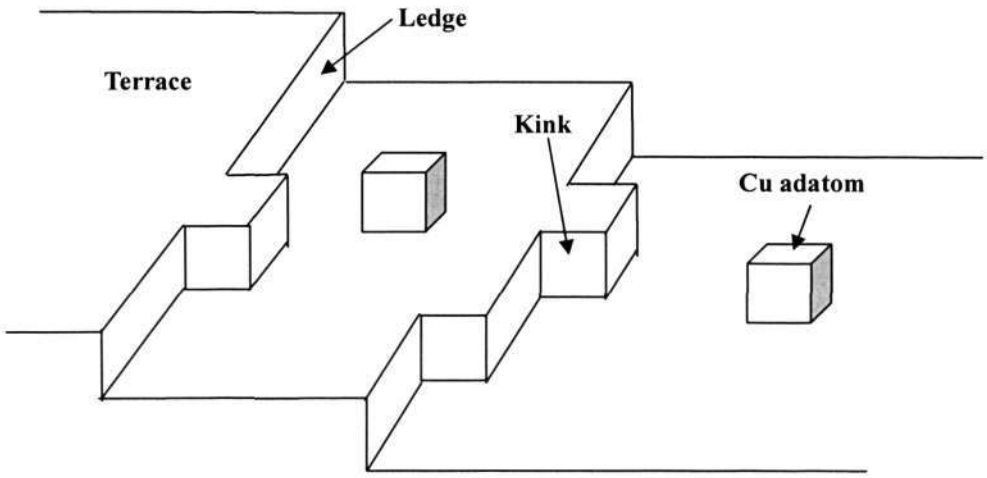


Figure 6.2 Schematic of the TLK (Terrace-Ledge-Kink) model of surface structure.

Microstructural changes arising from surface treatment cannot be completely ruled out, but this change and its effect on electromigration is likely to be less significant since the grain structure was stabilized due to post-Cu deposition anneal and TEM images (Figure 4. 12) showed bamboo-like grain structure with large grains. The observed improvement in electromigration performance due to surface treatment supports Cu/dielectric cap interface dominated electromigration failure mechanisms that we comprehended in our previous investigations [26, 65, 91, 92, 155].

6.3 Cu surface roughness change

Experimental observations have established that Cu is prone to diffuse along the Cu/SiN_x interface under electromigration test because of the weak bonding strength between Cu and dielectric SiN_x capping layer. During electromigration, atoms and vacancies redistribute under the electron wind force and the back stress force, which leads to vacancies capture at the Cu/SiN_x interface and more significantly at Cu/SiN_x/Ta edges. Vacancies in the Cu interconnect rise from the Cu surface region towards the Cu/SiN_x

interface. At this interface they agglomerate to form voids which are further swept opposite the direction of electron flow towards the cathode. Vacancies tend to accumulate preferentially towards the edges of the lines leading to agglomeration and formation of voids. During the course of electromigration-induced void formation and migration, the Cu atoms in the region of voids surface redistribute to form the new Cu surface. Owing to Cu atoms redistribution and reconstruction around the voids, the Cu surface is postulated to have become rougher induced as seen in the FESEM images (Figure 4.15).

The mechanical and thermal stresses are thought to be higher at Cu/cap/liner edges than in other areas at Cu/dielectric-cap interface. During electromigration test, vacancies are more likely to accumulate at these edges to relax the high stress gradient [217]. In addition, the vacancy density at Cu/cap/liner is thought to be higher than that in other areas at Cu/dielectric-cap interface. The vacancy gradient along the width direction also contributes to the motion of vacancies. Therefore, vacancies more likely accumulate at Cu/cap/liner edges and then span the most of the width of testing interconnect with void growth. The preferential agglomeration of the vacancies and voids at the Cu/SiN_x/Ta edges results in the grooving at edges of stressed Cu line, as observed in the Monte Carlo simulation and AFM observations as well (Figure 4.14). The proposal of Cu/cap/liner edge serving as the dominant electromigration path is put forward here. The detailed explanation will be given in the following section.

To explain the HF attack on SiN_x based dielectric cap and the SiO_2 IMD, one needs to consider the reactivity of HF with SiN_x and the SiO_2 as well as the stress in the cap layer. In occasion of electromigration voiding, the dielectric cap is subjected to a high stress and more intensively at Cu/cap/liner edges in testing line. It is proposed that the dielectric cap on top of tested line is possible to be in a state of high tensile stress under

electromigration stressing. While the dielectric cap is considered to be rarely stressed in dummy lines since very few changes in the Cu/cap/liner edges were found in unstressed dummy line. As an etching solution, HF acid etches SiO_2 much faster than SiN_x [218]. The stage of high tensile stress in SiN_x based dielectric cap and around the Cu/cap/liner edges make it easier for HF to attach the cap layers in the stressed lines; and the subsequent damage of the SiO_2 IMD along the barrier liner ensues. On the other hand the cap in unstressed lines is able to resist the HF attack and the IMD is unaffected.

6.4 Cu/cap/liner edge as the dominant electromigration path

Experimental observations have established that Cu is prone to diffuse along the Cu/dielectric-cap interface and the Cu/cap/liner edges owing to a combination of weakness due to low adhesion and bonding strengths, residual stress due to metallization process, grain growth during annealing treatment, and cooling down from annealing temperature (400 - 450 ^{o}C) [219-222]. During electromigration, atoms and vacancies redistribute under the electron wind force and ensuing vacancy capture at the Cu/cap interface and more significantly at Cu/cap/liner edges acts to relax these stresses [223].

Vacancies at Cu/cap/liner edge were deemed to have high possibility to migrate under driving force for electromigration given by $F_e = Z_{ef} eE$, where E is the externally applied electric field, and Z_{ef} is the effective valence, which is often presented as an intrinsic material property [224], is dependent on multiple electron scattering effects in the immediate vicinity of migrating vacancies [225, 226], as well as on scattering from all other vacancies in the line [227, 228]. Since the vacancies along with some primary voids are concentrated in a higher density at Cu/cap/liner edges, leading to an uneven interface at edges, the electron scattering effect at Cu/cap/liner edges

is believed to be higher than that in other areas including the top interface of the stressing line. Thus the value of Z_{ef} could be higher at Cu/cap/liner edges, which in turn provides a high driving force for Cu atoms at Cu/cap/liner edges. Therefore, Cu atoms at Cu/SiN_x/Ta edge have more possibility for migration because of the higher driving force compared to atoms at other regions of Cu/dielectric-cap interface.

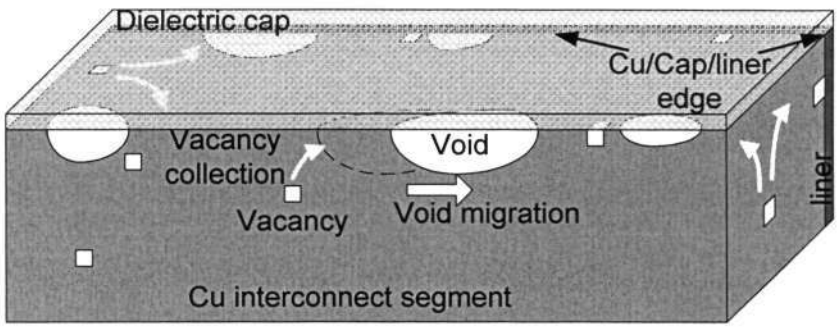


Figure 6.3 Illustration of vacancy collection and void migration towards Cu/cap/liner edges in stressed Cu interconnect.

Based on experimental and modelling results in this study, the course of vacancy accumulation, agglomeration, and void migration is illustrated in Figure 6.3 Electromigration mass transport is a vacancy sensitive process and it should be faster in the Cu interconnect where the vacancy concentration is higher [229]. Vacancies in the Cu interconnect migrate from the bulk towards the Cu/dielectric-cap interface. At this interface they agglomerate to form voids which are further swept opposite the direction of electron flow towards the cathode. Moreover, from the Monte Carlo simulation process in Figure 5.5, another effect of vacancy migration towards the Cu/cap/liner edges is also observable. Vacancies tend to accumulate preferentially towards the edges of the lines leading to agglomeration of voids at the Cu/cap/liner edges. It may be argued that voids

will heterogeneously nucleate at sites with highest defect density, thus nucleation of voids may be more likely at grain boundaries or Cu/cap/liner edge than at the Cu/cap interface. Based on the *qualitative* results of Monte Carlo simulation presented here, voids will agglomerate at the Cu/cap/liner edge and subsequently grow from both edges so as to span the entire width. The preferential agglomeration of the vacancies and voids at the Cu/cap/liner edge, as observed in the Monte Carlo simulation, is supported by the FIB and TEM observations of voiding along the Cu/cap/liner edges (Figure 4.19 and 4.20). These observations support the notion that the dominant electromigration driven void migration path is along the Cu/cap/liner edges.

6.5 Influence of Cu ECP on Electromigration

The influence of Cu ECP on electromigration behavior was examined in the previous chapter (section 4.5.1). This influence is seemed to correlate with the microstructure and surface topology of electroplated Cu interconnects. Based on the understanding of void migration, trapping and escape mechanism (section 4.5) and Monte-Carlo simulations (section 5.2.4), we demonstrated that different microstructures of Cu interconnect result in different kinetics of void formation and evolution. A schematic illustration of microstructure morphology and interface condition model was put forward in Figure 6.4.

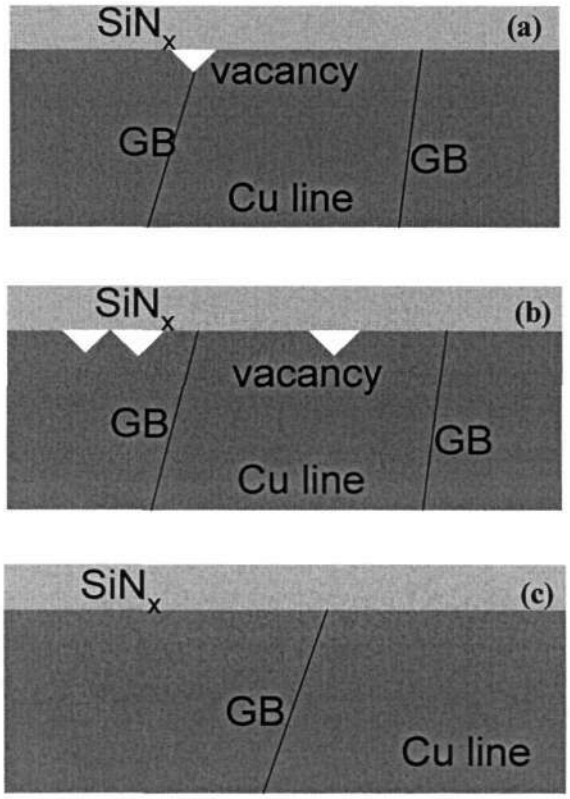


Figure 6.4 Illustration of microstructure and interface conditions in Cu interconnects made by (a) DC-plating; (b) multistep DC-plating; and (c) pulse-plating.

Pulse-plated Cu interconnects were reported to show denser structure with less porosity, large grain size, less impurities, and moderate CMP polishing rate, compared to DC-plated deposits for the same interconnects feature [230]. Thus the vacancy density in Cu bulk and the number of grain boundaries could be reduced notably by pulse-plating. The less vacancy source traded the propagation of electromigration voids, which leads to the slow increase of interconnects resistance. In addition, the possibility of lattice and gain boundary diffusion in Cu interconnects could be effectively minimized. It is also reported that pulse current had a smoothening effect on the Cu surface [231]. Hence, less defects and vacancies were present on pulse-plated Cu surface, which leads to a decrease

in the possibility of surface voids formation. More over, the clean and smooth Cu surface is expected to contribute to the good adhesion between Cu and dielectric cap, which cause the further improvement in electromigration resistivity of pulse-plated Cu interconnects. The good adhesion plus the less defects cause the gradual change in resistance during electromigration stressing. The adhesion study of ECP Cu to the dielectric cap can be one of our future works to pursue the in-depth understanding of the relationship between Cu ECP and electromigration behavior. Pulse plating has clearly improved the interface profile (i. e. less surface defects) and the microstructure (i. e. reduced number of grain boundary and vacancy density) Cu interconnects. Pulsed-plated Cu interconnects are also considered to have a reduced contribution to grain boundary diffusion and also reduce interfacial diffusion which is attributable to vacancies and surface defects.

The number of grain boundaries in multistep plated and DC plated Cu interconnects are higher than that in pulsed-plated Cu interconnects. This increase the possibility of grain boundary diffusion of standard DC-plated and multistep DC-plated Cu interconnects. On the other hand, the introduced impurities are more likely in Cu bulk, leaving few vacancies on Cu surface. The interface condition can still be good because of the reduced density of surface vacancy. Thus the electromigration lifetime of multistep DC plated Cu interconnects are a bit lower than that of pulsed-plated counterparts.

It has been generally recognized that the Cu atoms in grain boundary have the lower bonding strength and lower stability than the atoms in Cu bulk. Under electromigration stressing, it is easer for atoms in grain boundary to move away driven by the electron wind force. It also has been recognized that the electromigration-induced voiding preferentially occur at interface defects near cathode end. Thus the vacancies collection and agglomeration along Cu/SiN_x interface sensitively at the intersectional point between

surface defect and Cu grain boundary. As shown in TEM image in Figure 4.24 (a) and Monte Carlo simulations, surface defect connected to Cu grain boundary in DC-plated Cu interconnects exacerbate vacancies accumulation and thereby reduce electromigration reliability. As a result, void migration makes the concavity at the intersection point between Cu grain boundary and SiN_x cap more evident (Figure 4.25 (a)).

6.6 Grain size change subjected to electromigration stressing

Reduction in the grain size after electromigration at the M1 cathode end below the via was observed (Figure 4.26). When the Cu interconnect is subjected to high current densities, Cu atom transportation takes place along the direction of electron flow. Because Ta layer at the via bottom serves as a flux barrier, migrating atoms are blocked under the cathode via as illustrated in Figure 6.5. Atom concentration at the M1 end leads to mass increase with time. This mass transfer at micro scale [232] results in a large stress gradient accumulation along the M1 strip. As a result, equilibrium lattice structure is disrupted and dislocations are formed around the M1 end. When the number of accumulated dislocations reaches a critical value, new grain boundary nucleates at this point [233]. It is reported that the Cu recrystallization related to the amount of stress change in Cu interconnects during heat cycle [234]. Cu recrystallization in a 1.4 μm interconnect was observed during heating at 200 ^{o}C since a substantial amount of compressive stress change to about 20 MPa. The critical compressive stress for polycrystalline Cu bulk is about 8 kg/cm^2=0.8 MPa. Thin metal film often support higher stresses than their bulk counterparts, and their yield stresses is thought to relate to the grain size in metal thin films. As described in Hall-Petch relationship in Equation 6.1, the

critical stress for dislocation formation in Cu thin film interconnect depends on the reciprocal of the film thickness.

$$\sigma_y = \sigma_0 + k_y / \sqrt{d} \qquad (6.1)$$

Where k_y is the Hall-Petch coefficient, and σ_0 is the contribution from other strengthening mechanisms, such as impurities or dislocation interactions. If we take d≈0.4-0.5 μm in our case, with the function derived from Ref. [235], σ_y is estimated as less than 40 MPa at room temperature. With the temperature increases, the critical compressive stress decrease accordingly [236]. Note that the tensile stress at M1 end is around 100-150 MPa (Figure 5.2). The difference between the initial tensile stress and the critical compressive stress is only 140-190 MPa. During electromigration stressing at 300 °C, the tensile stressed relaxed along the thermal-elastic Cu line and became compressive stresses [236], as a results of mass transportation, as well as the constraint from SiN_x cap and surrounding SiO_2 IMD.

It should be noted that the Hall-Petch relationship may not exactly applicable for the nano regime in our case. In the thesis, it was used to explain the modification of grain size at certain condition qualitatively. From the current understanding, it is hard to fine the more suitable relationship compared to Hall-Petch equation. Therefore, Hall-Petch was employed in this case as the fundamental to present the author's viewpoint.

Moreover, electromigration test temperature is 300 °C in this study, higher than the recrystallization temperature of Cu, which is around 220 °C (Recrystallization Temperature is typically between one third and one half of the melting point temperature of a metal or alloy and depends on several factors including the strain and stress stage [233]. For Cu used in Cu interconnects fabrication, the Recrystallization Temperature is around 220 °C). The Cu yield and compressive stress between 150 MPa to 250 MPa were

observed in 500 nm Cu thin film [236]. Under electromigration and mechanical stressing, Cu grains at the M1 end were in a relatively high strain energy state, formation of a new set of strain-free and equiaxed grains that have low dislocation densities may take place [237]. Thus Cu recrystallization is likely to occur. Therefore the microstructure in the M1 Cu may be influenced by a combination of atoms diffusion induced by electron wind force, accumulated hydro-stress, and recrystallization aided by high diffusivities at electromigration test temperatures.

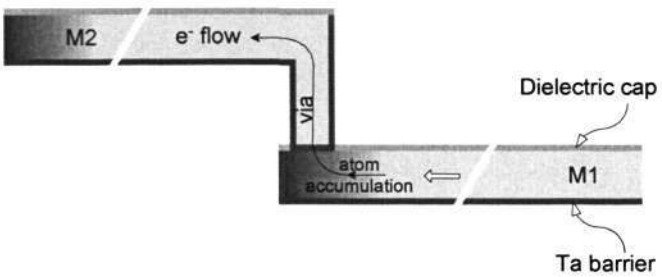


Figure 6.5 Illustration of stress gradient induced by electromigration in M1 Cu line.

Chapter Seven: Conclusions and Future Work

7.1 Conclusions

The objectives of this research were to study the effect of interconnect structure (specifically reservoir effect) on electromigration, the influence of Cu surface engineering and bulk microstructure on electromigration behavior, and the impact of electromigration stressing on the change in Cu surface evolution and microstructure profile. The main conclusions in this study are summarized below.

➢ **Interconnect structure Effects**

1. Electromigration induced voids, in Cu dual-damascene interconnects, were found to nucleate preferentially at the interface of Cu and dielectric cap away from the cathode region. This validates the proposed theory of heterogeneous void nucleation away from the cathode followed by void movement and coalescence at the cathode.
2. The reservoir effect was studied in Cu damascene interconnects with different M2 extensions ranging from 0 to 120 nm at 300 ^{o}C and 1.2 MA/cm^{2}. Improved lifetimes were observed with an M2 extension of 60 nm, however further increase to 120 nm did not significantly impact MTF values.
3. Improved lifetimes with M2 extensions can be explained on the basis of a "reservoir effect" where voids are collected in the M2 extensions and can thus delay the onset of open-circuit failures. The lack of noticeable improvement in MTF from 60 nm to 120 mm may be explained on the basis that the extension area

has very low current densities and the driving force to move the voids further into these areas may not be significant.

➢ **Cu surface engineering effect and surface evolution subjected to EM**

4. Silane gas and hydrogen plasma treatments were found to yield the best improvement in electromigration performance in previous study. TEM/EELS analysis and XPS survey exhibited the formation of Cu silicide prior to nitride formation which could improve EM lifetime appreciably.
5. The evolution of the Cu surface subjected to electromigration stresses is reported here based on AFM, TEM, FESEM characterizations. Roughness change in the Cu surface as well as the grooving of the Cu/SiN_x/Ta edge was observed.
6. The dominant electromigration-driven diffusion path is investigated here based on TEM, FIB, and simplified Monte Carlo simulations. A higher propensity of void formation along the Cu/cap/liner edge was observed. The experimental observations presented in this study along with the *qualitative* observations from Monte Carlo simulations yield a new understanding and scenario of electromigration failure mechanism in Cu interconnects.
7. This study suggests that in addition to the efforts made in strengthening the Cu/cap interface with alloying and surface cleaning, special attention also needs to pay towards the Cu/cap/liner interface to effectively impact electromigration lifetimes.

➢ **Cu microstructure effect and grain size change subjected to EM**

8. Pulse-plating resulted in the highest electromigration reliability owing to the perfectly smooth Cu/SiN_x interface with relatively few interface defects. Multistep DC-plating and standard plating on the other hand displayed rougher surfaces and

increased grain boundaries. These defects and grain boundaries are thought to result in lower electromigration lifetimes as compared with pulse plating.

9. Based on TEM imaging, grain size of Cu at M1 cathode end under the via was found to be reduced, possibly caused by the high compressive stress in conjunction with Cu recrystallization in the area under the via that was restrained by the Ta boundary.

➢ **FEA and Monte Carlo simulations**

10. Based on the FEA simulation, a low current density zone in the M2 extension corners above the cathode was observed. This region is seen to retard the void migration into the extensions. Based on the present analysis (simulation and experiment), a 60 nm extension appears to the critical extension length beyond which increasing extension sizes have no effect on electromigration lifetimes.
11. A simple dynamic model which was implemented using random atomic jumps based on Monte Carlo method was built to simulate electromigration-induced voiding process. This simplified methodology was shown to *qualitatively* explain electromigration induced void movements.
12. This simplified methodology was used to explain the experimental observations of the Cu/cap/liner being the dominant electromigration path.

7.2 Future work

7.2.1 Material characterization for study of Cu grain size change

The effect of grain boundary modification and interface improvement by Cu ECP

techniques on electromigration behavior was studied in previous part. It is reported that the strong <111> texture in Al interconnects contributed to the enhancement of electromigration lifetime [238] since the minimized number of high-angle grain boundaries which can act as fast diffusion paths [239]. In advanced Cu interconnects, the interfacial electromigration and Cu/dielectric-cap interface were found to be the key factors affecting the electromigration performance in Cu interconnects. Especially the Cu/cap/liner edge was found experimentally and numerically to serve as the dominant electromigration path. If the interface conditions are improved, the importance of Cu microstructure such as grain size, grain boundaries, and grain orientations will be revealed. Some study argued the <111> texture still contribute to enhance the electromigration reliability in Cu interconnects. But others rather referred to <110> texture. In our study, the grain boundaries conditions varied by Cu ECP were found to impact electromigration behavior. We here like to examine the impact of Cu grain orientations on electromigration as well. EBSD analysis would be employed in this further study.

7.2.2 Cu surface treatment effects on stress migration

The Cu/dielectric-cap interface and the Cu/cap/liner edges play a significant role in both in Electromigration and stress migration reliability. Previous research work also achieve some encouraging preliminary results on effect of the geometry structure [223], temperature and dielectric component effect on stress migration reliability [240, 241] (not included in this thesis). These issues would be pursued further and an in-depth study will be carried out.

Surface treatment has also been identified to be a key factor that governs

electromigration lifetimes. Furthermore, for stress migration study, at least one report in the literature was found to indicate an improvement in stress migration performance with better adhesion between Cu and dielectric cap layer [242]. The conditions of Cu/dielectric-cap interface and Cu/cap/liner edges are expected to affect SM significantly since SM is considered to have a significant contribution from bulk diffusivity. However the effect of Cu interface conditions on stress migration is not fully understood. The future study therefore would investigate the effect of composition, barrier layer, and surface modification on stress migration reliability.

7.2.3 Interaction between stress migration and electromigration

A few literatures that have studied Al interconnects report that the presence of stress induced voids prior to EM studies, reduce the EM lifetimes by reducing the Black's current exponent *n*. The exponent in pure EM studies is determined to be 1 to 2 [243]; whereas in the presence of voids prior to EM, the exponent is determined to be nearly 1 [244]. On the other hand, after an initial electromigration stress, the residual stress in Cu interconnect may accelerate stress migration voids growth during the successively stress migration test. Unfortunately, there are very few published papers on Cu stress migration and even fewer published papers on Cu stress migration combined with electromigration [244-246].

In real ICs, the operating temperatures (<125 ^{o}C) and current densities (<10^3 A/cm^2) the residual stress driven stress migration is present at these operating conditions. Therefore, study the combined effects of stress and electromigration is urgently needed. Thus, the future study will focus on this combined effect and will also address development of comprehensive reliability models that would account for both of these

effects.

7.2.4 Monte Carlo Simulation

The Monte-Carlo based model implemented in this research work can be further improved by developing rigorous model based on similar concepts, considering other important parameters such as microstructure, current density distribution, stress and temperature gradients, and introducing diffusivities for different atomic transport paths. Finite-element methods can be introduced in the Monte-Carlo loop to determine important parameters such as distribution of current density, stress and temperature. Kinetic Monte-Carlo methods can be employed to keep track of time during simulations. Such approaches will provide quantitative information and further in-depth understating of electromigration-induced voiding in damascene Cu interconnect structures. This rigorous model can also be particularly important to simulate void evolution during the last stage of electromigration-induced void evolution when the voids agglomerate at the cathode via region eventually leading to failure. By introducing strain energy parameter during atomic jump simulation in a Monte Carlo loop, stress-induced voiding can be simulated using the same model. Moreover, combined effect of stress-induced and electromigration-induced voiding can be studied. Another important electromigration mechanism that can be studied with this model is the short length effect. This effect is understood based increase in back-stress effect with reduction in length of the interconnect line which balances the electromigration wind force. Investigations can be pursued using the Monte-Carlo simulations to determine whether this effect is possibly due to reduction of available initial vacancy cluster volume in a short length interconnect line.

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Publications in progress:

11. Effect of Electromigration on the Surface Roughness Change in Cu interconnect.
12. Effect of Cu electrochemical related Microstructure and Interface Conditions on Electromigration Performance in Cu interconnect.

Appendix I:

Monte Carlo Simulation Tool Code Developed in MatLab

```
%using muldimentional arrays -1 is atom/void 2 is Ep(bond) and 3 is Ee (EM)
%dimension is the row and column dimension
rdimension=15
cdimension=150
%intializing array 1 to 1 at each location ie atom, if 0 means void

%ADDING VACANCY
vac_per=0.1
for r=1:1:rdimension
      for c=1:1:cdimension
            vac=rand(1,1)
               if vac < vac_per
                     intial_structure(r,c,1)=0
               else
                     intial_structure(r,c,1)=1
               end
     end
end

I = intial_structure (:,:,1)
image(I,'CDataMapping','scaled')
colormap(gray);
axis image

%axis([0 10 0 30])
pause(2);


%FUNCTION FOR VOID ASSIGNMENT
% assigning 0 to void locations

%void 1
for c=23:1:26
      for r=4:1:6
            intial_structure(r,c,1)=0
      end
end

%void 2
for c=73:1:77
      for r=3:1:5
```

```
            intial_structure(r,c,1)=0
        end
end

%void 3
for c=122:1:126
        for r=5:1:7
            intial_structure(r,c,1)=0
        end
end

%void 4
for c=128:1:132
        for r=3:1:4
            intial_structure(r,c,1)=0
        end
end

%void 5
for c=6:1:8
        for r=10:1:12
            intial_structure(r,c,1)=0
        end
end

%void 6
for c=46:1:53
        for r=9:1:11
            intial_structure(r,c,1)=0
        end
end

%void 7
for c=55:1:58
        for r=11:1:13
            intial_structure(r,c,1)=0
        end
end

%void 8
for c=96:1:100
        for r=8:1:12
            intial_structure(r,c,1)=0
        end
end

I = intial_structure (:,:,1)
image(I,'CDataMapping','scaled')
```

```
axis image
%axis([0 10 0 30])
pause(20);
%VOID ASSIGNMENT COMPLETED


%FUNCTION FOR EE ASSIGNMENT
%ee assignment in plane2
%ee_constant is for Fee=ee_constant*J
%J_normal is current density
ee_constant= 50
J_normal=1
ee_normal=ee_constant*J_normal

for r=1:1:rdimension
      for c=1:1:cdimension

     %adding a gradient here

     intial_structure(r,c,2)=ee_normal+0.5*ee_normal*(c/cdimension)

     end
end

I2 = intial_structure (:,:,2)
image(I2,'CDataMapping','scaled')
axis image

%axis([0 10 0 30])
pause(32);
% EE ASSIGNMENT COMPLETED


%FUNCTION FOR PP ASSIGNMENT
%pp assignment in plane3
%calculating No. of neighbours at each location-limited locations

%first defining seperately for row 1 and row rdimension only

temp_neigh_r=1
for temp_neigh_c=2:1:cdimension-1

     neigh_count(temp_neigh_r,temp_neigh_c)=(intial_structure(temp_neigh_r,temp_neig
     h_c-1,1) ...
          +intial_structure(temp_neigh_r,temp_neigh_c+1,1)...
          +intial_structure(temp_neigh_r+1,temp_neigh_c-1,1) ...
          +intial_structure(temp_neigh_r+1,temp_neigh_c,1) ...
          +intial_structure(temp_neigh_r+1,temp_neigh_c+1,1))*0.8
```

```
end

temp_neigh_r=rdimension
for temp_neigh_c=2:1:cdimension-1

    neigh_count(temp_neigh_r,temp_neigh_c)=(intial_structure(temp_neigh_r,temp_neig
    h_c-1,1) ...
        +intial_structure(temp_neigh_r-1,temp_neigh_c-1,1)...
        +intial_structure(temp_neigh_r-1,temp_neigh_c,1) ...
        +intial_structure(temp_neigh_r-1,temp_neigh_c+1,1) ...
        +intial_structure(temp_neigh_r,temp_neigh_c+1,1))*0.8
end

%now defining upper Cu/SiNx/Ta edge region

for temp_neigh_c=2:1:cdimension-1
    for temp_neigh_r=2:1:(rdimension+1)/2

        %adding upper interface diffusion area here using interface parameter
        interface_pmt=temp_neigh_r/10+0.3

        if interface_pmt>=1.0
            interface_pmt=1.0
        else
        end


    neigh_count(temp_neigh_r,temp_neigh_c)=(intial_structure(temp_neigh_r-1,temp_n
    eigh_c-1,1)...
        +intial_structure(temp_neigh_r-1,temp_neigh_c,1) ...
        +intial_structure(temp_neigh_r-1,temp_neigh_c+1,1)...
        +intial_structure(temp_neigh_r,temp_neigh_c-1,1) ...
        +intial_structure(temp_neigh_r,temp_neigh_c+1,1)...
        +intial_structure(temp_neigh_r+1,temp_neigh_c-1,1) ...
        +intial_structure(temp_neigh_r+1,temp_neigh_c,1) ...
        +intial_structure(temp_neigh_r+1,temp_neigh_c+1,1))*interface_pmt
    end
end

%now defining lower Cu/SiNx/Ta edge region

for temp_neigh_c=2:1:cdimension-1
    for temp_neigh_r=((rdimension+1)/2+1):1:rdimension-1

        %adding lower interface diffusion area here using interface parameter
        interface_pmt=2-temp_neigh_r/10

        if interface_pmt>=1.0
```

```
            interface_pmt=1.0
        else
        end


    neigh_count(temp_neigh_r,temp_neigh_c)=(intial_structure(temp_neigh_r-1,temp_n
    eigh_c-1,1)...
        +intial_structure(temp_neigh_r-1,temp_neigh_c,1) ...
        +intial_structure(temp_neigh_r-1,temp_neigh_c+1,1)...
        +intial_structure(temp_neigh_r,temp_neigh_c-1,1) ...
        +intial_structure(temp_neigh_r,temp_neigh_c+1,1)...
        +intial_structure(temp_neigh_r+1,temp_neigh_c-1,1) ...
        +intial_structure(temp_neigh_r+1,temp_neigh_c,1) ...
        +intial_structure(temp_neigh_r+1,temp_neigh_c+1,1))*interface_pmt
    end
end

%for column 1 and column cdimension to make fixed boundary condition

temp_neigh_c=1
for temp_neigh_r=2:1:rdimension
    neigh_count(temp_neigh_r,temp_neigh_c)=8
end

temp_neigh_c=cdimension
for temp_neigh_r=2:1:rdimension
    neigh_count(temp_neigh_r,temp_neigh_c)=8
end

%for grain boundary

gb_c1=39
gb_c2=98

temp_neigh_c=gb_c1
for temp_neigh_r=1:1:rdimension

neigh_count(temp_neigh_r,temp_neigh_c)=neigh_count(temp_neigh_r,temp_neigh_c)*0.8
end

temp_neigh_c=gb_c2
for temp_neigh_r=1:1:rdimension

neigh_count(temp_neigh_r,temp_neigh_c)=neigh_count(temp_neigh_r,temp_neigh_c)*0.8
end

intial_structure(:,:,3)= neigh_count (:,:)
image(intial_structure(:,:,3),'CDataMapping','scaled')
```

```
axis image

%axis([0 10 0 30])
pause(20);
%EEASSIGNMENT COMPLETED


%DIFINDING Ep AND Ee
%bond_pair_potential

%NOTE use higher to make bond energy dominanant
bond_pair_pt=2000
Ep(:,:)=bond_pair_pt*intial_structure(:,:,3)

%EM_constant_Zep
EM_const=2
Ee(:,:)=EM_const*intial_structure (:,:,2)

%for capturing void evolution in a video
aviobj = avifile('CuSuface_CV_GB.avi','fps',5);


%MONTE CARLO LOOP

for mcloop=1:1:100000000000
%selection of random location
[sizer,sizec]=size(Ep)
%random selection of element in matrix Ep
temp_rand_r=rand(1,1)*sizer
temp_rand_c=rand(1,1)*sizec

%note that random number is normalized to select element ONLY from Ep
for rand_r=1:1:sizer
      if (rand_r-1)<=temp_rand_r & temp_rand_r<=rand_r
            rnd_r=rand_r
      else
      end
end

for rand_c=1:1:sizec
      if (rand_c-1)<=temp_rand_c & temp_rand_c<=rand_c
               rnd_c=rand_c
      else
      end
end
%selection of random location completed --rnd_r, rnd_c

%checking whether it is a bulk or void location
```

```
%if yes reject and EXIT COMPLETELY from mc loop
if~(neigh_count(rnd_r,rnd_c)==8|intial_structure(rnd_r,rnd_c,1)==0|(rnd_r==1&neigh_co
unt(rnd_r,rnd_c)==5)|rnd_r==rdimension&neigh_count(rnd_r,rnd_c)==5|rnd_c==1|rnd_c
==cdimension)

    %selecting a neighbouring void location
    if 2<=rnd_r&rnd_r<=rdimension-1
        temp_rand_r2=rand(1,1)*8
        for rand_r2=1:1:8
            if (rand_r2-1)<=temp_rand_r2 & temp_rand_r2<=rand_r2
                rnd_ex=rand_r2
            else
            end
        end

        if rnd_ex==1
        ex_r=rnd_r
        ex_c=rnd_c-1

        elseif rnd_ex==2
        ex_r=rnd_r+1
        ex_c=rnd_c-1

        elseif rnd_ex==3
        ex_r=rnd_r-1
        ex_c=rnd_c-1

        elseif rnd_ex==4
        ex_r=rnd_r+1
        ex_c=rnd_c

        elseif rnd_ex==5
        ex_r=rnd_r-1
        ex_c=rnd_c

        elseif rnd_ex==6
        ex_r=rnd_r
        ex_c=rnd_c+1

        elseif rnd_ex==7
        ex_r=rnd_r+1
        ex_c=rnd_c+1

        elseif rnd_ex==8
        ex_r=rnd_r-1
        ex_c=rnd_c+1

        else
```

```
        end

    elseif rnd_r==1
        temp_rand_r1=rand(1,1)*5

        for rand_r1=1:1:5
            if (rand_r1-1)<=temp_rand_r1&temp_rand_r1<=rand_r1
                rnd_ex=rand_r1
            else
            end
        end


        if rnd_ex==1
        ex_r=rnd_r
        ex_c=rnd_c-1

        elseif rnd_ex==2
        ex_r=rnd_r+1
        ex_c=rnd_c-1

        elseif rnd_ex==3
        ex_r=rnd_r+1
        ex_c=rnd_c

        elseif rnd_ex==4
        ex_r=rnd_r
        ex_c=rnd_c+1

        elseif rnd_ex==5
        ex_r=rnd_r+1
        ex_c=rnd_c+1

        else
        end

    elseif rnd_r==rdimension
        temp_rand_r2=rand(1,1)*5

        for rand_r2=1:1:5
            if (rand_r2-1)<=temp_rand_r2&temp_rand_r2<=rand_r2
                rnd_ex=rand_r2
            else
            end
        end


        if rnd_ex==1
```

```
        ex_r=rnd_r
        ex_c=rnd_c-1

        elseif rnd_ex==2
        ex_r=rnd_r-1
        ex_c=rnd_c-1

        elseif rnd_ex==3
        ex_r=rnd_r-1
        ex_c=rnd_c

        elseif rnd_ex==4
        ex_r=rnd_r-1
        ex_c=rnd_c+1

        elseif rnd_ex==5
        ex_r=rnd_r
        ex_c=rnd_c+1

        else
        end
    end

temp_state1=intial_structure(rnd_r,rnd_c,1)
temp_state2=intial_structure(ex_r,ex_c,1)

%checking change in system energy
%deltaE=E(rnd_r,rnd_c)-E(ex_r,ex_c)
deltaE=(Ep(rnd_r,rnd_c)-Ee(rnd_r,rnd_c))-(Ep(ex_r,ex_c)-Ee(ex_r,ex_c))

if deltaE<0&temp_state2==0&~(intial_structure(ex_r,ex_c,3)==1)

intial_structure(rnd_r,rnd_c,1)=temp_state2
intial_structure(ex_r,ex_c,1)=temp_state1

%Revaluate Ep
%calculating no. of neighbours at each location-limited locations
%Box defines this box for    calculating no. of neighbours
Box=4
%using ONLY box recal
for temp_neigh_r=(ex_r-Box):1:(ex_r+Box)

for temp_neigh_c=(ex_c-Box):1:(ex_c+Box)

    if 2<=temp_neigh_r&temp_neigh_r<=(rdimension+1)/2
        interface_pmt=temp_neigh_r/10+0.3
    elseif ((rdimension+1)/2+1)<=temp_neigh_r&temp_neigh_r<=rdimension-1
        interface_pmt=2.0-temp_neigh_r/10
```

```
else
end

%first defining seperately for row 1 only
if temp_neigh_r==1&2<=temp_neigh_c&temp_neigh_c<=cdimension-1

    neigh_count(temp_neigh_r,temp_neigh_c)=(intial_structure(temp_neigh_r,temp_
    neigh_c-1,1) ...
        +intial_structure(temp_neigh_r,temp_neigh_c+1,1)...
        +intial_structure(temp_neigh_r+1,temp_neigh_c-1,1) ...
        +intial_structure(temp_neigh_r+1,temp_neigh_c,1) ...
        +intial_structure(temp_neigh_r+1,temp_neigh_c+1,1))*0.8

%difining row rdimension secondly
elseif
temp_neigh_r==rdimension&2<=temp_neigh_c&temp_neigh_c<=cdimension-1

    neigh_count(temp_neigh_r,temp_neigh_c)=(intial_structure(temp_neigh_r,temp_
    neigh_c-1,1) ...
        +intial_structure(temp_neigh_r-1,temp_neigh_c-1,1)...
        +intial_structure(temp_neigh_r-1,temp_neigh_c,1) ...
        +intial_structure(temp_neigh_r-1,temp_neigh_c+1,1) ...
        +intial_structure(temp_neigh_r,temp_neigh_c+1,1))*0.8

%Now for interface diffusion eare
elseif
2<=temp_neigh_r&temp_neigh_r<=rdimension-1&interface_pmt<=1.0&2<=temp_n
eigh_c&temp_neigh_c<=cdimension-1

    neigh_count(temp_neigh_r,temp_neigh_c)=(intial_structure(temp_neigh_r-1,tem
    p_neigh_c-1,1)...
        +intial_structure(temp_neigh_r-1,temp_neigh_c,1) ...
        +intial_structure(temp_neigh_r-1,temp_neigh_c+1,1)...
        +intial_structure(temp_neigh_r,temp_neigh_c-1,1) ...
        +intial_structure(temp_neigh_r,temp_neigh_c+1,1)...
        +intial_structure(temp_neigh_r+1,temp_neigh_c-1,1) ...
        +intial_structure(temp_neigh_r+1,temp_neigh_c,1) ...
        +intial_structure(temp_neigh_r+1,temp_neigh_c+1,1))*interface_pmt

%Now for central eare
elseif
2<=temp_neigh_r&temp_neigh_r<=rdimension-1&interface_pmt>1.0&2<=temp_nei
gh_c&temp_neigh_c<=cdimension-1

    neigh_count(temp_neigh_r,temp_neigh_c)=intial_structure(temp_neigh_r-1,temp
    _neigh_c-1,1)...
        +intial_structure(temp_neigh_r-1,temp_neigh_c,1) ...
        +intial_structure(temp_neigh_r-1,temp_neigh_c+1,1)...
```

```
                +intial_structure(temp_neigh_r,temp_neigh_c-1,1) ...
                +intial_structure(temp_neigh_r,temp_neigh_c+1,1)...
                +intial_structure(temp_neigh_r+1,temp_neigh_c-1,1) ...
                +intial_structure(temp_neigh_r+1,temp_neigh_c,1) ...
                +intial_structure(temp_neigh_r+1,temp_neigh_c+1,1)
        else
        end

end
end

%for column 1 and cdimension
temp_neigh_c=1
for temp_neigh_r=2:1:rdimension
        neigh_count(temp_neigh_r,temp_neigh_c)=8
end

temp_neigh_c=cdimension
for temp_neigh_r=2:1:rdimension
        neigh_count(temp_neigh_r,temp_neigh_c)=8
end

%for grain boudary
temp_neigh_c=gb_c1
for temp_neigh_r=1:1:rdimension

neigh_count(temp_neigh_r,temp_neigh_c)=neigh_count(temp_neigh_r,temp_neigh_c)*0.8
end

temp_neigh_c=gb_c2
for temp_neigh_r=1:1:rdimension

neigh_count(temp_neigh_r,temp_neigh_c)=neigh_count(temp_neigh_r,temp_neigh_c)*0.8
end

%intial_structure(:,:,3)= neigh_count (:,:)
%defining Ep and Ee
%bond_pair_potential
bond_pair_pt=2000
Ep(:,:)=bond_pair_pt*neigh_count (:,:)

image(intial_structure(:,:,1),'CDataMapping','scaled')
axis image

pause(0.5);

frame = getframe;
aviobj = addframe(aviobj,frame);
```

```
else
end

else
end
end
```