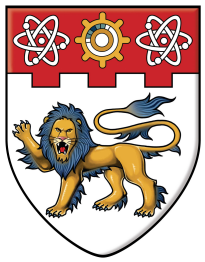
Dielectric/Metal Diffusion Barrier

In

Cu/Porous Ultra Low-*k* Interconnect Technology



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Statement of Originality

I hereby certify that the work embodied in this thesis is result of original research and has not been submitted for a higher degree to any other University or Institution.

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Summary

As Cu damascene process and low dielectric constant material (low-*k*) are introduced into back-end of line (BEOL) semiconductor manufacturing, a robust barrier system is highly essential for integrated circuit (IC) performance and reliability improvements. In this work, the application of dielectric diffusion barriers was explored using a novel dielectric/metal bilayer sidewall barrier structure. Our work demonstrates this bilayer barrier structure could efficiently enhance the sidewall barrier integrity. As a result, the electrical and reliability performance of Cu/porous ultra low-k interconnects, in terms of resistance-capacitance (*RC*) delay characteristics, leakage current, electrical breakdown strength (E_{BD}), thermal stability and electromigration resistance, were significantly improved by using the bilayer barrier approach. Detail studies indicate that an optimized bilayer barrier structure could be achieved by increasing the proportion of the dielectric barrier and correspondingly reducing the thickness of the metal barrier.

Meanwhile, a pseudo-breakdown mechanism was observed in Cu/porous ultra low-*k* damascene interconnects. The physics and kinetics behind this pseudo-breakdown behavior was investigated and related to the Cu penetration through the sidewall barrier. Our studies show that, by using an optimized dielectric/metal bilayer barrier structure, this undesirable interconnects failure due to porosity induced poor sidewall barrier degradation could be avoided.

Furthermore, our studies in Cu back end of line (BEOL) process and barrier integrity revealed that the Oxygen species, *e.g.* Oxygen content in low-*k* dielectrics

as well as Oxygen and/or moisture intake from ambient, have a negative influence on the long-term electrical and reliability performance of interconnects. This unstable Oxygen content may be released from low-*k* dielectrics during thermal cycling and deteriorates the interfacial condition between the sidewall barrier and low-*k* inter-metal dielectrics (IMD), which leads to an oxidation-induced (fast) Cu diffusion. Inserting a thin Al interlayer between the metal and the dielectric sidewall barrier is a practical way not only to stuff the grain boundary diffusion paths of Cu in polycrystalline Ta barrier, but also prevent its oxidation by forming a density Al_2O_3 sacrificial layer. Our results show this composite sidewall barrier has a better electrical and thermal stability for Cu/porous ultra low-*k* interconnects than simple dielectric/metal bilayer barrier structure. As another novel approach, in-line electron beam (E-beam) treatment was employed to modify the chemical bonds and release the Oxygen content at the sidewall surface of low-*k* IMD, which is found to be efficient to overcome the Oxygen-related reliability issue and has the advantages of process compatibility.

Table of Contents

List of Tables

List of Figures

List of Symbols

C	Concentration
C_m	Solid solubility
C_{OX}	Oxide capacitance
D	Diffusion coefficient (cm^2/s)
D_{drift}	Cu drift rate in dielectric materials
E	Electric field (MV/cm)
E_a	Activation energy (eV)
E_{bd}	Dielectric breakdown strength (MV/cm)
J	Mass flux density
J_E	Current density (A/cm^2)
k, ε_r	Dielectric constant
k_B	Boltzmann constant
Q_m	Mobile charge
q	Electronic charge
T	Absolute Temperature (K)
V_{FB}	Flat band voltage
ε_0	Permittivity of Vacuum
μ	Mobility ($cm^2/V \cdot s$)
Φ_B	Barrier height (eV)

List of Abbreviations

AES	Auger electron spectroscopy
AFM	Atomic force microscopy
ALD	Atomic layer deposition
ASTM	American society for testing and materials
BEOL	Back-end of line
BMF	Barrier-metal free
BPSG	Boron-phosphorus doped silicon glass
BTS	Bias temperature stress
CTE	Coefficient of thermal expansion
CVD	Chemical vapor deposition
CMP	Chemical-mechanical polishing
DDI	Dual damascene interconnect
DRAM	Dynamic random access memory
E-Beam	Electron-beam
ECP	Electrochemical plating
EDX	Energy disperse X-ray spectra
EM	Electromigration
ESL	Etch stop layer
EELS	Electron energy loss spectroscopy
FESEM	Field enhanced scan electron microscopy
FSG	Fluorinated silicate glass
FTIR	Fourier transform infrared spectroscopy

HCP	Hollow cathode plasma
HDP	High density plasma
HM	Hard mask
HSQ	Hydrogen silsesquioxane
IC	Integrated circuits
ILD	Inter-layer dielectric
IMD	Inter-metal dielectric
IMP	Ionized metal plasma
ITRS	International Technology Roadmap for Semiconductors
MOCVD	Metal organic chemical vapor deposition
MOS	Metal-oxide-silicon
MSQ	Methyl-silsesquioxane
MTF	Mean time to failure
NTRS	National Technology Roadmap of Semiconductor
PECVD	Plasma enhanced chemical vapor deposition
PVD	Physical vapor deposition
RBS	Rutherford back scattering
RC	Resistance-capacitance
RMS	Root mean square
RIE	Reactive ion etching
SEM	Secondary electron microscopy
SIMS	Secondary ion mass spectroscopy
SIP	Self-ionized plasma
SOD	Spin-on dielectric
TDDB	Time-depended dielectric breakdown

TEM	Transmission electron microscopy
ULSI	Ultra-large scale integrated circuit
USG	Undoped silicate glass
XPS	X-ray photoelectron spectroscopy
XRD	X-ray Diffraction

Chapter 1. Introduction

1.1 Multi-level Interconnects for ULSI

The semiconductor industry always attempts to develop more powerful integrated circuits (ICs). This approach basically advances in two directions [1]. One is to increase the speed of individual transistors through a continual reduction in the minimum size of device features. The other one entails developing increasingly complex interconnect systems, which now use multi-layer structures of metal wiring separated by interlayer dielectrics (ILD). This enables the higher-speed devices to be interconnected and results in ICs with enhanced performance and system functionality.

The tradeoffs between these two effects depend on the details of the circuit architecture [2]. During the early stages of IC industry (from the mid-1970s to about 1990), circuit design rules were still in large dimensions (1 ~ 5 μm). And interconnect delays could generally be ignored because they were typically much smaller than the device switching times (~ 20 ns). However, by the mid-1990s, microprocessors and other ultra large scale integrated (ULSI) devices with millions of circuit elements and speeds greater than 1 GHz were envisioned. Chip designers and manufacturing engineers began to realize that interconnect delays would become comparable to, and could eventually exceed, the intrinsic delays of transistors. Signal propagation delay, crosstalk noise and power dissipation in interconnects are increasingly becoming limiting factors in overall circuit performance. As shown in Figure 1.1, when the device dimensions are scaled to sub-micrometer (0.25 μm) range, the benefits of decreased transistor gate length

are offset by the increased resistance-capacitance (*RC*) delays of interconnects. Thus, the interconnect performance and back-end of line (BEOL) process becomes the bottle-neck for improvement in IC performance.

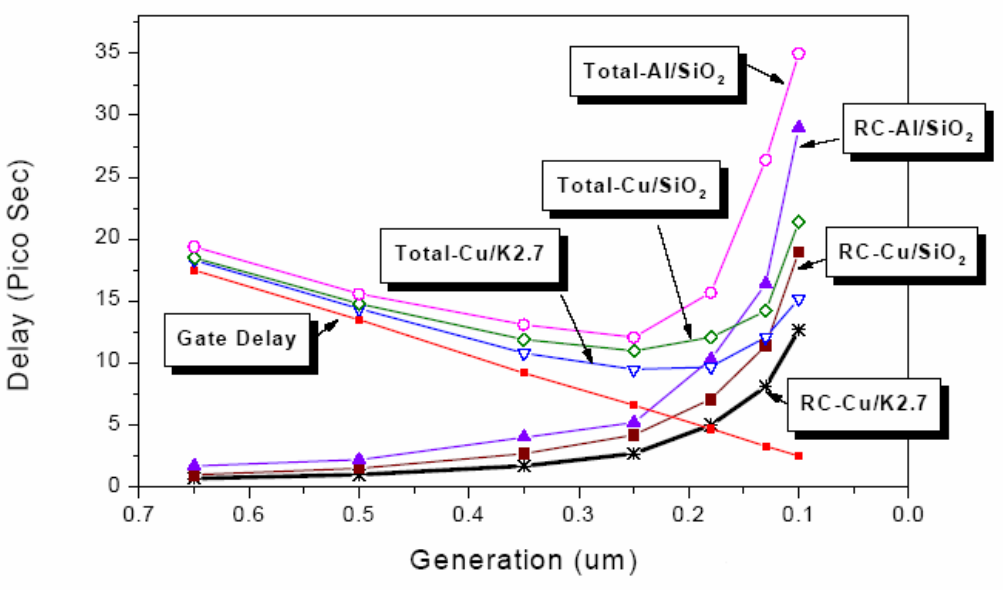

Figure 1.1 Signal propagation delay due to interconnects and transistor gate.

(Source: IBM)

1.2 Major Concerns of Interconnects

1.2.1 *RC* Delay

To estimate the effects of total resistance of metal and capacitance associated with the dielectric, one can approximate the *RC* delay time constant by simply multiplying the interconnect wire resistance with the capacitance of a simple parallel plate, leading to following expression [3]

$$RC = \frac{\rho}{T_M}\frac{L^2 \varepsilon_{IMD}}{T_{IMD}} \tag{1.1}$$

where ρ, T_M and L are the resistivity, the thickness and the total length of the interconnect line, respectively: ε_{IMD} and T_{IMD} are the permittivity and 1/2 pitch or line spacing of inter-metal dielectric (IMD), respectively. Note that $\varepsilon_{IMD} = k\varepsilon_0$, where k is the dielectric constant of the material between interconnect lines and ε_0 is the permittivity of vacuum.

As semiconductor manufacturing technology is continuously advanced, and keeping the famous Moore's Law (i.e. transistors per chip doubling every 18 months) in mind, the chip geometry is driven to shrink down. The conventional approaches force the line pitch T_{IMD} and the inter-layer thickness T_M to decrease for each technology generation. Also, increasing system complexity and die sizes are driving up total interconnect length L as well. Table 1.1 shows the near-term interconnect dimension requirement by the International Technology Roadmap for Semiconductors (ITRS). As a result, the signal delay will become considerably serious as technology node shrinks in the future.

Table 1.1 Requirement for local wiring pitch and total interconnect length (Source: *ITRS*, 2004 Edition [4])

Year of Product	Metal 1 wiring pitch (nm)	Total interconnect length (m/cm^2)
2003	240	579
2004	214	688
2005	190	907
2006	170	1002
2007	152	1117
2008	134	1401
2009	120	1559

It should be noted that the resistivity of interconnect metal is not constant and independent of the decreasing feature size in actual conditions. For the interconnect wire thickness or width near the mean-free path of the electron in the given film, the resistivity starts to rapidly increase with decreasing wire thickness/width [3]. Therefore, as the interconnect dimensions shrink beyond some critical value, the RC delay issue would be exacerbated unless the conductor is replaced by an entirely new material.

1.2.2 Power Dissipation

Power dissipation is another major concern for interconnects besides signal delay. Ever increasing frequencies and higher densities lead to a dramatic increase in power dissipation. There are two elements contributing to the power dissipation [5]. One is the dynamic power given by

$$P = \alpha C f V^2 \tag{1.2}$$

where P is the power dissipation, α is the wire activity (i.e. when the wire is transferring a signal), f is the operational frequency, V is the power supply voltage, and C is the effective capacitance which is represented by

$$C = C_{output} + C_{input} + C_{wire} \tag{1.3}$$

It describes the output and input capacitances of the transistors as well as the capacitance introduced by the wire. It is clear that a higher operational frequency leads to a higher power dissipation whenever a signal is propagated in the interconnect wires. Although decreasing the supply voltage is helpful to alleviate this problem, the budget is limited by other important circuit parameters (i.e. transistor input and output voltage, threshold voltage, *etc*.). The other factor important to power dissipation is the static power consumption, which is proportional to the leakage current and interconnects wire resistance ($\propto I^2 R$). Thus the overall power dissipation is still largely driven by the properties of materials used in and between the interconnect wires.

1.2.3 Electromigration

Electromigration is an atomic scale phenomena in which the electrons that constitute electric-current collide with the metal atoms of interconnect lines and push them in the direction of the current flow [6]. If this "electron wind" is strong enough, a significant migration of the metal atoms will occur. Over time this transport of material can lead to the electrical failure of interconnect lines by depleting the metal atoms in the line and causing an open-circuit, or by the formation of short-circuit to an adjacent line due to local accumulation of metal. The strength of the electron wind increases as the current density is increased. The upper-limit of current density to prevent electromigration in conventional Al (alloyed with 5% Cu) interconnects is 5×10^5 A/cm^2 for 20-year lifetime. This limit puts restrictions on circuit design and IC performance. Scaling of interconnect wires to increase functional density and IC performance inevitably leads to rise of operational current densities, make conventional Al interconnects less attractive for future technology [7].

1.3 Concept of Cu/Low-*k* Dual Damascene Interconnects

1.3.1 Demand for New Materials

In the simplest possible way, the signal propagation and power dissipation performance can be improved by modifying some "constant" parameters in the above mathematical expressions [for example, Equation (1.1)]: the interconnect resistance (R) can be decreased by using a lower resistivity metal as the conductor and isolating the conductor by a low dielectric constant (k) material could lower the interconnect capacitance (C). The interconnect chapter of the 1994 U.S.

National Technology Roadmap for Semiconductors (NTRS) described the first need for new conductor and dielectric materials that would be necessary to meet the projected overall technology requirement and reduce *RC* delay [8]. At that time, the conventional interconnect networks in the ICs consisted of Aluminum (Al) wiring which is isolated by silicon dioxide (SiO_2), silicon nitride (SiN) and boron-phosphorus doped silicon glass (BPSG).

For metallic conductors with electrical resistivity lower than Al (ρ =2.7 μΩ•cm), the candidates were limited to Silver (Ag), Copper (Cu) and Gold (Au). And the only practical choice for interconnect metal is Cu. Costs and manufacturability as well as silicon device reliability strongly favor the use of Cu. The additional gain of improved resistivity in going from Cu (ρ =1.7 μΩ•cm) to either Ag (ρ =1.6 μΩ•cm) or Au (ρ =2.2 μΩ•cm) would be quite minimal [9] this link is pointing to [9]. In addition, Cu is a more noble metal than Al, which means it has a higher melting point (1357 K) than Al (933 K). This gives Cu the advantage over Al in electromigration and possibly stresses migration as well. The typical ULSI application temperature range (~ 473 K) is about 51 % of Al melting point and 35% of Cu melting point [10]. This suggests that mass transport (atomic self-diffusion or vacancy diffusion) in Cu wires is generally slower than that in Al wires at high temperature and given current density.

1.3.2 Cu Dual Damascene Process

The subsequent implementation of using materials with lower dielectric constant (low-*k*) than SiO_2 (k ~ 4.2) as the intra- and inter-layer dielectrics for ULSI interconnects was widely expected, but was not successfully achieved until

recent years [11]. Many low-*k* candidates developed by different companies were attempting to take the place of SiO_2, including fluorinated silicon glass (FSG, k ~ 3.9), carbide doped silicon oxide (SiCOH, k ~ 2.7 - 3.0), organic/inorganic polymer dielectrics (k ~ 2.6) and even porous ultra low-*k* dielectrics (k ~ 2.0 - 2.4). However, these candidates must satisfy a large number of difficulties and diverse requirements in order to be successfully integrated into Cu metallization schedule. The requirements include high thermal and mechanical stability, good adhesion to other interconnect materials, resistance to processing chemicals, low moisture absorption, low cost, *etc.* [12]. These requirements present significant challenges to commercially implement Cu/low-*k* interconnect structures into IC fabrication process.

The commonly encountered problems with Cu are the difficulty to pattern Cu line by conventional reactive ion etching (RIE), self-evaluation of polycrystalline Copper [13], fast diffusion of Cu atoms and ions into dielectric and silicon even at room temperature, and subsequently serious contamination effects on the device performance [14]. In the 1990's, the Dual Damascene Interconnection (DDI) architecture was invented and resolved most of these problems.

Figure 1.2 illustrates the process flow of Cu dual damascene interconnects. Firstly, the inter-metal dielectric (IMD) with etch stop layer (ESL) is deposited and patterned to form a template for the metal line. An adhesion promoter/diffusion barrier is deposited by physical vapor deposition (PVD) before Cu filling to provide good adhesion between Cu and dielectric and also to prevent Cu diffusion into dielectrics. Cu is inlaid into the trench and via structures initially by depositing a thin Cu seed layer and then filling up by electrochemical plating (ECP). The extra Cu on the top will be removed by chemical-mechanical polishing

(CMP). Finally, a dielectric capping layer/diffusion barrier is coated on the Cu line for passivation and avoiding Cu diffusion into upper IMD layer. With this dual damascene architecture, people could begin the steps for the Cu metallization process in ICs.

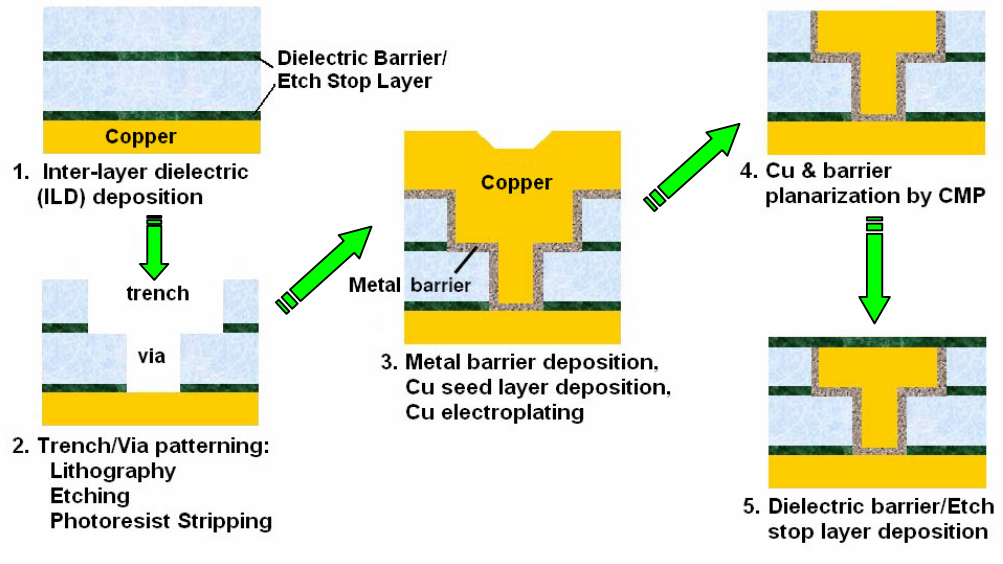

Figure 1.2 Process flow of Cu dual damascene interconnects.

1.4 Motivation for Research on Cu Diffusion Barrier

The most critical issue that must be resolved before Cu metallization can be actually realized in industrially manufacturing is "***How to effectively prevent Cu diffusion into the dielectric***?" It is well known that Cu atoms and ions can rapidly diffuse through silicon and many low-*k* dielectrics, even at low temperature range (< 400°C) [15]. And the presence of Cu forms deep level impurities in silicon device, leading to undesirable degradation of carriers lifetime, or deterioration of the insulating properties of interconnect dielectrics [16].

In the Cu damascene process, two different kinds of diffusion barriers are needed to enclose Cu line completely, as shown in Figure 1.3. One is a dielectric barrier, which is also used as a capping layer/etch stop layer and provides the insulation between the Cu lines in the same level. Silicon nitride (SiN) or silicon carbide (SiCN, SiCO and SiC) films, deposited by plasma enhanced chemical vapor deposition (PECVD) method, are usually used as dielectric barriers in back end of line (BEOL) process to prevent moisture intake and metal atom/ion diffusion [17], [18]. The other one is the conductive barrier, which is used on the sidewall and via/trench bottom to provide a good contact between the top and bottom Cu lines. This conductive barrier also acts as an adhesion promoter between Cu and surrounding dielectrics [19]. People have investigated several transition metals such as Ta, Ti and W and their compounds with N, C or Si as possible conductive diffusion barrier/adhesion promoter [19] - [21]. Ta or TaN layers deposited by Physical Vapor Deposition (PVD) were developed and are the most commonly used sidewall diffusion barriers in current Cu dual damascene process. They offer high reliability even at high temperatures and good adhesion to both Cu and most low-*k* materials [22], [23].

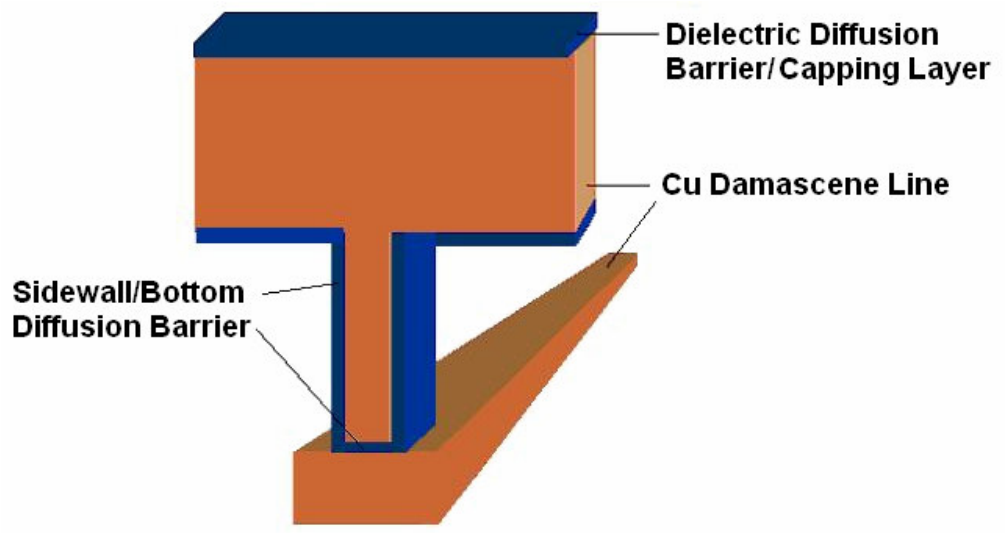

Figure 1.3 Conductive and dielectric barriers for Cu diffusion in Dual Damascene Interconnects.

However, these conventional diffusion barriers have some drawbacks as IC manufacturing technology shifts beyond 90 nm node, which requires Cu metallization processes to go ahead from Cu/SiO_2 to Cu/low-*k* and even Cu/ultra low-*k* metallization processes. They are:

1. It is challenging to deposit sidewall diffusion barriers with good uniformity and quality by traditional PVD method [24] in more and more narrow damascene structures as the interconnect line width continuously scales down. The new enhancements such as ionized metal plasma (IMP), self ionized plasma (SIP) and hollow cathode plasma (HCP) technologies extend the utility and efficiency of PVD tools very well, but is still hard to meet the requirements of the ITRS roadmap for future Cu/low-*k* and Cu/ultra low-*k* integration schedule [4]. In recent years, developing atomic layer deposition (ALD) and metal organic chemical vapor deposition (MOCVD) systems have become more promising for future generation metal barrier deposition

techniques due to the good uniformity and sidewall coverage they could achieve technically [25] [26]. However, the low deposition rate and the high cost of precursors limit their application to completely replace conventional PVD tools in Cu BEOL process, in the short-term future.

2. The vulnerable film properties of spin-on dielectric (SOD) and porous ultra low-*k* materials deteriorate the barrier integrity of PVD Ta or TaN deposited on top of them. It results in the poor step-coverage of barrier layer, especially on the trench/via sidewall and causes Ta delamination on the sidewall surface of porous low-*k* dielectrics [27].
3. As barrier thickness scales down with metal width to meet conductor effective resistivity goals, the coverage and uniformity issues become increasingly serious. And eventually, diffusion-resistant dielectrics are needed to be used instead of conventional PVD barrier to provide essentially "zero barrier thickness" type of solutions at the trench/via sidewall region.

Therefore, a more robust barrier is mandatory for the next generation Cu/low-*k* as well as Cu/ultra low-*k* damascene integration schedule. The technological requests for this novel barrier system are that it should have uniform sidewall coverage for the more and more narrow trench/via dimensions, but without showing any metal atom penetration problems during deposition. On the other hand, the solution for this robust barrier system, besides addressing the above issues, must be economical for mass-production IC manufacturing. That means it should be easy to be implemented in current Cu metallization process and minimize the use of any new equipment and processing materials.

1.5 Objectives

The approach to solve/minimize the above issues could also be realized by forming a thin modification layer with in-situ plasma chemical reaction [28], [29]. Initial studies of barriers with dielectric layers have shown no compromise in the performance as sidewall diffusion barriers in Cu/low-*k* damascene interconnects [30]. And some reports indicate it is possible to further use the PECVD dielectrics as "***pore sealing layers***" to modify the poor interface condition of sidewall barrier/porous low-*k* IMD. However, detailed research in this area, including fabrication feasibility, process optimization, electrical and reliability studies, is still limited and is essential before its successful implementation in the industrial manufacturing. There are simultaneous requirements for studies about the mechanism and influence of this dielectric modification layer on the sidewall barrier/ultra low-*k* IMD interface. They are as follows:

1. We need to get a complete knowledge of the electrical performance and reliability characteristics of this approach (*i.e.*, use of dielectric modification layer). It is necessary to develop suitable sidewall diffusion barriers, possibly enhanced by dielectric interfacial layer for current and future Cu/low-*k* and Cu/ultra low-*k* damascene interconnect technology.
2. The answer to "How it can do?" is always followed by the question of "Why it can do". What kind of interfacial modification process corresponds to the electrical/reliability behaviors observed in the experiments? What influence will be made by this novel barrier system on the interconnect reliability model and failure mechanisms? Besides the characteristics/performance evaluation of the new barrier system, people would also like to understand the physics and chemical mechanisms behind this novel barrier scheme.

3. Moreover, the sidewall interfacial condition between barrier and low-*k* IMD shows more and more importance in terms of reliability concerns for future Cu/low-*k* and Cu/ultra low-*k* damascene interconnects. In addition to employing new barrier materials and structures, we want to investigate other new techniques which could enhance the overall reliability performance of sidewall barrier by interface engineering approach. The final goal is to achieve optimized interconnect performance and reliability improvements by the novel sidewall barrier structure with interfacial engineering approach for next generation Cu/ultra low-*k* damascene process.
4. Based on the consideration for minimal process changes without increasing the fabrication complexity and costs, this research is focused on the process improvement under current Cu BEOL manufacturing circumstance. This requires the possible approaches that could be implemented with mature industrial tools, e.g. PVD metal barrier deposition system, PECVD dielectric deposition system and commercial porous low-*k* materials as interconnect dielectrics.

1.6 Major Contribution of the Thesis

Following achievements have resulted from this research work:

1. A novel dielectric/metal bilayer diffusion barrier with low-*k* Silicon Carbide dielectric layer, which is recently proposed by other researchers, has been fabricated and examined in Cu/porous ultra low-*k* damascene interconnects. Our studies show that this bilayer barrier will significantly improve the electrical performance and reliability against thermal/electrical stress of

Cu/porous ultra low-*k* interconnects, compared with the conventional PVD sidewall barrier.

2. A pseudo-breakdown (PBD) phenomenon in Cu damascene interconnects was observed and studied. The physical kinetics of this pseudo-breakdown behavior was investigated and correlated with barrier integrity and Cu transport mechanism in low-*k* IMD. The solution to address the pseudo-breakdown problem was also found and shown to enhance the barrier integrity
3. As a new concept, diffusion barriers with the ability to prevent oxygen/moisture intake have been developed by inserting Al stuffing layer, or employing electron-beam (E-beam) exposure to modify barrier/organic low-*k* interface. The electrical and reliability performance of Cu damascene interconnects showed considerable improvements by both these approaches.

1.7 Organization of the Thesis

This thesis is divided into nine chapters, starting with Chapter 1 introducing the background and motivation of the research work for Cu diffusion barriers. Chapter 2 reviews the mechanism of Cu diffusion/drift transport in dielectric materials as well as some research achievements in dielectric diffusion barriers. The major issues and possible solutions including the use of dielectric barrier for Cu/porous low-*k* integration are presented and discussed.

In Chapter 3, a novel dielectric/metal bilayer structure is introduced to replace the conventional PVD TaN/Ta sidewall barrier for Cu/porous ultra low-*k* damascene interconnects. The improvements in electrical and electromigration performance as well as interface modification by this bilayer barrier are investigated and compared with PVD TaN/Ta barrier. Chapter 4 focuses on the

process optimization for the bilayer barrier structure by using different dielectric and metal barriers thickness to achieve an even better barrier integrity as well as electrical performance and thermal stability. Chapter 5 presents the reliability characteristics of the bilayer barrier in Cu/porous ultra low-*k* interconnects, in terms of current-time (I ~ t) characteristics and time-dependent dielectric breakdown (TDDB). The pseudo-breakdown phenomenon in Cu damascene interconnects is investigated and its physical kinetics are explained. Also, a process solution to solve the pseudo-breakdown issue is provided. Based on these results, different low-*k* dielectric barriers were further integrated into the dielectric/metal bilayer sidewall barrier structure, and evaluated for their integrity with another kind of porous low-*k* ILD. The observations from this study are presented in Chapter 6.

In addition, attempts to achieve an even more robust sidewall barrier by further improving the interface condition between barrier and low-*k* ILD are also discussed. Chapter 7 presents the results on the use of an Al layer to stuff the grain boundary diffusion path in polycrystalline metal barrier and further improve the barrier efficiency against oxygen/moisture penetration. Chapter 8 describes the future trend and presents results on a novel process implementation, unlike other physical approaches, to modify the sidewall barrier/low-*k* IMD interface by using electron beam treatment.

Finally, Chapter 9 summarizes conclusions from this research work and proposes some suggestions for future research.

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Chapter 2. Literature Review on Dielectric Diffusion Barriers for Cu Metallization

2.1 Mechanism of Cu Diffusion in Dielectric Materials

2.1.1 Mathematics of Diffusion Theory

The diffusion phenomenon can be mathematically described by the famous *Fick's laws*. According to *Fick's first law*, the flux of the diffusant is related to the concentration gradient of the diffusant in the compound. In the steady state, it can be written as [1]

$$J = -D \cdot \nabla C + Cv \tag{2.1}$$

where J is the flux of the diffusant in the compound at certain time, C is its concentration at certain location, v is the velocity of mass which moves due to the extrinsic force applied on the diffusant, *e.g.* electrical field or chemical potential, and D is the diffusion coefficient at a given temperature. The *Fick's second law* describes the diffusion in a non-steady state condition when the concentration of diffusant changes with time. The concentration change over a period of time is equal to the gradient of the flux and hence can be written as [1]

$$\frac{\partial C}{\partial t} = -\nabla J = D \cdot \nabla^2 C - \nabla C \cdot v \tag{2.2}$$

Considering the one-dimensional case only, the above formula can be simplified as [2]

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial x^2} - v\frac{\partial C}{\partial x} \tag{2.3}$$

In the case that the diffusant is ionized and an electrical field was applied as the extrinsic force, the velocity of diffusant ions can be written as

$$v = \mu \cdot E \tag{2.4}$$

where μ and E are the mobility of diffusant ions in the compound and the strength of the applied electrical field, respectively. Notice that the mobility and the diffusion coefficient have following dependency, according to the Einstein relation

$$\frac{D}{\mu} = \frac{k_B T}{q} \tag{2.5}$$

where k_B, T, q are the Boltzmann constant, absolute temperature (K) and electronic charge, respectively. So the diffusion equation (2.3) can be written as

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial x^2} - \frac{qE}{k_B T} D\frac{\partial C}{\partial x} \tag{2.6}$$

The first part in equation (2.6) describes the thermal diffusion of neutral diffusant atoms or molecules, which is a statistical result of "random walk" of diffusant in its concentration gradient. The second part shows the drift movement of charged diffusant ions under the applied electrical field. Which mechanism will dominate the whole mass transport phenomena, the thermal diffusion of neutral diffusant or electrical drift of charged diffusant, is decided by the electrical contribution factor $qE / k_B T$. In the region of low temperature with high applied electrical field, the diffusion coefficient could be small but the electrical contribution factor may be large. For example, at room temperature (~ 300 K), the value of $k_B T / q$ is quite small (~ 0.026 eV). Thus the drift movements by electrical field will contribute more than the thermal diffusion in the mass transport phenomena. Therefore the flux of thermal diffusion is smaller than the flux of drift

and can even be ignored. The contrary situation will occur in the region of high temperature but with low applied electrical field.

2.1.2 Physical Model of Cu Diffusion in Amorphous Films

For the study of diffusion phenomena in microelectronics, the most widely used model in Silica-based glasses is the continuous random network of Zachariasen and Warren [2]. The diffused impurities can either interact with the glass network, *e.g.* occupying missing atom sites, or occupy interstitial positions such as ring sites [3]. The monovalent or divalent Cu ions do not enter the glass network while the compensation for additional charge is required. The unbound ions diffuse freely with low activation energy, as actually observed in the measurement of Cu diffusion coefficient in 4% phosphosilicate glass (PSG) [4].

In amorphous materials, the Cohen-Turbull free-volume theory envisages the movement of neighboring molecules due to natural thermal fluctuations [5]. This model describes the glass as having a net of passageways with periodic constrictions. Thus a sufficiently small diffusing ion will easily pass through this net. But a slightly larger ion might have to squeeze through the constructions, resulting in an energy barrier in the form of elastic energy. Thus a larger ion may result in a higher energy barrier. Most researchers agree on the explanation that the Cu transport in dielectric is dominated by the interstitial diffusion of charged Cu cations [6].

Driving forces of ionic motion under applied electric field can be modeled as an approximately periodic potential combined with a linearly sloped potential. Along the direction of electrical field, the barrier height is reduced but in the other direction it is increased. Increasing the electrical potential increases this effect and

allows easier ionic passage [6]. This explains the physical mechanism for the acceleration of Cu diffusion/drift under electrical bias. At a high electrical field, the diffusion flux due to the concentration gradient can even be ignored and only the ionic flux is described as

$$J = \frac{q}{k_B T} D C_m E \tag{2.7}$$

where D, C_m, and E are the diffusion coefficient, solid solubility limit of the ions in the glass and applied electrical field, respectively.

2.1.3 Kinetics of Cu Drift in Dielectrics under Electrical Field

The initial work of Cu diffusion in dielectric films was done by McBrayer *et al.* [7]. They measured the shift of the flat band voltage in the C-V characteristics of Cu gate MOS capacitors subjected to electrical fields in the range of 0.05 - 1.0 MV/cm and over a temperature range of 350°C - 400°C. The calculated diffusion coefficient of Cu (under bias) in SiO_2 was given by

$$D_{Cu} = 1.2 \times 10^{-11} e^{\frac{-1.82eV}{kT}} cm^2 / s \tag{2.8}$$

Shacham-Diamand *et al.* [8] also monitored the C-V characteristics of Cu gate MOS capacitors during bias temperature stress (BTS) tests. They observed an increase in the inversion capacitance above the high-frequency minimum capacitance and below the maximum oxide capacitance in the MOS C-V curve. This increase was attributed to Cu related generation-recombination centers formed in Silicon. They defined the time of Cu penetration through the oxide as the time when this catastrophic capacitance increase occurred, and calculated a

diffusion coefficient of Cu in SiO_2 subjected to an electrical field of 1 MV/cm over temperature range 250°C - 300°C, which was given by

$$D_{Cu} = 2.5\times10^{-8} e^{\frac{-0.85eV}{kT}} cm^2 / s \tag{2.9}$$

The difference in these two reported values is quite large. But generally, people believe that Cu diffusion/drift movement in SiO_2 and other dielectric material is very fast, especially when an electrical field is present.

Additionally, a low-bound calculation to estimate the Cu drift subjected to an applied electrical field was introduced by Loke *et al.* [9]. Cu drift rate was extracted from the slope of the flat-band voltage shift *vs.* stress time after BTS at different temperatures, and given by the following equation

$$D_{drift} = \frac{d[Cu^+]}{dt} = \frac{dQ_m}{dt} = -\frac{C_{OX}}{q}\frac{d\Delta V_{FB}}{dt} \tag{2.10}$$

By using this method, people now could investigate Cu migration movements in different dielectric materials under bias with thermal stress, and evaluate their resistance against Cu penetration [9] - [11].

Cu diffusion/drift transport into dielectric films is very fast and even occurs at low temperature ranges (100°C - 200°C) [8]. The electrical field applied on dielectrics has a strong influence on Cu migration behavior. According to previous work by Raghavan *et al.* [12], Cu transport through dielectric films at elevated temperature and with electrical field involves three stages. The first stage involves the injection of Cu ions and diffusion of Cu neutrals into the dielectric. The injection of ions leads to a built-in space-charge region in the dielectric, which weakens the applied electrical field and then limits the ionic current. In the second stage (Figure 2.1), thermal diffusion of Cu ions and neutrals leads to dielectric degradation and an increase in dielectric leakage. Current *vs.* time (I-t)

characteristics of Cu gate metal-oxide-silicon (MOS) structures subjected to bias-temperature stress (BTS) show an initial decrease in the leakage current followed by a region of low and constant current. Finally, the increased electron current is able to neutralize Cu ions resulting in an increase in Cu injection into the dielectric, leading to eventual failure.

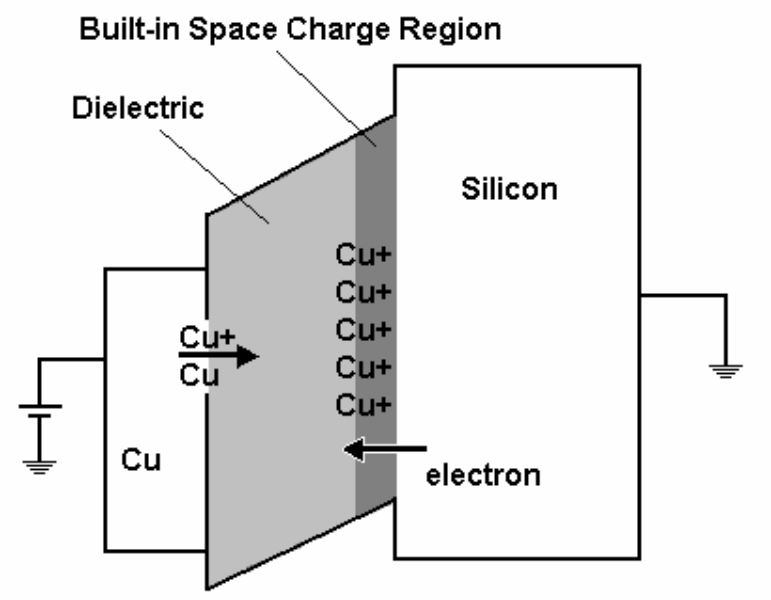

Figure 2.1 Kinetics of Cu drift in dielectric of a MOS structure under electrical field.

2.2 Low-*k* Dielectric Diffusion Barrier

Work on dielectric barrier against Cu diffusion mostly used the above discussed flat band shift method and time-dependent dielectric breakdown (TDDB) test to monitor the reliability and performance of dielectric barriers against Cu penetration during BTS [13], [14]. Surface analysis tools, such as secondary ion mass spectroscopy (SIMS), Auger electron spectroscopy (AES) and Rutherford

back scattering (RBS), were also used in identifying the Cu depth profile in the barrier films.

PECVD SiN, the conventionally used capping layer/etch stop layer, has good resistance against Cu atom/ion diffusion [14]. But it has a high dielectric constant (k ~ 7), which does not meet the technology trend to reduce effective dielectric constant of interconnect dielectrics [15]. The advantage brought by low-k inter layer dielectric (ILD) (k ~ 2 - 3) will be offset by such a high dielectric constant material due to the large amount of capping layer/ESL used in multi-level Cu metallization. Thus there is an urgent demand for developing low-k dielectric films as diffusion barrier/capping layer and ESL.

It is well known that low-k ILD normally contains carbon or carbon-based functional groups such as methyl group ($-CH_3$) and benzene ring. Carbon's low polarizability in Si-CH_3 bonding also contributes to the low dielectric constant of Si-C bonds containing amorphous films [16]. Thus PECVD silicon carbide based films, *e.g.* SiCO, SiCN and SiC, were developed for the low-k dielectric barrier/ESL application in next generation Cu/low-k and Cu/ultra low-k damascene interconnects beyond 0.1 μm technology node [17]. Most of these silicon carbide films deposition employed organosilicon precursors, *e.g.* trimethylsilane or tetramethylsilane, to involve methyl group, which can efficiently lower the dielectric constant of films by reducing the cross-linking and film density as well as occupying a larger volume. The PECVD SiCO, SiCN and SiC dielectric barriers showed an acceptable performance in terms of resistance against Cu diffusion/drift as well as electrical reliability, and were comparable to the conventional SiN films [18], [19] .

Another advantage of SiC based low-*k* dielectric barriers is that both silicon carbide based barrier and most low-*k* ILD materials contain large number of Si-C bonds and carbon involved functional groups (*e.g.* -CH_3, =CH_2, =$(CH_2)_n$). One could speculate that this similar composition may help to improve the weak interfacial condition between dielectric barrier and low-*k* ILD, which is a major source of defects and dangling bonds just after CMP process and is the major path for Cu diffusion/drift as well as the electrical failure [20]. As a further effort, additional post-CMP treatments were introduced to enhance the dielectric barrier integrity by modifying the critical interfacial condition of dielectric barrier/low-*k* ILD. It was reported that *in-situ* NH_3 plasma treatments on uncovered Cu/low-*k* damascene interconnects can passivate the unsaturated low-*k* surface by forming a very thin SiN layer (~ 10 Å) as well as remove Cu oxide [21]. H_2/He plasma treatment prior to the dielectric barrier/capping layer deposition is another efficient approach to improve the electrical reliability of Cu/low-*k* interconnects [22].

2.3 New Application of Dielectric Barrier in Cu/Ultra Low-*k* Damascene Interconnects

2.3.1 Issues Associated with Porous Ultra Low-*k* Integration

The integration of low-*k* dielectrics into the damascene interconnect architecture is always plagued by poor mechanical properties, thermal stability and low resistance to Cu penetration of the low-*k* material. Porosity, which is introduced into spin-on and CVD low-*k* dielectric materials to further lower the *k* value below 2.2, exacerbates these issues. The integration of Cu metallization process with porous ultra low-*k* material requires an efficient sidewall barrier to

avoid any Cu diffusion into low-*k* dielectrics. For the most advanced BEOL process beyond 90 nm technology node, barrier layers are generally deposited using advanced PVD methods. But the further reduction of the geometry size of interconnect structures also promotes the development of other deposition methods such as CVD and ALD. For the metal barriers deposited by PVD or CVD/ALD methods, the diffusion of precursor molecules, solvents, and plasma species, *etc.* into the near surface region and the bulk of porous low-*k* IMD via pores is a potential liability for the maintenance of the low dielectric constant during processing and the reliability during normal operation [23]. Ta precursor diffusion into the bulk of porous low-*k* dielectric instead of sealing it completely at the sidewall region is the main issue for porous ultra low-*k* integration [24]. Other major issues include poor coverage and uniformity of metal barriers due to high surface roughness of porous low-*k* IMD. Consequently significant Cu penetration through the barriers into the porous ultra low-*k* IMD may occur due to the discontinuities of metal barriers. Figure 2.2a shows the cross-section Transmission Electron Microscopy (TEM) image clearly indicating that Cu penetration through Ta barrier into porous low-*k* IMD occurred at sidewall after thermal stress at low temperature (200°C). Increasing the total barrier thickness is restricted by the high resistivity of Ta (175 μΩ•cm) and/or TaN (256 μΩ•cm) films, and does not match the technology trend of interconnect feature size scaling which demands conductive barrier thickness to shrink as well as the Cu line width. Thus it is necessary to keep the barrier layer as thin as possible but with no compromise in barrier integrity against Cu penetration.

Porosity of dielectrics may also compromise the functionality of the thin Cu diffusion barrier through the creation of pinholes in the barrier: There is a

significant difference in the thermal expansion coefficient (CTE) between metal (*e.g.* Ta ~ 6 ppm/°C) and porous low-*k* materials (*e.g.* Porous-SiLK™ ~ 65 ppm/°C). During thermal cycling even in low temperature range (200°C - 400°C), serious mechanical mismatch at the interface of barrier/porous low-*k* IMD may occur, leading to catastrophic distortion of the trench profile as shown in Figure 2.2b. This bending may cause serious cracks or pinholes in the sidewall barrier and deteriorates the barrier integrity.

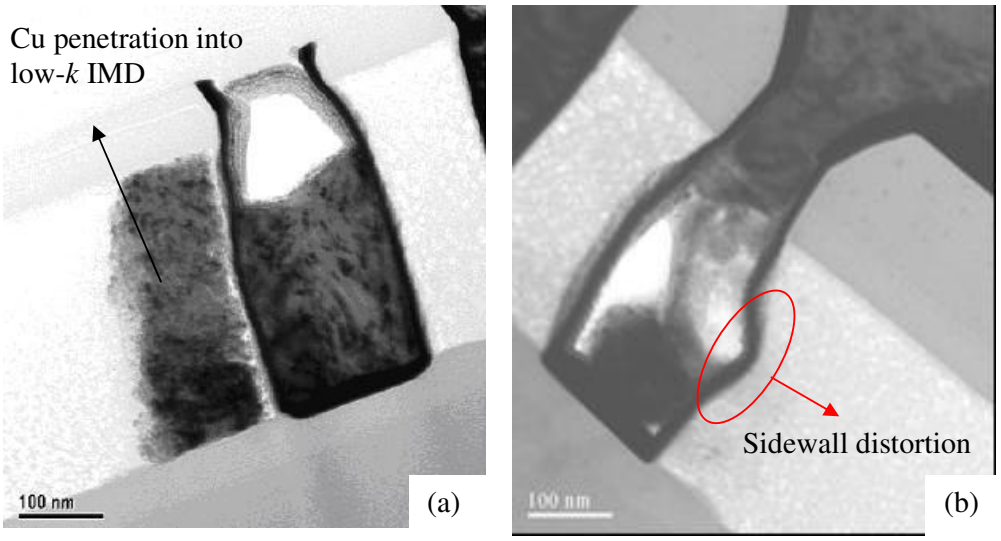

Figure 2.2 TEM images of Cu/porous low-*k* single damascene structures in the case of a) serious Cu penetration after thermal stress at 200°C for 120 h; and b) trench profile distortion after post-ECP annealing at 200°C for 30 min. (Source: C.Y. Li, *Internal Technical Report of Institute of Microelectronics, Singapore*, July 2003)

2.3.2 Process Solution: From Plasma Treatment to Dielectric Pore Sealing

The surface of a porous material can be modified under the influence of the plasma so that a densification of the surface is achieved [25]. Control of the plasma is critical in order to limit the densification to the first few nm of the surface. This way, the *k* value of the films is not significantly affected. This newly formed skin layer can also act as a protective layer to prevent any damage in the bulk of the film. It appears, however, that this technique is only suitable for microporous dielectrics (pore diameter less than 2 nm), which have a *k* value down to about 2.5. Until now, it could not be applied to mesoporous dielectrics which have a larger pore diameter, since the effect of plasma treatment can attain several hundreds of nm depth in such dielectrics. Furthermore, using post-etch plasma treatments is also able to achieve a uniform anti-diffusion layer at the sidewall region [26].

The deposition of a thin layer, which may be of dielectric or metallic nature, is an alternative sealing method. The sealing performance of a thin film depends on the nature of the deposition process itself, as well as on the porous structure of the surface to be sealed. By employing ALD or MOCVD methods, Ta, Ti or W based barrier films are able to seal the porous dielectric microchannels [27], [28]. However, when the porogen load was increased and the porous structure consisted mainly of mesopores, the required barrier thickness for sealing increased significantly [29]. Moreover, the precursor penetration into porous low-*k* material could be a serious concern for such kind of ALD or CVD metal barrier deposition processes. Finally, the huge cost of equipment and precursors further limits its application in industrial manufacturing.

Thin dielectric layers, *e.g.* PECVD silicon carbide based films, have been shown to be good pore-sealing layers [30] and also have considerable resistance

against Cu diffusion. Thus, people proposed the idea that using PECVD dielectric barriers to entirely replace conventional PVD conductive barriers as the sidewall diffusion barrier in Cu damascene structures, so called barrier-metal free (BMF) architecture [31]. The advantage of this approach is the good coverage and uniformity of dielectric barriers on the sidewall due to CVD type deposition method. However, this change may cause additional process difficulty and reliability concerns for Cu dual damascene interconnects because Ta or TaN layer, used as conductive diffusion barrier, also works as an adhesion promoter between Cu and low-*k* IMD. And Cu electromigration performance of damascene interconnects strongly depends on its adhesion with the surrounding low-*k* IMD [32].

A more practical approach is to employ a dielectric thin layer to modify the porous low-*k* surface, which could seal the open pores and provide a "flat ground" for the subsequent metal barrier deposition. Previous studies by *Iacopi* and *Tokei et al.* [30], [33] indicated that high Carbon concentration surface enables easier formation of a fully closed PVD Ta(N) cap layer. The reason was proposed to be the interaction between Ta and C at Ta/dielectric surface, which has a high formation enthalpy ($\Delta_f H^0$(TaC) = -34.44 kcal/mol). During the PVD sputtering, the tendency of Ta atoms/ions to react with C at the dielectric surface can lead to the formation of Ta-C bond. As a result, the wetting capability of Ta (or TaN) on the dielectric surface is enhanced and structural rearrangement of the bonds/charges takes place in the top layers of the dielectric matrix. At the Ta/dielectric interface, a "transition layer" with high intermixing forms. A considerable number of Ta atoms are dispersed in the initial matrix, either unreacted or in the form of Ta-C crystallites. Under these conditions, the pristine carbidic bonds in the dielectric

matrices (*e.g.* C-H_x bonds) are weakened [35], due to charge delocalization effects induced by the presence of neighboring Ta atoms. The high deposition temperature and ion bombardment energy released during PVD deposition may further accelerate breaking of these bonds, and can lead to crosslinking of the top layer of dielectric by forming C-C bonds across the polymer chain. A schematic diagram of this mechanism is shown in Figure 2.3.

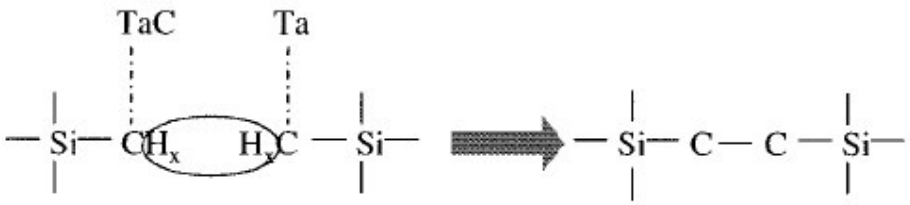

Figure 2.3 Mechanism leading to local cross-linking enhancement by transforming loose C-H_x functional groups to C-C matrix due to the presence of TaC crystallites or unreacted Ta. (Source: Ref. [33])

Therefore, it is possible to use a thin dielectric liner in the Cu/porous low-*k* damascene interconnect scheme, to act as pore sealing layer and prevent metal precursor diffusion into porous dielectrics. By measuring the ellipsometric porosimetry, Iacopi *et al.* [33] reported that ~10 nm dielectric layer of silicon carbide film followed by 10 nm Ta N film could seal the porous surface of the hydrogen silsesquioxane (HSQ) based porous low-*k* material on the blanket samples, rather than 30 nm of either TaN or a-SiC:H single sealing layer. Their initial work [34] also demonstrated that, by using this silicon carbide pore sealing layer prior to PVD TaN barrier deposition, the electrical characteristics of Cu/HSQ-based porous low-*k* interconnects could be improved. There are other

reports [36] that have shown that this silicon carbide liner could work as an efficient pore-sealing layer as well in other Cu/porous low-*k* integration schemes with CVD deposited TiN barrier. Also the pore-sealing silicon carbide liner did not have any negative influence on electromigration behavior of Cu damascene interconnect.

As a logical extension, the use of a combination structure of dielectric modification layer and PVD metal barrier should further enhance the sidewall barrier integrity for Cu/porous low-*k* integration. However, the use of higher *k* value silicon carbide films (k ~ 4.2 - 4.9) as pore sealing layers may (or may not) raise the concern of increasing the overall *k* value and affect other electrical characteristics, *e.g.* leakage current behavior and electrical strength, of interconnects. From a manufacturing point of view, the influence of this new barrier structure on the reliability performance of Cu/porous low-*k* interconnect, should be further evaluated before it is fully implemented in Cu BEOL process. Moreover, for the continued improvement, the researchers and engineers in Cu BEOL process would like to know if there is any other approach to further enhance the barrier integration scheme for future Cu/ultra low-*k* damascene processes. The research in these topics is quite new and limited results are available. The detailed studies of barrier integrity and reliability of this new sidewall barrier structure form the basis of this thesis, and initiate the innovation for a more robust barrier integration schemes.

The development of CVD/ALD metal barrier deposition system is not maturated yet for full implementation in mass-production Cu BEOL process. Due to the resource limitations of this research work (we do not have access to CVD/ALD systems), further studies on the ability of dielectric pore sealing layer

with CVD/ALD type metal barriers are not possible. Thus this thesis focuses mainly on the integration of dielectric pore sealing layer with the high density plasma (HDP) PVD type Ta based sidewall barrier, deposited by advanced SIP technique. This improved PVD system is the mainstream Cu/metal barrier deposition technique used for current 90 nm Cu BEOL process [38], [39] and probably will be extended to future 65 nm Cu metallization technology.

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Chapter 3. Dielectric/Metal Bilayer Sidewall Barrier for Cu/Porous Ultra Low-*k* Interconnects

3.1 Introduction

The integration of porous low-*k* dielectric into Cu damascene process demands a robust barrier system. It is necessary for this sidewall barrier to have a good pore-sealing capability as well as to prevent the Ta penetration into porous low-*k* IMD. This new barrier system needs to satisfy, at least not be contrary to, the technology trend to further scale the barrier layer thickness. For the diffusion barrier properties, it should not be compromising in terms of resistance against Cu diffusion/drift movement, especially when an electrical field is applied. Additionally, electrical and reliability performances of Cu/porous low-*k* interconnects, in terms of low leakage current and thermal stability, should be further improved by the robust barrier.

As stated in Chapter 2, previous studies by other researchers has explored the possibility to introduce additional thin dielectric layer prior to PVD Ta barrier deposition, in order to address all these challenges simultaneously. In this Chapter, this concept is further developed to a bilayer barrier structure consisting of a dielectric modification layer and PVD Ta barrier as the sidewall diffusion barrier for Cu/porous low-*k* damascene interconnects, which does not exhibit any adhesion related problems. The electrical characteristics and barrier integrity of the bilayer barrier with different dielectric underlying layers will be evaluated and compared with the conventional PVD TaN/Ta sidewall barrier.

3.2 Fabrication of Cu/Porous Ultra Low-*k* Damascene Interconnects with Bilayer Sidewall Barrier

Three kinds of PECVD dielectrics were selected as the modification layer/dielectric sidewall barrier. They are SiN (k ~ 6.9) which is the most efficient dielectric barrier/passivation layer, SiO_2 (k ~ 4.2) which has a well-behaved IMD as well as reliable film properties and is usually used as the hard mask (HM) layer in Cu/porous low-k damascene process, and a-SiC:H (k ~ 4.9), which was reported as an efficient low-k dielectric diffusion barrier [1] with a similar chemical structure as most other low-k IMD materials [2].

Interconnect structures with different bilayer sidewall barriers were fabricated in a 0.13 μm Cu single damascene process. The porous organic ultra low-k dielectric, Porous-SiLK™ [3], which has a low dielectric constant of ~2.2, was used as the IMD with a SiO_2 hard mask on top of it to alleviate CMP and surface leakage issues. After the trench etching and cleaning processes were completed, a very thin (< 100 Å) dielectric layer (SiN, SiO_2 or a-SiC:H) was deposited as the modification layer/dielectric barrier on the sidewall, followed by the deposition of 250 Å PVD Ta diffusion barrier/adhesion promoter. All the dielectric layers were deposited in an Applied Material Centura™ 5200 PECVD system. The process flow of this bilayer sidewall barrier is shown in Figure 3.1.

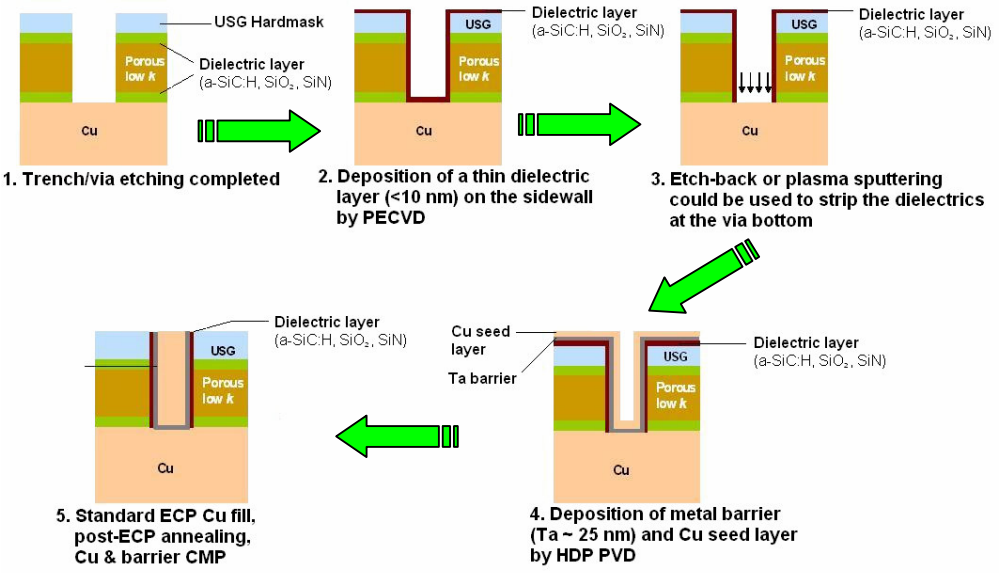

Figure 3.1 Process flow of dielectric/metal bilayer sidewall diffusion barrier for Cu/porous low-*k* damascene interconnects.

For comparison purposes, a conventional 250 Å PVD TaN/Ta sidewall barrier, consisting of 125 Å PVD Ta layer on top of 125 Å PVD TaN layer, was also fabricated. This PVD TaN/Ta barrier was reported as an efficient sidewall diffusion barrier for Cu/porous low-*k* damascene interconnects [4]. All Ta and TaN barriers were deposited in an Applied Material Endura™ high density plasma physical vapor deposition (HDP PVD) system with SIP technique. Subsequently, Cu seed layer deposition was carried out in the same system without breaking the vacuum. After ECP Cu fill, a standard annealing process at 200°C for 30 min., was carried out to stabilize the Cu grain structures and make it easy for the subsequent CMP process. Finally, the capping layers consisting of a 500 Å SiCN dielectric barrier and a 3000 Å SiO_2 passivation layer were deposited on top of the damascene structure to prevent moisture intake and Cu out-diffusion. Blanket samples of each type of bilayer barrier as well as PVD TaN/Ta barrier with Cu top

layer on non-patterned Porous-SiLK™ substrates were also fabricated using the same process sequence for physical characterization.

It should be pointed out that, in the dual damascene process, the unwanted dielectric on the via-bottom could be etched back by ion sputtering during the pre-clean step before the PVD metal barrier deposition, or removed simultaneously with the underlying etch-stop layer, to ensure a good contact with the underlying Cu line. Such dielectric removal steps for via bottom have been successfully realized and integrated in Cu dual damascene process, which also show no compromise in terms of via contact resistance [5], [6].

3.3 Evaluation on Electrical Performance and Thermal Stability

3.3.1 Electrical Test Structures

Electrical tests, including Cu line resistance measurement, line-to-line capacitance measurement, leakage current test and voltage ramp test, were carried out to evaluate the electrical characteristics and reliability of different dielectric/metal bilayer barriers. The Cu line resistance was measured from a 1 m long serpentine line width 0.18 μm width and spacing. The line-to-line capacitance and leakage current were measured from the 1 m long comb test structures, consisting of 0.18 μm wide lines with 0.18 μm spacing as shown in Figure 3.2a. Voltage ramp test was performed on 0.192 m long serpentine lines, sandwiched between comb structures (see Figure 3.2b). Both the line width and spacing were equal to 0.24 μm. All the electrical measurements were carried out before and after different thermal annealing cycles and BTS tests.

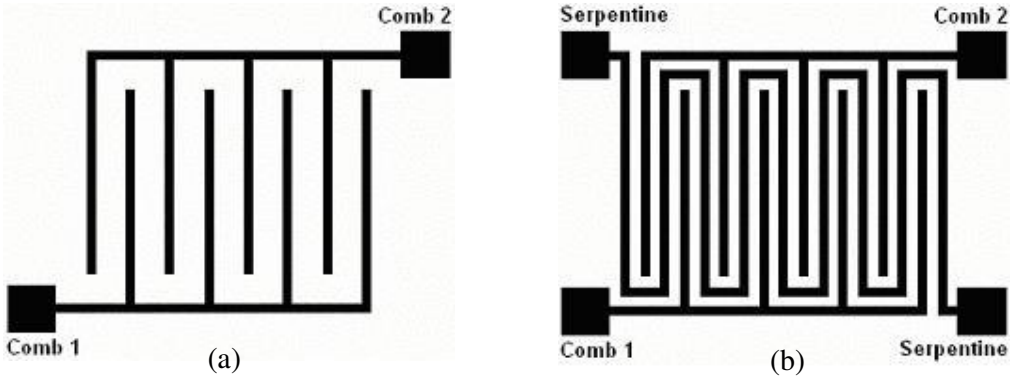

Figure 3.2 Schematic diagrams of a) comb structure, and b) comb/serpentine sandwich structure.

3.3.2 *RC* Delay Consideration

It is known that high resistance of metal barrier layer is the driving-force to shrink the sidewall barrier thickness when Cu BEOL process advances to the 65 nm and beyond technology nodes [7]. As the high frequency applications (clock speed >100MHz) are inevitable for the modern semiconductor device, the contribution of sidewall barrier to overall interconnect line resistance becomes more and more important, due to the frequency-dependent Skin Effect. Figure 3.3a shows the Cu line resistance distribution of interconnect structures with different sidewall barriers. It is clearly seen that the use of a-SiC:H/Ta sidewall barrier could lower the overall metal line resistance, compared with the PVD TaN/Ta barrier. One possible reason is attributed to the Ta barrier used in the bilayer barrier structure, which has a lower resistivity (175 μΩ•cm) than that of multi-stacked TaN/Ta barrier (380 μΩ•cm). However, the samples with SiN/Ta and SiO_2/Ta bilayer barrier did not show any improvement but performed worse than TaN/Ta barrier in terms of Cu line resistance. Obviously, dissimilar surface modification results when different dielectric components are used in the bilayer barrier.

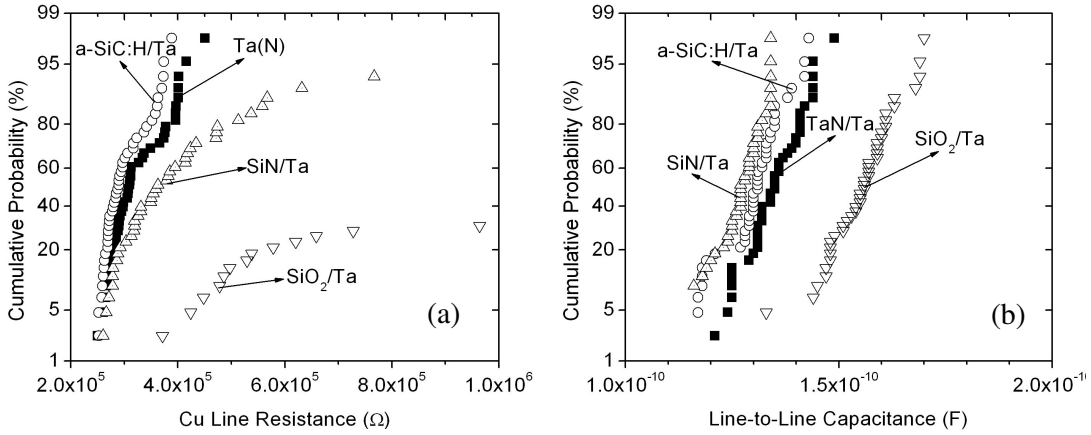

Figure 3.3 Distribution of a) Cu line resistance, and b) line-to-line capacitance, of Cu/porous ultra low-*k* interconnects with different sidewall barriers.

The replacement of PVD TaN/Ta barrier by a-SiC:H/Ta or SiN/Ta bilayer barrier reduced the line-to-line capacitance except for the SiO_2/Ta barrier, as shown in Figure 3.3b. It suggests that a lower effective dielectric constant (k_{eff}) of overall inter metal layer dielectrics could be achieved by using appropriate bilayer barrier. The fringe capacitance from surrounding dielectric film stacks (*e.g.* hardmask, passivation/capping layer and underlying supporting layer between damascene structure and Silicon substrate) was also considered for k_{eff} calculation by using the following equation:

$$C_{line} = \frac{\varepsilon_0 k_{eff}}{d} A + C_{fringe} \qquad (3.1)$$

Where C_{line} is measured line-to-line capacitance, d is IMD spacing measured from cross-section TEM images of Cu /porous ultra low-*k* damascene structure. A is total sidewall area of electrical testing structure calculated by 3000 Å IMD thickness and totally 1 m line length of comb structure. C_{fringe} is the parasitic

capacitance contributed from surrounding dielectric film stacks due to fringe effect. Table 3.1 lists the k_{eff} calculated from the line-to-line capacitance for different sidewall barriers, by assuming that fringe effect contributes to ~1/3 of the measured line-to-line capacitance for single damascene interconnects [8], [9]. Low k_{eff} values were calculated by including C_{fringe}, which is due to the significant parasitic capacitance contributed by surrounding material in our single damascene interconnect structures.

Table 3.1 Calculated effective dielectric constant k_{eff} from line-to-line capacitance with different sidewall barriers.

Sidewall barriers	Mean of line-to-line Capacitance (pF)	Measured IMD spacing (nm)	Calculated k_{eff}	
			(excluding C_{fringe})	(including C_{fringe})
PVD TaN/Ta	135.3	147.1	3.7445	2.497
a-SiC:H/Ta	126.9	151.6	3.620	2.413
SiN/Ta	124.5	153.9	3.606	2.404
SiO_2/Ta	143.7	~150	3.641	2.704

The use of the additional dielectric layer on the sidewall, which has a higher k value ($k_{\text{a-SiC:H}}$ ~ 4.9, k_{SiN} ~ 6.9) than that of porous ultra low-k IMD ($k_{\text{Porous-SiLK™}}$ ~ 2.2), did not increase but slightly reduced the line-to-line capacitance, except for the SiO_2/Ta barrier. The sidewall coverage of different barrier structures is listed in Table 3.2, measured by cross-section TEM. We believe that the use of thin dielectric layers on the sidewall will influence the

characteristics of line-to-line capacitance in opposite ways: The increase in IMD spacing (2 times of dielectric layer thickness on the sidewall) should slightly decrease the capacitance, while the higher k value of the additional dielectric layers ($k_{\text{a-SiC:H}}$ ~ 4.9, k_{SiN} ~ 6.9, k_{SiO2} ~ 4.2) should increase k_{eff}, and therefore the capacitance, of the interconnect. Since the dielectric layer deposited on the sidewall is quite thin (< 40 Å), the contribution of these thin dielectric layers (a-SiC:H, SiO_2 and SiN) to the effective k value of interconnect dielectrics should be small. A similar *RC* delay reduction was also observed by other researchers [10], [11] by using a-SiC:H liner structure prior to metal barrier deposition. However, the inconsistent *RC* characteristics of SiO_2/Ta barrier is dramatically increased, which suggested a different influence compared with other two kind of bilayer barriers. The effects of different bilayer barriers on metal line resistance and interconnect capacitance will be discussed later in Section 3.5.2.

Table 3.2 Measured sidewall coverage of different barrier structures, the sidewall thickness of SiO_2 layer is not available due to the distorted profile.

Barrier Structures		Actual Film Thickness on the Sidewall
PVD TaN/Ta	TaN 125 Å Ta 125 Å	TaN/Ta 30~50 Å
a-SiC:H/Ta	a-SiC:H 100 Å Ta 250 Å	a-SiC:H 14~28 Å Ta 71 Å
SiN/Ta	SiN 100 Å Ta 250 Å	SiN 29~35 Å Ta 45 Å
SiO_2/Ta	SiO_2 100 Å Ta 250 Å	SiO_2 (N/A) Ta 69 Å

3.3.3 Electrical Characteristics and Thermal Stability

The leakage current vs. electric field (I *vs*. E) characteristics is shown in Figure 3.4. Cu/porous ultra low-*k* interconnects with a-SiC:H/Ta bilayer barrier have a better breakdown electrical field (E_{BD}) of ~2.4 MV/cm at room temperature, compared with ~1.7 MV/cm for interconnects with conventional PVD TaN/Ta barrier. At an elevated temperature of 150°C, a smaller leakage current was achieved and E_{BD} improved from ~1.3 MV/cm (TaN/Ta barrier) to ~2.0 MV/cm (a-SiC:H/Ta bilayer barrier). After a thermal stress at 350°C for 1 h, E_{BD} of samples with a-SiC:H/Ta bilayer barrier is still ~40 % higher (~2.2 MV/cm) than that of the TaN/Ta barrier (~1.6 MV/cm). Even after BTS at 0.5 MV/cm, 350°C for 1 h, the interconnect structures with a-SiC:H/Ta bilayer barrier show an E_{BD} of ~1.0 MV/cm, while samples with other barriers have already failed (Figure 3.4d).

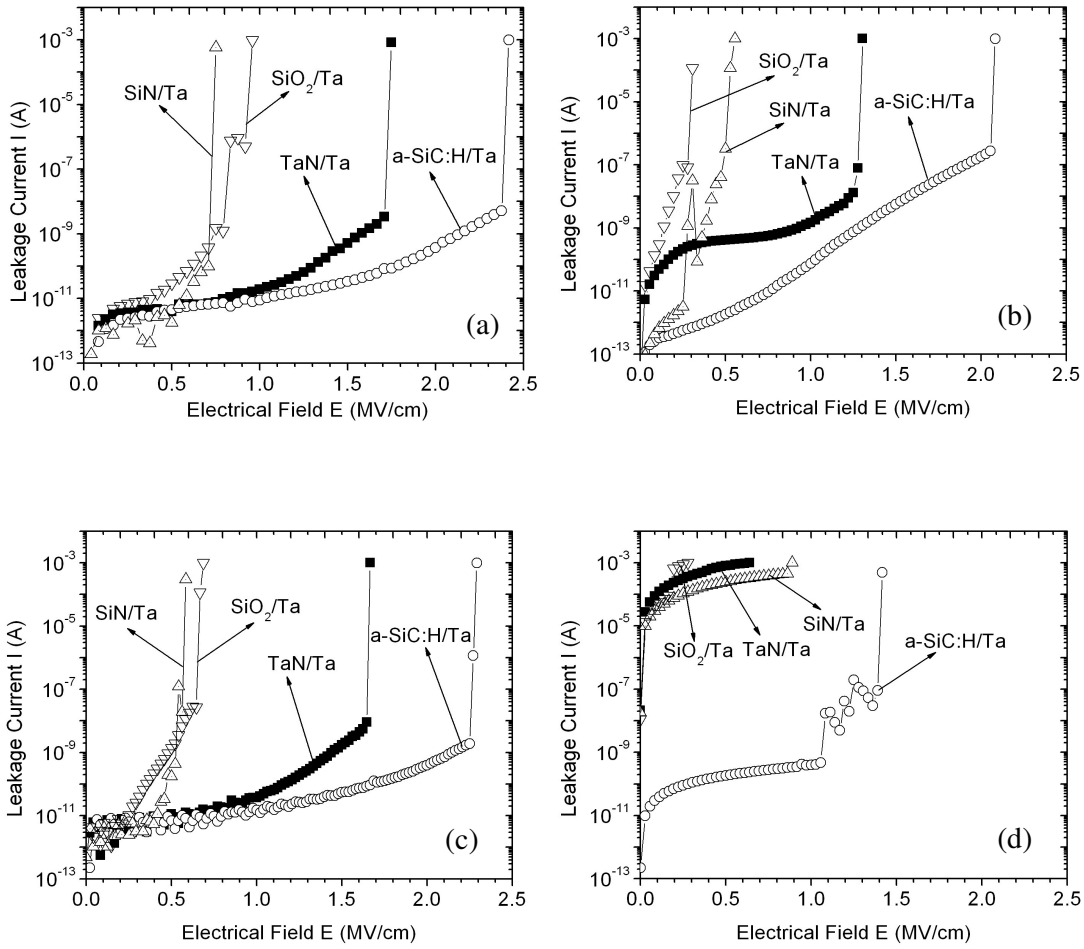

Figure 3.4 Leakage Current *vs*. Electrical Field with different sidewall barriers: a) at room temperature, b) at 150°C, c) after thermal stress at 350°C for 1 h, and d) after BTS at 0.5MV/cm 350°C for 1 h.

Figure 3.5 shows the distribution of the line-to-line leakage current of interconnects, measured at 1 V, subjected to different conditions of thermal stress. The leakage current of sample with a-SiC:H/Ta bilayer sidewall barrier is about 1 to 2 orders of magnitude smaller than that of PVD TaN/Ta barrier. When tested at an elevated temperature of 150°C, a similar improvement was observed as shown in Figure 3.5b. Even after long time burn-in test at 200°C for 72 h in air ambient, the sample with a-SiC:H/Ta bilayer barrier still shows a smaller line-to-line leakage current than that of PVD TaN/Ta barrier (Figure 3.5d). An identical behavior was observed when the measurements were repeated at 3 V (Figure 3.6). These results indicate improved electrical performance and good thermal stability in Cu/porous ultra low-*k* interconnects when a-SiC:H/Ta bilayer sidewall barrier was used.

The line-to-line leakage current improvements in SiN/Ta bilayer barrier are not only unstable but also unpredictable under different thermal stress conditions. The SiO_2/Ta bilayer barrier seems to have the worst characteristics amongst the different barriers used in this study. Samples with either SiN/Ta or SiO_2/Ta bilayer barriers show a poor electrical breakdown strength (< 1 MV/cm) even without any thermal stress (Figure 3.4a). The widely varying and contradictory results between SiN, SiO_2 and a-SiC:H films as dielectric sidewall barriers are likely to be due to their differing influences on the underlying porous ultra low-*k* dielectric and barrier integrity, which will be discussed in the next sections .

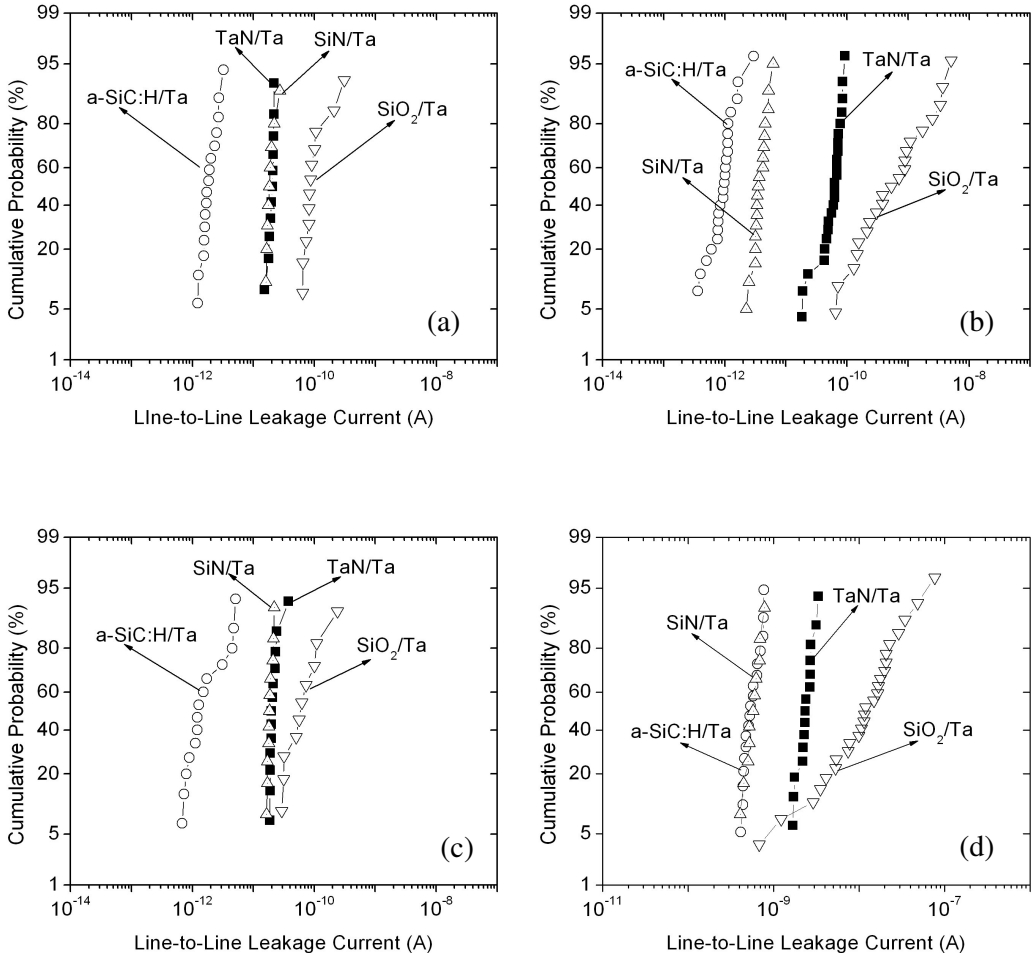

Figure 3.5 Line-to-line leakage current distribution at 1 V with different sidewall barriers: a) at room temperature, b) at 150°C, c) after thermal stress at 350°C for 1 h, and d) after burn-in at 200°C for 72 h.

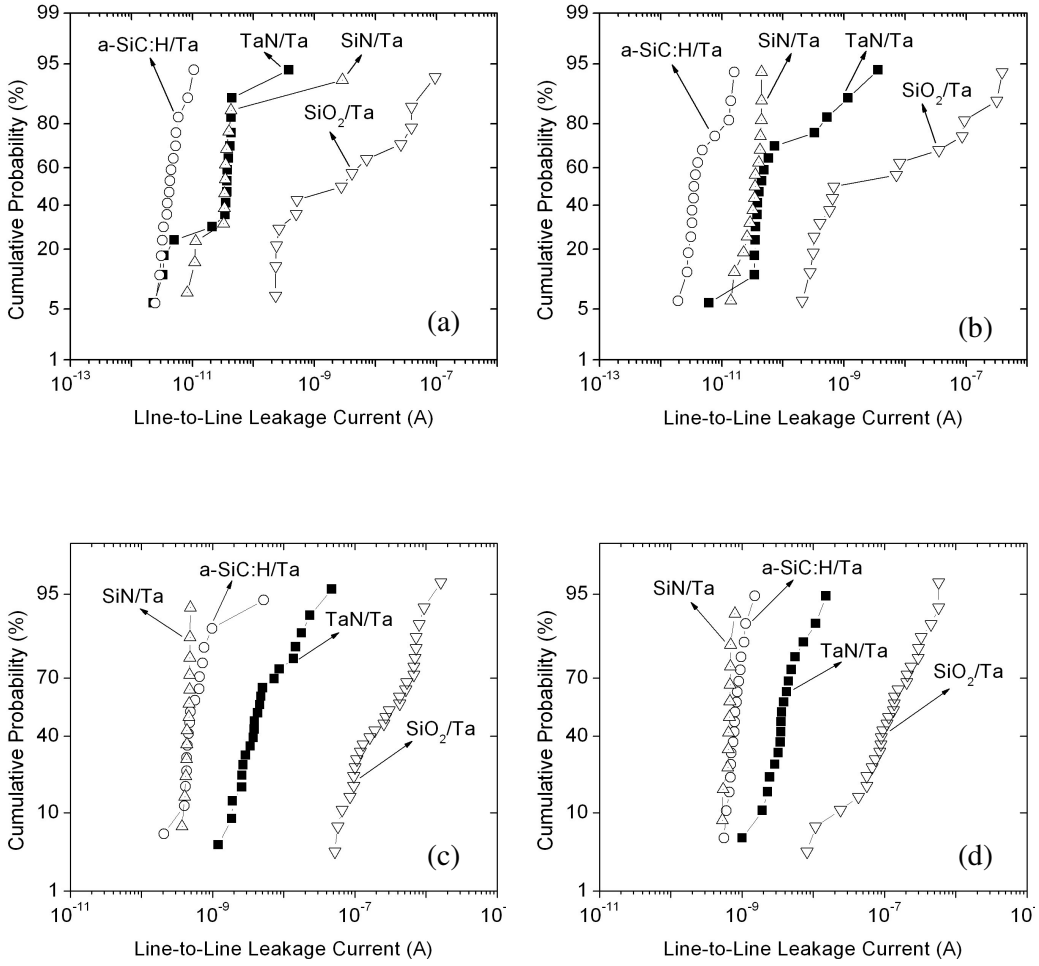

Figure 3.6 Line-to-line leakage current distribution at 3 V with different sidewall barriers: a) at room temperature, b) after thermal stress at 350°C for 1 h, c) after burn-in at 200°C for 48 h, and d) after burn-in at 200°C for 72 h.

3.4 Surface Morphology Modification

In order to investigate the physical mechanisms and the influence of different dielectric layers on the porous ultra low-*k* material, atomic force microscope (AFM) was used for the surface morphology studies. Figure 3.7a shows the bare Porous-SiLK™ sample exhibiting a rough surface which is mainly due to the porosity in the film. The root-mean-square (RMS) value of surface roughness was ~15 Å for this kind of porous low-*k* dielectric (Table 3.3). It is difficult for such a rough surface to be filled and covered uniformly by the conventional PVD Ta or TaN barrier, especially at the trench/via sidewalls [4]. Such high surface roughness was shown to cause surface diffusion and subsequent penetration of the deposited Ta or TaN into the underlying porous low-*k* IMD [12]. The interface of Ta barrier and porous low-*k* IMD was shown to be irregular and uneven [13]. Therefore, the effective barrier thickness to cover the porous surface and block potential Cu diffusion is significantly reduced, leading to a poor interface as well as discontinuities and defects in the PVD barrier [14]. The increased surface roughness (RMS values ~45 – 76 Å) after the deposition of different PVD metal barriers is a direct proof of such an effect. As a result, the coverage of the PVD barrier on such a rough sidewall will be very poor. Our experiments show that the coverage of PVD Ta or TaN barrier on Porous-SiLK™ was only 12 - 18 % on the sidewall. Thus, the barrier film qualities of PVD Ta or TaN would be considerably weakened, and the risk of defects located in barrier layer, *e.g.* pinholes and cracks, will be increased. These defects may provide pathways for Cu penetration into porous low-*k* IMD, and even allow Cu to come in direct contact with porous low-*k* IMD in areas that may not be completely covered by the metal barrier. The end result would be the fast failure of

PVD barrier directly deposited on porous low-*k* IMD, especially when subjected to thermal cycling and electric stress.

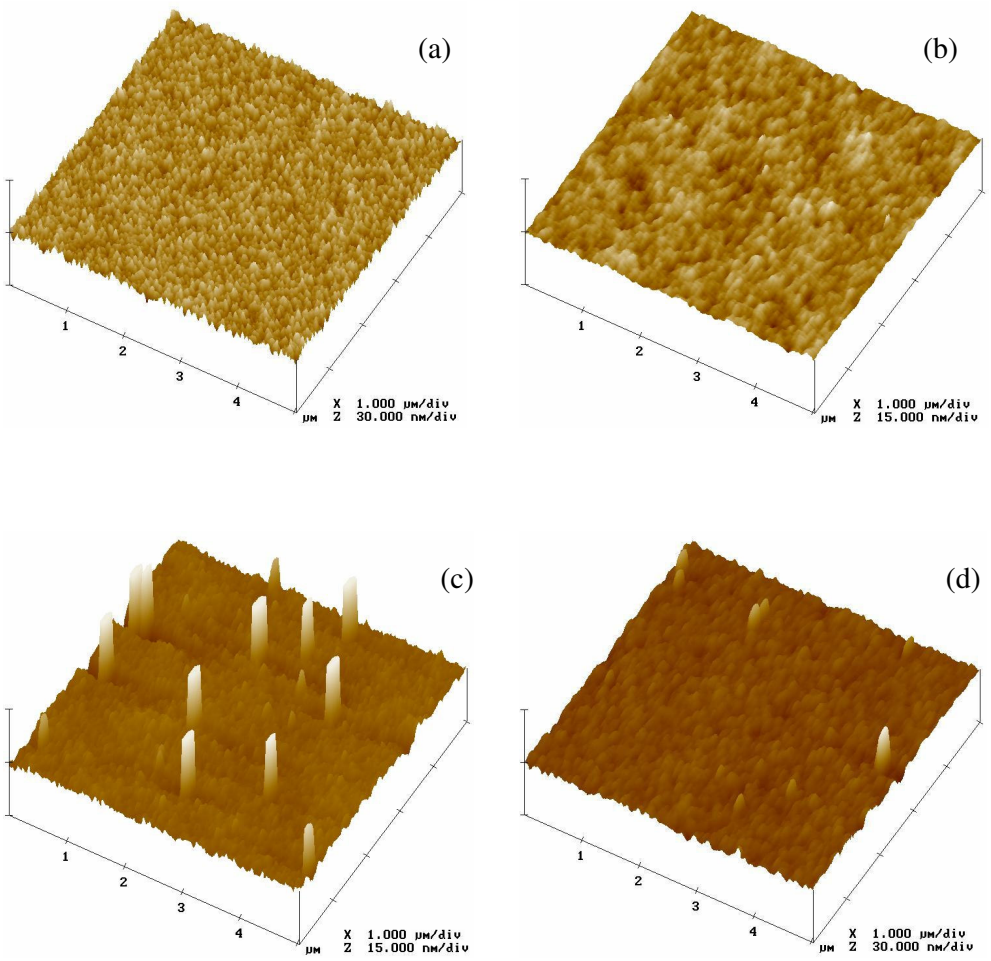

Figure 3.7 Surface morphology of a) bare Porous-SiLK™ film, and after the deposition of b) PECVD a-SiC:H, c) PECVD SiN, d) PECVD SiO_2 layers.

After the deposition of a thin PECVD a-SiC:H layer (<100 Å), the surface becomes smoother (Figure 3.7b). The RMS value of surface roughness was reduced to ~4.3 Å. The much smaller surface roughness after a-SiC:H dielectric layer coating implies that the a-SiC:H film could seal the porous surface of porous low-*k* dielectric. Similar results were also reported, either for Cu/porous low-*k*

interconnect process with PVD Ta based metal barrier [15], [16] or CVD TiN barriers [10], [11]. The detailed results by previous researcher were discussed earlier in Section 2.3.2. It was indicated that the a-SiC:H capping layer on the porous dielectric has a fairly low pinhole density and good stability to moisture absorption. Therefore, this flatter and smoother surface could make the subsequently deposited PVD Ta barrier to be more uniform and with a better step-coverage. As a result of surface modification by a-SiC:H thin layer, the subsequently deposited PVD Ta barrier could be more continuous and with less defects, which is helpful to minimize/eliminate the Ta penetration issue. Our experiment results are in agreement with this conclusion and show that the use of a-SiC:H/Ta bilayer structure leads to a good uniformity of the PVD Ta layer, with the Ta barrier coverage increased to ~30 % on the sidewall.

Table 3.3 Surface roughness before/after the deposition of different barrier films on porous low-*k* dielectrics

Type of Film Stacks	RMS of Surface Roughness (Å)
Porous-SiLK™	15
Ta/Porous-SiLK™	54.2 – 56.1
TaN/Porous-SiLK™	44.5 – 50.1
TaN/Ta/Porous-SiLK™	57.6 – 76.5
a-SiC:H/Porous-SiLK™	4.3
SiN/Porous-SiLK™	9.2
SiO_2/Porous-SiLK™	13.3

It was also reported [12]~[16] that the incorporation of high concentration of carbon (~45% in a-SiC:H film) from a-SiC:H coating layer would slow down the Ta surface diffusion and promote the sealing efficiency. It is attributed to the interaction between Ta and C in the a-SiC:H layer, which could help to transform the loose C-H_x function group to C-C crosslinking in the covalent -Si-C- matrix [16]. The local crosslinking enhancement in dielectric matrices could help to terminate, and/or enable the sealing of open pores at a-SiC:H and/or porous low-*k* IMD surface, especially where the thin a-SiC:H layer may not completely seal the porous low-*k* IMD surface. The Ta surface diffusion into a-SiC:H and porous low-*k* IMD could be further reduced through the dense -Si-C- matrix structure. Since the a-SiC:H layer on the sidewall surface of porous low-*k* IMD is quite thin (<100 Å on the blanket film and 14~28 Å only on the sidewall), it is reasonable to believe that this crosslinking enhancement may also occur at the porous low-*k* IMD surface by the Ta-C present in a-SiC:H layer. A schematic diagram of this mechanism is shown in Figure 3.8.

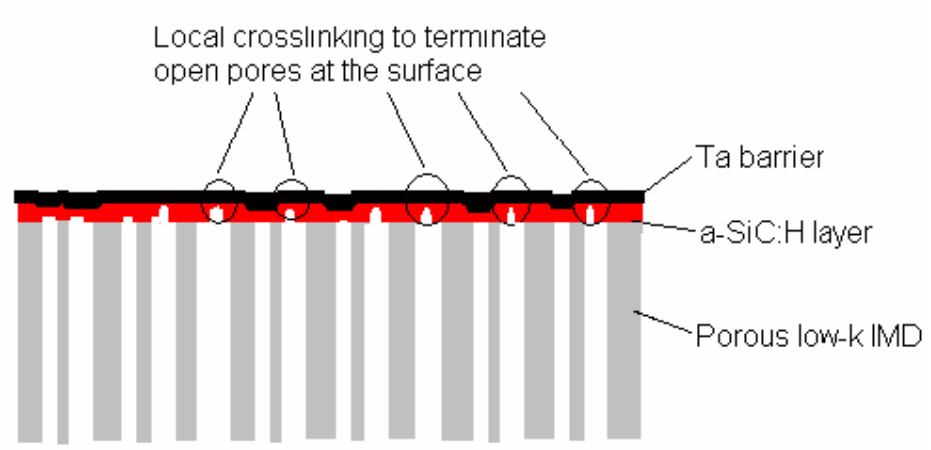

Figure 3.8 schematic diagram of local crosslinking enhanced pore sealing at a-SiC:H layer/porous low-*k* IMD surface.

PECVD SiN deposition process with Silane (SiH_4) and Ammonia (NH_3) precursors may cause a high particulate contamination due to excess gas phase nucleation [17], which appears as sharp "spikes" in the AFM images (Figure 3.7c). Although the surface roughness is fairly low (~9.2 Å) after SiN layer deposition on porous low-*k* dielectric, these particulates may punch through the whole barrier layer during the subsequent PVD Ta barrier deposition process. Thus it would form new defects in the subsequent PVD Ta barrier as well as exacerbate the discontinuity and coverage issues. The surface morphology after PECVD SiO_2 thin layer coating on porous low-*k* IMD also showed similar spikes (Figure 3.7d), though shorter and fatter than the spikes associated with SiN. We believe that the use of Silane as the silicon supplying precursor in PECVD SiO_2 deposition, similar to the PECVD SiN deposition process, may be responsible for such an observation.

3.5 Barrier Integrity of Bilayer Sidewall Barrier

3.5.1 Resistance against Cu Penetration

Secondary ion mass spectroscopy (SIMS) performed on blanket samples with different barrier layers shows an almost identical Cu penetration profile in a-SiC:H/Ta, SiN/Ta bilayer barriers as well as TaN/Ta barriers after BTS at 350°C, 0.5 MV/cm for 1 h (Figure 3.9). But the Cu migration into SiO_2/Ta bilayer barrier seems to be slightly tougher than that of the other two bilayer barriers. The Cu/Ta barrier interface is defined as the location where the Cu intensity dropped to 10 % of the bulk intensity in Cu film. The Ta/dielectrics interface (when a-SiC:H/Ta, SiO_2/Ta, or SiN/Ta bilayer barriers were used), or TaN/porous IMD interface (when TaN/Ta barrier was used) were defined as locations where the Ta intensity dropped to 10 %

of the bulk intensity in the Ta (or TaN) barrier film. However, the interface between dielectric layer (a-SiC:H, SiN and SiO_2) and porous low-*k* IMD can not be distinguished due to their similar chemical composites (Si, O and/or C). And the surface roughness of porous low-*k* IMD leads to additional inaccuracy and difficulties to identify the interface of such thin dielectric layers (<100 Å) between Ta barrier and porous low-*k* IMD in SIMS sputtering profile. The secondary ion counts of Cu in each sample were normalized to Ta signal [18], in order to minimize the measurement inaccuracy due to knock-in effect and matrix effect commonly observed in SIMS technique [19], [20].

Due to the different dielectric "buffer" layer (a-SiCH, SiO_2 or SiN) used in the bilayer barrier structure, the quality of Ta barrier (deposited on top of them) will be different as mentioned in section 3.4, while these dielectric layers also have different resistance to Cu movement. When Cu started to diffuse/drift towards the porous low-*k* IMD under thermal/electrical stress, the boundary conditions for the Cu migration in each barrier structure are not the same. Therefore, the final Cu intensity profiles in PVD TaN/Ta barrier and bilayer barriers are different as shown in Figure 3.9, which suggests different barrier resistance against Cu penetration. The PVD TaN/Ta layer should have a better performance against Cu diffusion than single PVD Ta layer of the same thickness [21], due to the amorphous-type TaN layer but with a higher resistivity. It is well known that PECVD SiN and a-SiC:H films are good dielectric barriers which can effectively prevent Cu penetration even when subjected to thermal and/or electrical stress. Their applications in Cu damascene process as dielectric diffusion barriers were shown to be efficient and reliable [22], [23]. When used as thin underlying layers with PVD Ta, PVD Ta barrier uniformity and quality is further improved leading to a more robust and reliable barrier performance. We therefore

believe that the use of thin (~100 Å) SiN and a-SiC:H dielectric layers, in addition to PVD Ta barrier, can enhance the total barrier layer against Cu penetration, but would not affect the total Cu line resistance. Thus the bilayer barriers of a-SiC:H/Ta and SiN/Ta structures were shown to have an equal resistance to Cu diffusion/drift as the PVD TaN/Ta barrier. But the particulate issues associated with PECVD SiO_2 and SiN layers may undermine their barrier efficiency against Cu penetration.

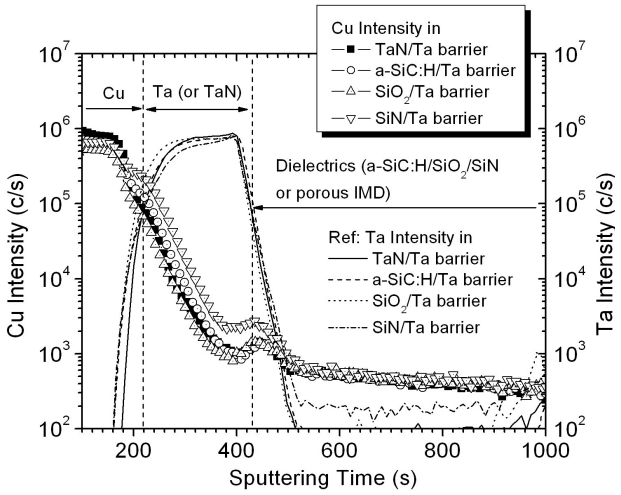

Figure 3.9 Cu depth profiles in different barriers after BTS at 0.5 MV/cm, 350°C for 1h. The Cu/Ta interface shown here is for PVD TaN/Ta barrier only for clarity.

3.5.2 Barrier Integrity in Cu/Porous Ultra Low-*k* Damascene Interconnects

An independent investigation of the interface between Cu, barrier and porous low-*k* IMD, in the fabricated damascene structure, was carried out using TEM. The cross-section TEM images of trench sidewall with different bilayer barriers and conventional PVD TaN/Ta barrier, after the BTS test at 350°C, 0.5 MV/cm for 1 h, are shown in Figure 3.10. In the case of PVD TaN/Ta barrier, there is an unclear and

rough interface between the metal barrier and the porous low-*k* IMD, even at a magnification only half that of a-SiC:H/Ta barrier. This "blur" interface corresponds to the poor surface morphology of barrier/porous low-*k* IMD by direct PVD metal barrier deposition, and suggests a high surface diffusion and subsequent Ta penetration into the porous low-*k* IMD [12], [14]. This result is in agreement with the report by Iacopi *et al.* which indicated that TaN layer exhibits a high degree of porosity and could not seal the porous surface of low-*k* IMD [24]. After the BTS test, Cu residue in porous low-*k* IMD was detected in the porous low-*k* IMD by electron energy loss spectroscopy (EELS) mapping. This is a strong evidence of the existence of pathways in the PVD TaN/Ta barrier for Cu penetration into porous low-*k* IMD. Such a barrier failure is consistent with the electrical failure after the BTS test, shown in Figure 3.4d.

On the other hand, the a-SiC:H/Ta bilayer barrier, shown in Figure 3.10b intentionally at a higher magnification, exhibited a clear interface between Ta and the porous low-*k* IMD. This is in agreement with the successful surface modification by the a-SiC:H thin layer as previously discussed. Ta surface diffusion and penetration issues into porous low-*k* IMD could be alleviated or eliminated on the smoother surface with the modification by a-SiC:H thin layer. As a result, the Ta barrier deposited on it obviously has a good uniformity and higher step-coverage on the sidewall (~70 Å) than that of PVD TaN/Ta barrier (30~50 Å) of the same thickness. The end result of this a-SiC:H/Ta bilayer structure is an efficient and reliable sidewall diffusion barrier. No Cu residue was detected after the BTS test, which is in agreement with the good electrical performance and thermal stability as demonstrated earlier (see Figure 3.4d). This is a good evidence that the a-SiC:H modification layer could prevent the Ta and Cu diffusion into the porous low-*k* IMD. An improved

interface between the Ta barrier and porous low-*k* IMD was achieved without the formation of Ta or Cu compounds (*e.g.* Ta or Cu oxide), which are believed to exhibit not only high resistivity, but also high *k* values (*e.g.* k_{Ta2O5} ~ 25). The use of a-SiC:H modification layer on the sidewall eliminates, or at least alleviates, the metal surface diffusion into porous low-*k* IMD, leading to less metal contamination at the barrier/porous IMD interface region [10], [11]. Thus the overall Cu line resistance and the effective *k* value of Cu/porous low-*k* interconnects will be reduced, as shown in Figure 3.3 and Table 3.1 by using a-SiC:H/Ta bilayer barrier structure.

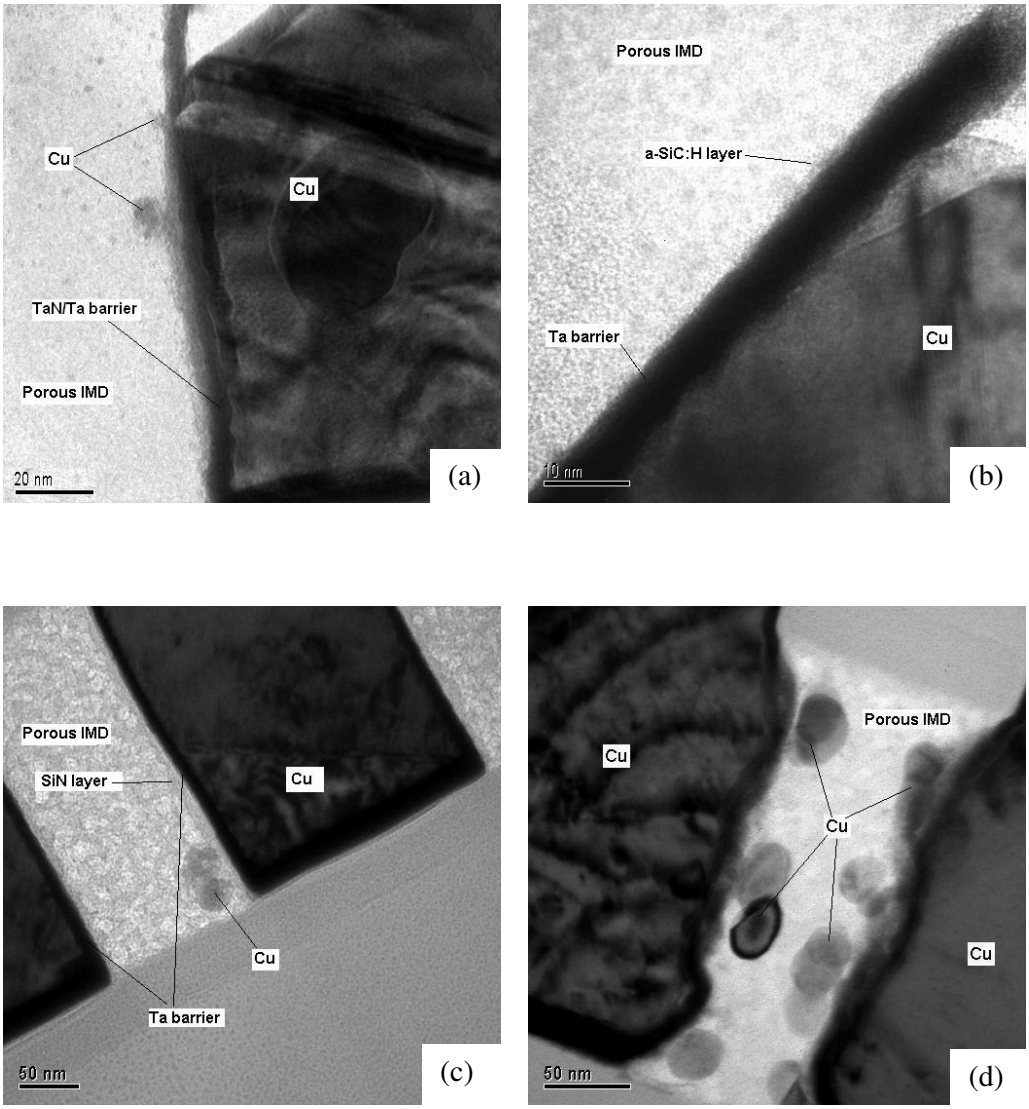

Figure 3.10 TEM images of Cu/Porous-SiLK™ single damascene trench sidewall with different barriers after BTS test at 350°C, 0.5 MV/cm for 1 h: a) conventional PVD TaN/Ta barrier, b) a-SiC:H/Ta bilayer barrier, c) SiN/Ta bilayer barrier, and d) SiO_2/Ta bilayer barrier.

In the case of SiN/Ta barrier (Figure 3.10c), Cu residue was also detected after an identical BTS test by EELS mapping, although the trench cross-section has a well-defined profile. However, no Ta penetration was found. Similar to the case of a-SiC:H/Ta bilayer barrier, the clear interface between Ta barrier and porous low-*k* IMD has a positive effect on interconnects capacitance. However, the particulates on the SiN/porous low-*k* surface (Figure 3.7c) will pierce the whole barrier layer and leave pinholes, as we pointed out earlier. The high pinhole density would provide potential pathways for Cu penetration into porous low-*k* IMD, leading to its eventual electrical failure, but its sidewall profiles are still well-defined. In the case of using SiO_2 as the dielectric modification layer, the shorter and fatter spikes observed on SiO_2/porous low-*k* surface (Figure 3.7d) need not pierce the whole Ta barrier but could lead to the development of cracks in the barrier layer. After subsequent thermal cycles (*e.g.* thermal processing at 200°C - 400°C during fabrication process or BTS at 350°C, 0.5 MV for 1 h), the mechanical stress from Cu trench may enlarge the cracks or even rip the barrier out entirely. As shown in Figure 3.10d, this destructive failure of sidewall barrier would result in serious Cu penetration into the porous low-*k* IMD with a catastrophic sidewall profile distortion.

For the SiN/Ta and SiO_2/Ta bilayer barriers, the uncompleted pore sealing leaves a possible path on the sidewall for Ta and (subsequently) Cu penetration into porous low-*k* IMD. Therefore, high-resistivity and high-*k* compounds may be formed at the barrier/porous IMD interface and contribute to higher Cu line resistance and/or line-to-line capacitance measured for SiN/Ta barrier and SiO_2/Ta barrier, as shown in Figure 3.3. Since the use of SiO_2 modification layer actually exacerbated the weakness of the sidewall barrier rather than sealing the porous low-*k* surface, the *RC* characteristics for SiO_2/Ta barrier degraded significantly due to the huge amount of

metal residue present in porous IMD as well as the catastrophic sidewall distortion of the profile as shown in Figure 3.10d.

3.6 Reliability Improvement on Electromigration Performance

In order to investigate the effects of bilayer barrier on interconnect reliability, wafer-level electromigration (EM) test was performed in our studies. Figure 3.11 shows a American Society for Testing and Materials (ASTM) standard EM test structure which was used in our work. Table 3.4 shows the dimensions of line width, spacing and length of this EM test structure. The EM testing was conducted at 250°C with a current density of 3 MA/cm^2. The temperature used here is not so high to avoid any destructive influence on the porous low-*k* IMD (due to the weak chemical properties of organic porous ultra low-*k* material) before the EM failure happened. The interconnect structures were considered to have failed when the line resistance increased by 100 %. Not all barriers are suitable for the EM test. The samples with SiN/Ta or SiO_2/Ta bilayer barrier show a rapid failure just at the beginning of the test. Considering the electrical performance improvements achieved, the major work here is to investigate EM performance of Cu/porous ultra low-*k* interconnects with conventional PVD TaN/Ta barrier and a-SiC:H/Ta bilayer barrier.

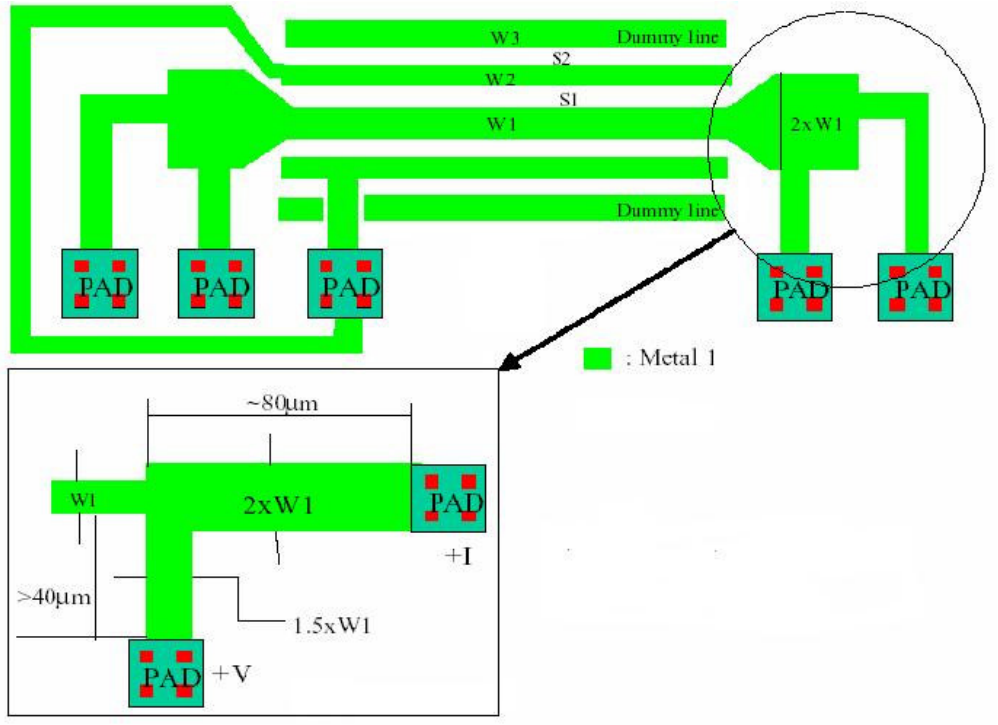

Figure 3.11 ASTM standard EM test structure used in this work.

Table 3.4 Dimensions of major parameters of the EM test structure.

W1 (µm)	Length (µm)	S1 (µm)	W2 (µm)	S2 (µm)	W3 (µm)
0.28	800	0.28	0.28	0.5	1.0

The interconnect structures located at the edge and center of the wafer will have different electromigration and stress migration performance due to process non-uniformity as well as equipment limitation [25]. As it is well known, the EM lifetime of Cu interconnects is strongly dependent on the surface morphology of Cu/barrier interface [26]. But it is hard for the Ta barrier deposited at the wafer edge to have an equal conformity as that at the wafer center due to the nature of the

PVD tools [25]. Therefore the diffusion barrier at the edge of the wafer will have lower adhesion strength with the Cu line, leading to a shorter EM lifetime compared with that at the wafer center. Figure 3.12 shows a typical line resistance *vs.* stress time characteristic, tested at 250°C and 3 MA/cm^2, of Cu/porous ultra low-*k* interconnects with different sidewall barriers. We can see that the EM lifetime of interconnects from the wafer center is almost 1 order higher than that of interconnects from the wafer edge.

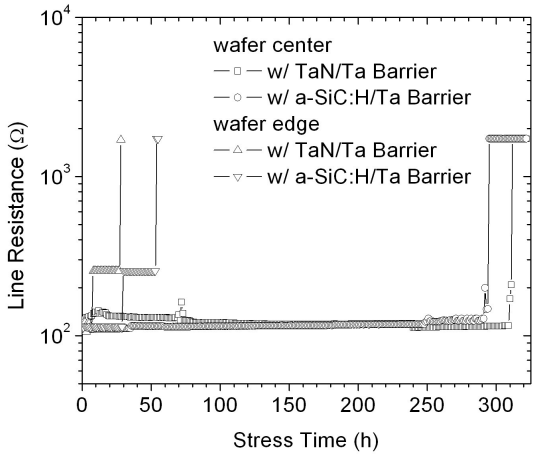

Figure 3.12 Typical line resistance *vs.* stress time characteristics of Cu/porous low-*k* interconnects with conventional PVD TaN/Ta barrier and a-SiC:H/Ta bilayer barrier, tested at 250°C and a current density of 3 MA/cm^2.

In spite of the fact that testing was performed at the edge or center of the wafer, there is a dependence of EM lifetimes on the kind of sidewall barrier used. At the wafer edge, the non-uniformity issue of PVD metal barrier is more serious. Therefore the a-SiC:H underlying layer is more desirable for good quality of PVD metal barrier as well as the surface morphology of Cu/barrier interface, which will result in a better EM performance of interconnects. As shown in Figure 3.13, there

is a clear trend in EM failure distribution when testing at the wafer edge: interconnects with a-SiC:H/Ta bilayer barrier showed longer EM lifetimes than those with PVD TaN/Ta barrier. On the other hand, the process variables have been optimized in order to achieve the best conformity of the PVD metal barrier at the center of the wafer. Thus the influence of a-SiC:H underlying modification layer on the EM lifetimes of interconnects here was not obvious as that shown at the wafer edge. But improvements on EM lifetimes still could be found by using a-SiC:H/Ta bilayer sidewall barrier, when looking at the absolute change of mean time to failure values (Table 3.5). Figure 3.14 shows the voids formed in the Cu interconnect line, which is responsible for the EM failure by Focused Ion Beam (FIB) technique.

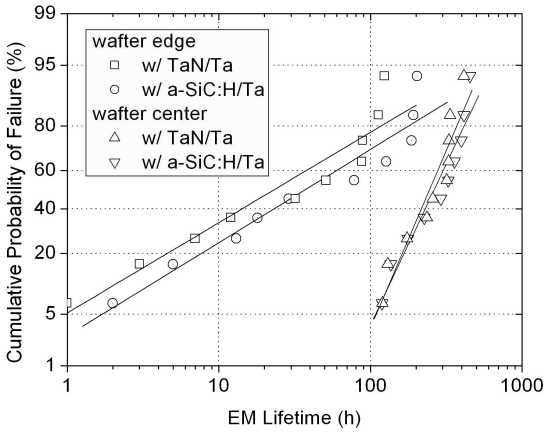

Figure 3.13 Cumulative Distribution of EM failure of Cu/porous ultra low-*k* interconnects with conventional PVD TaN/Ta barrier and a-SiC:H/Ta bilayer barrier, tested from wafer edge and center**.**

Table 3.5 Mean time to failure (MTF) due to EM degradation of Cu/porous ultra low-k interconnects with different sidewall barriers, calculated from Weibull Distribution of EM failures.

	MTF at wafer edge (h)	MTF at wafer center (h)
w/ TaN/Ta Barrier	107	264
w/ a-SiC:H/Ta Barrier	165	299

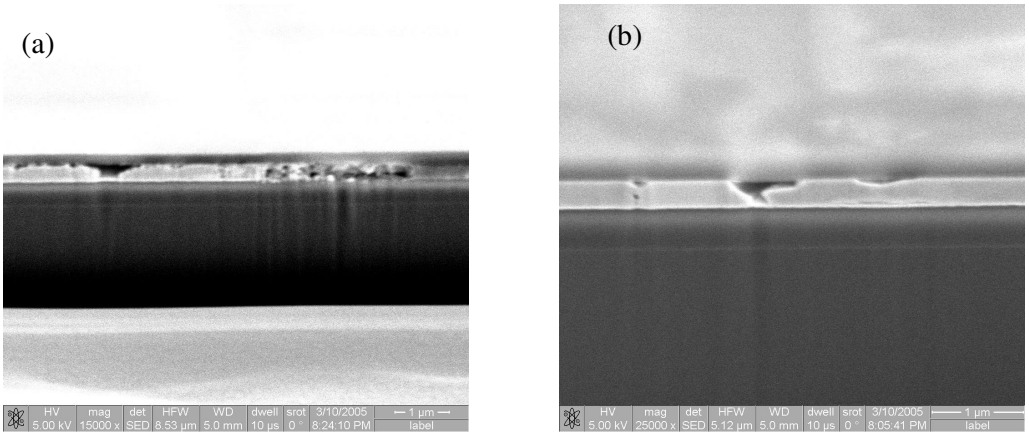

Figure 3.14 FIB cross-section images of EM failure for Cu/porous ultra low-*k* interconnects with a) conventional PVD TaN/Ta barrier, and b) a-SiC:H/Ta bilayer barrier.

The reliability concerns, mostly in EM and stress migration performance, indicated that it is not yet practical to employ current Cu/porous ultra low-*k* integration scheme. This is mostly due to the poor thermal conductivity and mechanical properties of the porous dielectric [27]. Although the EM results shown here are far from meeting the criteria for real-life IC operation, they demonstrate that the using a-SiC:H/Ta bilayer barrier do not introduce any unwanted adhesion issue at

sidewall interface,.and therefore do not compromise EM performance of Cu/ultra low-*k* damascene interconnects.

3.7 Conclusions

Dielectric/metal bilayer structures with different dielectric layers, *i.e*. a-SiC:H, SiN and SiO_2, were integrated as sidewall diffusion barriers in Cu/porous ultra low-*k* damascene interconnects. Compared with the conventional PVD TaN/Ta sidewall barrier, the a-SiC:H/Ta bilayer structure was found to improve the electrical performance and reliability against thermal and/or electrical stress, for Cu/porous ultra low-*k* damascene interconnects significantly. The use of a-SiC:H/Ta bilayer also resulted in a reduction of both line resistance and line-to-line capacitance, which is extremely desirable in current interconnect technology. Detailed investigations on the surface morphology and barrier integrity indicated that these achievements are due to the successful surface modification of the porous low-*k* IMD by the thin PECVD a-SiC:H layer. AFM, SIMS and TEM analyses showed that a-SiC:H dielectric layer, in addition to being a good barrier against Cu diffusion, could effectively smoothens the rough surface of porous low-*k* IMD, minimize the defect sites in the barrier layer and hence reduce the possibilities of barrier failure. However, the use of dielectric layers such as SiN or SiO_2 in the dielectric/metal sidewall barrier offer no improvement. Instead, the sidewall barrier and hence the interconnect performance and reliability are severely degraded due to particulate contamination issues.

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Chapter 4. Process Optimization for a-SiC:H/Ta Bilayer Sidewall Barrier

4.1 Introduction

In Chapter 3, we demonstrated that the bilayer structure of a-SiC:H/Ta was a more efficient sidewall diffusion barrier for Cu/porous ultra low-k interconnects, in terms of electrical performance and reliability. The major reason is due to the successful surface modification and pore-sealing by the PECVD a-SiC:H dielectric layer. However, when it is integrated into realistic Cu BEOL process schedule, one question may be raised from the manufacturing side, *i.e.*, what is the optimized process condition for this bilayer barrier fabrication, in terms of PVD Ta metal barrier and PECVD a-SiC:H dielectric components? Should we use a thinner or thicker a-SiC:H modification layer to achieve better interconnect performance, without compromising the effective k value of interconnect structures? On the other hand, as the feature size of Cu/low-k and Cu/ultra low-k interconnects continuously shrinks down beyond 0.13 μm, there is a need to minimize the thickness of the high-resistivity metal barrier in order to match the (more and more) challenging requirement of overall interconnects resistance [1]. It was reported that PECVD a-SiC:H film is a good dielectric barrier material against Cu diffusion/drift [2], [3]. Accordingly we want to know how efficient the a-SiC:H/Ta bilayer barrier is to prevent Cu penetration especially when thermal stress and/or electrical stress are applied, compared with the conventional PVD Ta metal barrier. Based on that, we would like to explore the possibility of using a bilayer barrier structure of a

thicker PECVD a-SiC:H dielectric layer together with a correspondingly thinner PVD Ta metal barrier as the sidewall barrier, in order to reduce the contribution of the high-resistivity metal barrier to the overall interconnect resistance. Therefore further investigation in this area is necessary, in terms of the barrier efficiency of a-SiC:H/Ta bilayer structure against Cu diffusion as well as the influence of bilayer barriers with different dielectric and metal composites on the electrical and reliability characteristics of Cu/ultra low-*k* interconnects.

4.2 Experimental Setup and Barrier Coverage on the Sidewall

The samples were fabricated in a 0.13 μm Cu/Porous-SiLK™ single damascene process. Two kinds of bilayer barrier structures were studied in this work. One is 100 Å thick a-SiC:H layer followed by 250 Å thick PVD Ta layer while the other is 200 Å thick a-SiC:H layer followed by 125 Å thick PVD Ta layer. The multi-stack TaN/Ta sidewall barrier of 125 Å PVD TaN followed by 125 Å PVD Ta was also fabricated for comparison purposes. After the CMP process was done, a 500 Å thick PECVD SiCN capping layer and 3000 Å thick PECVD SiO_2 passivation layer were deposited on the top to prevent Oxygen permeation from air. Blanket samples of PVD TaN/Ta barrier and a-SiC:H 100 Å/Ta 250 Å bilayer barrier were also fabricated on Porous-SiLK™ substrates and coated by Cu layer for physical characterization.

The interconnect structures for electrical tests are identical to those used in Chapter 3: standard serpentine and comb structures of ~1 m length, with a 0.18 μm line width and line-to-line space, was used for Cu line resistance, line-to-line capacitance and leakage current measurements. I-E characteristics were measured

on a 0.192 m long serpentine/comb sandwich structure, with a 0.24 μm line width and line-to-line space.

It should be noted that the thickness of the barrier layers shown here corresponds to recipe thickness which is measured on the blanket substrate during recipe setup. The a-SiC:H and Ta deposition recipes for bilayer barrier thickness were modified from the normal recipes used in a pilot research line. Due to the non-linear deposition rate at the initial deposition stage and the non-optimized process conditions (e.g. within wafer variation and sidewall coverage, etc.) for the new recipes, the actual film thickness on the trench sidewalls is expected to be different. The barrier thickness on the sidewall is also dependent on the equipment capability of the PVD and PECVD tools. The rough surface of porous low-*k* IMD, depending on its porosity, may further exacerbate the step-coverage issue of barrier layer deposited on it, especially on the trench/via sidewall [4], [5]. The recipe film thickness and corresponding actual film thickness on the sidewalls for the barriers used in our work are shown in Table 4.1, measured from cross-section TEM images. The sidewall barrier thickness varied depending on the measurement location (*e.g.* wafer center & edge), due to within wafer process variation. The unclear interface between TaN (or a-SiC:H) barrier and porous low-*k* IMD also leads to the measurement inaccuracy for TEM microscopy, when the actual film thickness is quite small (<50 Å). Therefore, a large range of measured sidewall barrier thickness was seen.

In the case of the bilayer barrier of a-SiC:H 200 Å/Ta 125 Å structure, the actual thickness on the trench sidewall measured by TEM is ~60 Å for a-SiC:H and ~53 Å for Ta, respectively. For the bilayer barrier of a-SiC:H 100 Å/Ta 250 Å

structure, the sidewall coverage is 14~28 Å for a-SiC:H and ~71 Å for Ta, respectively. It is not practical to overcome this sidewall step-coverage issue merely by increasing the thickness of the Ta and/or a-SiC:H layers in the deposition process because this change will also increase the thickness of the barrier films deposited on the top of the trench as well as the via bottom simultaneously, leading to extra difficulties in the CMP process as well as etch-back process for removing the dielectric layer on the via bottom in a typical dual damascene process.

That the sidewall coverage of the same a-SiC:H layer and PVD Ta barrier on different low-*k* IMD may vary, depending on the deposition conditions and porosity of the low-*k* materials. The process fine tune to achieve better sidewall coverage of bilayer barrier is possible by further optimizing the process conditions. In this thesis, we prefer to use recipe thickness for the bilayer barrier structures rather than the actual sidewall thickness (measured from a limited number) of samples by cross-section TEM.

Table 4.1 Actual film thickness on the of different sidewall barriers.

Barrier Structures		Actual Film Thickness on the Sidewall
PVD TaN/Ta	TaN 125 Å Ta 125 Å	TaN/Ta 30~50 Å
a-SiC:H/Ta bilayer	a-SiC:H 100 Å Ta 250 Å	a-SiC:H 14~28 Å Ta 71 Å
	a-SiC:H 200 Å Ta 125 Å	a-SiC:H 60 Å Ta 53 Å

4.3 Enhancement on Barrier Resistance against Cu penetration by a-SiC:H Dielectric Layer

Figure 4.1 shows the Cu penetration profiles in the different barrier layers on blanket Porous-SiLK™ films by SIMS, after thermal and/or electrical stress. The Cu/Ta barrier interface is defined as the location where the Cu intensity dropped to 10 % of the bulk intensity in Cu film. The Ta/dielectrics interface (when a-SiC:H/Ta bilayer barriers was used), or TaN/porous IMD interface (when TaN/Ta barrier was used) were defined as the locations where the Ta intensity dropped to 10 % of the bulk intensity in the Ta (or TaN) barrier film. The interface between a-SiC:H layer and porous low-*k* IMD is not defined due to the technique limitation mentioned in Section 3.5.1. The secondary ion counts of Cu in each sample were normalized to Ta signal to minimize the measurement inaccuracy due to knock-in effect and matrix effect usually observed in theTOF-SIMS technique [6]-[8].

As mentioned before, PVD TaN/Ta barrier has a better resistance against Cu diffusion than either single layer of either PVD Ta or TaN [9], [10], and was shown to have a two layer structure, the top α-Ta layer with texture preferences of (110) and (211) and the bottom Ta(N) layer with an amorphous structure [11], [12]. When the stress condition is not too severe (BTS at 350°C, 0.5 MV/cm for 1 h), there is no noticeable difference between the Cu penetration profiles in either the TaN/Ta barrier or the a-SiC:H/Ta bilayer barrier (Figure 4.1a). However, when more severe stress conditions are applied, *e.g.* increasing the applied electrical field and stress duration (BTS at 350°C, 2 MV/cm for 2 h) or burn-in test at 200°C for 48 h in air environment, a notable divergence is observed. The detected Cu intensities in Ta barrier dropped when moving towards the Ta/a-SiC:H interface and porous IMD, when a-SiC:H/Ta bilayer barrier was used (Figure 4.1b,c). One reason is the beneficial effects of the use of a-SiC:H layer on the quality and surface morphology of the PVD Ta barrier top of it. The other reason is due to the ability of the a-SiC:H film itself to act as an efficient barrier against Cu drift/diffusion, even at elevated temperature with high electrical stress [3]. Therefore, even a thin a-SiC:H layer (~100 Å), in addition to the PVD Ta barrier, can enhance the total barrier performance against Cu penetration considerably. We believe that the ability of the a-SiC:H/Ta bilayer barrier to prevent Cu diffusion may be further enhanced by using a thicker a-SiC:H layer and reducing the thickness of the PVD Ta layer so that the total barrier thickness is roughly same and the overall interconnect resistance could be further reduced.

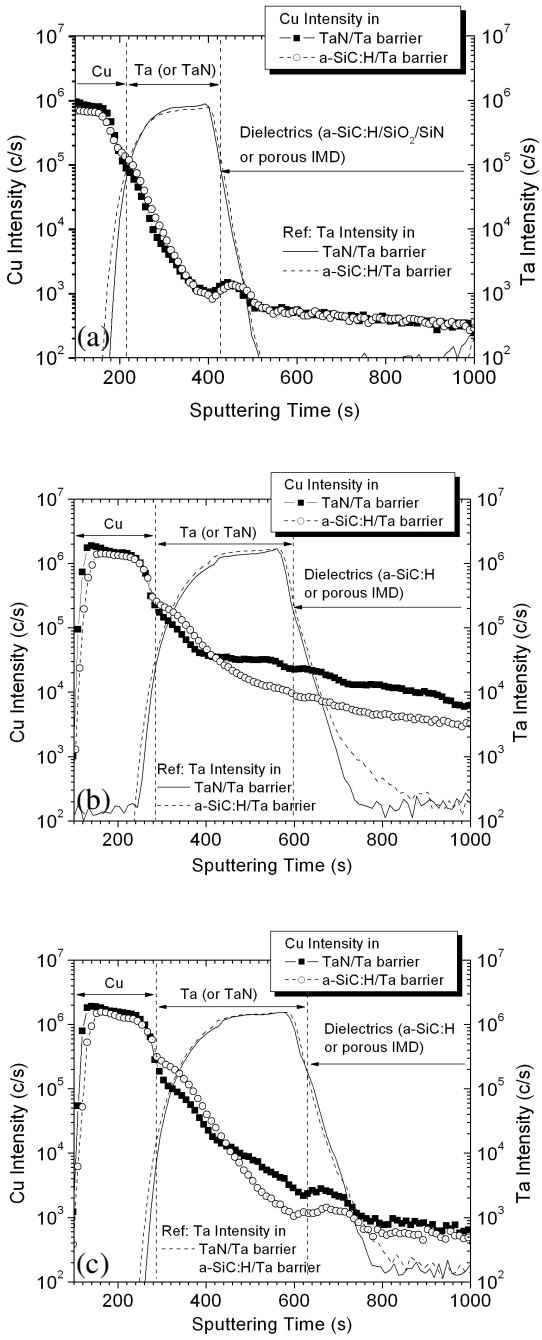

Figure 4.1 Comparison of Cu penetration profiles in 250 Å PVD multi-stack TaN/Ta barrier and a-SiC:H 100 Å/Ta 250 Å bilayer barrier on Porous-SiLK™: a) after BTS at 350°C, 0.5 MV/cm for 1 h, b) after BTS at 350°C, 2 MV/cm for 2 h, and c) after thermal stress at 200°C for 48 h.

On the vertical trench sidewall of the damascene structure, the situation is similar but maybe not be the same as that on the blanket samples. As shown in Figure 4.2, although PECVD tools offer a considerable step coverage for the a-SiC:H layer, the coverage of 200 Å PECVD a-SiC:H layer on the sidewall is still a fraction of its recipe thickness (~30%). As mentioned earlier, it is not possible to increase the thickness of barrier layer on the sidewalls; this would mean an even thicker barrier layer on the top surface of damascene structures and would bring additional difficulties for the CMP process. The process fine tune to achieve better sidewall coverage for barrier deposition recipe is possible in the industrial manufacturing, which is out of the discussion area of this thesis.

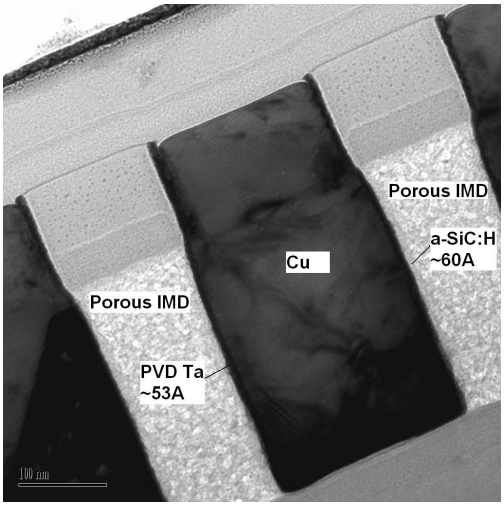

Figure 4.2 TEM image of actual barrier coverage at the trench sidewall for the bilayer structure of PECVD a-SiC:H 200 Å followed by PVD Ta 125 Å. Note the significant difference in the thickness of the bilayer on the sidewall (only 60 Å of a-SiC:H compared to the recipe thickness of 200 Å and 53 Å of Ta compared to the recipe thickness of 125 Å).

4.4 Electrical and Reliability Performance of Different a-SiC:H/Ta Bilayer Barriers

4.4.1 *RC* Characteristics

Figure 4.3 shows the distribution of Cu line resistance and line-to-line capacitance measured on Cu/porous ultra low-*k* interconnects with PVD TaN/Ta barrier and different bilayer barrier structures. The slopes of the individual curves are a measure of the spread in the experimental data. The higher the slope, the smaller is the variation in the measured electrical parameter. By using the bilayer barrier with a thinner PVD Ta barrier (125 Å) and a thicker a-SiC:H layer (200 Å), the total Cu line resistance could be further reduced as shown in Figure 4.3a. As shown in Figure 4.2, the Cu line width is much larger than the drawn value of 0.18 μm, due to the damascene etch profile on porous low-*k* IMD, Therefore, the ~ 60 Å a-SiC:H layer thickness on both sidewalls is too small for Cu line narrowing and is unlikely to affect the line resistance. The reduction in Cu line resistance is likely due to the use of thinner PVD Ta barrier in a-SiC:H 200 Å/Ta 125 Å bilayer barrier, as well as an even better pore-sealing on the sidewall by thicker a-SiC:H layer and subsequently an even more conformal deposition of the PVD Ta barrier.

Moreover, the use of thicker a-SiC:H sealing layer would achieve an even better pore-sealing on the sidewall. This subsequently leads to a more conformal deposition of the PVD Ta barrier, as well as a "clear" interface between barrier/porous low-*k* IMD without forming any high-resistivity and/or high-*k* oxide compounds (*e.g.* Cu or Ta oxide). The end result is an even better *RC* characteristic by using the bilayer barrier of thicker a-SiC:H layer (200 Å) and correspondingly

thinner Ta barrier (125 Å), compared with PVD TaN/Ta barrier and the bilayer barrier of a-SiC:H 100 Å/Ta 250 Å.

As mentioned in Section 3.3.2, the use of thin and thick a-SiC:H layers on the sidewall may affect the line-to-line capacitance in two opposite ways - the increase in IMD spacing will decrease the capacitance while the additional a-SiC:H layer with higher k value (~4.9) will increase k_{eff}, and therefore the capacitance, of interconnects. The calculated k_{eff} of overall inter metal layer dielectrics with different sidewall barriers are listed in Table 4.2, using the same method that was used in Section 3.3.2 by considering the fringe capacitance effects. For a thin a-SiC:H layer (< 30 Å) on the sidewall, its influence on k_{eff} is negligible. But for a-SiC:H layer more than 60 Å thick, the influence of higher k value a-SiC:H layer on the line-to-line capacitance may have to be considered. This may partialy contribute to the line-to-line capacitance characteristic in Figure 4.3b and the effective dielectric constant calculated in Table 4.2 for bilayer barrier with thicker a-SiC:H layer.

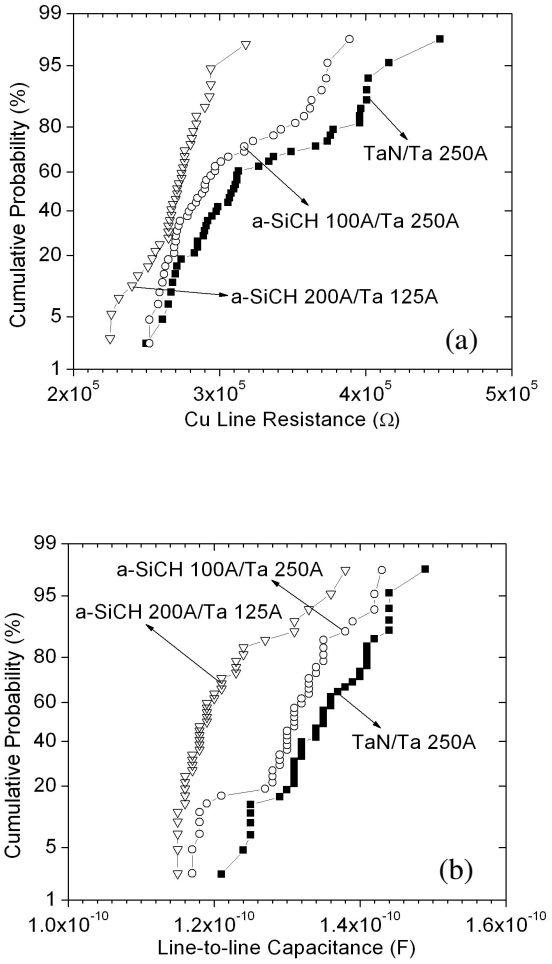

Figure 4.3 Comparison of a) Cu line resistance, and b) line-to-line capacitance of Cu/porous ultra low-*k* interconnects with different sidewall barriers.

Table 4.2 Calculated effective dielectric constant k_{eff} from line-to-line capacitance with different sidewall barriers.

Sidewall barriers	Mean of line-to-line Capacitance (pF)	Measured IMD spacing (nm)	Calculated k_{eff}	
			(excluding C_{fringe})	(including C_{fringe})
PVD TaN/Ta 250 Å	135.3	147.1	3.745	2.497
a-SiC:H 100 Å Ta 250 Å	126.9	151.6	3.620	2.413
a-SiC:H 200 Å Ta 125 Å	120.5	156.5	3.3551	2.367

4.4.2 Electrical Performance and Thermal Stability

When looking at the electrical characteristics before and after long time thermal stress (Figure 4.4 and Figure 4.5), it was found that the two kinds of a-SiCH/Ta bilayer barriers with different thickness proportions have a similar electrical performance before any thermal stress. However after long time thermal stress in air ambient, a clear difference emerges in both I-E characteristics and line-to-line leakage current distribution. The beneficial effects of thicker a-SiC:H layer begin to emerge. The line-to-line leakage current of samples with bilayer barrier of thin a-SiC:H (100 Å) modification layer and standard Ta (250 Å) barrier remains more than one order of magnitude lower than that of the conventional PVD TaN/Ta barrier before any thermal stress. But after a burn-in test at 200°C for 120

h, the leakage current of this a-SiC:H 100 Å/Ta 250 Å bilayer barrier shows a large increase and shifts closer to that of PVD TaN/Ta barrier after identical stress (Figure 4.4b). Although this drawback did not induce any electrical failure, the E_{BD} of a-SiC:H 100 Å/Ta 250 Å bilayer barrier dropped to < 1 MV/cm, and its I-E characteristic significantly deteriorated (a large increase in leakage current even at low electrical fields), similar to that of PVD TaN/Ta barrier (Figure 4.5b). The sample with bilayer barrier of thicker a-SiC:H (200 Å) and thinner Ta (125 Å) layers exhibits only a slight change in the I-E characteristic and still has a considerable high E_{BD} of ~2.3 MV/cm. Clearly, the use of thicker a-SiC:H and correspondingly thinner Ta barrier achieved a better thermal stability than that of a-SiC:H 100 Å/Ta 250 Å bilayer barrier.

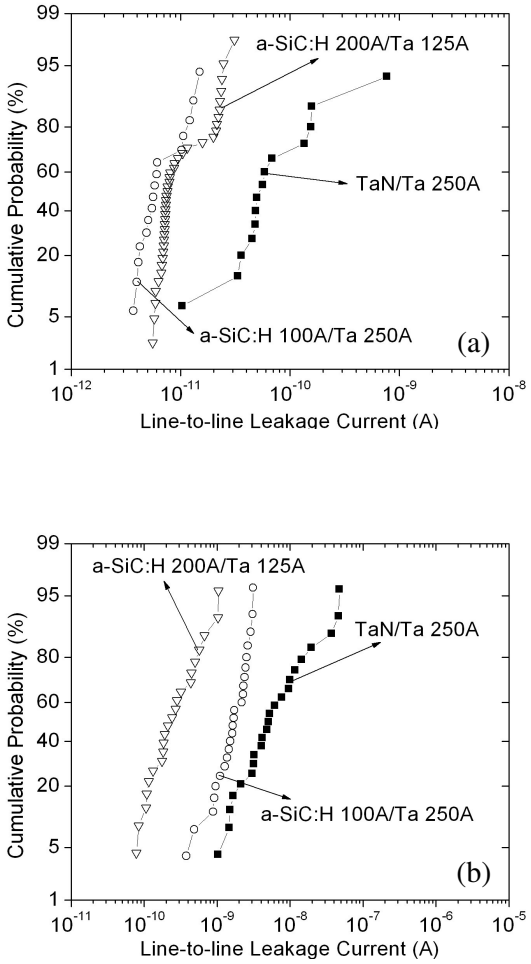

Figure 4.4 Distribution of the line-to-line leakage current of Cu/porous ultra low-*k* interconnects, measured at 5 V, with different sidewall barriers: a) as deposited, and b) after thermal stress at 200°C for 120 h.

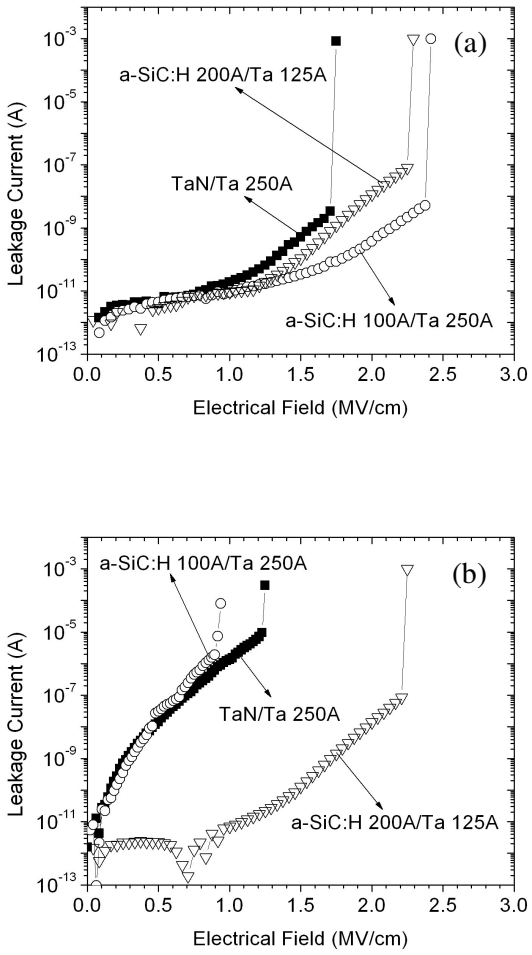

Figure 4.5 I-E characteristics of Cu/porous ultra low-*k* interconnects with different sidewall barriers: a) as deposited, and b) after thermal stress at 200°C for 120 h.

4.4.3 Physical Analysis of Electrical Degradation after Burn-in Test

The physical evidence for the serious electrical degradation after the burn-in test is shown in Figure 4.6. After the burn-in test at 200°C for 120 h, Cu was found to punch through the PVD TaN/Ta sidewall barrier and leaked out into the porous low-*k* IMD, which led to its poorer electrical performance (Figure 4.6a). Similarly, the TEM and EELS analysis indicated that this long time thermal stress also made the Cu begin to penetrate through the a-SiC:H 100 Å/Ta 250 Å bilayer barrier at the sidewall (Figure 4.6b). However this Cu penetration is at an initial stage and is not prevalent yet (notice the scale of the TEM image), and not significant enough to cause a catastrophic interconnect failure. It would not yet form a destructive conductive path in the porous low-*k* IMD, but would still result in the increase of the leakage current, as well as a large slope in I-E curve and low breakdown strength, which are similar to those of PVD TaN/Ta barrier. In the case of bilayer barrier with thicker a-SiC:H layer (200 Å) and thinner PVD Ta layer (250 Å), Cu was not able to penetrate into the IMD after identical thermal stress. A clear interface at the sidewall was maintained (Figure 4.6c), and no Cu penetration was detected by EELS mapping, which is consistent with the stable electrical characteristics of the samples with a-SiC:H 200 Å/Ta 125 Å bilayer barrier as shown in Figure 4.4b and Figure 4.5b. This clearly demonstrates that the thicker a-SiC:H layer with a correspondingly thinner Ta layer could act as an even more efficient “buffer” layer between Cu and porous low-*k* IMD to prevent the Ta and subsequent Cu diffusion into porous low-*k* IMD. This is due to the excellent barrier properties of the a-SiC:H layer against Cu diffusion and its role in the enhancement of the quality of the PVD Ta barrier deposited on top of it [13], [14],

thus enabling the reduction in the PVD Ta layer thickness without any compromise in the overall sidewall barrier performance.

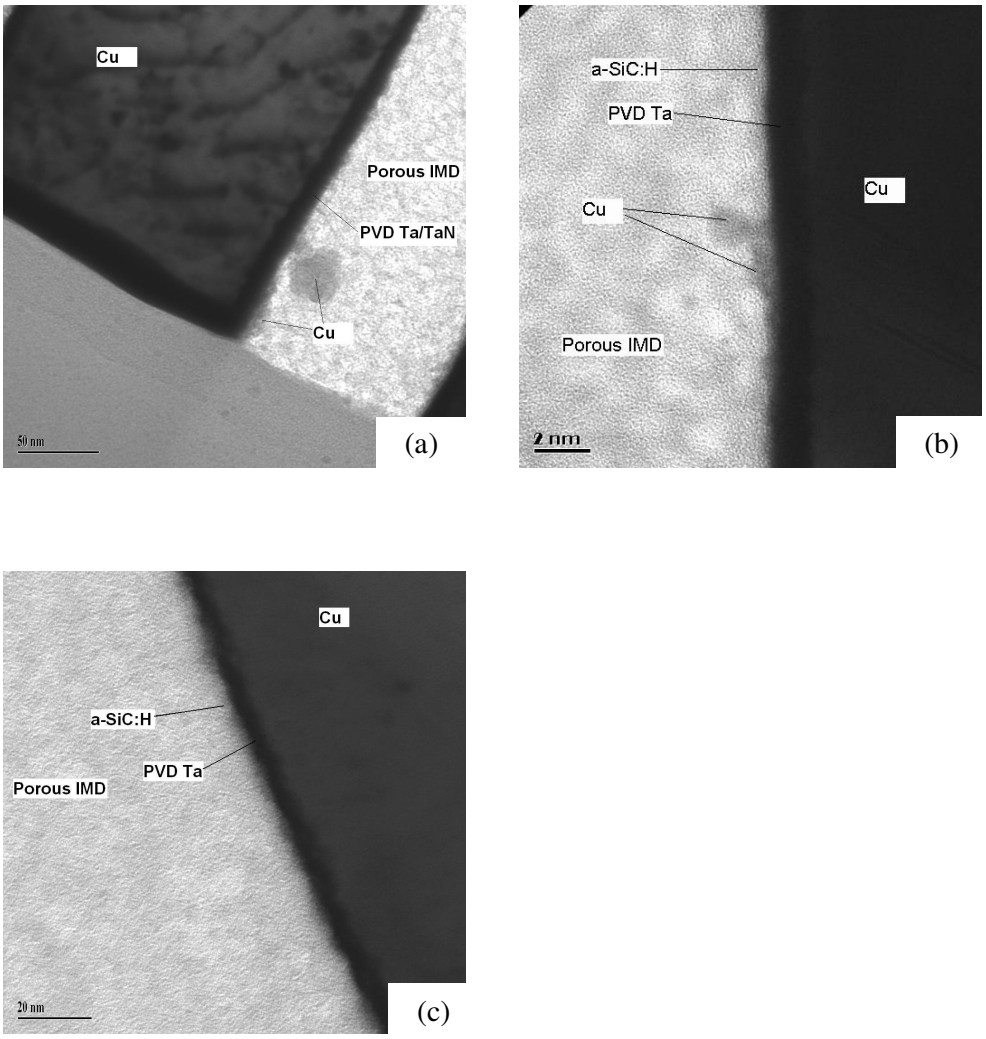

Figure 4.6 TEM images of sidewall profile after thermal stress at 200°C for 120 h with a) conventional 250 Å PVD TaN/Ta barrier, b) a-SiC:H 100 Å/Ta 250 Å bilayer barrier, and c) a-SiC:H 200 Å/Ta 125 Å bilayer barrier.

A detailed reliability study of all the three types of barriers was carried out. These studies will be discussed separately in Chapter 5, associated with a pseudo-

breakdown behavior that was observed in both PVD TaN/Ta and a-SiC:H 100 Å/Ta 250 Å bilayer barrier structures.

4.5 Conclusions

The use of a-SiC:H/Ta bilayer sidewall barrier improves the electrical performance of Cu/porous ultra low-*k* interconnects due to the successful surface modification by the PECVD a-SiC:H layer to seal the porous low-*k* IMD surface. When looking at the barrier efficiency against Cu diffusion/drift, the a-SiC:H/Ta bilayer barrier exhibited a reduced Cu penetration profile compared to the PVD TaN/Ta barrier when high stress conditions were applied, *e.g.* long time burn-in test in air ambient or BTS at high temperature (~350°C) with high electrical field. Our studies indicate that the a-SiC:H layer is the more "powerful" component in the bilayer barrier. This good ability of the PECVD a-SiC:H dielectric makes it is possible to implement a bilayer structure of thicker a-SiC:H layer and correspondingly thinner PVD Ta barrier as an even better robust sidewall barrier. Cu/porous ultra low-*k* interconnects with such a bilayer barrier exhibit an even better performance in terms of electrical characteristics, thermal stability and barrier integrity, compared to the bilayer barrier consisting of a thinner a-SiC:H layer and thicker PVD Ta barrier as well as PVD TaN/Ta barrier. The use of thicker a-SiC:H and correspondingly thinner Ta a-SiC:H/Ta bilayer barrier also showed positive effects in terms of a reduction in both the overall Cu line resistance and line-to-line capacitance, which are crucial and highly desirable for future Cu/ultra low-*k* interconnect technologies.

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Chapter 5. Pseudo-Breakdown Phenomenon and Barrier Integrity in Cu/Porous Ultra Low-*k* Interconnects

5.1 Introduction

In the Cu/low-*k* and Cu/ultra low-*k* damascene process integration, major concerns are focused on their reliability issues, mostly due to the fast diffusion of Cu as well as the poor resistance against Cu migration of this kind of low-*k* dielectric [1]. When porosity is introduced into dielectrics (porous ultra low-*k* dielectric materials) to achieve further reduction in the *k* value, this problem becomes more serious. Cu drift/diffusion processes in such Cu/porous low-k interconnects, their deterioration mechanisms and subsequent influence on interconnect performance and reliability are still not well-understood. An interesting pseudo-breakdown behavior in the Cu BEOL process has been reported [2] and also observed in our experiments, which may be helpful in understanding the Cu drift/diffusion induced low-*k* dielectrics degradation. In this Chapter, we will investigate this pseudo-breakdown phenomenon as well as the influence of barrier integrity on dielectrics and hence the interconnect reliability.

5.2 Experimental Setup

The fabrication process is similar to the process that we introduced in Chapter 3. We used 0.13 μm Cu/Porous-SiLK™ single damascene process with a SiO_2 hard mask. After the trench formation, three kinds of diffusion barriers were deposited on the sidewall: conventional PVD TaN/Ta metal barrier (125Å TaN followed by

125 Å Ta), standard PVD Ta barrier (250 Å) with a thin a-SiC:H underlying layer (< 100 Å), and an improved bilayer barrier consisting of a thinner PVD Ta (125 Å) barrier with a correspondingly thicker a-SiC:H (~ 200 Å) dielectric layer, identical to the dielectric/metal bilayer barrier we used in Chapter 4. The a-SiC:H layer was deposited by the PECVD method using Applied Material Centura™ 5200 PECVD system. The TaN/Ta, Ta barrier and subsequent Cu seed layer were deposited using the Applied Material Endura™ HDP PVD system with the SIP technology. Due to processing limitations, it was not possible to have all the three types of diffusion barriers of identical thickness, either at the trench/via bottom or at the top surface. However, it should be noted that the actual barrier thickness on the sidewall is only a small fraction (20 – 40 %) of that deposited on the trench/via bottom and the top surface. This was already addressed in Chapter 4. As a result, the barrier thickness on the sidewall was roughly the same for all the three types of barriers used in this study.

The test structure is a 0.192 m long serpentine/comb sandwich structure, with a 0.24 μm line width and spacing. There are two sets of identical structures in each sample for electrical tests: one set is used for time dependent dielectric breakdown (TDDB) tests at elevated temperature (150°C - 300°C) with an electric field of 0.5 - 1 MV/cm while the other set is for thermal stress only, *i.e.,* not subjected to any electric field during TDDB tests. The TDDB testing condition is selected in a low temperature range, but compromising to the overall testing time and cost accordingly to each set of samples with different sidewall barriers. And the applied electrical field is selected to be closed with the worst IC operation condition at 0.5 MV/cm.

5.3 Pseudo-Breakdown Behavior in Cu/Porous Ultra Low-*k* Interconnects

5.3.1 Pseudo-Breakdown Phenomenon during TDDB Tests

To investigate the Cu transport mechanism in porous ultra low-*k* IMD, leakage current *vs.* stress time (I-t) characteristics were monitored during TDDB tests. Figure 5.1a shows the typical I-t characteristics for conventional PVD TaN/Ta barrier at 200°C with an electric field of 0.5 MV/cm. Time-to-Failure is defined as the time at which the line-to-line leakage current shows an abrupt jump and is limited by the constant current compliance of the power supply [3]. The pseudo-breakdown behavior occurred during the TDDB test. A rapid increase in current of 2 to 3 orders of magnitude, followed by some degree of noise or current fluctuation before the eventual breakdown was always seen in the I-t plot.

When we looked at the I-t characteristics of samples with the bilayer structure of standard PVD Ta barrier (250 Å) with a thin a-SiC:H underlying layer (< 100 Å), it was found that TDDB lifetimes were significantly extended. However, the pseudo-breakdown behavior was not eliminated (Figure 5.1b). An identical rapid current increase and current fluctuation was always observed during the TDDB test at 150°C - 300°C and electric field of 0.5 - 1 MV/cm, for both conventional PVD TaN/Ta barrier or a-SiC:H 100 Å /Ta 250 Å bilayer barrier.

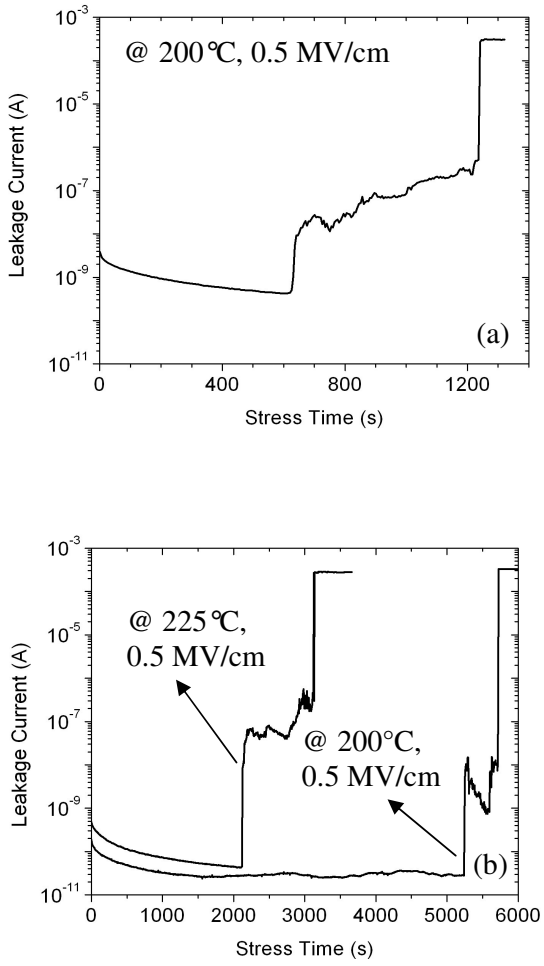

Figure 5.1 Current-time (I-t) characteristics of Cu/porous ultra low-*k* interconnects with a) conventional PVD TaN/Ta barrier at 200°C, 0.5MV/cm; and b) PVD Ta barrier and a-SiC:H modification layer (a-SiC:H 100 Å/Ta 250 Å) at 200°C and 225°C, 0.5 MV/cm.

5.3.2 Electrical Characteristics after Pseudo-Breakdown Occurrence

Electrical tests indicate that the interconnect structures are still functional if the TDDB test was stopped immediately after this pseudo-breakdown occurred. Figure 5.2 shows the post-stress leakage current (I) *vs.* applied electric field (E) characteristics measured after pseudo-breakdown occurrence, either with or without an electrical field applied during TDDB tests. There is a rapid increase in the leakage current when the applied electric field is increased during the I-E measurements, associated with a much smaller breakdown strength compared to samples without any thermal and electrical stress. The PVD TaN/Ta barrier exhibits significant degradation after thermal stress only (Figure 5.2a). The addition of an electric field during thermal stress further exacerbates the degradation. We believe there is significant Cu penetration into porous low-*k* IMD with thermal and/or electrical stress, leading to degradation and eventual failure of interconnect structure. However, for bilayer barrier with standard PVD Ta barrier and thin a-SiC:H modification layer, there is virtually no degradation after thermal stress only (Figure 5.2b). PVD TaN/Ta barrier exhibits serious discontinuities and localized defects if directly deposited on the sidewall of porous low-*k* IMD. This is because the sidewall of the porous low-*k* IMD has a high surface roughness, leading to the Ta penetration and consequent discontinuity issues as described in Chapter 3. Thus, merely applying a thermal stress could cause significant Cu diffusion into the porous low-*k* IMD through the weak points in the barrier layer. But such a Cu diffusion is no longer made possible by thermal stress only in the modified PVD Ta barrier with the thin a-SiC:H underlying layer. The reason is the improved barrier integrity due to the presence of thin a-SiC:H modification layer. However, it is well known that Cu diffusion/drift could be significantly enhanced

by the presence of an electrical field [4]. When an electrical field was applied during the TDDB tests, this PVD Ta barrier with the thin a-SiC:H modification layer is still not able to prevent the field-assisted Cu penetration through the sidewall. As a result, the pseudo-breakdown phenomenon was not completely eliminated, but considerably delayed as seen in Figure 5.1b.

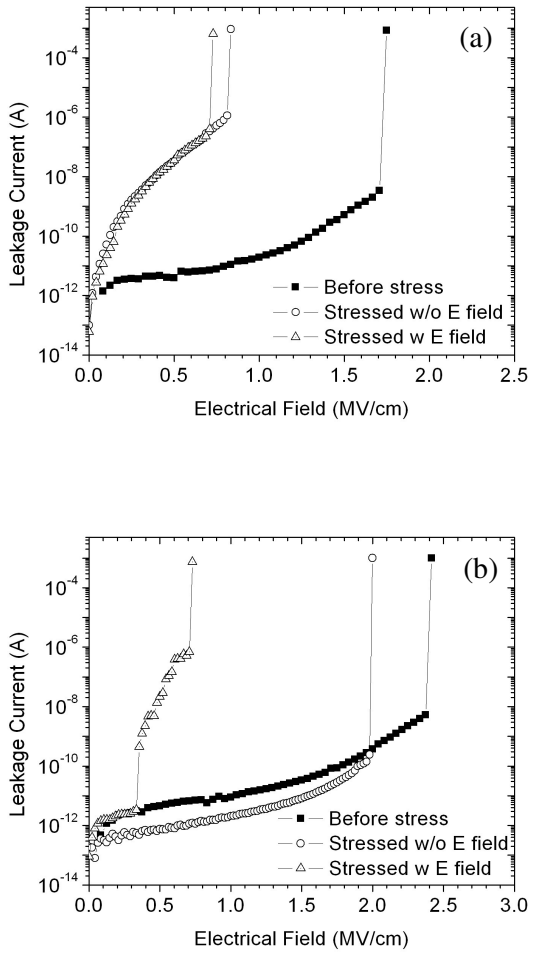

Figure 5.2 I-E characteristics of interconnects after pseudo-breakdown occurrence at 200°C with (or without) an electrical field of 1MV/cm: a) with conventional PVD TaN/Ta barrier and b) with a-SiC:H 100 Å/ Ta 250 Å bilayer barrier.

5.4 Cu Transport Mechanism in Dielectric Materials

The physical mechanisms behind this pseudo-breakdown phenomenon should be attributed to localized defects, such as discontinuity or thinning of the sidewall barrier, where thermal stress in conjunction with (or without) electrical stress acts as a driving force for Cu diffusion/drift through the barrier/IMD interface [2]. A schematic diagram of this Cu transport phenomenon is shown in Figure 5.3, which is similar to the Cu diffusion/drift process in dielectric materials introduced in Chapter 2. During thermal and electrical stress conditions, Cu ions and neutrals begin to get injected from the anode into porous low-*k* IMD through localized defects in the sidewall barrier/porous low-*k* IMD interface, leading to local barrier failure. This process corresponds to the rapid leakage current increase, indicating that pseudo-breakdown has just occurred [5]. Subsequently, the injection of Cu ions would lead to a charge build-up region in the porous low-*k* IMD, which then limits the ionic injection current [6]. Such ionic injection and self-limitation processes occur randomly along the entire sidewall of interconnect lines, resulting in a time window of current fluctuation between the pseudo-breakdown and the eventual hard breakdown. The injected Cu ions and neutrals accumulate and drift/diffuse through the porous low-*k* IMD towards the cathode, leading to the dielectric degradation [7] by acting as traps for electron leakage current. Finally, the eventual hard breakdown occurs when a conductive path is formed by the Cu residues that have leaked into the low-*k* IMD.

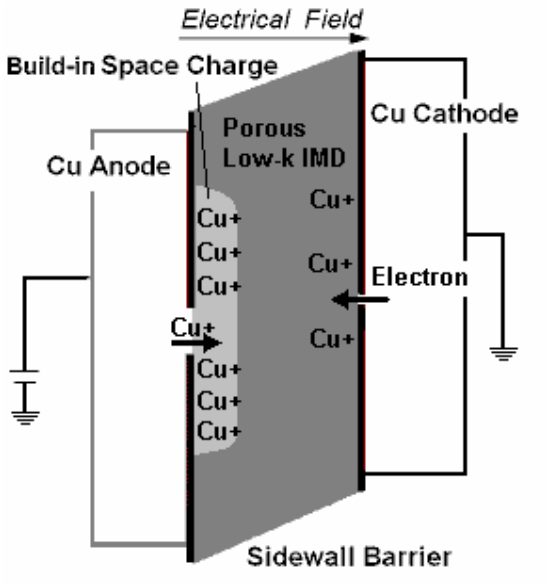

Figure 5.3 Kinetics of Cu transport through IMD under thermal and electrical stress.

A physical evidence of this Cu drift/diffusion induced dielectric failure mechanism is shown in Figure 5.4a, detected by TEM analysis and EELS mapping. Cu has clearly leaked out of the PVD TaN/Ta barrier into the porous IMD after electrical failure during TDDB tests at 200°C with an electric field of 0.5 MV/cm. As we mentioned before, the use of thin PECVD a-SiC:H modification layer will efficiently seal the rough sidewall surface of porous low-*k* IMD, thereby reducing the localized defects and improving the uniformity as well as step-coverage of the PVD Ta barrier subsequently deposited on top of it. Therefore it benefits the electrical performance and reliability of Cu/porous ultra low-*k* interconnects significantly. When such a bilayer barrier of standard PVD Ta barrier with thin a-SiC:H layer was used, the pseudo-breakdown appearance was considerably delayed, but not completely eliminated as shown in Figure 5.1b. This suggests that Cu ions/atoms need a longer time to penetrate this bilayer barrier due to the

improved barrier integrity. But it is still not capable of entirely preventing the Cu diffusion/drift into porous IMD through the sidewall during TDDB tests. As shown in Figure 5.3b, Cu residues were also detected after electrical failure. The a-SiC:H modification layer is, obviously, not thick enough to provide a defect-free sidewall barrier and inhibit Cu penetration into porous IMD. If a sidewall barrier which is not fully dense is used, Cu diffusion from damascene lines and Cu drift in the porous low-*k* dielectric will occur, degrading the dielectric and leading to a poor TDDB performance [8].

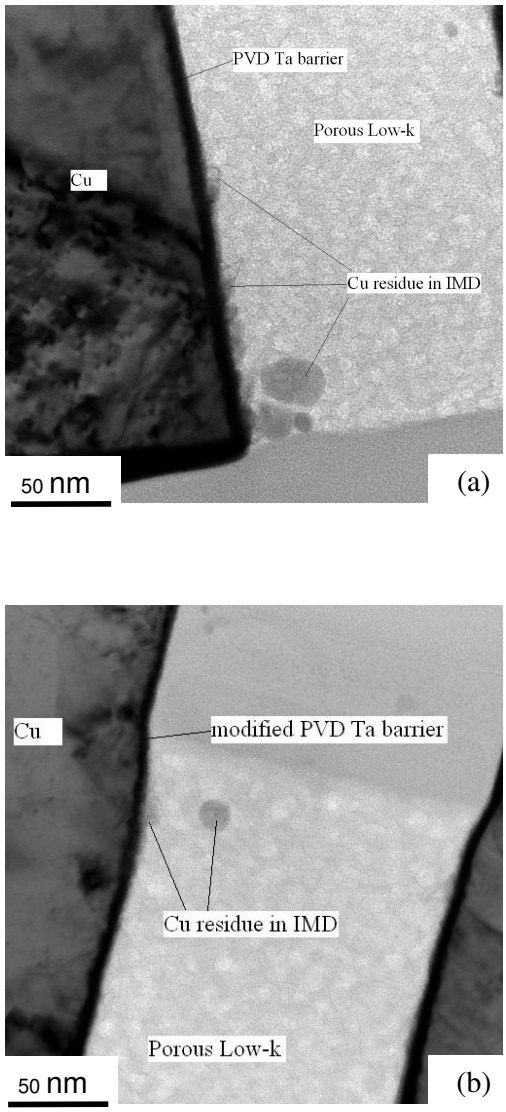

Figure 5.4 Cross-sectional TEM images of interconnects after electrical failure during TDDB tests at 200°C and 1 MV/cm with: a) conventional PVD TaN/Ta sidewall barrier and b) a-SiC:H 100 Å/ Ta 250 Å bilayer sidewall barrier.

5.5 Enhanced Barrier Integrity by Optimized Bilayer Barrier Structure

The PECVD a-SiC:H layer can efficiently seal the rough surface of the underlying porous low-*k* IMD, as pointed out earlier. However, if this a-SiC:H underlying layer is too thin, the bilayer barrier may still exhibit some degree of discontinuity on the sidewalls. As shown in Figure 5.4b, when an electrical field was applied at elevated temperatures, field-assisted Cu penetration through the sidewall barrier occurred, leading to the pseudo-breakdown behavior and interconnects failure. If a thicker a-SiC:H layer is incorporated, it would result in better sealing of the porous low-*k* IMD. This would lead to eliminating any barrier discontinuities at the sidewall barrier and hence eliminate Cu penetration into porous low-*k* IMD. Furthermore, it may allow a reduction in the thickness of PVD Ta barrier without any compromise in the overall barrier performance. Thus, one would expect a better electrical performance and possible elimination of the pseudo-breakdown behavior by such a bilayer barrier structure.

5.5.1 Elimination of Pseudo-Breakdown Behavior by Optimized Bilayer Barrier Structure

When a bilayer barrier of thicker a-SiC:H (200 Å) and correspondingly thinner Ta (125 Å) was used, it was found that the interconnect structures, as expected, did not exhibit any pseudo-breakdown and current fluctuation behaviors during the TDDB tests: they exhibit a smooth I-t curve followed by an abrupt hard breakdown behavior, as shown in Figure 5.5. Identical abrupt breakdown behavior was also observed at different temperatures from 175°C to 300°C with different electric

fields (0.5 to 1 MV/cm). And there is no evidence of Cu leaking out into porous low-*k* IMD, as shown in Figure 5.6, after the TDDB tests.

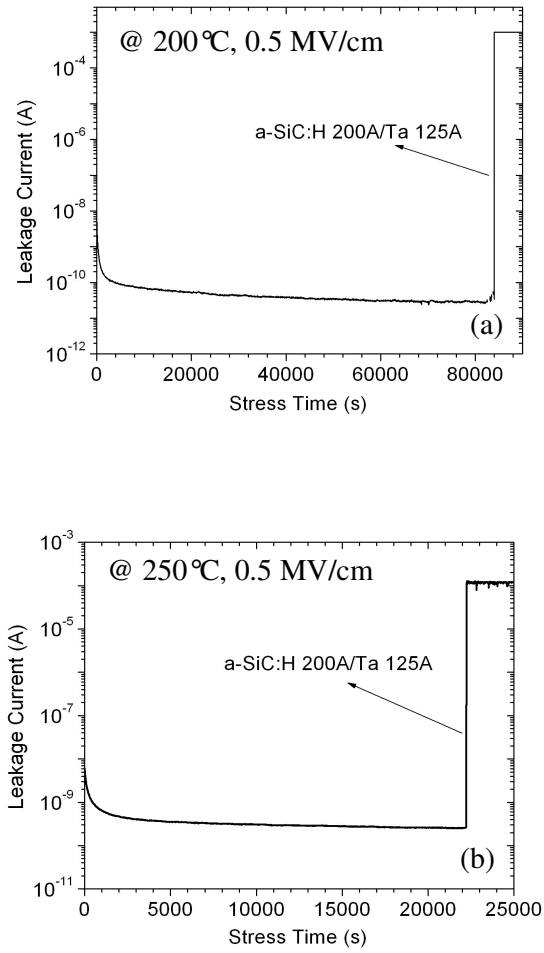

Figure 5.5 Current-time (I-t) characteristic of Cu/porous ultra low-*k* interconnects with a-SiC:H 200 Å/Ta 125 Å bilayer barrier at: a) 200°C, 0.5 MV/cm, and b) 250°C, 0.5 MV/cm.

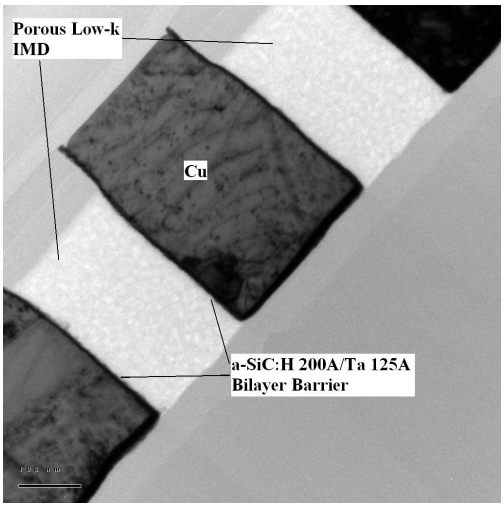

Figure 5.6 Cross-sectional TEM images of interconnects structures with a-SiC:H 200 Å/Ta 125Å bilayer barrier after TDDB tests at 200°C and 0.5 MV/cm. No Cu residue was detected in the porous low-*k* IMD.

5.5.2 TDDB Activation Energies (*Ea*) with Different Sidewall Barriers

To investigate the failure mechanism associated with different sidewall barriers, Mean Time to Failure (τ_{BD}) *vs.* Inverse Temperature (1000/T) of Cu/porous ultra low-*k* interconnect was measured at 0.5 MV/cm (Figure 5.7). The TDDB activation energies (E_a) for samples with conventional 250 Å PVD TaN/Ta barrier and bilayer barrier of standard 250 Å PVD Ta barrier and thin a-SiC:H modification layer (< 100 Å) have similar value of ~0.89 eV. It is well known that the Cu diffusion/drift through the sidewall barrier is strongly temperature dependent [9], and hence requires high activation energy. The identical E_a value and similar pseudo-breakdown behavior suggest that the same kinetics of Cu diffusion/drift through the sidewall into porous low-*k* IMD is the dominating failure mechanism in the interconnect structures with these two barriers. The use of

thin a-SiC:H modification layer extended the lifetime of interconnect structures, but did not eliminate the Cu penetration through the sidewall barrier completely.

For samples with a bilayer barrier of thicker a-SiC:H (200 Å) and correspondingly thinner PVD Ta (125 Å) barrier, the experimental TDDB activation energy is somewhat lower (E_a ~ 0.57 eV). However, the time-to-failure significantly increased at each testing temperature (Figure 5.7). The thicker a-SiC:H layer not only provides more desirable surface smoothening on the sidewall of porous IMD, but also could act as an alternative Cu diffusion barrier [10], despite the use of a thinner PVD Ta layer. In another TDDB study on porous low-*k* silica-based interconnect dielectrics, similar low activation energies of 0.49 - 0.66 eV were reported by Ogawa *et al.*[11]. Their studies on interconnect failure are based on a percolation model, where the pores in the low-*k* dielectric material act as defect sites and strongly affect the breakdown strength and the time-to-failure of the dielectric. As we know, the reliability issue associated with porous low-*k* dielectrics is a major concern of the Cu/porous ultra low-*k* BEOL integration and is still not completely resolved [12]. Tokei *et al.* [8] also indicate that, for a fully dense barrier, the primary cause for the dielectric failure in Cu/porous low-*k* interconnects is unlikely to be copper drift/diffusion but the defects located at the meander of test structure. Thus, it is reasonable to conclude that the failure kinetic associated with the more robust a-SiC:H 200 Å/Ta 125 Å bilayer barrier is not due to Cu diffusion/drift through the sidewall barrier, but may be more likely to be either the intrinsic dielectric breakdown of the porous low-*k* dielectric [11], or due to defects introduced in the interconnect structures during fabrication process [8], [13]. Although the extrapolation of TDDB lifetime for a-SiC:H 200 Å/Ta 125 Å bilayer barrier is not yet satisfied the reliability criteria for real-life IC operation at

low temperature (~100°C), the different activation energy and failure mechanism associated here have demonstrated that, by using a bilayer sidewall barrier consisting of a thicker a-SiC:H and thinner Ta layers, the sidewall region was better protected and was not the weakest point for the electrical and/or physical failure of Cu/porous ultra low-*k* interconnects.

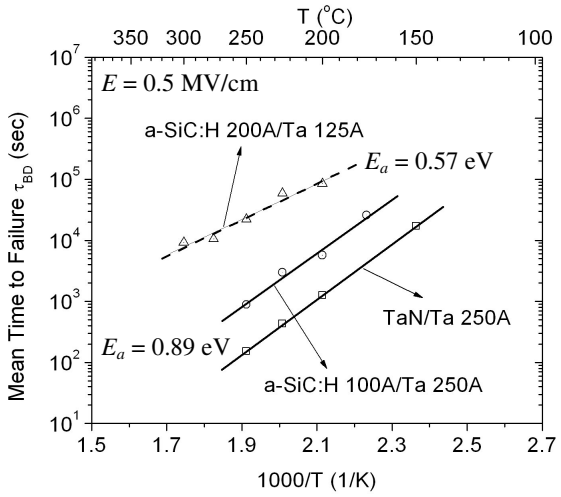

Figure 5.7 Arrhenius plot of Mean Time to Failure (τ_{BD}) for Cu/porous ultra low-*k* interconnects with different sidewall barriers at 0.5 MV/cm.

5.6 Cu Drift Mobility in Porous Organic Ultra Low-*k* IMD

According to our previous discussion, the pseudo-breakdown behavior and subsequent current fluctuation are associated with Cu transport process in low-*k* IMD. Thus, by assuming that

1) Cu begins to move into porous IMD at the occurrence of pseudo-breakdown and arrives the cathode at the time of eventual breakdown; and

2) Cu drifts across porous IMD with a constant velocity during the time of current fluctuation;

we can estimate the drift mobility of Cu in the porous ultra low-*k* IMD using the following equation

$$\mu = \frac{d}{t_{drift} E} \tag{5.1}$$

where t_{drift} is the duration of current fluctuation after the pseudo-breakdown occurred, d is the spacing of interconnect structures, E is applied electrical field and μ is the Cu drift mobility in the porous ultra low-*k* IMD. Figure 5.8 shows the Arrhenius plot of the estimated drift mobility of Cu in the Porous-SiLK™ dielectric from the I-t data of both PVD TaN/Ta barrier and the bilayer barrier of a-SiC:H 100 Å/Ta 250 Å. The calculated Cu drift mobility obeys the relation

$$\mu = 8.44 \times 10^{-7} \, e^{-\frac{0.717eV}{k_B T}} \ \mathrm{cm^2/V \cdot s} \tag{5.2}$$

This value is slightly higher than the reported Cu drift mobility in a hydrogen silsesquioxane (HSQ) based inorganic porous low-*k* dielectric [14], which was measured using a MIS structures and capacitance-voltage (C-V) shift method. The difference in the mobility values is mostly due to the choice of different low-*k* material (Porous-SiLK™ is a polymer based porous low-*k* material) and structure/method used to calculate the Cu drift mobility in this work. In any event, the Cu drift mobility calculated from our I-t data is still an estimated value because the Cu drift towards cathode in porous IMD is also enhanced by the built-in electric field near the anode by injected Cu ions. Nevertheless, this Cu drift mobility value could tell us how long it would take for Cu to go through the low-*k* IMD to cause interconnect failure at a given electrical field and temperature, if the via/trench sidewall is not well protected against Cu penetration. Furthermore, the

estimated drift mobility value by this method indicates the resistance of the low-*k* dielectrics against Cu migration. It is clear that people prefer to use a low-*k* IMD with a small drift mobility value.

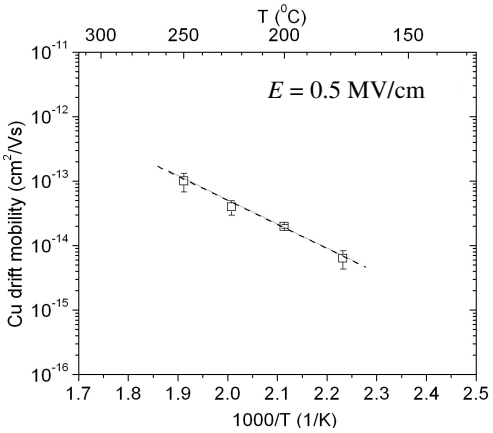

Figure 5.8 Arrhenius plot of estimated Cu drift mobility in organic porous ultra low-*k* IMD (Porous-SiLK™).

5.7 Conclusions

The pseudo-breakdown and TDDB studies indicate that the Cu penetration through the sidewalls of the barrier into porous dielectric was the dominating failure mechanism in Cu/porous ultra low-*k* interconnects with conventional PVD TaN/Ta barrier. When a thin a-SiC:H layer (<100 Å) was introduced to smoothen the rough sidewall surface of porous low-*k* IMD, Cu penetration was significantly delayed but not completely eliminated. Degradation of conventional PVD TaN/Ta barrier is significantly affected by both thermal and electrical stress. However, the degradation of the bilayer barrier of a-SiC:H 100 Å/Ta 250 Å structure layer has a significantly better resistance against Cu penetration when only subjected to thermal stress. Both these barriers exhibit pseudo-breakdown behavior when an

electrical field was introduced along with the thermal stress. A bilayer sidewall barrier of thicker a-SiC:H (200 Å) and thinner Ta (125 Å) layers will further improve the barrier integrity against Cu penetration. I-t characteristics of samples with this a-SiC:H 200 Å/Ta 125 Å bilayer barrier did not exhibit the pseudo-breakdown behavior. A different activation energy for the a-SiC:H 200 Å/Ta 125 Å bilayer barrier was calculated from TDDB tests and corresponds to either the intrinsic dielectric breakdown and/or defects in the porous low-*k* dielectric rather than Cu diffusion/drift mechanism. Thus, by using this improved a-SiC:H/Ta bilayer barrier structure, the sidewall interface between Cu and porous low-*k* IMD was well-protected and was not the weakest point corresponding to the fast failure in Cu/porous ultra low-*k* interconnects

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Chapter 6. Silicon Carbide Based Low-*k* Dielectric Barriers for Dielectric/Metal Bilayer Sidewall Barrier Application

6.1 Introduction

Our work in Chapters 3 and 4 have demonstrated that using the dielectric/metal bilayer sidewall barrier structure could efficiently improve the electrical and reliability performance of Cu/porous ultra low-*k* damascene interconnects. And we find that the silicon carbide based dielectric films (a-SiC:H), deposited by organosaline precursor, are most suitable for this application. This a-SiC:H also has the advantage of lower dielectric constant (k ~ 4.9) which is very important to *RC* delay consideration for Cu/low-*k* interconnects. Furthermore, we believe that the methyl groups (-CH_3 or -$(CH_2)_n$) in the a-SiC:H film are helpful for the pore sealing capability because most of the low-*k* materials are also in rich of such carbon content. Thus, we want to further investigate the possibility of using other kinds of low-*k* silicon carbide based dielectric film, *e.g.* SiCO and SiCN, for bilayer barrier application. In this work, different dielectric composites were used and investigated for their effects on barrier integrity and electrical performance of Cu/porous ultra low-*k* interconnects.

6.2 Experimental Setup

A Silica based spin-on porous ultra low-*k* dielectric (Nanoglass™ [1], *k*~ 2.4) was used as the IMD. 500 Å SiCN and 2000 Å SiO_2 layer were coated on top of this porous low-*k* IMD as etch stop layer and hard mask, respectively. All the samples were fabricated using a 0.13 μm technology Cu single damascene process. After the trench etch was complete, ~200 Å dielectric barriers of SiCO, SiCN and a-SiC:H (hereinafter referred to as "SiC") were deposited on the sidewall using PECVD tools (a Novellus Exquel™ system for SiCO deposition and an Applied Material Centura™ system for SiCN and SiC deposition). The subsequent 125 Å Ta barrier was deposited by the Applied Material Endura™ HDP PVD system with SIP technique to form the dielectric/metal bilayer sidewall barrier. The Cu seed layer was deposited in the same HDP PVD system without breaking vacuum. After the CMP process was complete, a capping layer consisting of 500 Å SiCN and 3000 Å SiO_2 were deposited on the top immediately to prevent oxidation and moisture intake. The samples with standard PVD Ta sidewall barrier only (250 Å) were also fabricated for comparison purposes. Blanket samples of bilayer barriers and standard Ta barrier, complete with Cu, were also fabricated on non-patterned porous ultra low-*k* wafers. For these blanket samples, a thin layer of PVD Ta layer was deposited on top of Cu to prevent any oxidation.

The line-to-line leakage current of the Cu/porous low-*k* interconnects was measured using identical comb structure as shown in Chapter 3. The line width and line-to-line spacing of the comb structure are both equal at 0.18 μm with a total line length of ~1 m. The electrical characteristics and breakdown strength were monitored on a 0.192 m long serpentine/comb sandwich structure, with a 0.24 μm line width and line-to-line space.

6.3 Characterization of Bilayer Barrier Structure with Low-*k* Silicon Carbide Layer

6.3.1 Characterization of Silicon Carbide Based Low-*k* Films

Table 6.1 shows the composition (at. %) of PECVD SiCO, SiCN and SiC films, used in our study, by Auger Electron Spectroscopy (AES). At the surface of SiCN and SiC films, which are not supposed to have any Oxygen content, Oxygen contamination was observed. It should be attributed to O_2 and moisture in the air ambient because no Oxygen contained precursors were used in the PECVD SiCN and SiC deposition process. At several nanometers below the surface (after 50 s Ar sputtering), the Oxygen content was negligible in these two films. On the other hand, a constant Oxygen concentration (22 - 27 at.%) is presented both at the surface and the bulk of SiCO film, due to the use of Oxygen containing precursor in the PECVD SiCO deposition process.

Figure 6.1 shows the Fourier transform infrared (FTIR) spectra of PECVD SiCO, SiCN and SiC dielectric films. There is no Oxygen related chemical bonds in SiCN and SiC films, consistent with the AES data, compared to the Si-O-Si peak in the SiCO film. The incorporation of Si-O-Si bonds is helpful in achieving a lower dielectric constant value for the SiCO film (k ~ 4.37) [2]. The major reason for the low dielectric constant value in Silicon Carbide based dielectrics such as SiCO (k ~ 4.37), SiCN (k ~ 4.75) and SiC (k ~ 4.40) is due to the large volume occupied by methyl groups (-CH_3 and -$(CH_2)_n$) and Carbon's low polarizability, which is benefited by using tetramethylsilane or trimethylsilane precursors [3].

Table 6.1 Relative concentration of PECVD SiCO, SiCN and SiC films.

Sputtered Sample	C	N	O	Si
At Surface (at.%)				
SiCO	14	--	27	49
SiCN	25	14	9	52
SiC	33	15	17	34
After 50 s Ar Sputtering (at.%)				
SiCO	25	--	22	53
SiCN	25	15	3	57
SiC	45	--	2	54

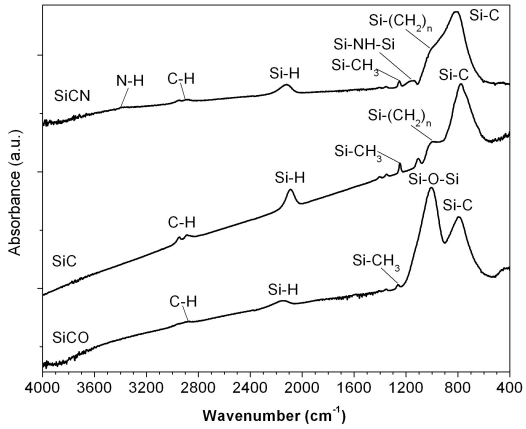

Figure 6.1 FTIR spectra of PECVD SiCO, SiCN and SiC dielectric films.

6.3.2 Influence of Underlying Dielectric Layers on Ta Crystallographic Texture

Figure 6.2 shows X-ray diffraction (XRD) spectra of PVD Cu seed layer and Ta barrier, with or without PECVD SiCO, SiCN or SiC underlying layer, on porous low-*k* substrates. The peaks of metastable tetragonal (β-phase) Ta structure were identified from the XRD spectra in the case of Cu seed layer and Ta barrier directly deposited on porous low-*k* dielectric as well when the PECVD SiCO underlying layer was used. On the other hand, when Cu seed layer and Ta barrier were deposited on SiCN or SiC underlying layers, body-centered cubic (α-phase) Ta structure was identified from the XRD spectra. The α-phase Ta film is more desirable for diffusion barrier application in Cu damascene interconnects. This is because of the lower sheet resistance of α-phase Ta film. Also, β-phase Ta films exhibit high compressive stress [4], [5] as well as reliability problems in Cu metallization [6]. Thus the β-phase Ta barriers on top of either porous low-*k* dielectric or SiCO layers are prone to thermal stress, especially after long-time aging, leading to localized defects or barrier failure. As a result, Cu migration into porous low-*k* IMD may occur, leading to electrical characteristics degradation of interconnects after long-time thermal stress.

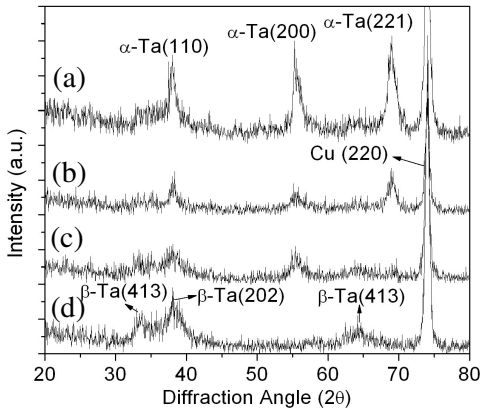

Figure 6.2 XRD spectra of PVD Cu seed layer and Ta barrier with different underlying layer on porous low-*k* dielectric: a) Cu/Ta/SiC, b) Cu/Ta/SiCN, c) Cu/Ta/SiCO, and d) Cu/Ta directly deposited on porous low-*k* dielectrics.

6.4 Interconnect Performance and Reliability of Bilayer Sidewall Barrier with Different Low-*k* Silicon Carbide Layers

6.4.1 Electrical Characteristics and Thermal Stability with Different Bilayer Barriers

The typical Leakage Current (I) *vs.* Applied Electrical Field (E) characteristics of Cu/porous low-*k* interconnect structures with different sidewall barriers are shown in Figure 6.3. The as-deposited I-E characteristic of Cu/porous ultra low-*k* interconnects was considerably improved by using the bilayer barrier structures. Before any thermal stress, the E_{BD} of SiCO/Ta, SiCN/Ta and SiC/Ta bilayer barriers shows a mean value of 2.0 - 2.3 MV/cm (Figure 6.4a), which is higher than that of the conventional PVD Ta sidewall barrier (~1.3 MV/cm). Similar improvements were also seen when looking at the line-to-line leakage current distribution (Figure 6.5a). The samples with bilayer sidewall barriers show better

characteristics in terms of smaller leakage current and smaller spread. The different Silicon Carbide based dielectrics of SiCO, SiCN and SiC layer in the bilayer barrier structure exhibit not much difference in electrical performance improvements before any electrical/thermal stress.

However, after a BTS at 350°C, 0.5 MV/cm for 1 h, only interconnect structures with SiCN/Ta and SiC/Ta bilayer barriers could survive and still have functional I-E characteristics. Samples with SiCO/Ta bilayer barrier and conventional PVD Ta barrier exhibited an immediate breakdown after this BTS test. To investigate the influence of different bilayer barriers on reliability of Cu/porous low-*k* interconnects, a long time burn-in test at 200°C for 120 h in air environment was performed on all samples. The samples with SiCO/Ta bilayer barrier structure begin to exhibit some degree of divergence in leakage current characteristic (Figure 6.5b). Samples with PVD Ta barrier exhibit maximum divergence. This is consistent with the degraded I-E characteristics of SiCO/Ta bilayer barrier as well as PVD Ta barrier, as shown in Figure 6.3b, after burn-in at 200°C for 120 h. The I~E curves of samples with these two barriers show a large slope. It results in higher line-to-line leakage currents for SiCO/Ta barrier compared with that of SiCN/Ta and SiC/Ta bilayer barrier, especially when the applied electrical field is increased. Moreover, the mean value of E_{BD} with SiCO/Ta drops to a value of ~1.5MV/cm and is comparable to the value of conventional PVD Ta barrier after such long-time burn-in test (Figure 6.4b). Such electrical degradation after the thermal/electrical stress indicates poor reliability of Cu/porous low-*k* interconnects when PECVD SiCO was used as the dielectric layer in the bilayer barrier structure.

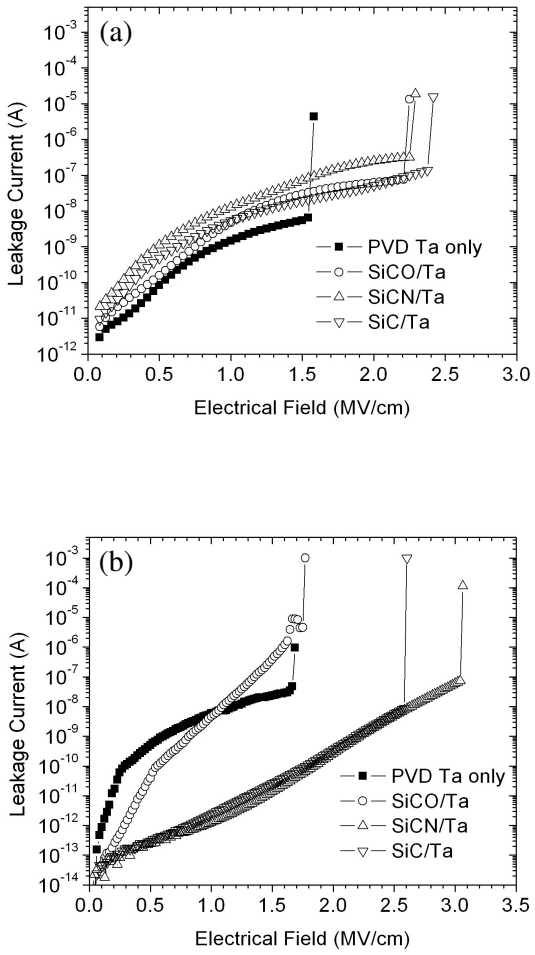

Figure 6.3 Leakage Current (I) *vs.* Applied Electrical Field (E) characteristics of Cu/porous ultra low-*k* interconnects with different sidewall barriers: a) before any thermal stress; and b) after burn-in at 200°C for 120 h.

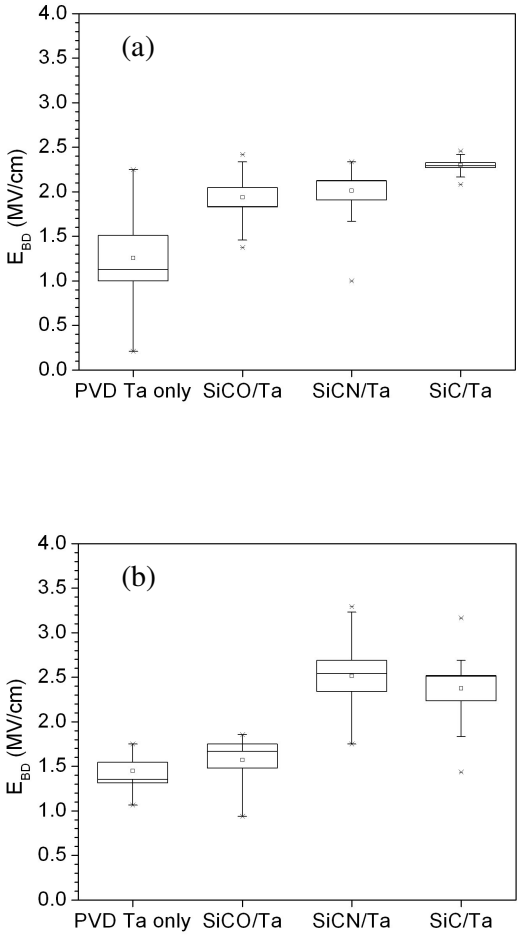

Figure 6.4 Statistic plots of E_{BD} for Cu/porous low-k interconnects with different sidewall barriers: a) before any thermal stress; and b) after burn-in at 200°C for 120 h.

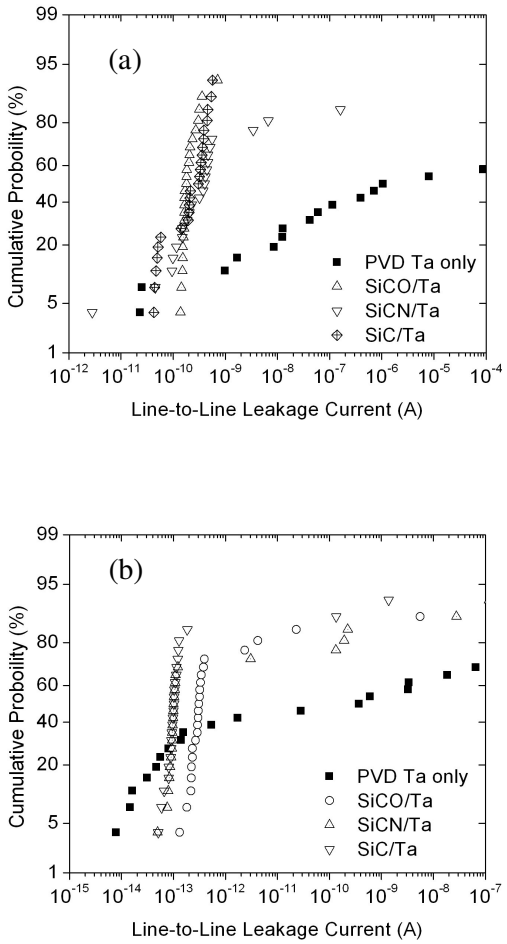

Figure 6.5 Line-to-line leakage current distribution of Cu/porous low-*k* interconnect structures with different sidewall barriers measured at 5 V measured a) before any thermal stress; and b) after burn-in at 200°C for 120 h.

6.4.2 Post-stress I-E characteristics of Interconnects with SiCO/Ta Bilayer Barrier

Introduction of PECVD Silicon Carbide layer at the trench/via sidewall of porous low-*k* IMD was demonstrated to have positive effects on barrier integrity and electrical performance of Cu/porous low-*k* damascene structure, as demonstrated in Chapters 3 and 4. These improvements are attributed to the uniform PECVD Silicon Carbide layer deposited on the sidewall. It could efficiently seal the porous surface of porous low-*k* IMD to prevent Ta penetration. In addition, it could also help in curing the sidewall damage, *e.g.* Carbon depletion issue, caused by trench etching/photoresist strip process [7]. With the results shown above, we believe PECVD SiCN and SiC are both good candidates for application in dielectric/metal bilayer sidewall barrier in terms of electrical performance and reliability improvements. However, our study indicates that PECVD SiCO, unlike other two low-*k* Silicon Carbide based dielectrics, is not suitable for such applications.

When looking in the post-stress current conduction with SiCO/Ta barrier, different conduction models, *e.g.* Poole-Frankel emission and Schottky emission, were used to fit the post-stress I~E characteristics. A clear linear region was shown in Ln(J/E) *vs.* $E^{1/2}$ plot from 0.2 MV/cm until electrical breakdown (Figure 6.6). This degraded electrical characteristic fitted well with Poole-Frankel conduction mechanism which is described by:

$$J \sim E \times \exp\left[\frac{q(\sqrt{qE/\pi\varepsilon_r\varepsilon_0} - \phi_B)}{k_B T}\right] \qquad (6.1)$$

where J is the current density, E is the applied electrical field, Φ_B is the barrier height and ε_r is the effective dielectric constant of the dielectric [8]. Using the

slope of the linear region and Poole-Frenkel emission model, the corresponding effective dielectric constant ε_r was calculated as 3.36. This value is quite reasonable for the Cu/porous low-*k* single damascene architecture used in this experiment, considering the contribution of effective dielectric constant from surrounding materials, *e.g.* passivation/capping layer (k ~ 7), etch stop layer (k ~ 4.7) and SiO_2 hard mask (k ~ 4.2) [9], [10]. For the fitting of post-stress I~E characteristics with Schottky emission model, effective dielectric constant of less than 1 was extrapolated from LnJ *vs.* $E^{1/2}$ plot – a value very low and unreasonable These results suggest the post-stress current conduction for Cu/porous low-*k* interconnects with SiCO/Ta barrier is dominated by Poole-Frenkel emission.

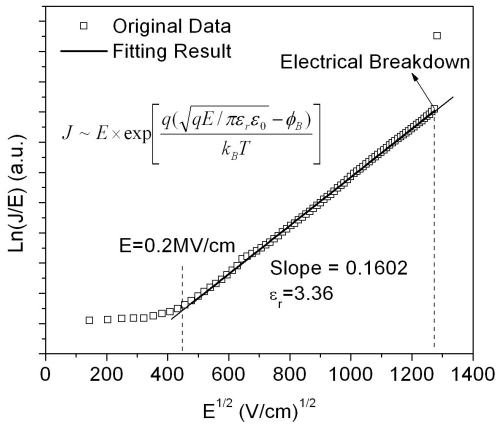

Figure 6.6 Plot of Ln(J/E) *vs.* $E^{1/2}$ showing Poole-Frenkel conduction in Cu/porous ultra low-*k* interconnects with SiCO/Ta sidewall barrier after burn-in test at 200°C for 120 h.

Poole-Frenkel emission results from the field-enhanced excitation of trapped electrons into conduction band of dielectrics, often observed in heavily damaged insulators [8]. The Poole-Frenkel emission is a bulk-limited conduction

mechanism and its existence indicates the presence of electron traps. For the Poole-Frenkel mechanism to occur, the insulator must have a wide band gap and contain donors or acceptors [11]. At room temperature, they do not generally donate electrons to the conduction band (creating free electrons) or accept electrons from the valence band (creating free holes) as they are located many k_BT below the conduction band (for donors) or above the valence band (for acceptors). Hence, Poole-Frenkel emission is generally observed at elevated temperature with high fields whereby electrons in the dielectric bulk traps could gain sufficient energy to be excited to the conduction band. A schematic band diagram of the Poole-Frenkel emission is shown in Figure 6.7.

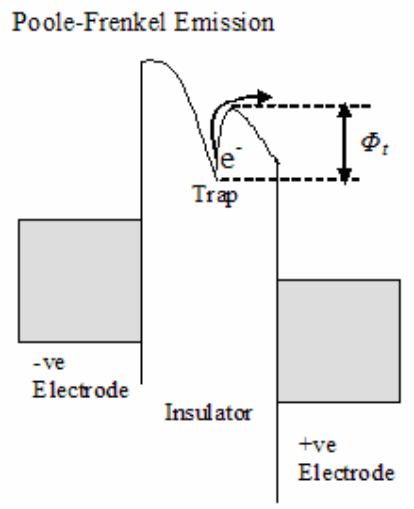

Figure 6.7. Schematic band diagram of Poole-Frenkel emission, whereby electrons in the dielectric bulk traps gain sufficient energy to be excited to the conduction band.

The domination of Poole-Frenkel conduction mechanism at room temperature and even low electrical field (E > 0.2 MV/cm) in the post-stress electrical

characteristic in the case of SiCO/Ta barrier suggests that electron traps were introduced into porous low-*k* IMD, leading to degraded dielectric properties. One possible source of the electron traps corresponding to this abnormal Poole-Frenkel emission is the Cu ions present in the low-*k* IMD during the thermal stress [12]. On the contrary, no electrical characteristics degradation and Poole-Frenkel emission were observed in Cu/porous low-*k* interconnects when SiCN/Ta or SiC/Ta bilayer sidewall barrier were used, after identical long-time burn-in test at 200°C for 120 h.

6.4.3 Reliability Concerns of Oxygen Content in Cu/Porous Ultra Low-*k* Interconnects with SiCO/Ta Bilayer Barrier

Michael *et al.* [13] demonstrated an oxidation-driven failure mechanism in Cu/porous ultra low-*k* interconnects. The oxidants could be those initially trapped in porous low-*k* dielectric, *e.g.* O_2/moisture uptake [14], or those generated by porous low-*k* dielectric during baking. During the thermal stress, the oxidants could be released. They diffuse through porous low-*k* IMD and subsequently through defects in the sidewall barrier to react with Cu. When oxidized, Cu ions become fast diffusion species and move out of the interconnect line into porous low-*k* IMD, in order to reach more oxidants [15]. The oxidation potential provides a sufficient and persistent driving force for pulling Cu through weak spots in sidewall barrier. This enables the possibility that other thermodynamic potentials across the barrier, *e.g.* compressive stress of β-Ta as well as stress gradient between Cu and porous low-*k* IMD, may act as additional driving force for Cu out-diffusion. The loss of Cu by out-diffusion induces extensive voiding and subsequent failure in Cu interconnects [14], [15]. Figure 6.8 shows a schematic diagram of this oxidation-driven Cu out-diffusion mechanism.

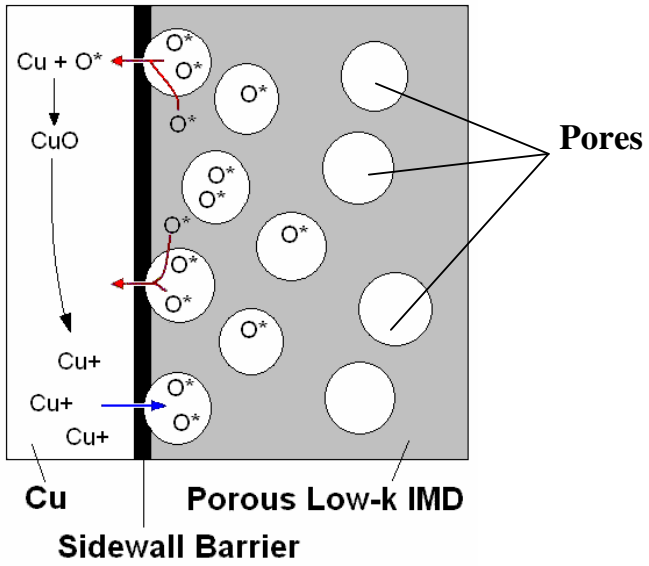

Figure 6.8 Schematic diagram of oxidation-driven Cu out-diffusion mechanism in Cu/porous low-*k* damascene interconnects.

Cu is prone to oxidation even at a low temperature range of 200°C - 400°C, which leads to reliability issues in Cu/low-*k* based interconnects. Murarka *et al.* [16] indicated that oxidized Cu shows a much faster diffusion in SiO_2 than that without oxidation below 400°C. The possible reason is Cu cation has a smaller radius by losing outer shell electrons so that it could move faster in SiO_2 network, as well as low-*k* materials, than as Cu atom according to the "free volume" theory [16], [17]. Another strong oxidant, Fluorine, shows a similar contamination behavior in Cu/Fluorinated Silicon Glass (FSG) damascene interconnects, where Fluorine could fast diffuse/drift to the Cu/barrier interface under electrical and/or thermal stress and ionize Cu atoms to more active ionic state [18].

The oxidant source is predominantly Oxygen species, either as O_2 and/or moisture coming from ambient which is absorbed by the porous low-*k* dielectric

during fabrication process, trapped in the pore structures [19]. Moreover, the incorporation of pores and/or methyl groups (*e.g.* $-CH_3$ and $=CH_2$) impairs, at least partially, the Si-O-Si bridging network in the silica porous low-*k* IMD as used this work. This may also occur in the SiCO film because they (SiCO and Nanoglass™) are chemically similar. The bonding angle and length change and shift away from stable state, as that in a fine Si-O-Si bridging network of SiO_2, due to structural changes by pores and/or methyl groups, and unsaturated Si-O- bonds may also be present (see Figure 6.9). As a result, the Oxygen content in porous low-*k* IMD and SiCO film may no longer be as stable as that in pure SiO_2. With sufficient energy from applied thermal and/or electrical field, Oxygen species may be released from the chemical bonding with Silicon, and will be able to move easily in SiCO film as the free volume has been enlarged by the incorporated pores and/or methyl groups. PECVD SiO_2 begins to dissociate and releases free oxygen to oxidize the top Ta in the Ta/SiO_2 films stacks after rapid thermal annealing at 650ºC [20], [21]. In the Cu/porous low-*k* damascene structure with SiCO/Ta bilayer sidewall barrier, Oxygen content in the SiCO layer and porous low-*k* IMD may also exhibit similar behavior - it would be released and contributes to the oxidation-driven Cu out-diffusion phenomenon during the long-time thermal stress.

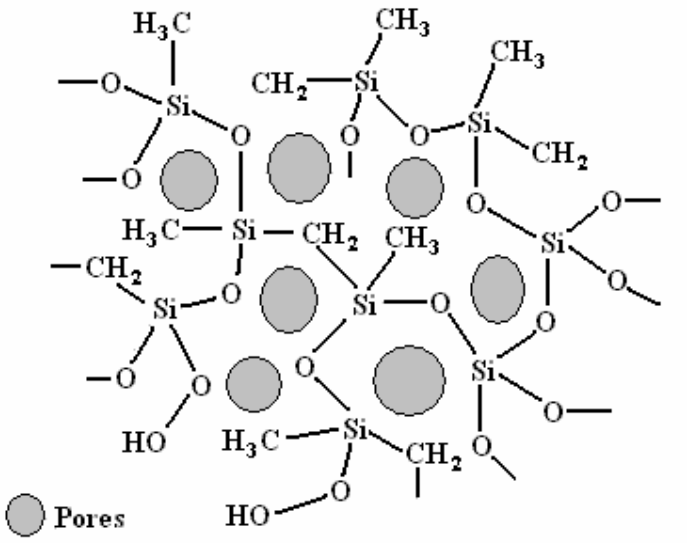

Figure 6.9 Schematic diagram of porous low-*k* dielectric and SiCO film, showing the incorporated pores and methyl groups (-CH_3 and =CH_2) disrupting the Si-O-Si bridging network.

If the Oxygen content, either from O_2/moisture trapped in pore structures or unstable Oxygen bonds (Si-O-Si or unsaturated Si-O-) in porous low-*k* IMD as well as SiCO layer, could be released and act as oxidant to induce Cu out-diffusion during thermal and/or electrical stress with long enough time, it should result in a poor reliability performance of interconnects. However, electrical data for SiCO/Ta bilayer barrier, after long-time thermal stress at 200°C for 120 h, did not reveal any interconnect failure. TEM analysis and EELS mapping did not show any noticeable Cu out-diffusion into low-*k* IMD. We believe that this situation corresponds to initial stages of the oxidation-driven Cu out-diffusion failure mechanism and is not sufficient enough to cause eventual breakdown of interconnects. However reliability concerns have to be addressed for long-term interconnects performance of SiCO/Ta bilayer barrier.

A preliminary examination of these Oxygen contents released from low-*k* IMD and/or Silicon Carbide based dielectric underlying layer was carried out by annealing blanket Ta/Cu/Ta/SiCO as well as Ta/Cu/Ta/SiCN and Ta/Cu/Ta/SiC film stacks on porous low-*k* substrates at 400°C for 3 h in vacuum. The Ta layer coated on the top is to protect oxygen/moisture intake from ambient during annealing. The thickness of bottom Ta barrier and SiCO, SiCN, SiC layers were the same as that used in the bilayer barrier structure (Ta 125 Å / SiCO, SiCN, SiC 200 Å respectively). The relative concentrations of Cu, Ta and Oxygen were estimated by energy disperse X-ray spectra (EDX) and is shown in Table 6.2 as we gradually progress from porous low-*k* dielectric to the bulk of Cu layer (spots 1 to 4). Figure 6.10 shows the cross-section TEM image of this planar film stacks after annealing and the exact location of spots for EDX analysis. The Oxygen concentration in porous low-*k* dielectric and SiCO underlying layer is quite high (spots 1 and 2). However, the Oxygen concentration decreases as we move into Ta and bulk Cu (spots 3 and 4). The Oxygen concentration gradient from porous low-*k* IMD to Cu layer suggests that the Oxygen content came from SiCO and/or porous low-*k* dielectric, but not from the ambient during annealing. This result is consistent with our earlier discussions. During the long-time thermal anneal (120 h at 200°C), Oxygen species could be released from porous low-*k* IMD and/or SiCO layer and diffuse towards Ta/Cu in a similar way, resulting in oxidation of Cu and consequent electrical performance degradation. However, with the use of either SiC or SiCN dielectric layer in the bilayer barrier structure, the Oxygen content in the dielectric layer (SiC or SiCN), Ta layer and bulk Cu is significantly lower. This is a clear indication that interconnects with either SiC or SiCN sidewall barrier

layer would exhibit better long-term reliability due to the reduction of oxygen diffusion from low-*k* into Ta and bulk Cu.

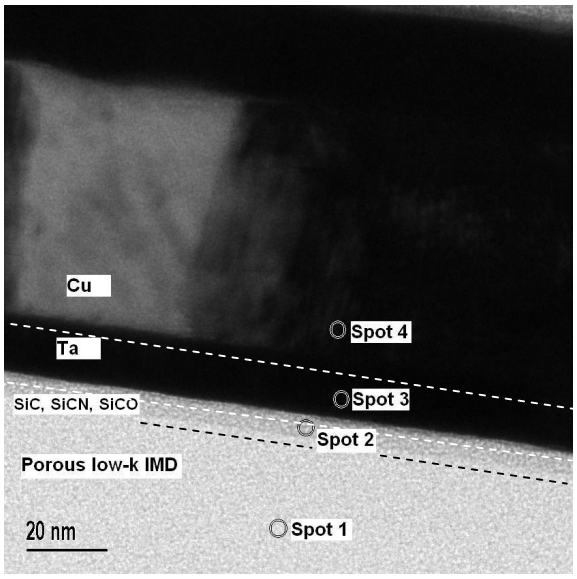

Figure 6.10 TEM cross-section with EDX spots of Ta/Cu/Ta/SiC, SiCN, and SiCO film stacks on porous low-*k* substrate after annealing at 400°C for 3 h.

Table 6.2 Oxygen concentration (at.%) in different film stacks by cross-section TEM and EDX after annealing at 400 °C for 3 h. The different spots refer to locations shown in Figure 6.10.

Film Stacks	Ta/Cu/Ta/SiC on porous low-*k*	Ta/Cu/Ta/SiCN on porous low-*k*	Ta/Cu/Ta/SiCO on porous low-*k*
Spot 1	29.5	29.3	29.4
Spot 2	5.2	10.1	22.2
Spot 3	3.3	5.4	6.1
Spot 4	1.4	2.7	4.4

During the long-time thermal stress, Oxygen contents could be released from porous low-*k* IMD and/or SiCO layer and diffuse towards Ta/Cu in a similar way, resulting in Cu oxidation and consequent electrical performance degradation. Figure 6.11a shows the sidewall interface of Cu/porous low-*k* interconnects after burn-in test at 200°C for 120 h in the case that SiCO/Ta bilayer sidewall barrier was used (Figure 6.11b). A clear delamination between Ta barrier and Cu was observed. EELS mapping for Oxygen indicates that at this time Oxygen has penetrated through the sidewall barrier and reached the Cu trench, possibly leading to the formation Cu oxide. It was reported that even monolayer coverage of Oxygen on the polycrystalline Ta surface would significantly degrade the strength of Cu/Ta chemical reactions [22], which may respond to the disassociation of Cu with Ta barrier. In the case of SiC/Ta or SiCN/Ta bilayer barrier, no such Cu delimitation issue and Oxygen penetration were observed after identical burn-in test. Thus we believe the SiCO/Ta bilayer sidewall barrier has a poorer thermal stability and reliability characteristics due to unstable Oxygen content, compared to the other two bilayer barriers with SiC or SiCN underlying dielectric layer.

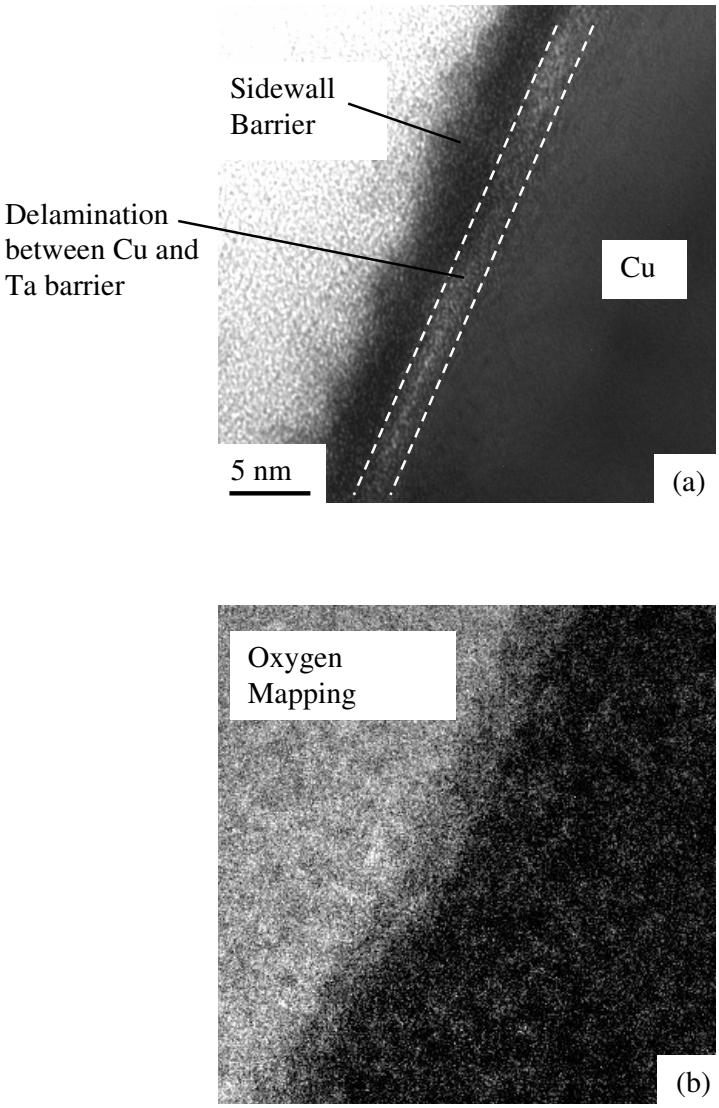

Figure 6.11 a) cross-sectional TEM image, and b) Oxygen mapping by EELS on the trench sidewall of Cu/porous low-*k* interconnects with SiCO/Ta bilayer barrier after burn-in at 200°C for 120 h.

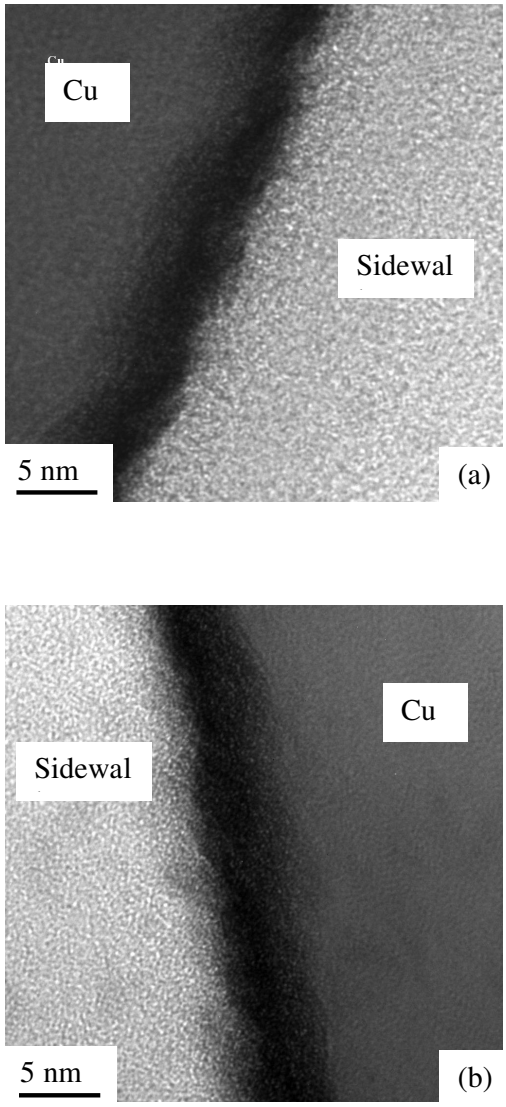

Figure 6.12 cross-sectional TEM images on the trench sidewall of Cu/porous low-*k* interconnects with a) SiC/Ta bilayer barrier, and b) SiCN/Ta bilayer barrier after burn-in at 200°C for 120 h. No delamination between Cu and Ta barrier was observed.

6.5 Conclusions

In this study, dielectric/metal diffusion barriers with different PECVD Silicon Carbide based films (SiCO, SiCN and SiC) were fabricated and used in Cu/Silica-based porous ultra low-*k* damascene interconnects. The bilayer sidewall barriers show significant performance improvements in terms of E_{BD}, leakage current distribution and I-E characteristic compared with conventional PVD Ta barrier. After long time burn-in tests or BTS at high temperature, the bilayer barriers with SiCN or SiC dielectric layer exhibit good reliability. But the situation for SiCO/Ta bilayer barrier is different - its electrical characteristic degrades after identical stress conditions. This unreliable behavior is partly attributed to the different Ta crystallographic texture in the bilayer barrier, which is affected by dielectric underlying layer. α-phase Ta was formed when deposited on SiCN or SiC layer and β-phase Ta was formed when deposited on SiCO or directly on the porous low-*k* dielectric. The unstable oxidant species from porous low-*k* IMD as well as SiCO film also contribute to this unreliable electrical behavior - reliability degrades as a result of an oxidation-driven Cu out-diffusion mechanism.

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Chapter 7. Further Improvements to Sidewall Barrier Efficiency by Al Stuffing Layer

7.1 Introduction

As the IC manufacturing technology continues to evolve below 90 nm or 65 nm nodes, porous low-*k* materials are necessary for the Cu BEOL process due to their ultra-low dielectric constant ($k < 2.0$) [1]. However, incorporating pores in the dielectrics raises reliability issues in terms of Oxygen and moisture intake/uptake during the process. On the other hand, the polycrystalline PVD Ta (either with or without TaN) sidewall barrier is not efficient enough to block Cu diffusion due to the grain boundary diffusion issues [2], [3]. The high resistivity of PVD TaN (256 μΩ•cm) and Ta/TaN barriers (380 μΩ•cm), compared to Cu metal line (1.67 μΩ•cm), limits their application in Cu metallization scheme due to *RC* delay considerations. Moreover, the PVD barrier thickness can not be scaled down with Cu line width in order to form an efficient diffusion barrier. As the feature size continues to shrink below 0.1 μm, the influence of high-resistivity TaN and TaN/Ta barriers on overall interconnect resistance will become more critical and so their usage needs to be carefully re-considered. Therefore, a robust sidewall barrier is required to overcome these issues for future generations of Cu/porous ultra low-*k* interconnects.

Aluminum has an easy tendency to be oxidized/ionized, but only at the surface to form a dense Al_2O_3 layer, which blocks Oxygen penetration and further oxidation of bulk Al film [4]. Therefore, we try to explore the idea of using a thin

Al stuffing layer in addition to the dielectric/metal bilayer structure to further improve the sidewall barrier efficiency against Cu diffusion and minimize/overcome oxidation induced reliability issues. Our experiments will show that a marked improvement in the electrical and reliability performance of Cu/porous ultra low-*k* interconnects can be achieved by using the composite sidewall barriers with an Al stuffing layer.

7.2 Experimental Setup

The samples were fabricated in a 0.13 μm technology Cu/Porous SiLK™ single damascene process. 500 Å SiCN and 2000 Å SiO_2 layers were deposited on the top of the porous low-*k* IMD as ESL and hard mask by PECVD tools to alleviate the processing issues associated with photo-resist strip and CMP steps. After the trench was formed, Silicon Carbide based dielectrics (~200 Å), including SiCO, SiCN and SiC, were deposited in the trench and on the sidewall by Novellus™ Sequel™ Express PECVD system (for SiCO) and Applied Material™ Centura™ PECVD system (for SiCN and SiC), respectively. Subsequently, a very thin Al layer (~100 Å) was sputtered on the damascene structure, followed by Ta barrier (125 Å) and Cu seed layer deposition in an Applied Material™ Endura™ HDP PVD system without breaking the vacuum. Samples with 250 Å PVD Ta sidewall barrier only were also fabricated for comparison purposes. After ECP and subsequent annealing process were completed, the superfluous Cu, barrier layer and SiO_2 hard mask on the top surface of damascene structure were removed by CMP. Finally, a dielectric barrier and passivation layer of 500 Å SiCN and 3000 Å SiO_2, respectively, were deposited on the top to prevent oxygen and moisture

penetration. Figure 7.1 shows a schematic diagram of this composite sidewall barrier structure with Al interlayer. Blanket samples of Cu/barrier layers/Porous SiLK™ film stacks were also fabricated in an identical manner for physical analysis.

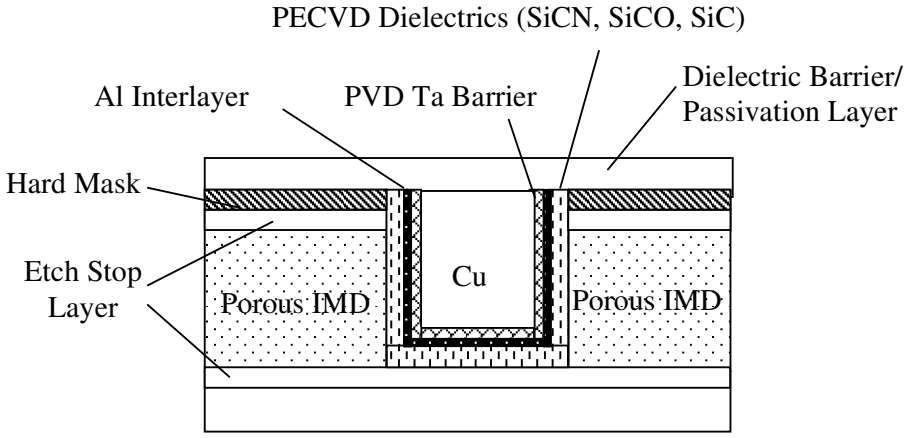

Figure 7.1 Schematic diagram of the composite sidewall diffusion barrier with Al interlayer.

The Cu line resistance and line-to-line leakage current of the Cu/porous low-*k* interconnects were measured using identical serpentine and comb structures as shown in Chapter 3 and Chapter 6. The line width and line-to-line spacing of these two structures are both equal at 0.18 μm with a total line length of ~1 m. The electrical characteristics and breakdown strength were monitored on a 0.192 m long serpentine/comb sandwich structure, with a 0.24 μm line width and line-to-line space. However, due to the different porous low-*k* IMD used ((Porous-SiLK™ here and Nanoglass™ in Chapter 6), we can not entirely compare the data here with that in Chapter 6.

The thin Al layer was deposited by conventional PVD method, which was not optimized for uniform Al sidewall coverage in the narrow damascene trench/via. Therefore the PVD Al deposition may not form a continuous and conformal Al layer on the sidewall. But it is possible to leave a very thin, may be discontinuous, Al monolayer (probably several atomic layers only) on the sidewall. The thickness of such ultra thin Al interlayer on the sidewall cannot be measured by cross-section TEM. This additional Al interlayer may not act as a diffusion barrier between a-SiC:H layer and Ta barrier. But it is expected that the influence of Al underlying layer on the grain structure of Ta barrier will enhance the performance of whole sidewall barrier scheme.

7.3 Effects of Al Interlayer on Ta and Cu Crystallographic Texture

The Al interlayer shows a positive influence on the crystallographic texture of Ta barrier and Cu seed layer on the top. The peaks of α-phase Ta were identified in the XRD spectra when the Ta barrier was deposited on the thin Al layer (Figure 7.2). As mentioned in Chapter 6, α-Ta film has a lower sheet resistance and insignificant stress related issues compared to its β-phase counterpart [5], [6]. Consequently, a Cu (111) orientation was observed in the subsequent Cu seed layer deposited on such α-Ta barrier, which has a low resistivity, low defect density and better wetting properties [7]. A strong textured Cu seed layer will promote the growth of a similar texture in the subsequently electroplated Cu film on the top. If the Cu seed layer has a strong (111) texture, the ECP Cu film will also develop a strong (111) texture [8]. The Cu (111) orientation is more preferred than other grain textures in Cu metallization process due to its low sheet resistance and better reliability performance against Cu electromigration [8]-[10]. Since the

actual Al interlayer deposited on the sidewall is quite thin and can not be measured, it should not significantly affect the overall Cu line resistance. But the use of Al promotes a better growth of α-phase Ta barrier, which has a lower resistivity. Moreover, the Al interlayer could prevent Ta oxidation and also stuff the grain boundaries in the Ta layer (discussed later in Section 7.5), thus minimizing any Cu out-diffusion and the formation of high resistivity Cu compounds at the sidewall interface. As shown in Figure 7.3, the end result is a much lower Cu line resistance for Cu/porous ultra low-*k* interconnects with this composite sidewall barrier and Al interlayer, compared with the conventional PVD Ta barrier.

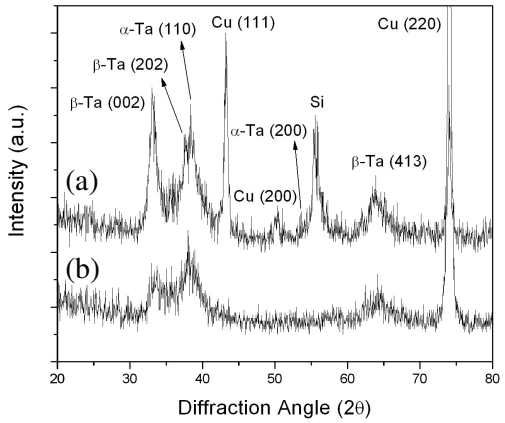

Figure 7.2 XRD spectra of Cu seed layer/Ta barrier on porous low-*k* dielectric a) with Al underlying layer, and b) without Al underlying layer.

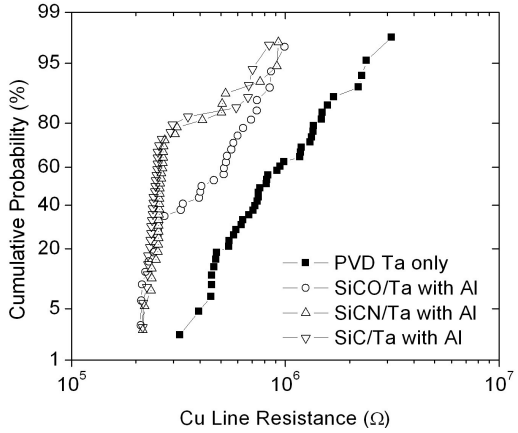

Figure 7.3 Comparison of overall Cu line resistance with different sidewall barriers.

7.4 Electrical Performance and Thermal Stability

Electrical tests indicate the composite sidewall barrier with Al interlayer improved the breakdown strength (E_{BD}) of Cu/porous ultra low-*k* interconnects from ~1.5 MV/cm to ~2.5 MV/cm (Figure 7.4a), compared to the conventional PVD Ta barrier only. Correspondingly, lower line-to-line leakage current characteristics were also achieved, as shown in Figure 7.5a. Furthermore, this Al interlayer, together with the dielectric barriers (SiCO, SiCN and SiC) on the sidewall, also contributes to a better thermal stability of Cu/porous ultra low-*k*. After a long-time burn-in test at 200°C for 120 h in air ambient, the interconnect structures with this composite barrier still show good I-E characteristics with the E_{BD} around 2 MV/cm as shown in Figure 7.4b. Similarly, the line-to-line leakage current with this composite barrier and Al interlayer was almost 2 orders of magnitude lower than that of conventional PVD Ta barrier after such a burn-in test (Figure 7.5b).

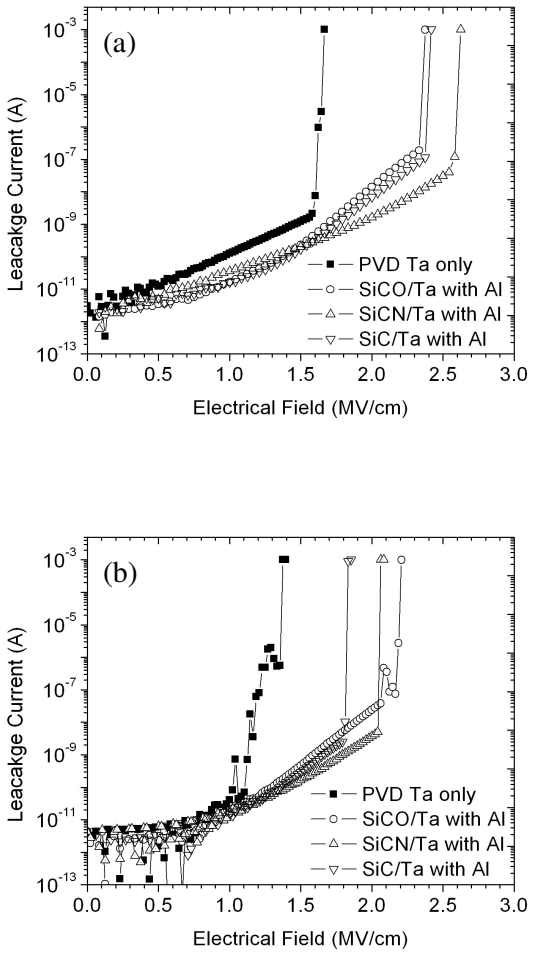

Figure 7.4 Leakage current *vs.* applied electrical field characteristics of Cu/porous ultra low-*k* interconnects with different sidewall barriers a) before and b) after burn-in test at 200°C for 120 h in air.

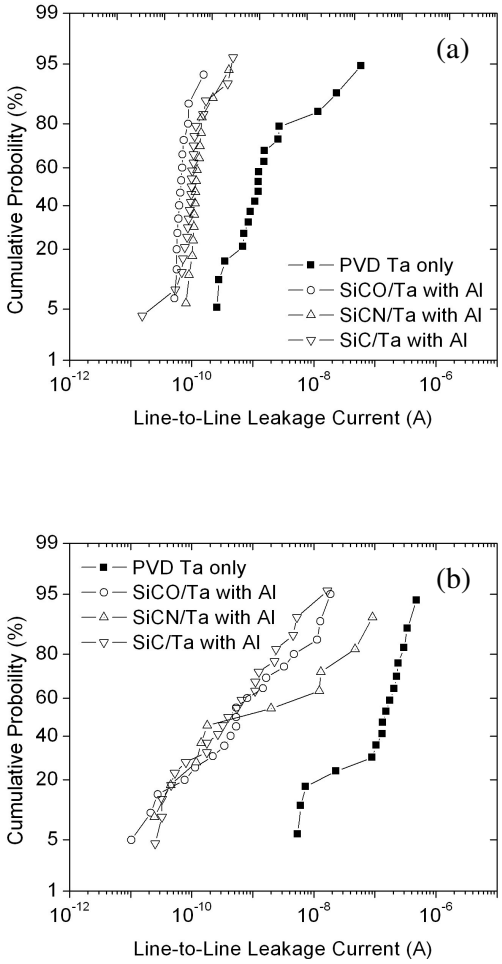

Figure 7.5 Line-to-line leakage current distribution of Cu/porous ultra low-*k* interconnects with different sidewall barriers a) before and b) after burn-in test at 200°C for 120 h in air.

7.5 Improved Barrier Efficiency by Al Stuffing Layer

The Ta diffusion barrier has two major concerns when integrated with Cu and porous ultra low-*k* dielectrics. One is its poor coverage and uniformity on the sidewall due to the high surface roughness of porous low-*k* IMD, leading to Ta penetration into the porous IMD instead of sealing it. Secondly, the polycrystalline structure of Ta is not good for use as a diffusion barrier [11], because Cu can diffuse along its grain boundaries and escape into the neighboring dielectric due to reactions between Ta and Cu even at low temperatures (200°C - 400°C) [12]. Thus new strategies for sidewall diffusion barrier need to be developed [13].

Our experimental results in Chapter 3 and Chapter 6 have shown that PECVD Silicon Carbide films could efficiently smoothen the rough sidewall surface of porous dielectrics and are helpful in achieving better step coverage and uniformity for subsequently deposited PVD Ta barrier. But the Oxygen content released from the underlying porous low-*k* IMD as well as the Oxygen contained Silicon Carbide barrier, *i.e.* SiCO film, raised another reliability concern in the Cu metallization process. It is well known that Aluminum is prone to oxidation and forms a dense Al_2O_3 layer at the surface, which could prevent further oxidation of the bulk film. A very thin Al (~10 Å) monolayer on top of Cu and/or Ta films is able to prevent the Oxygen atoms going through and protect the underlying metal layers against thermal oxidation even at high temperatures, up to 600°C [14]. Theoretical work on Cu diffusion in polycrystalline Ta barrier indicated that Cu out-diffusion could be slowed down if some dopants or impurities were added in the Ta barrier, especially in the Ta grain boundaries [15]. It was reported that a thin Al interlayer is also able to stuff the grain boundaries of TiN barrier in TiN/Al/TiN sandwich structure, and hence leading to a better barrier performance against Cu diffusion by

the formation of Al_2O_3 [16]. The mechanism was attributed to the decoration effect that Al diffuses into the TiN grain boundaries and forms Al_2O_3 by reaction with the oxygen therein [17], so that the fast diffusion paths in the polycrystalline metal barrier were stuffed. Thus further improved barrier integrity could be achieved by inserting a thin Al stuffing layer between the Silicon Carbide based dielectric layers (SiCN, SiCO and SiC) and PVD Ta barrier to block the Cu diffusion through the grain boundaries in the polycrystalline PVD Ta barrier. As a result, the electrical performance and thermal stability are significantly improved even after reducing the thickness of Ta barrier from 250 Å to 125 Å, which meets the challenging requirements for the next generation Cu/ultra low-*k* interconnect technology. As mentioned in Chapter 6, using SiCO/Ta bilayer sidewall barrier showed a poorer electrical reliability in Cu/porous ultra low-*k* interconnects after long time thermal stress compared to that of SiCN/Ta and SiC/Ta bilayer barrier. However, when the Al stuffing layer was inserted between SiCO layer and PVD Ta barrier, the Cu/porous ultra low-*k* interconnects showed a improved post-stress electrical characteristics, and did not exhibit any difference/degradation compared with other two kinds of composite sidewall barrier with SiCN or SiC underlying layers (see Figure 7.3b and Figure 7.4b). This should be attributed to the Al_2O_3 layer formed between the underlying SiCO dielectric layer and PVD Ta barrier, which could efficiently prevent Oxygen content going through and reacting with Ta barrier and Cu damascene line.

7.6 Conclusions

A composite dielectric/metal sidewall barrier with Al stuffing layer was integrated in Cu/porous ultra low-*k* damascene interconnects. The Ta barrier and

Cu seed layer exhibit α-phase texture and the preferred Cu (111) orientation when deposited on the thin Al underlying layer. As a result, lower Cu line resistance was achieved by using the composite sidewall barrier with Al stuffing layer, as well as improvements in the line-to-line leakage current and electrical breakdown strength. The electrical performance did not exhibit any degradation even after long-time burn-in test at 200°C for 120 h in air ambient. The stuffing of Al at the grain boundary diffusion paths of polycrystalline Ta barrier by the formation of Al_2O_3, in addition to preventing the Oxygen penetration, also contributed to the vastly improved electrical performance and reliability for Cu/porous ultra low-*k* damascene interconnects. The research work shown here is to investigate the possibility of using this Al interlayer/stuffing layer as a further improvement for the sidewall barrier integrity. Detailed studies in this topic could be further carried out and may require a uniform Al thin film deposition on the trench/via sidewall of damascene structures, *e.g.* employing CVD or ALD tools. This topic need to be further studied and is beyond the scope of this thesis.

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Chapter 8. Towards the Future: Sidewall Modification of Barrier/Low-*k* IMD Interface by Electron Beam Treatment

8.1 Introduction

In Chapters 3 - 7, we developed a novel dielectric/metal bilayer sidewall barrier structure for Cu/porous ultra low-*k* damascene interconnects. Detailed studies of this bilayer barrier including electrical characteristics and reliability performance were conducted. Some suggestions were also provided in order to enhance its barrier efficiency not only to prevent Cu diffusion but also to eliminate any other undesirable effects, *viz.*, oxygen penetration associated issues, associated with barrier degradation during long-term operation. This bilayer sidewall barrier is a promising candidate for the application in future 65/45 nm BEOL process, by which time feasible organic and porous low-*k* dielectrics have to be integrated with Cu damascene schedule.

As the technology node for IC manufacturing continuously progresses, the interconnect dimensions of line width and line-to-line spacing, as well as the barrier thickness, have to scale down in order to satisfy even more challenging requirements. And the interface related issues, *e.g.* surface leakage, Cu mass migration and interface condition on the sidewall, will become dominating factors for improving the interconnect performance and reliability [1]. In this situation, a more precise and efficient process control needs to be developed for Cu BEOL integration to reach the real-time IC operation criteria. The concept of bilayer

sidewall barrier structure is one approach in this direction, which improved interface condition on the sidewall by introducing dielectric modification layer and/or Al stuffing layer.

Deposition of dielectric barrier on the trench sidewall, as well as the trench/via bottom and top surface, needs additional sputtering or etch-back process before PVD metal barrier deposition and process optimization/qualification for CMP dielectric removal on the top surface. As a result, the process complexity and manufacturing cost will be increased. On the other hand, the barrier thickness on the sidewall has to be further reduced to meet the scaling down schedule. Thus, improvements only on the barrier material/structure itself are no longer enough for achieving a reliable interconnect performance. Therefore, a simple but efficient method is needed as a supplement and/or alternative way for the novel barrier system.

As revealed in Chapters 6 and 7, the unreliable Oxygen content located at barrier/low-*k* IMD interface is a key factor for interconnect reliability degradation and barrier failure. As another solution, we would like to explore a novel approach to modify the interface properties of sidewall barrier/organic low-*k* IMD, which could alleviate and/or eliminate the interfacial Oxygen contamination issue, by implementing an in-line electron beam (E-beam) treatment.

8.2 Implementation of in-line E-beam Treatment for Cu/Organic Low-*k* Damascene Interconnects

0.13 μm Cu single damascene interconnect structures were fabricated by using a spin-on organic low-*k* IMD (SiLK™ [2], k ~ 2.6). 500 Å SiCN ESL and 2000 Å

SiO_2 hard mask were deposited on top of the blanket low-*k* IMD to alleviate CMP and surface leakage issues. After the trench etching and photoresist strip were completed, the E-beam exposure was performed in a vacuum chamber at room temperature by employing an E-beam scan/lithography system. The dose and energy for this E-beam exposure are 40 μC/cm^2 and 50 keV, respectively. Since the accurate exposure/patterning is not necessary in this experiment, the E-beam spot size was intentionally adjusted to be quite big (~ few μm), in order to increase the speed of scanning cross the wafer. An identical set of samples without E-beam exposure was also fabricated for comparison purposes. Subsequently, a rapid thermal annealing step (called "Degas") at 350°C for 20 seconds was performed on all samples with and without E-beam exposure, followed by 250 Å Ta barrier and 1500 Å Cu seed layer deposition without breaking vacuum. The Degas process and Ta barrier/Cu seed layer deposition were carried out in an Applied Material™ HDP PVD system with SIP technology. After ECP Cu fill and post-ECP thermal annealing process (200°C for 30 min.), superfluous Cu and SiO_2 hard mask were removed. Then the SiCN dielectric barrier (~500 Å) and SiO_2/SiN passivation layer (~3000 Å) were deposited on the damascene structure to prevent Cu diffusion and moisture/oxygen intake during subsequent processes and thermal stress. The process flow of this E-beam treatment process is shown in Figure 8.1. Blanket samples of Ta barrier/SiLK™ film stacks were also fabricated using an identical process and thickness, with or without the E-beam exposure respectively, for physical analysis.

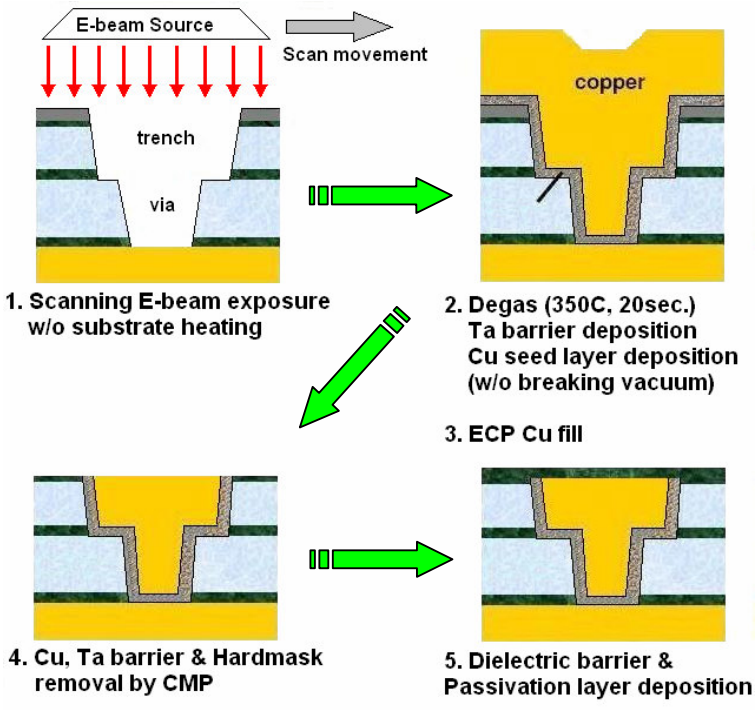

Figure 8.1 Process implementation of in-line E-beam treatment for Cu damascene integration.

Line-to-line leakage current was measured on 1 m long comb test structures, consisting of 0.18 μm wide lines with a spacing of 0.18 μm. Voltage ramp tests were performed on 0.912 m long serpentine structures sandwiched between comb structures. The line width and spacing were both equal to 0.20 μm. Both electrical measurements were carried out before and after thermal annealing cycles at 200°C in air ambient. X-ray photoelectron spectroscopy (XPS) measurements and *in-situ* Ar sputtering were carried out in a Kratos AXIS spectrometer with the monochromatic Al Kα X-ray radiation at 1486.71 eV.

8.3 Electrical Performance and Reliability Improvements

Figure 8.2 shows the typical leakage current *vs.* applied electrical field (I-E) characteristics of Cu/organic low-*k* damascene interconnects before and after burn-in at 200°C for different times in air ambient. The divergence of I-E curves before and after long-term thermal cycles (500 h burn-in at 200°C), for samples with or without E-beam treatment, should be attributed to the poor thermal/electrical properties of the organic low-*k* dielectric. However, the breakdown strengths (E_{BD}) of interconnect structures with E-beam treatment are noticeably higher than those without the E-beam treatment, regardless of before and/or after different thermal cycles. About 0.5 MV/cm improvement in E_{BD} was achieved by this in-line E-beam treatment process. Also, the line-to-line leakage current measurement shows a better characteristic for samples with the E-beam treatment (Figure 8.3a), especially after thermal annealing for different times. The leakage current was reduced by about one order of magnitude compared to samples without E-beam exposure, and even more after long-term burn-in test at 200°C for 500 h (Figure 8.3d). It is clear that the in-line E-beam treatment not only improved the electrical performance of Cu/organic low-*k* interconnects, but also had benefits on its reliability characteristics and thermal stability.

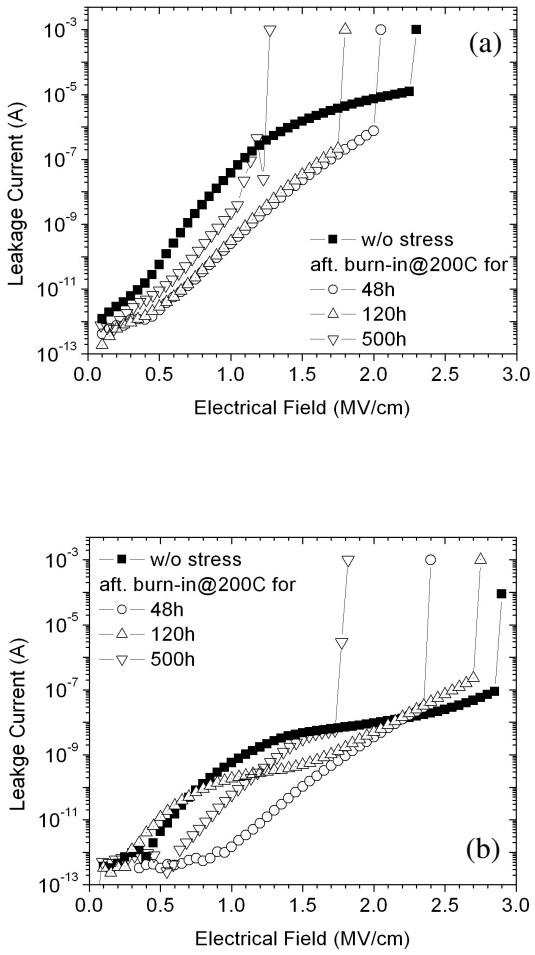

Figure 8.2 Leakage current *vs*. applied electrical field (I-E) characteristics of Cu/organic low-*k* interconnect before/after different thermal cycles at 200°C in air ambient: a) without and b) with the E-beam treatment.

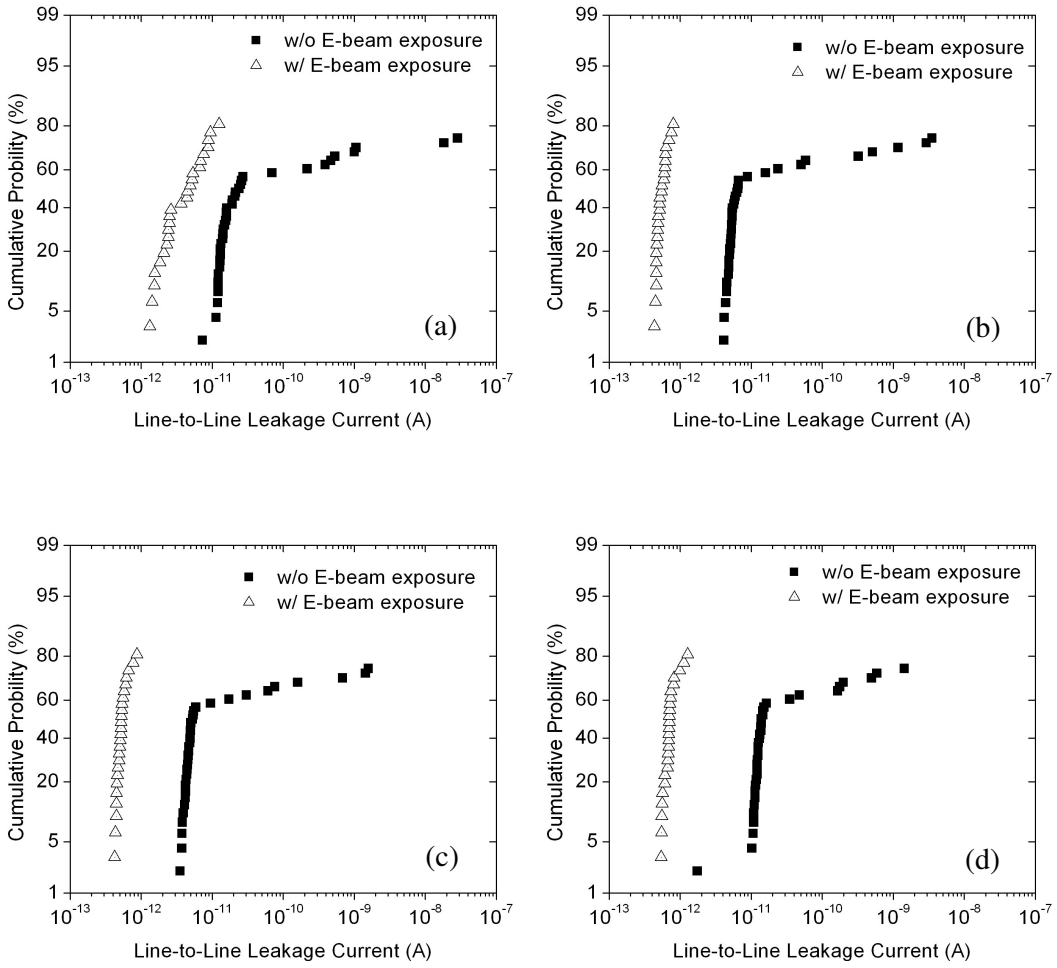

Figure 8.3 Comparison of line-to-line leakage current for Cu/organic low-*k* interconnects with and without E-beam treatment a) before any thermal stress, and after thermal stress at 200°C in air ambient for b) 48 h, c) 120 h, and d) 500 h respectively.

8.4 Influence of Scanning E-beam Exposure on the Sidewall Surface

The E-beam exposure would firstly affect the top surface of the wafer. However, very few electrons from E-beam scanning system may penetrate the 2500 Å hard mask and etch stop layers to reach the top low-*k* IMD surface, due to energy loss by scattering and/or reflection. In addition, the substrate was not heated unlike a typical immersing E-beam curing system, where the substrate is heated to high temperature (300°C - 400°C) [3]. The sacrificial SiO_2 hard mask layer on the top surface was completely removed during the CMP process. Thus the effects of E-beam exposure on top surface of low-*k* IMD are negligible. On the other hand, the direct high energy (50 keV) electrons from the E-beam source could reach the sidewall of low-*k* IMD because of the non-ideal trench profile and considering the horizontal movement of E-beam scanning. The number of electrons reaching the sidewall would be low as the trench profile is close to being perfectly vertical, and would not go deeply into the low-*k* IMD due to the small injection angle. However, the electron beam entering the trench would be scattered by trench bottom by which it will slow down and/or generate low energy secondary electrons. Some of these electrons will reach the sidewall surface. Thus, there is some fraction of low-energy secondary electrons involved in the sidewall surface modification of the organic low-*k* IMD and most of them will have much smaller energy than the E-beam source itself. Therefore the influence of this E-beam exposure on the low-*k* dielectric will be limited to the sidewall surface only. And the dielectric constant increase due to this E-beam exposure is unlikely compared to conventional as-deposited E-beam curing process, in which the entire blanket low-*k* film will be immersed and modified by the E-beam together with a thermal process [4], [5].

Curing the entire low-*k* film by immersing E-beam system could densify the low-*k* dielectric as well as improve its mechanical properties by introducing new chemical bonds, but at the expense of undesirable increase in the dielectric constant. This is because of the dissociation of the Si-CH_3 bonding and Si-O-Si random network [6], [7]. The scanned E-beam exposure system is different. It is designed as a surface engineering tool. Thus it only introduces small amount of electrons in one area for a short time and without heating the substrate. FTIR spectra from our work showed no noticeable changes in chemical bonds, which means that our scanned E-beam treatment did not affect the chemical/physical properties of the bulk low-*k* film (Figure 8.4). In-line mercury probe C-V measurement indicated the dielectric constant change of the organic low-*k* dielectric before and after the E-beam treatment was less than 1 % (Table 8.1).

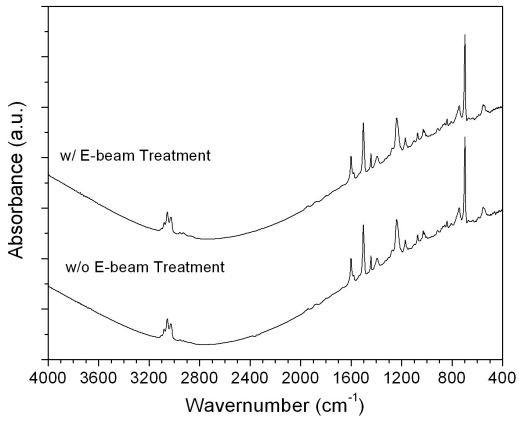

Figure 8.4 FTIR spectra of organic low-*k* dielectric with and without E-beam treatment. No noticeable changes as well as new peaks were found as a result of E-beam exposure.

Table 8.1 Measured *k* value of organic low-*k* dielectric before and after E-beam treatment

	Before E-beam Treatment	After E-beam Treatment	Percentage Change (%)
Measured *k* value (Mean of 5 samples)	2.543	2.554	0.426
Std. Dev. (%)	0.836	0.835	--

Moreover, the E-beam scanning system we used reduces the risk of charge damage due to high energy E-beam injection. The scanned E-beam moves from one small area to another on the wafer, and would not induce too many high energy electrons during the process time compared to the conventional immersing E-beam curing system [8]. The E-beam dose (40 μC/cm^2) is lower than that of immersing system (~500 μC/cm^2). As a result, no charge damage was observed under microscope as well as in-line field emission scan electron microscopy (FESEM) inspection.

8.5 Interfacial Modification by E-beam Treatment on the Surface of Organic Low-*k* IMD

Blanket Ta/organic low-*k* film stacks were employed to investigate the interfacial conditions between Ta sidewall barrier and organic low-*k* IMD by *in-situ* Ar sputtering and XPS techniques. There is a clear Oxygen peak (O1s) located at the Ta/organic low-*k* interface but not seen in the bulk of low-*k* film, after

conventional process without E-beam treatment (Figure 8.5a). The O1s spectra could be deconvoluted into two components (peaks): one corresponds to O-Ta bond (Figure 8.7a), and the other one corresponds to O-C bond (Figure 8.6b). At the Ta/organic low-*k* IMD interface, the intensity of the peak for O-Ta bond is higher than that of O-C bond. This Oxygen related chemical bonds are probably due to oxygen/moisture absorption during process transfer from deposition/etching to PVD barrier deposition, which is done in air ambient. Even though the time delay for process transfer is kept as low as possible, this surface contamination can not be avoided due to the chemical vivacities of unsaturated surface of low-*k* dielectric and Oxygen species (O_2 or moisture) in the air [9]. During the thermal process step, *e.g.* post-ECP annealing at 200°C for 30 min. or final annealing at 350°C for 30 min., it could be further trapped by forming bonds with Ta and Carbon, but may not be stable. The Oxygen contamination at the Cu/Ta barrier/IMD interface was shown to have a negative effect on the thermal stability and failure of the barrier layer [10]. As discussed in Chapter 6, the Oxygen species at the sidewall barrier/low-*k* IMD interface could diffuse out through defects located in the sidewall barrier to react with Cu in the trench [11]. When Cu is oxidized to the ionic state, it becomes a fast diffusion species and would move out of interconnects into low-*k* IMD to reach more oxidant during thermal cycles [12]. Therefore the Oxygen content located at the barrier/low-*k* IMD interface would weaken the electrical characteristics and thermal stability of interconnects [12], [13]. Furthermore, the exposure in O_2 based plasma, which is commonly used in modern back-end of line (BEOL) process to remove Photoresist [14], would considerably exacerbate this issue [15].

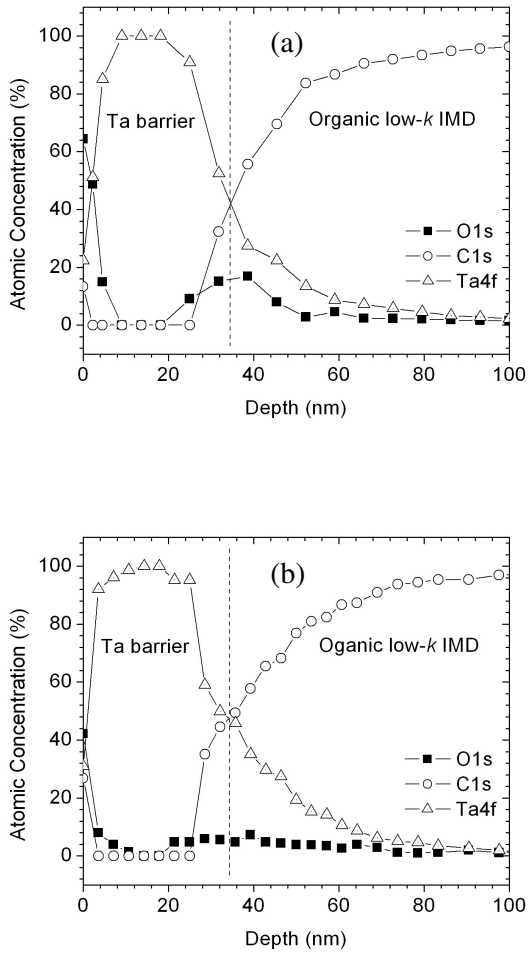

Figure 8.5 XPS depth profile of Ta barrier/Organic low-*k* IMD interface: a) without and b) with the E-beam treatment.

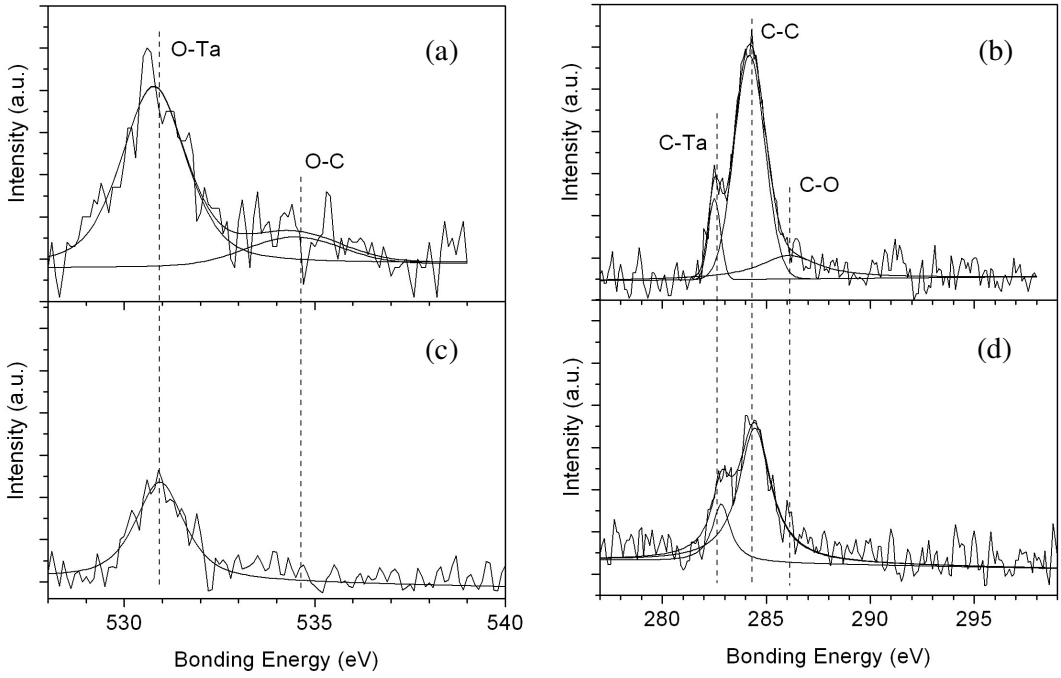

Figure 8.6 Deconvolution of XPS spectra without E-beam treatment: a) O1s and b) C1s; and with E-Beam treatment: c) O1s and d) C1s.

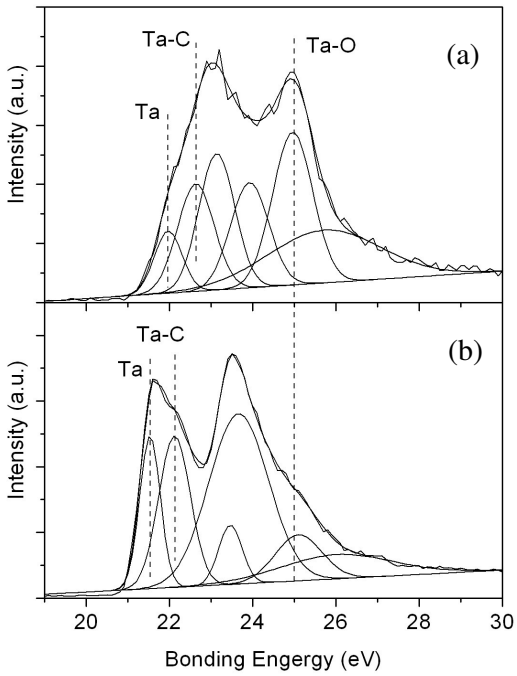

Figure 8.7 Deconvolution of XPS spectra for Ta4f: a) without E-beam treatment, and b) with E-beam treatment.

When looking at the depth profile of Ta/organic low-*k* interface with the E-beam treatment, the situation is different. As shown in Figure 8.6c, d, the C-O bond at organic low-*k* surface is not detected any more after the E-beam treatment process. And the intensities of Ta-O bond at barrier/organic low-*k* interface were obviously reduced (Figure 8.7b). As a result, Oxygen contamination was not observed in XPS depth profile after the E-beam treatment (Figure 8.5b). We hence believe that the injected electrons on the trench sidewall would break the chemical bonding of surface contaminated Oxygen, or make them easy to escape from the bonding states during E-beam treatment. During the subsequent Degas process at high temperature for a short time, the surface contaminated Oxygen would be released from the organic low-*k* dielectric. This is responsible for the electrical

performance and reliability improvements in the Cu/organic low-*k* damascene interconnect.

8.6 Conclusions

An in-line E-beam treatment was used to modify the interface condition of Ta barrier/organic low-*k* IMD without compromising the film properties and dielectric constant. Line-to-line leakage current and breakdown strength of Cu/organic low-*k* interconnects were improved by using this in-line E-beam treatment. The elimination of Oxygen contamination at the Ta barrier/organic low-*k* interface, which came from the Oxygen/moisture intake during the fabrication process, was observed as a result of the E-beam treatment process. And it is the elimination of this oxygen contamination that is responsible for the improvement in the electrical properties of Cu damascene interconnects. By using this new method of non-destructive E-beam modification, a simple and precise control of interface condition between barrier layer and low-*k* IMD was achieved, which is important for the reliability enhancement of future 65/45 nm technology node Cu/ultra low-*k* BEOL process.

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Chapter 9. Conclusions and Recommendations for Future Research

9.1 Conclusions

In this work, a novel dielectric/metal bilayer sidewall barrier was developed for Cu/porous ultra low-*k* damascene interconnects. Detailed studies of this bilayer barrier structure demonstrated that Silicon Carbide based dielectric layers could efficiently seal the porous surface on the sidewall and result in improved electrical characteristics and reliable interconnect performance. This bilayer sidewall barrier is a promising candidate for the application in future 65/45 nm BEOL process, by which time feasible organic and porous low-*k* dielectrics have to be integrated with Cu damascene schedule. Moreover, a pseudo-breakdown phenomenon was observed in Cu/porous ultra low-*k* damascene interconnects. And the physical mechanisms behind this pseudo-breakdown behavior was investigated and related to the barrier integrity. Our studies showed that, by using the optimized bilayer barrier structure which increases the proportion of dielectric modification layer/diffusion barrier, this undesirable pseudo-breakdown behavior could be avoided.

In addition, our studies in Cu BEOL process and barrier integrity found that unstable Oxygen content in low-*k* dielectrics as well as Oxygen containing dielectric barrier have a negative influence on long-term interconnect reliability. It may exacerbate the interface condition between the sidewall barrier and low-*k* IMD and lead to an oxidation-induced (fast) Cu diffusion. Some suggestions and

preliminary experiments were carried out to further enhance the barrier efficiency, not only to prevent Cu diffusion but also to address this Oxygen-related barrier degradation issue. Inserting an Al interlayer between the metal and the dielectric sidewall barrier is a practical way not only to stuff the grain boundary diffusion paths for Cu in polycrystalline Ta barrier, but also prevent its oxidation by forming a dense Al_2O_3 sacrificial layer. Another approach is using an in-line E-beam treatment to release the Oxygen content at the sidewall surface of the low-*k* IMD during the process. It has the advantages of process compatibility and easy implementation, which means low fabrication cost.

9.2 Recommendations for Further Research on Cu Diffusion Barrier

9.2.1 Barrier Material Evaluation

PECVD dielectric barriers have some advantages in Cu damascene process. CVD method provides ideal step-coverage on the sidewall of high respect-ratio Cu via/trench [1]. And its chemical compatibility with most low-*k* and ultra low-*k* dielectrics (Silicon and/or Carbide based) may be helpful to alleviate the interface issues, *e.g.* interfacial defects and dangling bonds, in Cu metallization process [2], [3]. However, conventional SiN dielectric diffusion barrier/passivation layer is no longer acceptable for Cu/low-*k* and Cu/ultra low-*k* BEOL integration due to its high dielectric constant. The efficient way to lower the *k* value of dielectric barrier is to incorporate low polarizability Carbide as well as methyl groups (-CH_3 and -(CH_2)n) by using organosaline precursors, which is similar to CVD low-*k* dielectrics. But this would also compromise the diffusion barrier performance.

Therefore there must be a trade-off between the barrier efficiency and its dielectric constant [4]. Moreover, recent studies indicate that Nitrogen species in the ESL/dielectric barrier will considerably poison the phtoresist during lithography process and lead to undesirable pattern results, especially on narrow lines [5]. Thus, the Nitrogen-free ESL/dielectric barrier system is urgently required for BEOL integration schedule.

Additionally, there is an increasing trend to develop a new low-*k* IMD which is also able to work as a diffusion barrier [6], [7]. Initial work in this area was to employ plasma, E-beam or ion implantation technique to modify the low-*k* dielectrics to form a thin and dense barrier layer on its surface [8], or properly change the properties of the whole low-*k* film. The final goal is to achieve a barrier-free low-*k* material which has a low enough dielectric constant and also has good resistance against Cu diffusion/drift.

9.2.2 New Barrier Architecture

Reliability issues are getting more and more serious in Cu BEOL process because the interconnect feature size continuously scales down towards 65/45 nm technology node, and new kinds of low-*k* and ultra low-*k* dielectrics are scheduled for Cu damascene integration [9]. In conventional Cu damascene architecture, poor interface condition between Cu and above dielectric barrier is always the weak point for Cu electromigration and stress migration failure [10]. As a new architecture, conductive metal films were coated as a barrier layer instead of dielectric capping layer/diffusion barrier on the top of Cu damascene lines and showed an improved electromigration performance [11], [12]. On the other hand, surface leakage current as well as interfacial Cu diffusion along dielectric capping

layer/low-*k* interface is another issue which considerably degrades the TDDB lifetime of Cu/low-*k* damascene interconnects [13]. The heterojunction interface between dielectric barrier and low-*k* IMD, which involves interface defects and unsaturated chemical bonds, is a major reason for such electrical and reliability degradation. The process solution for this issue could be achieved by inserting a dielectric layer between dielectric capping layer and low-*k* IMD, or leave some amount of hard mask layer without completely polishing [14], [15]. Research work in these new barrier architectures are just in the initial stages and need to be further developed.

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9.2.3 Demands and Application in 3D Interconnects

Interest in Three-dimensional (3D) interconnects has grown significantly in the last few years as the industry works towards high-density and multi-functional ICs. It is a promising technology to increase the IC functionality, which enables high-density interconnect not only at the conventional horizontal IC surface, but also in the vertical direction through the active layer and substrate of IC chips by employing large diameter (~10 μm) through-wafer Cu via [16]. On the via sidewall, a thick dielectric barrier/buffer layer (>100 nm) is necessary between Silicon active layer/substrate and Cu via for electrical insulation. Besides the good properties against Cu diffusion/drift, this dielectric layer also needs to work as a thermal/mechanical buffer between Cu film and Silicon substrate due to the CTE difference (Cu ~ 16.12 ppm/ºC and Si ~ 2.6 ppm/ºC) as well as thermal/mechanical stress problem [17], [18]. Therefore a low-stress and thermally/mechanically matched dielectric barrier is highly essential for the 3D interconnect architecture.

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