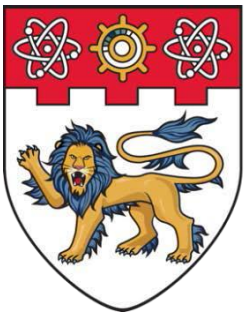

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RELIABILITY STUDY OF COPPER WIRE BONDING AND THROUGH SILICON VIA

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SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

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A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

2020

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

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Authorship Attribution Statement

This thesis contains material from 6 papers published in the following peer-reviewed journals and from papers accepted at conferences in which I am listed as an author.

Chapter 3 is published in the following papers:

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The contributions of the co-authors are as follows:

- Assoc Prof Tan Cher Ming provided the initial project direction.
- Assoc Prof Tan Cher Ming, Assoc Prof Tan Chuan Seng and Mr. Lee Kheng Chooi edited the manuscript drafts.
- I prepared the manuscript drafts.
- I performed all reliability stress test and physical failure analysis at Infineon Technologies Asia Pacific Pte Ltd.
- All electrical characterization was conducted by me in the Electronic System Measurements Laboratory. I also analyzed and interpret the data.

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[1] J. M. Chan, X. Cheng, K. C. Lee, W. Kanert, C. S. Tan, “Reliability Evaluation of Copper (Cu) Through-Silicon Via (TSV) Barrier and Dielectric Liner by Electrical Characterization,” in *2016 IEEE 18th Electronics Packaging Technology Conference (EPTC)*, Singapore, 30 Nov – 3 Dec 2016, pp. 478 – 82.

[2] J. M. Chan, C. S. Tan, K. C. Lee, X. Cheng, and W. Kanert, “Observations of copper (Cu) transport in through-silicon vias (TSV) structure by electrical characterization for its reliability evaluation,” in *2017 IEEE International Reliability Physics Symposium (IRPS)*, Monterey, CA, USA, 2-6 April 2017, pp. 4A3.1-4A3.6.

[3] J. M. Chan, X. Cheng, K. C. Lee, W. Kanert, C. S. Tan, “Reliability Evaluation of Copper (Cu) Through-Silicon Via (TSV) Barrier and Dielectric Liner by Electrical Characterization and Physical Failure Analysis (PFA),” in *2017 IEEE 67th Electronic Components and Technology Conference (ECTC)*, Orlando, FL, USA, 30 May – 2 Jun 2017, pp. 73-9.

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- Assoc Prof Tan Chuan Seng, Mr. Lee Kheng Chooi, Ms. Xu Cheng and Mr. Werner Kanert edited the manuscript drafts.
- I prepared the manuscript drafts.
- I performed all reliability stress test and some of the physical failure analysis at Infineon Technologies Asia Pacific Pte Ltd.
- All electrical characterization was conducted by me in the Semiconductor Characterization 2 laboratory. I also analyzed and interpret the data.

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Table of Contents

Acknowledgements I

Executive Summary VI

List of Tables X

List of Figures XI

Chapter 1 Introduction 1

1.1 Background 1

1.2 Motivations 3

1.3 Research Objectives 5

1.4 Major Contributions of the Thesis 7

1.5 Organization of Thesis 10

References 12

Chapter 2 A Review of Copper Interconnects and its Reliability Challenges 13

2.1 Overview of Wire Bonding 13

2.1.1 Wire Bonding Process 15

2.1.2 Challenges of Cu Wire Bond 19

2.1.3 Wire Bond Evaluation Techniques 24

2.1.3.1 Destructive Techniques 24

2.1.3.1.1 Pull Test 25

2.1.3.1.2 Shear Test 30

2.1.3.2 Non-destructive Techniques 32

2.1.3.3 Diode Series Resistance Extraction Method 33

2.2 Overview of Copper TSV 36

2.2.1 TSV Fabrication Process 37

2.2.2 Cu TSV Reliability Concerns 41

2.2.3 Current Reliability Study Status 43

2.2.4 Conduction Mechanisms 44

2.2.4.1 Fowler-Nordheim (FN) Tunneling 46

2.2.4.2 Schottky Emission (SE) 48
2.2.4.3 Poole-Frenkel (PF) Emission 50
2.2.4.4 Ohmic Conduction 52
2.2.4.5 Space-Charge Limited Conduction (SCLC) 53
2.2.4.6 Ionic Conduction 55
2.2.5 Time Dependent Dielectric Breakdown (TDDB) 56
2.2.5.1 E Model 57
2.2.5.2 $\frac{1}{E}$ Model 58
2.2.5.3 $\sqrt{E}$ Model 59
2.2.5.4 Lloyd Model 60
2.2.5.5 Power Law Model 61
2.2.5.6 Uncertainties and Current Status of TDDB Models 62
2.3 Accelerated Stress Test 65
2.3.1 Temperature Cycling 65
2.3.2 High Temperature Storage Life 66
2.3.3 Unbiased Highly-Accelerated Temperature and Humidity Stress Test 66
2.4 Summary 67
References 68
Chapter 3 Study of Copper Wire Bonding 78
3.1 Introduction 78
3.2 Experiment Setup 79
3.3 Results and Discussion 82
3.4 Summary 92
References 94
Chapter 4 Study of Copper TSV 95
4.1 Introduction 95
4.2 Experiment Setup 96
4.3 Results and Discussion 99
4.3.1 Non-destructive Detection of Barrier Degradation 99

4.3.2 Electrical Characterization Post-Reliability Stress Test 105
4.3.3 Comparison between Dielectric Material 115
4.3.4 Comparison between Structure with and without Si_3N_4 Capped Layer 116
4.3.5 Comparison between Stress Condition 119
4.3.6 Current Conduction Mechanism 122
4.4 Summary 126
References 128
Chapter 5 Effects of Cu Migration on TDDB 130
5.1 Control and Monitoring of Cu Drifts 130
5.2 Influence of Copper on TDDB Lifetime 135
5.2.1 Oxidation state of Cu ions 138
5.2.2 Extension of TDDB lifetime 144
5.3 TDDB Modelling 146
5.4 Summary 148
References 149
Chapter 6 Conclusion and Future Work 150
6.1 Conclusion 150
6.2 Future Work 154
List of Achievement and Publications 156

Executive Summary

Interconnects are necessary for the electrical connection of an integrated circuits (IC). Therefore, its quality and reliability are vitally important to ensure that a device is working as it is intendedly designed. The continued scaling of devices and the desire for higher functionality and capability has led to the exploration for new interconnect technologies and new materials in order to enhance chip performances. One of the most widely used interconnect method by the IC manufacturing industry is wire bonding. In order to remain competitive as one of the key interconnect technologies in the market, copper (Cu) wires have recently been adopted to replace gold (Au) due to its lower costs and more desirable material properties. Apart from Cu wire bonding, through silicon via (TSV) technology has also in recent years, been actively pursued and has become one of the key enablers for three dimensional (3D) IC. It allows for vertical interconnection of dies, which not only overcome spatial limitations, but also enables the possibility of heterogeneous integration to enhance functionality and performance. Although there are several advantages that Cu wire bonding and TSV interconnect technology can offer, there are also several reliability concerns that have not been well addressed which requires further study. Therefore, the reliability of Cu wire bonding and the reliability of Cu TSV will be studied in this work.

In the first part, wire bonding and its reliability are discussed. The migration to Cu wire from Au has resulted in more stringent and narrower wire bonding process window. During the wire bonding process, several parameters need to be well controlled in order to achieve a well-bonded wire. Current industrial practice for evaluating the quality of wire bonds after the packaging and assembly process are either done destructively or non-destructively, which may result in loss of critical information or are limited by resolution, cost and time respectively. In this work, Cu wire bonds are subjected to accelerated stress test of temperature cycling (TC) -65/175 °C up to 700 cycles for its quality and reliability assessment. The Cu wires are evaluated by electrical means which

are non-destructive, fast and accurate. This makes it suitable for use in the production line for wire bond quality evaluation. Based on the electrical measurement results, it can be observed that the change in resistance increases with the number of temperature cycles, and it is significant between 600 and 700 cycles with a percentage increase of more than 300%. In addition, Cu wires evaluated using the electrical measurement results also showed that there is good correlation with conventional wire pull test assessment method, where an increase in resistance resulted in a decrease in pull strength. However, the rate of change in pull strength was found to be more than 2 times slower for wires breaking at the span as compared to wires breaking at the neck region. This suggests that the electrical method could be more sensitive to detect degradation at the wire span region as compared to the pull test wire method. Failure analysis by removal of the mold compound of the package and inspecting the wires using scanning electron microscopy (SEM), were also performed and verified the degraded wire measured using the electrical method. One observation is that the stress condition of TC -65/175 °C up to 700 cycles did not cause significant degradation on the bond pad interface as Cu ball remnant was observed to be left behind on the bond pad after shear test.

In the second part, TSV interconnect technology and its reliability is discussed. Currently, most studies concentrate on reliability studies under mild and less harsh stress conditions as compared to the automotive stress test standards. In this work, qualification stress test of automotive standards were performed on TSV structures which are fabricated using optimized processes. Experimental results reveal that the leakage current performance after accelerated stress test was dependent on the dielectric layer material, as well as the presence of silicon nitride (Si_3N_4) deposition above the TSV structures, used to emulate die stacking in the experiment. Results show that the leakage current is higher for low-k liner TSV structures as compared to the plasma enhanced tetraethylorthosilicate (PETEOS) liner TSV structures. The difference is approximately 1 order of magnitude after high temperature storage life (HTSL) stress

test at 175 °C for 1000 hours and TC stress test at -55/150 °C for 2000 cycles, under an electric field of 1.5 MV/cm. This is expected due to the higher porosity of low-k dielectric. Results also reveal that permanent dielectric breakdown was observed for TSV structures that were suppressed by a layer of Si_3N_4 after accelerated stress test. On the other hand, no breakdown was observed for TSV structures without the existence of the Si_3N_4 layer suggesting that there might be thermomechanical stress induced on the TSV side wall for the suppressed TSV structure. Failure analysis performed on a PETEOS liner TSV sample with decreasing leakage trend after HTSL 225 °C for 1000hrs found severe Cu protrusion as much as 4.7 um above the wafer surface. As a result of the severe Cu protrusion, voids within the TSV and in the dielectric layer, as well as delamination between the Cu TSV and dielectric layer interface were present. As Cu diffuses readily in dielectric layer and the silicon substrate, a non-destructive electrical characterization was performed to detect copper migration in a degraded TSV structure after various stress conditions such as at an elevated temperature, temperature cycling and electrical biasing. The stress test were performed either independently without electrical bias or in a combination with electrical bias for comparison. Variations in the electrical characteristics in the form of a change in the inversion capacitance of a *C-V* characteristic curve reflects the presence of copper ions within the dielectric layer. Physical failure analysis (PFA) was performed and verified the presence of migrated copper, correlating to the changes observed in the electrical characteristics. Various conduction mechanisms were fitted with experimental data before and after degradation and it was deduced that the Poole-Frenkel (PF) conduction mechanism is the most dominant mechanism on degraded structure after a period of idle. This is found to be dependent on the oxidation state of copper, which was verified to change from Cu_2O to CuO over time as indicated in the x-ray photoelectron spectroscopy (XPS) analysis.

In the third part, with the understanding of the change in the non-destructive electrical characteristics with respect to the presence of Cu ions within the dielectric layer,

attempts were made to demonstrate the ability to monitor and control the transport of Cu ions by applying an appropriate *E*-field, which will be useful for subsequent reliability assessment. TDDB experiments were performed and found that the presence of copper could play different roles within the dielectric and may accelerate or decelerate time to failure dependent on the applied *E*-field, temperature and also the oxidation state of the Cu ions. TDDB lifetime models were fitted experimentally and is found to be in good agreement to the $\sqrt{E}$ model. The $\sqrt{E}$ model was verified experimentally by measuring the time to failure at low *E*-field, rather than extrapolating data from high *E*-field.

List of Tables

Table 2.1: Material properties of Au, Cu and Al [4, 5]. 14

Table 2.2: Comparison of different bonding techniques. 16

Table 2.3: Summary of current conduction mechanism in insulators. 45

Table 4.1 List of test structures. 96

List of Figures

Figure 1.1 Keeping up with Moore's Law (1971-2018) [2]. 1
Figure 2.1 General wire bonding process cycle [4]. 17
Figure 2.2 Irregular FAB formation resulting in a golf club ball formation. 20
Figure 2.3 Irregular FAB formation resulting in a flat ball bond formation. 20
Figure 2.4 Aluminum pad squeezed after wire bonding. 21
Figure 2.5 Cratering on bond pad revealing internal circuitry post wire bond shear test. 21
Figure 2.6 Pitting on the Cu wire ball surface due to corrosion. 22
Figure 2.7 X-section image of Cu creep corrosion between bonding interface. 22
Figure 2.8 Overly etched Cu wire surface due to un-optimized decapsulation recipe. 23
Figure 2.9 Location of failures after destructive pull test [4]. 26
Figure 2.10 Grain structure of a wire after ball formation [19]. 28
Figure 2.11 Geometrical variables of a wire bond pull test [19]. 29
Figure 2.12 Pull force against wire loop height [19]. 30
Figure 2.13 Failure modes after shear test [4]. 31
Figure 2.14 Shear force against wire bonded area [19]. 32
Figure 2.15 TSV fabrication by (a) via-first; (b) via-middle; (c) front side via-last; and (d) back side via-last approach [27]. 38
Figure 2.16 Brief process flow of Cu TSV [28]. 39
Figure 2.17 Schematic of a BOSCH RIE process [27]. 40
Figure 2.18 Schematic energy band diagram of FN tunneling in MOS structure [53]. 46
Figure 2.19 Schematic energy band diagram of direct tunneling in MOS structure [53]. 47
Figure 2.20 Schematic energy band diagram of SE in MOS structure [53]. 49
Figure 2.21 Schematic energy band diagram of PF emission in MOS structure [53]. .50
Figure 2.22 Schematic energy band diagram of hopping conduction in MOS structure [53]. 51

Figure 2.23 Schematic energy band diagram of Ohmic conduction in MOS structure [53].....52
Figure 2.24 A typical Log (J) Vs Log (V) plot of a SCLC leakage current [53].....53
Figure 2.25 Percolation path between the cathode and anode. 56
Figure 2.26 Various TDDB model showing divergence at lower *E*-field and convergence at higher *E*-field. 62
Figure 3.1 Resistor components in current path during electrical measurement. 79
Figure 3.2 Ball bond inspection of an unstressed wire using (a) optical image and (b) SEM image after dry plasma decapsulation. 80
Figure 3.3 Dual pad structure with different loop height.....81
Figure 3.4 Delta R/R vs Stress Cycle plot. 82
Figure 3.5 t-score at various readout for statistical significance 83
Figure 3.6 SEM micrograph of bonded wires after temperature cycling of (a) 400 cycles; (b) 600 cycles and (c) 700 cycles. 83
Figure 3.7 Resistance Change Vs Pull Strength plot after temperature cycling of (a) 400 cycles; (b) 600 cycles and (c) 700 cycles. 84
Figure 3.8 Wire neck and span break mode after wire pull test. 85
Figure 3.9 Resistance Change Vs Pull Strength plot separating wire loop height and failure mode. 86
Figure 3.10 Normal probability plot using Benard's median rank method on inner pad wires after temperature cycling of (a) 400 cycles; (b) 600 cycles; (c) 700 cycles; and on outer pad wires after temperature cycling of (d) 400 cycles; (e) 600 cycles and (f) 700 cycles. 87
Figure 3.11 SEM micrograph of wires out of confidence bound and within confidence bound at (a) 400 cycles; (b) 600 cycles and (c) 700 cycles. 88
Figure 3.12 Resistance Change Vs Shear Strength plot. 90
Figure 3.13 SEM micrograph showing Cu ball remnant on pad after shear test. 90
Figure 3.14 SEM cross-sectioned image of (a) as received and (b) post TC 700 cycles ball bond. 91

Figure 4.1 Schematic diagram of test structure 1 with blind via. 97
Figure 4.2 *C-V* curve of as received and high temperature stressed samples. 100
Figure 4.3 *J-E* curve of as received and high temperature stressed samples. 101
Figure 4.4 TEM micrograph of (a) as received sample and (b) high temperature stressed sample. 102
Figure 4.5 TEM-EDX elemental mapping comparing the Ti barrier layer of (a) as received sample and (b) high temperature stressed sample. 103
Figure 4.6 TEM-EDX elemental mapping by area scan showing Cu diffusion into the dielectric layer of a high temperature stressed sample.....103
Figure 4.7 TEM-EDX elemental mapping by line scan showing Cu diffusion into the dielectric layer of a high temperature stressed sample.....104
Figure 4.8 TEM-EDX elemental mapping by line scan showing no Cu diffusion into the dielectric layer as received. 104
Figure 4.9 Comparison of C-V curves of fresh sample with (a) TC -55/150 °C readout; (b) TC -65/150 °C readout and (c) HTS 175 °C readout. 106
Figure 4.10 Comparison of Log (J) vs E curves of fresh sample with (a) TC -55/150 °C readout; (b) TC -65/150 °C readout and (c) HTSL 175 °C.....106
Figure 4.11 Comparing *C-V* curve before and after subsequent electrical bias post (a) TC -65/150 °C 1000 cycles and (b) HTSL 175 °C 1000 hours. 107
Figure 4.12 Schematic diagram of test structure 3 without blind via. 108
Figure 4.13 Comparing *C-V* curves of structures without blind via when as-received, as-received + electrical bias, TC -65/150 °C 1000 cycles and TC -65/150 °C 1000 cycles + electrical bias. 109
Figure 4.14 X-sect SEM micrographs of blind via structure after TC -65/150 °C, 1000 cycles showing (a) overview; (b) bottom; (c) crack site 1 propagating into dielectric layer; and (d) crack site 2 propagating into dielectric layer. 110
Figure 4.15 X-sect SEM and TEM micrographs of blind via structure as received showing (a) overview; (b) bottom; (c) TEM of site 1; and (d) TEM of site 2. 111

Figure 4.16 (a) Overlay of 3 TEM micrographs showing the overview cross-sectioned blind via structure at a crack site; (b) TEM micrograph indicating EDX spot near a crack site; (c) TEM micrograph indicating EDX spot away from a crack site; (d) Energy spectrum of EDX spot in (b); and (e) Energy spectrum of EDX spot in (c). 112
Figure 4.17 Optical image (top view) of test structure 2 with an array of 200 blind vias. 113
Figure 4.18 *C-V* characteristics of as received and TC -65/150 °C, 2000 cycles post stressed array structure. 114
Figure 4.19 Log (J) Vs E characteristics of as received and TC -65/150 °C, 2000 cycles post stressed array structure. 114
Figure 4.20 Schematic diagram of test structure 4 with Ta diffusion barrier. 115
Figure 4.21 Leakage current between PETEOS and low-k liner after (a) 1000 hours of HTSL 175 °C; and (b) 2000 cycles of TC at -55/150 °C. 116
Figure 4.22 Schematic diagram of test structure 5 with Si_3N_4 layer capping. 117
Figure 4.23 Breakdown observed for Si_3N_4 capped structures for PETEOS liner blind via after 500 hours of HTSL 225 °C. 118
Figure 4.24 Breakdown irrecoverable after three measurements for PETEOS liner blind via after 500 hours of HTSL 225 °C. 118
Figure 4.25 Leakage current different readouts for (a) PETEOS liner blind via at HTSL 225 °C; (b) low-k liner blind via at HTSL 175 °C; and (c) PETEOS liner blind via at TC -55/150 °C. 119
Figure 4.26 SEM micrograph of Cu blind vias for (a) PETEOS liner blind via after HTSL 225 °C; (b) low-k liner blind via after HTSL 175 °C; and (c) PETEOS liner blind via after TC -55/150 °C. 120
Figure 4.27 Cross-sectioned SEM micrograph of a PETEOS liner blind via after 1000 hours of HTSL 225 °C stress. 121
Figure 4.28 Cross-sectioned SEM micrograph showing delamination between Cu and PETEOS liner interface after 1000 hours of HTSL 225 °C stress. 122

Figure 4.29 TEM micrographs showing voids within the PETEOS dielectric layer at (a) bottom of blind via; and (b) bottom right corner of blind via. 122
Figure 4.30 Refractive index of fabricated dielectric layer measured from an optical ellipsometer. 124
Figure 4.31 Poole-Frenkel plot of samples at various stages. 125
Figure 5.1 *C-V* characteristics after high temperature stressing at 400 °C , negative bias and positive bias sequentially. 131
Figure 5.2 *C-V* characteristics of a high temperature stressed sample with different biasing sequence and duration. 132
Figure 5.3 *C-V* characteristics of high temperature stressed samples measured at various elevated temperature after negative *I-V* sweep. 133
Figure 5.4 *C-V* characteristics of high temperature stressed samples measured at various elevated temperature without negative *I-V* sweep. 134
Figure 5.5 TDDB comparison of samples between positive drift, negative drift and without pre-stress at 7 MV/cm, 75 °C. 135
Figure 5.6 TDDB comparison of samples between negative drift and positive drift at 3-4 MV/cm, 175 °C. 136
Figure 5.7 TDDB comparison of samples between negative drift and positive drift at 6-7 MV/cm, 125 °C. 137
Figure 5.8 Leakage current profile of samples that are (a) newly stressed at 400 °C and (b) stressed at 400 °C with a period of idle. 139
Figure 5.9 Leakage current profile of stressed samples with (a) negative drift and (b) positive drift. 139
Figure 5.10 De-convoluted peaks showing different Cu oxidation states after exposure to (a) a few hours, (b) 1 day, (c) 3 days, (d) 7 days, (e) 14 days and (f) more than 2 months in air. 141
Figure 5.11 TDDB lifetime comparison after negative and positive drift on newly stressed (400 °C) and stressed (400 °C) samples with a period of idle. 143

Figure 5.12 TDDB comparison of samples with negative drift of different durations at 7 MV/cm, 75 °C.....144
Figure 5.13 TDDB comparison of samples with various drift sequence at 5 MV/cm, 175 °C.....145
Figure 5.14 TDDB model of a degraded sample after high temperature stress.....146

Chapter 1

Introduction

1.1 Background

Interconnects which are responsible for the transmission of electrical signals and providing power to an integrated circuit (IC) can be classified into 2 major categories namely the on-chip interconnect and off-chip interconnect [1]. On-chip interconnects usually refers to metal layers that are deposited on the wafer, during the front end of line (FEOL) IC fabrication step. Off-chip interconnects on the other hand, are usually interconnections between the IC chip and the outside world, formed at the back end of line (BEOL) IC fabrication step.

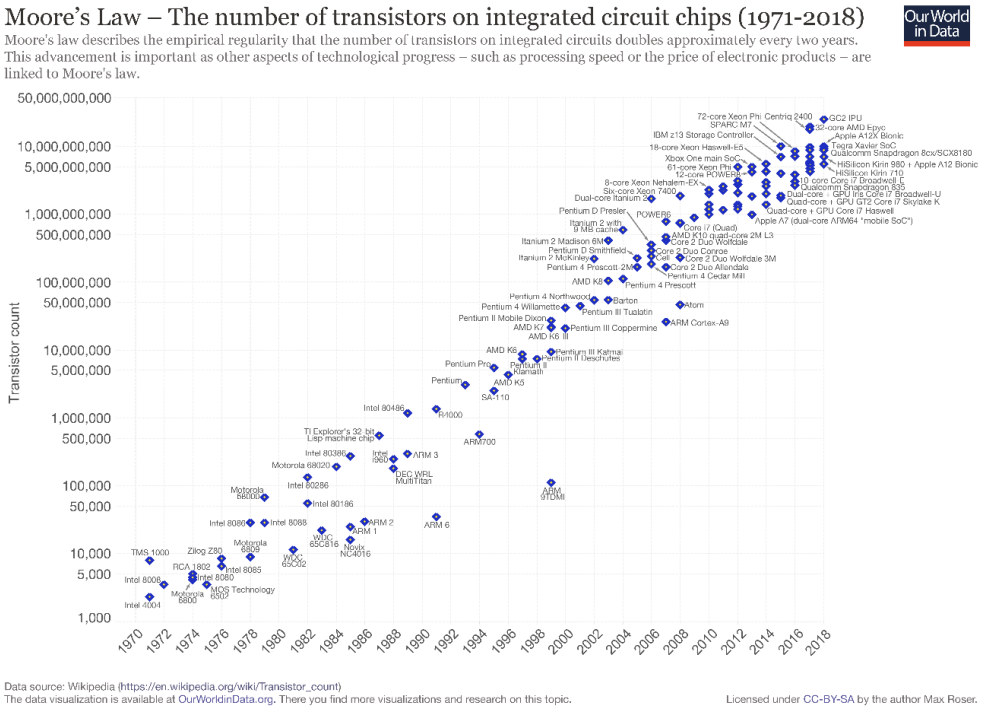

Figure 1.1 Keeping up with Moore's Law (1971-2018) [2].

According to Gordan E. Moore in 1965, he predicted that the number of transistor on a single chip is expected to double every two years, which is also known as

Moore's law today. As shown in Figure 1.1, Moore's law seems to be accurate even recently into 2018. However, the last revision of the International Technology Roadmap of Semiconductors (ITRS) was published in 2015, suggesting the end of the Moore's law era. It takes huge investments and efforts from semiconductor manufacturers to keep up with Moore's law over the years and it is inevitable that it will slow down not only due to design manufacturing cost, but also physical limitations to further shrink a transistor.

The microelectronic industry desire for higher functionality and capability in the IC chip, has led to problems in interconnect technologies. In order to meet the demands of increasing input/output (I/O) count, manufacturers resort to explore new interconnect technologies and new materials to keep up with device scaling in order to fully enhance chip performances. One of the most widely used interconnect technology in the microelectronic industry is gold (Au) wire bonding. However, due to its long wire span formed during wire bonding process, resistance is inevitably increased resulting in a drop in device performance. As a result, different wire bonding materials are considered such as copper (Cu). Cu have gain popularity as the material of choice for interconnects in recent years due to its superior electrical and thermal conductivity. Cu has an advantage of having a lower electrical resistivity of 1.7×10^{-8} Ω.m as compared to 2.2×10^{-8} Ω.m for Au wire, which is highly desirable for device performance. Cu also has a better thermal conductivity of 400 W/mK as compared to 320 W/mK for Au, which allows quicker heat dissipation making it suitable for high power applications. In addition, quicker heat dissipation also improves the overall interconnect reliability as failure mechanisms are often accelerated by increased temperatures [3]. Last but not least, Cu also has an added advantage of being relatively cheaper as compared to Au. While Cu has many advantages, they are not without challenges. Depending on the interconnect technology, Cu also possesses properties that may be challenging during the interconnect process. Difficulties also arise from having to address new reliability concerns and the need for stringent process control.

Alternatively interconnect technologies such as through silicon via (TSV), which is a three dimensional (3D) interconnect technology has also attracted much attention in recent years. It has added advantage over the conventional wire bonding technology which is limited by both electrical performance and interconnect density, since wire bonding can often only be bonded at the peripheral of the die. TSV on the other hand, is able to achieve shorter and denser interconnection through vertical interconnects that passes through the silicon die. However, fabricating vertical interconnects that pass through dies containing substrate, devices, and metal layers, poses manufacturing and performance challenges. Therefore, interconnect technologies, whether wire bonding or TSV, are in no doubt one of the important factors that determines the overall IC package form factor, electrical and reliability performance.

1.2 Motivations

The introduction of Cu to replace Au wire bonding, may have brought several advantages to the interconnect technology, but it also introduces several new failures modes and mechanism which were not previously observed in Au wire bonding. These failure mechanisms, as well as potentially new failures, are still not fully understood and require more in-depth study. Manufacturing processes and tools also needs to be altered to accommodate the difference in material properties between Cu and Au in order to achieve quality bonding and to meet its subsequent reliability requirements.

Alternative interconnect technology such as TSV which has been one of the key enabler for 3D IC have also been explored due to several advantages that it can provide over conventional wire bonding. However, due to its design and structure which is embedded within the silicon die, it has to be electrically isolated with a barrier and dielectric layer. Moreover, due to its close proximity to neighboring active devices, the integrity of the barrier and dielectric layer becomes even more

important as it determines if the entire device eventually works well throughout its reliability lifetime. In addition, given its small dimensions and limitations in aspect ratio during process fabrication, quality issues are bound to surface which needs to be identified and understood on its impact on reliability performance.

Therefore, interconnects in the form of new material and new interconnect technologies are still facing several process, manufacturing as well as reliability challenges, especially in harsher automotive grade reliability requirements. Such challenges needs to be well addressed before it can be fully adopted and implemented by the manufacturing industries. Therefore it is the motivation of this work to perform reliability studies on interconnects such as Cu wire bond and Cu TSV by performing various accelerated stress test and to use electrical characterization techniques to detect early degradation for reliability studies. Physical failure analysis (PFA) will also be performed to validate observations from reliability stress out intervals as well as electrical characteristics, to understand the degradation of interconnects and the physics behind it.

1.3 Research Objectives

The objective of this research is to study the reliability of interconnect in the form of Cu wire bonding and Cu TSV under various accelerated stress test conditions, especially in harsher automotive grade conditions. The intention is to understand if the interconnect is able to survive the reliability stress test and to understand critical failure modes and mechanisms that is associated with it.

The first part of the research focuses on Cu wire interconnect technology to detect the degradation of Cu wires after reliability stress test using a non-destructive electrical characterization method, where the sensitivity of a series resistance extraction method through a package electrostatic discharge (ESD) diode can be explored. A non-destructive detection method is useful especially in high volume manufacturing quality check as well as for reliability study since high amount of effort is required during PFA to decapsulate a unit in its molded packaging form. As a result, it is impractical to decapsulate every individual unit to assess its wires. Moreover, the decapsulated package will no longer be usable after wire assessment as it is a destructive and non-reversible process. In this research, the results and effectiveness of the non-destructive electrical characterization will be validated with PFA and conventional destructive wire assessment methods.

The second part of the study focus on the reliability of Cu TSV interconnect technology post reliability stress test. The objective is to use specially designed test structures to study important features of the TSV such as emulating a stacked die with silicon nitride (Si_3N_4) capping layer, TSV position induced mechanical stress and also different barrier and dielectric materials. Electrical characterization such as capacitance-voltage (*C*-*V*) and current density-electric field (*J*-*E*) curve will be plotted to assess its reliability performance together with PFA. In addition, electrical characterization of a degraded structure can be performed to understand the characteristics when Cu migration and diffusion takes place in the TSV

structure. This is useful for the evaluation on the impact of Cu migration within the TSV structure for the identification of the dominant leakage current conduction mechanisms, where a comparison can be made between structures that are either influenced or not influenced by the presence of Cu. Furthermore, with the understanding of the electrical characteristics, the research attempts to control and monitor the transport of Cu ions for time dependent dielectric breakdown (TDDB) study, where the influence of Cu ions is still not fully understood with no common agreement on the most appropriate model to be used. A suitable TDDB model can be proposed in this research with actual experimental data.

1.4 Major Contributions of the Thesis

A non-destructive electrical characterization method using a diode series resistance extraction method to detect degradation on Cu wire has been studied. It is demonstrated by its working principle that the diode series resistance extraction method is more sensitive with the ability to achieve lower detectable resistance and better resolution as compared to a direct resistance measurement method. The proposed method is experimented on a fully packaged, actual productive chip with an already existing ESD diode for the first time. Electrical characterization using the diode series resistance extraction method were performed on samples post reliability stress test and the results validated with conventional and destructive wire assessment method. The results showed that there is a correlation between the non-destructive diode series resistance extracted and the destructive wire assessment. This technique becomes a good starting point for reliability evaluation especially for degradation studies, focusing on a failure mechanisms based approach with a different bill of material and stress test.

Another interconnect technology in Cu TSV is studied for its reliability assessment with various test structures and material fabricated to emulate actual application scenarios to study its structural integrity. A plasma enhanced tetraethylorthosilicate (PETEOS) and black diamond low-k dielectric layer were studied and compared after post reliability stress test with low-k dielectric layer having a higher leakage, expected due to its higher porosity. It was observed that both dielectric material did not have any catastrophic failure even after harsh accelerated stress test at high temperature storage life (HTSL) at 175 °C up to 1000 hours and temperature cycling (TC) at -55/150 °C up to 2000 cycles. However, it was found that severe protrusion post HTSL 225 °C at 500 hours and 1000 hours, leads to voiding and delamination resulting in a decreased current performance. On the other hand, a Si_3N_4 layer suppressing the TSV structure emulating stacked chips were found to have an increased leakage current and

eventually catastrophic dielectric breakdown due to lateral stress onto the TSV structure.

The impact of Cu migration in a TSV structure and its impact on its reliability and electrical characteristics were studied on a degraded Ti barrier structure after stressing at 400 °C. It was found that the inversion capacitance increases when there is presence of Cu in the dielectric layer, validated with PFA results. On the other hand, post reliability stress test of HTSL 175 °C up to 1000 hours and TC -65/150 °C up to 2000 cycles did not seem to have any impact to the electrical characteristics initially but it was found that it could be due to the concentration of Cu ions migrated, where the electrical measurement is not sensitive enough to detect on a single TSV structure. When an additional electrical bias was applied to drive Cu ions into the dielectric layer, the increase in the inversion capacitance was observed suggesting that degradation to the TSV structure has already taken place even though it was not detected initially. Furthermore, when an array of 200 similar TSV structures were subjected to similar reliability stress condition, the increase in the inversion capacitance can be observed without any additional electrical bias.

The electrical characteristics observed on the increase in the inversion capacitance from Cu presence in the dielectric together where an additional electrical bias was required for single structure post stress test, suggest that it was possible to monitor and control the transport of Cu ions. It was demonstrated that with an appropriate direction of *E*-field applied, the inversion capacitance is observed to increase and decrease where Cu ions are being drifted towards the dielectric layer and Cu TSV respectively. The ability to control and monitor Cu ions within the dielectric is useful to understand the influence Cu have on it's the leakage current conduction mechanism and TDDB study.

TSV test structures with and without Cu presence in the dielectric were fitted to various current conduction mechanism for the best fit to determine the most dominant conduction mechanism. It was found that a single conduction mechanism does not adequately describe TSV structures that are without Cu presence suggesting that there is a possibility that several mechanisms are present and overlapping simultaneously. However the TSV structure with Cu ions present in the dielectric layer after degradation was found to fit well with a poole-frenkel (PF) conduction mechanism validated with experimentally measured optical dielectric constant from the optical ellipsometer. It was also interesting to observe that the leakage current conduction is dependent on the oxidation state of the migrated Cu ions where the PF mechanism is dominant only when the oxidation state of Cu ions is in the CuO form. X-ray photoelectron spectroscopy (XPS) analysis suggest that the oxidations state of Cu changes over time from Cu_2O to CuO.

Cu ions play different roles in the dielectric layer which can accelerate and decelerate TDDB lifetime, which is influenced by the applied *E*-field, temperature and also the oxidation state of the Cu ions. This suggests that TDDB may not be a simple plug and play test. Proper understanding of the different mechanism possibly induced by the presence of Cu within the dielectric layer will be necessary for an accurate lifetime analysis. TDDB lifetime models were fitted experimentally and is found to be in good agreement to the $\sqrt{E}$ model. The $\sqrt{E}$ model was verified experimentally by measuring the time to failure at low *E*-field, rather than extrapolating data from high *E*-field.

1.5 Organization of Thesis

There are in total 6 chapters in this thesis and is organized as follows.

Chapter 1 presents a brief overview and background of interconnect technologies, as well as some of its advances due to challenges from device scaling. The motivation to study the reliability of Cu interconnects, research objective as well as major contributions of this thesis are presented.

Chapter 2 presents a detailed literature review on both Cu wire bonding and Cu TSV interconnect technologies. In the first part, the challenges of Cu wire bonding will be discussed. Various destructive and non-destructive techniques used for wire bond quality evaluation will also be presented including the use of the diode series resistance extraction method. The second part touch on the challenges faced by Cu TSV interconnects. It presents various defects observed in TSV and its possible root causes and the general overview of reliability stress standards and conditions reported by researchers on the study of Cu TSV interconnects. Various leakage current conduction mechanism and TDDB models are also described. The third part presents some of the different types and purpose of various reliability stress tests performed by the packaging and assembly industry.

Chapter 3 presents the experimental setup and results from the study of thermomechanical reliability of Cu wire bonding. The sensitivity of the series resistance extraction method to detect degradation of the Cu wire bond together with the correlation with PFA will be discussed.

Chapter 4 presents the experimental setup and results from the study of the structural integrity of a Cu TSV structure using various test structures, materials and subjected to various reliability stress test. Electrical characterization is performed and the increased in the inversion capacitance due to the presence of

Cu is demonstrated. In this chapter, the fitting of the PF current conduction mechanism is conducted with validated to experimentally measured dielectric constant using the optical ellipsometer.

Chapter 5 presents the ability to control and monitor the transport of Cu ions within the dielectric for TDDB study. The role of Cu ions to accelerate or decelerate TDDB lifetime influenced by applied *E*-field, temperature and also the oxidation state of the Cu ions is demonstrated. An appropriate TDDB model is proposed using experimental data fitted towards low *E*-field.

Last but not least, Chapter 6 attempts to summarise all essential findings from this research work and provide recommendations for future work.

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Chapter 2

A Review of Copper Interconnects and its Reliability Challenges

2.1 Overview of Wire Bonding

Wire bonding is one of the most commonly used and widely developed interconnect method for the integrated circuits (IC) assembly and packaging industry. The main role of the wire bonds is to provide electrical signal paths between the outside world and the IC chip. Therefore, its failure will be disastrous and detrimental to the overall functionality of the device. In addition, as wire bonding is done towards the end of the entire package manufacturing and assembly process, its failure translates to high manufacturing cost, resource and time invested. As a result, industry is constantly trying to improve its yield by improving and developing the wire bonding process to ensure better quality wire bonds. Moreover, the assembly and packaging house are also constantly trying to keep in step with the development and accommodate the ever increasing pin count and decreasing chip size, resulting in an even more challenging wire bonding process [1-3]. The pressure to achieve high yield, fine pitch and low cost wire bonding naturally lead to manufacturers considering other wire materials outside of Au, which is traditionally the main and well-established material of choice for wire bonding. Au wire is also considered to be a mature technology where most industry players have the experience in terms of manufacturability and to ensure its quality and reliability. Aluminium (Al) wire has also been used for wire bonding for decades but it is mainly used for wedge to wedge bonding due to its inability to form good quality free air ball (FAB) for the ball bonding process. While wedge bonds enables fine pitch application due to the absence of a ball bond, the disadvantage is that it has lesser flexibility during the bonding process such that tool alignment is required for the wire to be drawn in a straight line according to the first bond. As a result, it slows down the bonding cycle

significantly with a lower throughput. This work will focus on Cu ball to wedge bonding.

Table 2.1: Material properties of Au, Cu and Al [4, 5].

Material Properties	Au	Cu	Al
Thermal Conductivity (W/mK)	320	400	222
Electrical Resistivity (10^{-8} Ω m)	2.2	1.72	2.8
Young's Modulus (GPa)	60	130	70
Vicker's Hardness (MPa)	216	369	167

As the price of Au increases rapidly through the years, there becomes a need to look for an alternative material for cost reduction to stay competitive. Table 2.1 shows a comparison of the material properties between Au, Cu and Al, which are considered for wire bonding. The thermal conductivity which is the ability for a material to transfer heat, the young modulus which is a mechanical property that measures the stiffness of the material and Vicker's hardness which measures the hardness of a material are important properties to be considered for the wire bonding process. On the other hand, the electrical resistivity which is a measure of how strongly the material resist electric current, is a material property that is considered for the overall electrical performance of the device.

In recent years, one of the material actively studied for ball bonds is Cu as it is relatively cheaper as compared to Au. In addition, it has better electrical and thermal conductivity, which makes Cu wire technology a good option for high power application. It also allows for smaller diameter wire to be used with equivalent electrical and thermal performance thus enabling scaling. In addition, the higher thermal conductivity of Cu allows for a shorter heat affected zone (HAZ) during free air ball (FAB) formation, desirable for wire bond reliability. More details on the HAZ will be discussed in section 2.1.3.1.1. With a higher

young's modulus as compared to Au and Al, Cu is able to have better looping and wire sweep performance during the bonding and molding process respectively.

Although there are clear advantages to use Cu for wire bonding, the implementation is however not straightforward and manufacturer are faced with several challenges in the Cu wire bonding process which have resulted in potential reliability concerns [6-8]. These challenges will be discussed in detail in section 2.1.2.

2.1.1 Wire Bonding Process

Wire bonding is an electrical interconnection technique using thin wire together with a combination of heat, pressure and/or ultrasonic energy during the bonding process. During the wire bonding process, the two metallic material (wire and pad surface or wire to lead surface) are brought into intimate contact. Once the surface are in intimate contact, electron sharing or inter-diffusion of atoms takes place, resulting in a metallurgical bond. Depending on the wire and bond pad material used, alloys such as in the form of a solid solution or intermetallic compound (IMC) can be formed at the bonding interface. Solid solutions are continuous with similar crystal structure with the parent material, while IMC have stoichiometric composition with a unique crystal structure from the parent material.

There are three main wire bonding techniques today such as the ultrasonic, thermosonic and thermocompression bonding. Ultrasonic bonding utilizes ultrasonic and low impact force, to bond on two metallic surfaces under pressure to form a bond. Thermosonic bonding also utilizes ultrasonic and low impact force, but with added temperature to form a bond. Thermocompression uses high temperature and high impact force to form a bond without any ultrasonic force. Ultrasonic bonding is commonly associated with Aluminum (Al) wedge bonding which is in the absence of

free air ball formation by electric flame off (EFO), while thermosonic and thermocompression bonding is often associated with ball bond formations. Depending on the physical constraints of the IC package, either bonding technique can be considered although the thermocompression technique is less commonly used today. The three main bonding agents, bonding force, ultrasonic energy and temperature for the different bonding techniques can be compared and summarized in Table 2.2 below.

Table 2.2: Comparison of different bonding techniques.

Wire Bonding	Temperature	Pressure/Force	Ultrasonic Energy	Typical Wire
Ultrasonic	25°C	Low	Yes	Au, Al
Thermosonic	100-240°C	Low	Yes	Au, Cu
Thermocompression	300-500°C	High	No	Au

In general, the wire bonding cycle can be illustrated in Figure 2.1 below for a typical thermosonic ball bonding process. The main difference between a thermosonic ball bonding and the ultrasonic wedge bonding apart from the bonding agent applied, is the additional step of an EFO ball formation for thermosonic ball bonding. Therefore the same cycle can also be used to describe an ultrasonic wedge bonding process without the EFO step. At present, the most widely used bonding technique is by thermosonic ball bonding, mainly due to its faster speed as compared to ultrasonic wedge bonding. Therefore, the focus of this thesis will be on thermosonic ball bonds.

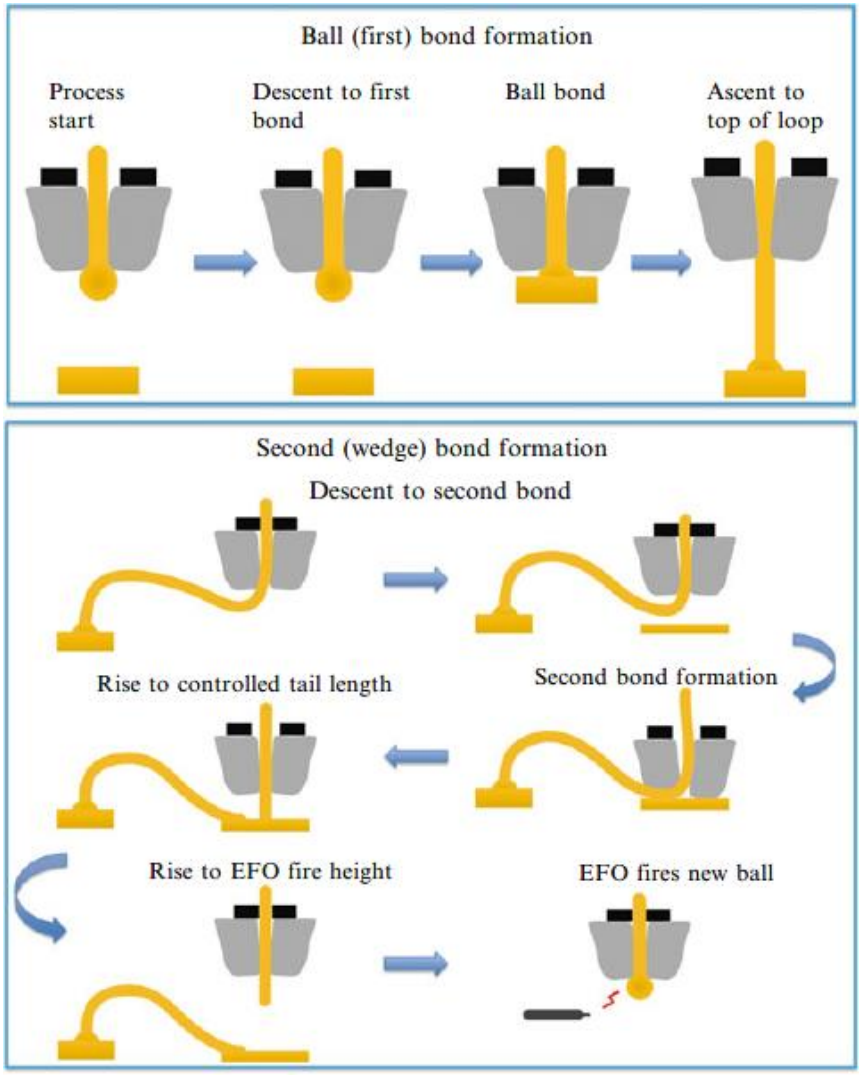

Figure 2.1 General wire bonding process cycle [4].

As shown in Figure 2.1, the bonding cycle can be divided into four different segments namely the first bond, looping, second bond and finally the electric flame off (EFO) in preparation for the next bonding cycle. During EFO, a high voltage is generated between the EFO wand and the wire which results in a high current spark to discharge that melts the end of the wire. The process where the molten wire turns into a spherical ball due to surface tension is called free air ball (FAB) formation. The bonding process starts with the EFO process for FAB formation at the end of the capillary and descends towards the desired bond pad. The FAB eventually come into contact with the bond pad and deforms as it is squashed against

the pad by the capillary at a predetermined impact force. During the process, a combination of parameters such as temperature, ultrasonic energy, force and time further squashes the ball and cause it to bond to the pad. The interaction of these parameters needs to be carefully optimized in order to ensure a reliable bond. The quality of a bond formation can be assessed after the bonding process which will be further discussed in section 2.1.3.

After the first bond is formed, the capillary is raised and follows a specified trajectory towards the second bond site which can be another bond pad or lead frame, to form a loop of desired shape and height. Similarly, the capillary then descent and with the application of temperature, ultrasonic energy, force and time, the second bond which is a wedge bond is formed. The capillary then rises slightly after the second bond formation where a combination of a pull force and the closing of the wire clamp breaks the wire. Wedge bonds unlike the ball bonds, does not have the shape of a ball when bonded as it does not form a FAB before bonding. In the last stage, the wire is then raised to the EFO height, where a spark is made against the end of the wire. The spark melts the wire to form a FAB and the bonder is ready to repeat the cycle for the next bond. A single bonding cycle can be typically completed in less than 0.15 seconds.

2.1.2 Challenges of Cu Wire Bond

There are several challenges that needs to be addressed before Cu wire can be fully rolled out into the manufacturing line. These challenges can be found during the bonding process as well as post bonding which requires further understanding to overcome.

During the bonding process, Cu wires requires either an inert or reducing gas environment to ensure a symmetrical and spherical free air ball (FAB) formation as Cu itself is easily oxidized. Typical gas environment used to prevent oxidation during Cu wire bonding is N_2 or a mixture of N_2 and H_2 also known as forming gas. Any deviation in the size or shape of the FAB due to oxidation may cause poor adhesion between the bond pad interface resulting in reliability issues [9, 10]. The result of an irregular FAB formation could be a golf club ball formation or flat ball bond formation as shown in Figure 2.2 and 2.3 respectively. The need for special gas environment to eliminate oxidation problem in Cu wire bond implies that the wire bonder needs to have a gas purging system. As a result, modification or investments on a new wire bonder may be required, resulting in a more complex wire bonding process and stringent process window.

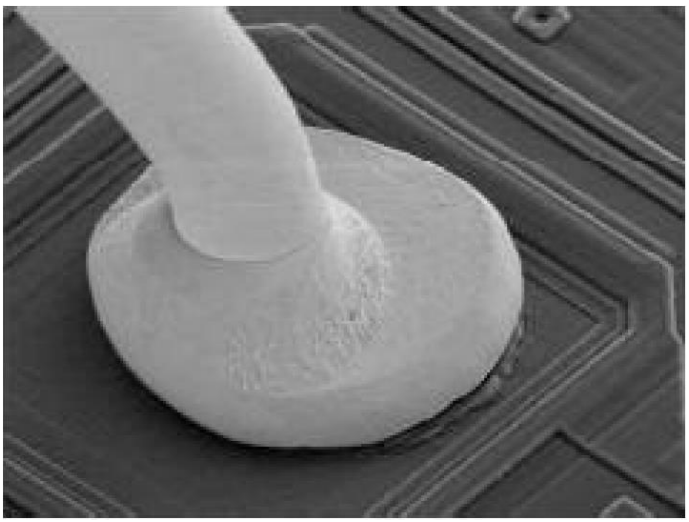

Figure 2.2 Irregular FAB formation resulting in a golf club ball formation.

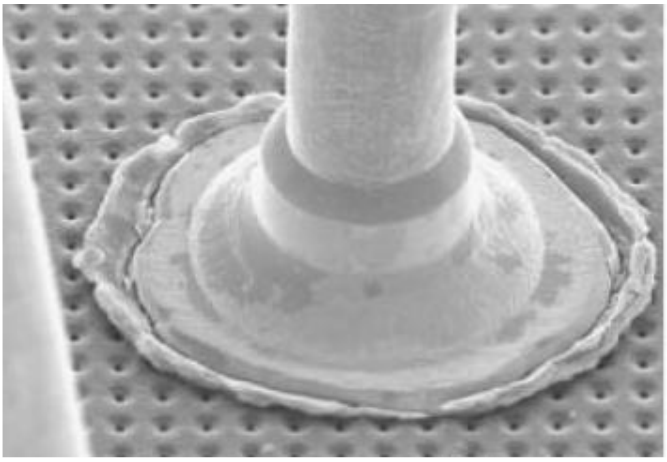

Figure 2.3 Irregular FAB formation resulting in a flat ball bond formation.

Due to a higher hardness and Young's modulus of Cu, it requires a higher bonding force during the bonding process resulting in higher pad stress. As a result, there will be a higher risk for pad splash, cracks and cratering issues created, which may lead to the damage of the underlying circuitry [11-14] leading to electrical functionality failure. Figure 2.4 shows Al pad squeeze after the wire bonding process. In worst case, the squeezed Al metallization may extend so far out of the bond pad that it electrical shorts to the neighboring wire resulting in a device failures. Figure 2.5 shows signs of cratering on the bond pad post wire ball shear test where the bond

pad was being sheared off together with the wire bond at its weakest point, exposing the silicon and internal circuitry underneath the bond pad. In order to eliminate damage during the bonding process, manufacturers may lower the bonding force. However, if the bonding force is not well optimized, a low bonding force may lead to other reliability problem such as poor bond pad adhesion or even an open contact when there is a non-stick on pad (NSOP) or non-stick on lead (NSOL).

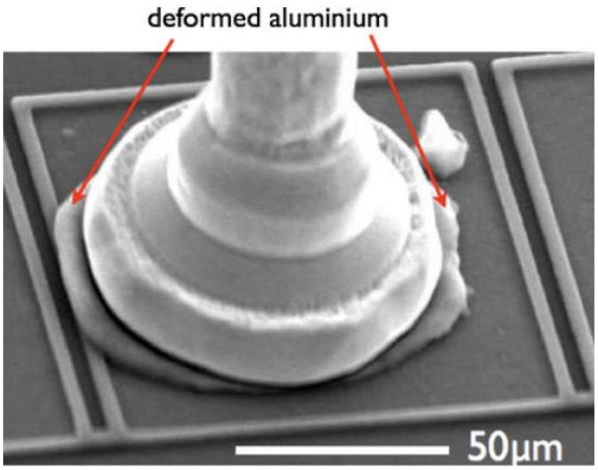

Figure 2.4 Aluminum pad squeezed after wire bonding.

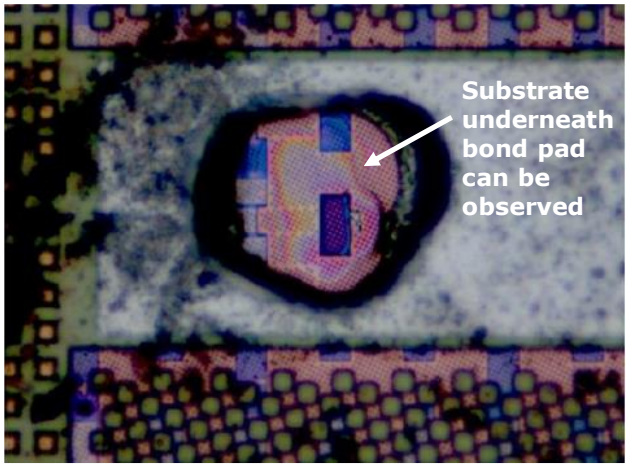

Figure 2.5 Cratering on bond pad revealing internal circuitry post wire bond shear test.

Cu is also very prone to corrosion, which lead to research and development works to explore protected coated Cu wires, various stable pad finishes as well as the halogen content and pH level of molding compounds are taken into consideration to minimize corrosion [15-18]. Figure 2.6 shows pitting on the wire ball surface due to corrosion. A cross-section image as shown in Figure 2.7 shows Cu creep corrosion between the Cu ball bond and bond pad interface. Creep corrosion is a failure mode that describes Sulfur (S) corrosion from S containing mold compound on Cu wire bonds, where corrosion products migrates into the bonding surface resulting in a weak bonding connection. These corrosion in severe cases, may cause unintended electrical open between bonding connections and a lifted wire.

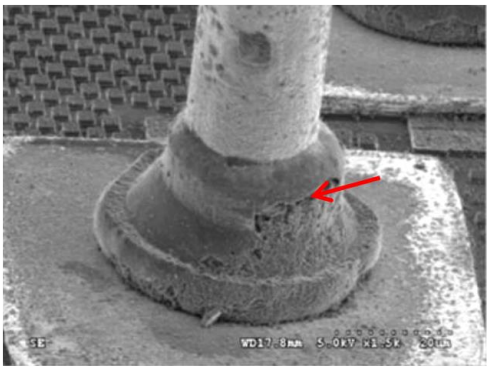

Figure 2.6 Pitting on the Cu wire ball surface due to corrosion.

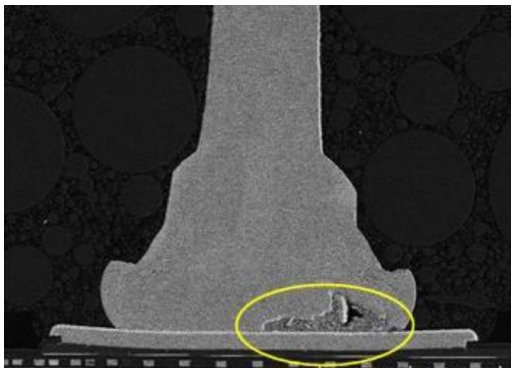

Figure 2.7 X-section image of Cu creep corrosion between bonding interface.

During failure analysis, inspection on wire bond requires the decapsulation process to remove the mold compound of the package in order to expose the wire bonds. There are several techniques used to remove the mold compound such as laser ablation, wet chemical and plasma etching. Depending on the complexity, a single technique or mixture of techniques may be administered. The most cost effective and fast method is by chemical etching, which usually involves the use of nitric and sulfuric acid which are effective to dissolve the organic material of the mold compound. However, nitric and sulfuric acid while suitable for Au wire, becomes a challenge for Cu wire since Cu is susceptible to the chemical attacks by the acids. Therefore, optimization in the chemical ratio, etch time and temperature is required to prevent damages or over etching to the Cu wire for accurate wire bond assessment. Alternatively, other decapsulation techniques such as the plasma etching or laser ablation which are clean and selective can be considered. An example of an overly etched Cu wire at the ball bond as well as the wedge bond can be observed in Figure 2.8 below.

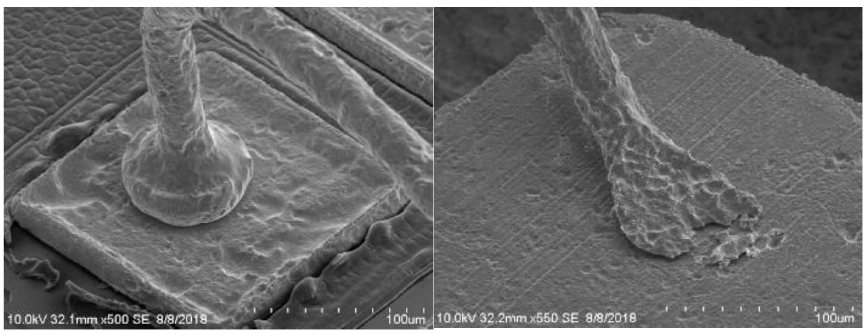

Figure 2.8 Overly etched Cu wire surface due to un-optimized decapsulation recipe.

These challenges require the need for a stringent process control and any process deviation may affect the quality and reliability of the wire bond.

Therefore the evaluation and inspection of the bonded wires after the assembly and packaging process, as well as after any reliability stress test, becomes important to identify any abnormal wires during the process in order to ensure good quality and reliable wire bonds.

2.1.3 Wire Bond Evaluation Techniques

Process response of the ball bond should be immediately evaluated after the wire bonding process. A quality ball bond with acceptable bond integrity will be able to demonstrate adequate process control in the assembly line. It also serves as an early indicator of qualification success, as defects prior to any reliability activities will not recover but only be further aggravated during accelerated stress test. Furthermore, analysis of any failure relating to wire bonds becomes complicated should the defects not be addressed from the wire bonding process. Some of the common accelerated stress test performed during qualification will be discussed in section 2.3.

A reliable bond can be developed with good knowledge on the design, material and process control of wire bond during production. However in reality, knowledge can be limited due to constant new developments, alteration and modifications to the fabrication process. In order to ensure a reliable bonded wire, it is also important to check for any degradation or failure after reliability stress testing. Several methods are used within the industry for wire bond evaluation and they can be categorized generally as a destructive or non-destructive test which will be elaborated in the following sections.

2.1.3.1 Destructive Techniques

The mechanical strength of the wires after bonding can be assessed most conventionally by the wire pull and shear test [4,

19] and are used in the qualification of wire bonds to test for process or stress induced degradation and failures. They are considered destructive as the wires are damaged during the test and cannot be used for further analysis. On the other hand, evaluation of the wire bonds can also be done by visual inspection using the Optical Microscope or Scanning Electron Microscopy (SEM) for smaller dimensioned and higher density wires. However, prior to any possible visual inspection, there is a destructive decapsulation process on any molded products, where the device can no longer be shipped and sold in the market. In addition, the decapsulation process may subject the wires to be damage by chemical attacks during decapsulation, causing important information on defects to be lost in the process which results in inaccuracies during subsequent analysis. Cross-section analysis is also another destructive analysis that is often performed to evaluate wire bonds especially at the bond-pad interface. However, it is impractical as it is time consuming to implement in the production line. It can also be costly to implement especially for packages that involves a complex fabrication processes.

2.1.3.1.1 Pull Test

Wire pull test is used widely by manufacturing industry to assess the strength of the bonded wire. During a ball bond pull test, the hook is positioned below the wire as close to the ball bond as possible, usually using the apex of the looping profile as a guide. The wire is then being pulled with the hook at a pre-determined pull speed and is perpendicular to the bonding surface to avoid any lateral or peeling effect on the wire bond.

The failure location on the wire bond after the destructive wire pull test and some of the common failure modes is shown in Figure 2.9. It is important to look at the failure modes after wire pull test to assess if there are any weakness in the wire or bonding process, especially when an unexpected failure mode is observed.

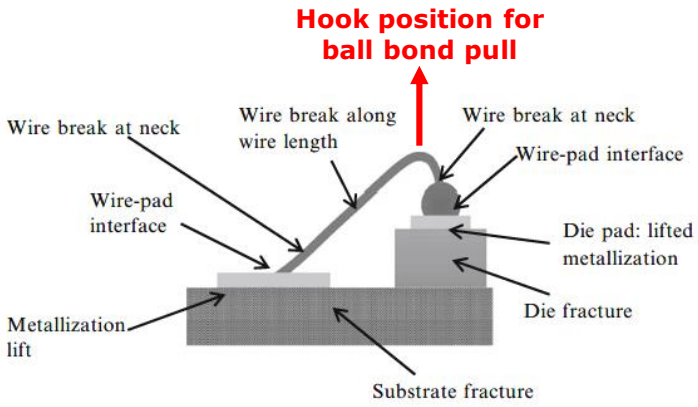

Figure 2.9 Location of failures after destructive pull test [4].

When lifted bonds together with fractures of die/substrate, or lifted metallization is observed, it is potentially the result of an un-optimized bonding process or bad adhesion between the pad metallization and die/substrate material respectively. Since the higher hardness of Cu wires require higher bonding force, high stress induced on the bonding interface can lead to cracking or cratering beginning at the pad metallization into the die/substrate.

On the other hand, lifted bonds from pad metallization could indicate poor bond-pad adhesion or a weakening of the bond-pad interface. Poor bond pad adhesion could be a result of poorly optimized bonding parameters or contamination of bond pad surface before bonding. The weakening of bond-pad interface could be due to an excessive IMC formation during aging.

Bond breakage at the wire neck region or along the span of the wire after a wire bond pull test as shown in Figure 2.9., is expected and acceptable unless the minimum pull strength of the wire is below the acceptable specification and requirements. It can be caused by wire sweeping during the molding process or an inappropriate looping condition. The pull force for breakage along the span is often higher as compared to the pull force for breakage at wire neck. This could be due to work hardening which refers to the strengthening of metal by plastic deformation during the first and second wire bond formation where plastic deformation generates dislocations within the crystal structure of the metal. These dislocations can move, accumulate and eventually gets trapped or tangled to other dislocations. As a result, the decrease in mobility of the dislocation results in the strengthening of the material. In addition, the neck region which is part of the heat affected zone (HAZ) is weakened after electric flame off (EFO) during ball formation. At high

temperature, the grains grow in size due to recrystallization. With larger grain size, the grain density becomes lower resulting in lesser grain boundaries to act as barriers to the movement of dislocations in the crystal structure. Therefore, smaller grains with more grain boundaries will impede the movement of dislocations thus have a higher hardness as compared to the same material with larger grain size. The grain structure of the HAZ region is larger as compared to the rest of the wire, resulting in a weakest region with lower hardness [19] as shown in Figure 2.10.

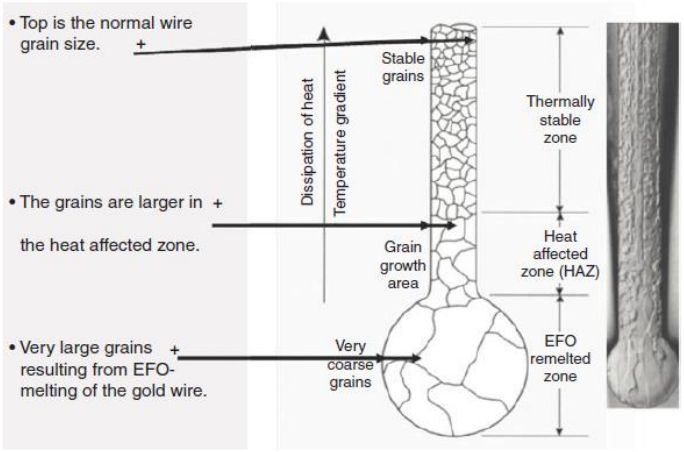

Figure 2.10 Grain structure of a wire after ball formation [19].

Since the entire wire bonding system consists of several geometrical configurations, the placement of the hook and pull angle during pull test is an important consideration. Changes to these configurations will cause a redistribution of force at the wire bonds which

may lead to an entire different failure mode and result in an inaccurate evaluation. The geometrical variables of a wire bond pull test are illustrated in Figure 2.11. The symbol f is the pull force at the hook, fwt is the force acting on the wire bond at the terminal, fwd is the force acting on the wire at the semiconductor die, ϕ is the pull angle at the hook, Θt is the angle between the wire and the terminal, Θd is the angle between the wire and the die, ε is the ratio of the hook position with respect to the distance between the bonds at the terminal and die, d is the distance between the bonds at the terminal and die, h is the loop height calculated from either bonds whichever is at the higher level, and H is the height difference between the die and terminal bonds.

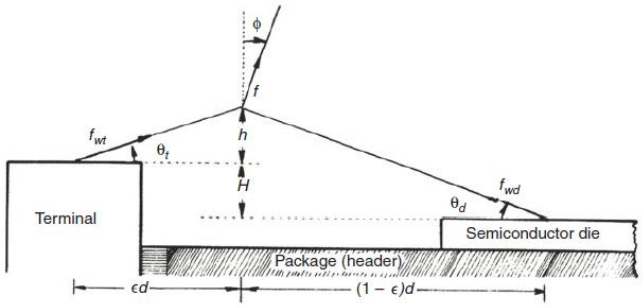

Figure 2.11 Geometrical variables of a wire bond pull test [19].

The loop height of the bonded wire is an important factor which can determine the pull strength. Higher loop height often yield higher pull strength as it lowers the stress induced on the wires caused by unintended

flexure fatigue. This could be due to the CTE mismatch between wire and package during TC test, or wire sweep during molding process. Figure 2.12 shows that as the loop height increases, wire pull strength also increases.

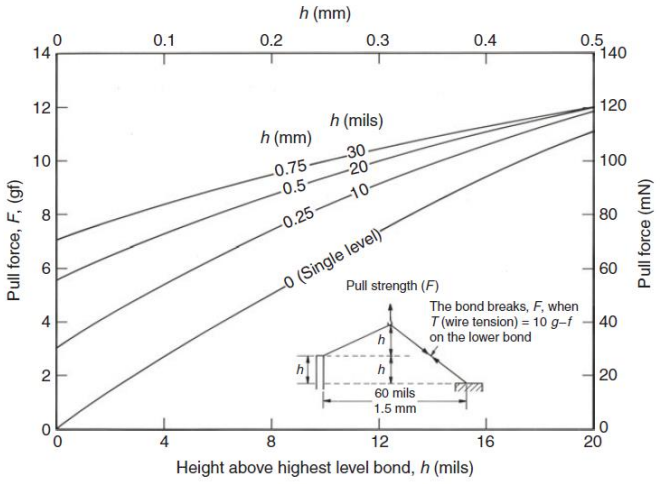

Figure 2.12 Pull force against wire loop height [19].

2.1.3.1.2 Shear Test

Shear test is another method used to assess the strength of bonded wires. It is mainly performed for the evaluation of bond-pad interface strength and degradation. Shear test is carried out with a shear tool making sure that it does not come in contact with any adjacent structures other than the bond to be tested throughout the shearing process. The shear tool must be larger than the ball bond diameter and positioned adjacent to the bond to be tested, at a pre-determined height above the surface of the die. Typically the shear tool is positioned above the bonding surface

approximately at a quarter to half of the bonded ball height for accurate results. During the shear test, the shear tool pushes off the ball bond at a pre-determined shear force until bond failure. Some of the failure modes of a shear test are as shown in Figure 2.13 below.

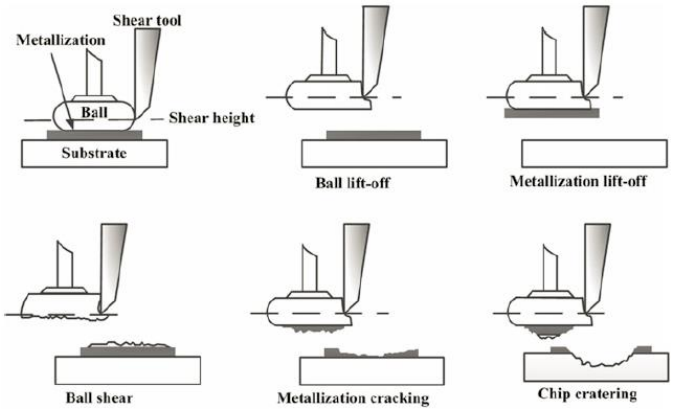

Figure 2.13 Failure modes after shear test [4].

The failure modes and failure mechanisms observed in a shear test is similar to what can be observed in a pull test. However in most wire bonds, the bonded cross-sectional area between the bond-pad interfaces is larger as compared to the wire cross-sectional area. In other words, the ball diameter is larger as compared to the wire diameter. Furthermore, the wire neck region is often the weakest due to the larger grain boundary formed after EFO. As a result, pull test will often break the wire at this region or at the smaller diameter wire, even before any bond-pad interface failures. Therefore little information of the bond-pad degradation can be gathered from pull test. Shear test on the other hand can

focus the failures between the bond-pad interfaces. Figure 2.14 shows that shear strength increase as bonded area increases.

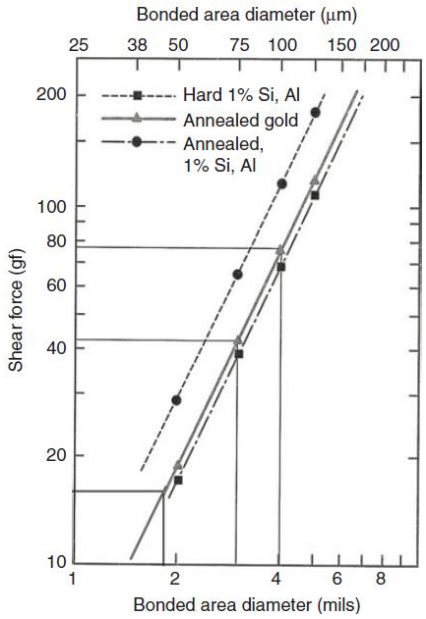

Figure 2.14 Shear force against wire bonded area [19].

2.1.3.2 Non-destructive Techniques

Scanning Acoustic Microscopy (SAM), X-ray imaging and Computerized Tomography (CT) scan are also some commonly used non-destructive techniques for wire bond evaluation used in the industry. However, they can be time consuming to perform, costly to implement and often limited by its resolution for any useful analysis. On the other hand, non-destructive electrical testing are also performed in the industry for a simple open and short electrical evaluation but no information on the degradation of wire can be provided. There are potential in using electrical means to evaluate the quality and reliability of bonded wires for assessment where several studies have already been performed.

McCracken *et al*. [20] attempted to study the degradation of wire using specially built piezo-resistive stress sensors that are strategically placed around the bond pads to detect changes in the stress originating from the bond-pad interface for evaluation. In their study, specially built chip with sensors are required that make its application on actual productive chips limited. In addition, the resistance change detected by the stress sensor is not able to give information of any degradation on the wire, focusing only on the bonding interface. Maiocco *et al*. [21] on the other hand, attempted to study the degradation of wire bonds by directly probing onto the wire ball bonds for its resistance measurement while Mayer *et al*. [22] performed the direct measurement on the wire bond pad for its pad resistance measurement. These methods however, will only be applicable for chips before the molding process and are limited as it can only be evaluated in the assembly line. In addition, all of the above studies concentrated solely on degradation coming from the bond-pad interface, ruling out any possible form of quality issues or degradation on the entire wire span. Nevertheless, these methods showed the potential of making use of electrical characteristics, to assess the quality and reliability of a bonded wire.

2.1.3.3 Diode Series Resistance Extraction Method

In a packaged chip, resistance of the wire can be either measured directly [23, 24] or indirectly extracted from an ESD protection diode that is connected in series with the bonded wire. The indirect extraction method can be found in the work of Tan *et al*., where the extraction of series resistance from a power diode was found to be quick and accurate [25].

The proposed method for series resistance extraction involves first the collection of the diode *I-V* curve which can be described by the Shockley diode equation as shown in equation 2.1 where I_d is the diode current, I_s is the saturation current, V_D is the voltage across the diode, n is the ideality factor and V_{th} is the thermal voltage.

$$I_d = I_s e^{V_D/nV_T} \tag{2.1}$$

$$G\,(I_2, V_2) = \frac{(I_2V_2 - I_1V_1) - 2\int_{V_1}^{V_2} I'dV'}{I_2}$$
$$= nV_T\left[ln\frac{I_2}{I_s} - 2\right] - \frac{I_1}{I_2}nV_T\left[ln\frac{I_1}{I_s} - 2\right] \tag{2.2}$$

The *I-V* characteristics curve is then fitted into the proposed *G* function curve as shown in equation 2.2 where I_1 and V_1 is the lower limit of the selected current and voltage range of the *I-V* curve, I_2 and V_2 is the upper limit of the selected current and voltage range of the *I-V* curve. As the operating current is influenced by the ideality factor, careful selection of the current and voltage range is required for analysis. Using a software, the n and I_s value of the diode can be extracted by fitting the experimented *I-V* curve into the *G* function equation. In a good fitting, the extracted n value should match the selected range of operating current. Base on Equation 2.1, the series resistance R_s, can be calculated with the extracted n and Is, by computing the gradient against I_d plot as shown in equation 2.3, where V_s the source voltage.

$$I_d = I_s e^{(V_s - I_d R_s)/nV_T}$$
$$\ln(I_s) + \frac{V_s}{nV_T} - \ln(I_d) = \left(\frac{R_s}{nV_T}\right) I_d \tag{2.3}$$

There are several advantages of the series resistance extraction method as compared to a direct wire resistance measurement. An advantage is that the ESD protection diodes are readily available, often already part of the IC design as it is only practical that the internal circuitries within the IC are protected from any possible ESD shocks. By making use of the ESD diodes, electrical measurements can easily be made without any modification to existing design and can be easily applied to any wires that are protected with an ESD protection diode. In addition, the measurement can be made through the diodes without powering on the entire circuitry which is useful especially for sensitive products. The other advantage is that the series resistance extraction method have the capability to detect lower resistance as compared to direct resistance measurement suggesting that it is more sensitive. Based on specifications from the source meter and device, it is calculated that the minimum resistance detectable is smaller for the diode series resistance extraction method as compared to direct wire resistance measurement as illustrated below.

$$R_{min} = \left(\frac{V_{min}}{I_{max}}\right) \qquad (2.4)$$

$$R_s = \frac{V_s - nV_T \ln(I_d) + nV_T \ln(I_s)}{I_d} \qquad (2.5)$$

Using Ohm's law as shown in equation 2.4, the minimum resistance detectable using direct wire measurement can be easily calculated where V_{min} is based on source meter specification and I_{max} depended on device maximum current limit. The minimum

detectable resistance is therefore, calculated to be 6.25 mΩ based on the Keithley 2606A source meter which is used in this work. On the other hand, based on equation 2.5 which is derived from the diode equation from equation 2.3, the minimum resistance detectable using the diode method can be calculated. I_s, n and V_T are assumed to be 10^{-12} A, 1 and 0.026 V respectively while I_d is capped by the device current limit. Based on equation 2.5, the minimum resistance detectable using the diode method can achieve much lower than 6.25 mΩ, approaching 0 Ω with V_s being 0.635 V.

2.2 Overview of Copper TSV

Apart from Cu wire bonding, TSV technology has in recent years been actively pursued and has become one of the key enablers for 3D IC integration. TSV allows for vertical interconnection of dies which not only overcome spatial limitations but also enabled the possibility of heterogeneous integration to enhance functionality and performance. TSV is able to achieve better electrical performances due to shorter interconnect length as compared to wire bond. As a result, TSV is able to achieve lower resistance current path, lower power consumption and smaller signal propagation delay [26].

While there are several benefits with the integration of TSV interconnect technology, there are also several challenges such as thermomechanical stress due to high coefficient of thermal expansion (CTE) mismatch between Cu and silicon (Si), as well as TSV fabrication process which poses concerns in the reliability of TSV interconnects for mass production.

2.2.1 TSV Fabrication Process

There are a few approaches to the fabrication of TSVs as shown in Figure 2.15. The final approach depends on the required application, process parameters, materials and desired layout of the wafer design. The first approach is the via-first approach as shown in Figure 2.15a, where TSVs are fabricated in the bulk of the substrate before any active devices are formed. This approach needs to be compatible to FEOL process, therefore the conducting material of the TSV is polysilicon. As the resistivity of doped polysilicon is higher as compared to Cu via, the diameter of polysilicon via are usually large in order to have an overall acceptable resistance.

The second approach is the via-middle approach where TSVs are fabricated after active devices are created but before the on-chip interconnect stack are formed as shown in Figure 2.15b. As active devices are already formed, appropriate process parameters and temperatures used during via-middle fabrication of TSVs must be considered so that it will not degrade active device performance. For example, low temperature dielectric deposition less than 600 °C should be used to avoid degrading device performance. The advantage of the via-middle process is that it allows for a lower resistivity material such as Tungsten (W) and Cu to be used thus smaller TSV diameter and pitch is possible. However, the via-middle approach have relatively expensive process such as deep reactive-ion etching (DRIE), Cu plating and chemical mechanical polishing (CMP) process.

The third approach is the via-last approach and can be further categorized as front side via-last and back side via-last approach as shown in Figure 2.15c and Figure 2.15d respectively. The via-last approach forms the TSVs

after the on-chip interconnect stacks are formed. The advantage of front side via-last approach allows the connection of multiple layers within the interconnect stack. However, etching through the thick stack of interconnect, dielectric and silicon may be challenging and take up precious space for wiring, resulting in less routing freedom and a larger die size. On the other hand, the back side via-last approach is formed from the back side of the wafer which provided some advantage during stacking as the process flow can be simplified with several back side metallization process steps eliminated [38]. Similar to the via-middle approach, via-last TSV fabrication needs to take into consideration any process influence on the earlier fabricated active devices.

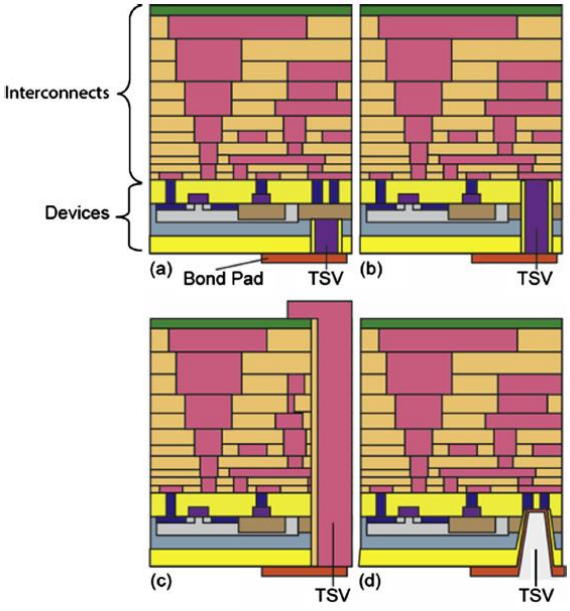

Figure 2.15 TSV fabrication by (a) via-first; (b) via-middle; (c) front side via-last; and (d) back side via-last approach [27].

A brief process flow of Cu TSV can be found in Figure 2.16. The main process units for TSV fabrication are etching, dielectric layer deposition, barrier and seed layer deposition, Cu via filling and the removal of excess Cu.

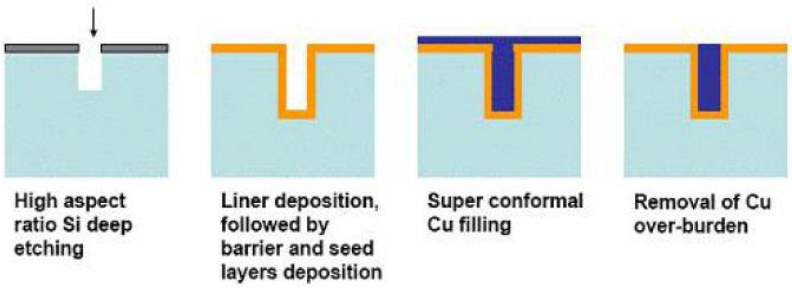

Figure 2.16 Brief process flow of Cu TSV [28].

The main requirement of etching TSV is to have good control over the high aspect ratio etching profile as well as good side wall roughness. When the side wall roughness becomes too significant, it may lead to a high current leakage as the electrical isolation between the Cu and Si provided by the dielectric layer, as well as the diffusion barrier which prevents Cu diffusion into the dielectric and Si, cannot be deposited uniformly. Therefore, a commonly used method for high aspect ratio trench formation is the BOSCH DRIE process. The BOSCH DRIE consists of a series of rapid switching between the isotropic etching and passivation steps. Gases such as Sulfur hexafluoride (SF6) is primarily used for the silicon etching while octafluorocyclobutane (C4F8) is used for the passivation process. The passivation process is important to prevent lateral etching within the via in the next etching step where ion bombardment will remove the passivation layer at the bottom of the via for continuous Si etching. Alternatively, a de-passivation step can also be introduced using O_2/Ar to remove the passivation layer at the bottom of the via. The etching and passivation cycle is typically alternated within a few seconds to achieve an anisotropic etching profile. If the etching and passivation sequence are not well balanced, a rough sidewall called the scallop effect will occur which continues to be a challenge due to the tradeoff between throughput and sidewall uniformity. Figure 2.17 shows a schematic of the BOSCH etching and passivation sequence and the scalloping effect on the side wall.

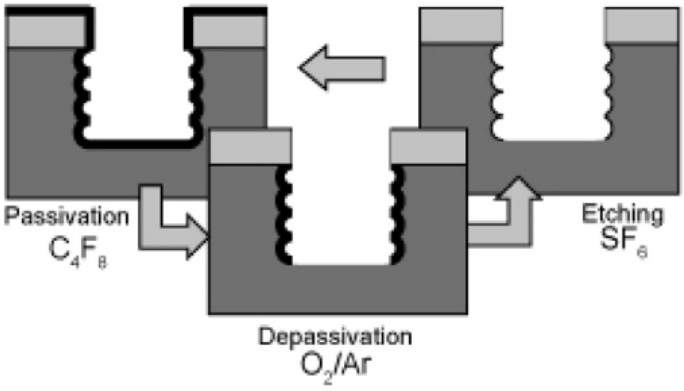

Figure 2.17 Schematic of a BOSCH RIE process [27].

After the deep trench is formed, the filling process begins with the insulation layer for electrical isolation between the via and silicon substrate. Depending on the limitations of the process to the application, different process for oxide growth are considered. For example, in via-first structure, high quality thermal oxide processed at high temperature in the range of 800 °C to 1100 °C is possible. However, this will not be possible for a via-middle integration where active devices are already processed. Therefore, amorphous oxide are usually deposited either by chemical vapor deposition (CVD) or plasma-enhanced chemical vapor deposition (PECVD) process at much lower temperature below 400 °C. Next a diffusion barrier layer such as titanium (Ti), titanium nitride (TiN) and Tantalum (Ta) will be deposited to prevent Cu diffusion in a Cu filled TSV, followed by the Cu seed layer deposited by the physical vapor deposition (PVD) process. The via is then filled with Cu by the electroplating process, capable to provide void free filling of the high aspect ratio TSV. The filling of the high aspect ratio TSV needs to be uniform and conformal to avoid reliability issues.

Last but not least, the removal of excess Cu is done by the CMP process. It removes excessive Cu by polishing the wafer against a rotating plate covered with a polish pad filled with an abrasive chemical slurry. The slurry flow rate and polishing force will influence the removal rate and planarity of the surface. Therefore, an unoptimised CMP process may leave behind Cu residues causing electrical short and leakages during reliability testing.

Each unit process has its own objective and requirement in order to produce reliable TSV interconnects. Therefore constant fine tuning to optimize the process parameters is often required to achieve a robust TSV structure.

2.2.2 Cu TSV Reliability Concerns

There are a number of factors affecting the reliability of Cu TSV and one of the main concern is the large CTE mismatch between TSV and Si wafer. Due to the CTE mismatch, stress can be induced in high temperature environment during fabrication, reliability stress test and during field application. Reliability concerns such as Cu extrusion [29-31], interfacial delamination [32, 33], cracks in the Si substrate [34], cracks in the dielectric layer [35] as well as the alteration of neighboring active device performances [36, 37] have been reported. Besides the CTE mismatch from materials, the positioning and design layout of TSV within the Si substrate, can also induce stress interactions with neighboring TSV structures causing potential reliability issues.

Another concern is that Cu readily diffuse into most dielectrics and silicon substrate which leads to high electrical leakage current, premature breakdown and eventually device failure [38]. As a result, in order to

prevent Cu migration that leads to device failure, a reliable diffusion barrier is necessary and is highly desired. Currently, there have been some studies performed on planar structures that looks into the characteristics and impact on the migration of Cu [39-41]. However, despite some insights gained from the study of planar structures, it is also necessary to carry out similar studies on an actual TSV structures as there are geometrical as well as fabrication process differences which may eventually accelerate, modify and even introduce new failure mechanisms which may not be identified in a planar structures.

For example, barrier integrity depends partially on the side wall roughness after the via etching process. Deep Si etching are often used to create a TSV trench which results in a rough sidewall surfaces. This leads to problem in the subsequent liner deposition process to be non-conformal, which may result in the structure to have an overall high leakage current. Furthermore, Cu may be inevitably introduced into the dielectric layer during the subsequent Cu filling process, due to a non-uniformly deposited barrier layer. One of the commonly used anisotropy etch techniques to achieve deep straight and high aspect ratio trench is the BOSCH DRIE process. However, the technique which uses cyclical etch and passivation steps, cause rough and sharp sidewall scallops which may serve as high stress concentration points resulting in barrier failure [42]. Moreover, when subjected to long term reliability stress test, it may be difficult to achieve and maintain a diffusion barrier that is robust enough that continues to fully eliminate Cu from migrating into the dielectric layer.

Currently, available research work on the understanding of the electrical characterization, failure mechanism and detection methods that are related to Cu migration through the TSV barrier layer, dielectric layer and into the

Si substrate are still limited and incomprehensive. This work will attempt to understand the observations of the electrical characteristics relating to Cu migration, allowing reliability assessment to be made for Cu TSV degradation studies.

2.2.3 Current Reliability Study Status

Presently most studies focus on reliability evaluation under temperature cycling (TC), high temperature storage life (HTSL) and unbiased highly-accelerated temperature and humidity stress test (uHAST) conditions, and found that the TSV structures studies passed reliability evaluation with no failures [43, 44]. The stresses are however usually not severe enough to meet even the usual industrial qualification standard stated in JEDEC standard for TC [45], HTSL [46], and uHAST [47]. Typical stress conditions can also be found in the JEDEC standard JESD47 [48] for stress driven qualification of integrated circuits. Typical stress condition used in the industry is performed at TC -55/150 °C up to 1000 cycles, HTSL 150 °C up to 1000 hours and uHAST 130 °C or 110 °C with a relative humidity of 85% up to 96 hours or 264 hours respectively.

On the other hand, Bahareh *et al.* [49] as well as Kauerauf *et al.* [50] performed reliability stress test on TSV interposers and standalone TSV structure respectively, which were in alignment with industrial standards. Their reliability evaluations were positive and without any failures detected. However, the stress test performed is still incomparable to the harsher grade 0 conditions required by the automotive standards as stated in the AEC-Q100 revision H [51]. The AEC-Q100 revision H, Grade 0 requirement suggest a TC condition of TC -55/150 °C up to 2000 cycles and HTSL 150 °C up to 2000 hours. uHAST condition is similar to the JEDEC standards.

Nonetheless, current studies so far have proven that the TSV interconnect reliability has continuously improved over the years and is now ready for more severe stress testing. Therefore, to explore the potential of implementing TSV in automotive applications, more reliability data is required from reliability evaluations under the automotive standards and requirements. This is to ensure that a comprehensive understanding of potential failure mechanisms are understood and proposal for improvements are in place for mitigation.

2.2.4 Conduction Mechanisms

A TSV structure can in principle, be also seen as a metal oxide semiconductor (MOS) structure. An ideal oxide would provide electrical insulation preventing any flow of electrical current through it. However, this is not possible in the real world as a perfect insulator does not exist due to imperfections in the manufacturing process. In addition, it gets more and more difficult due to continuous scaling where dielectric gets thinner and with device functioning at higher electric fields. The leakage current mechanism in a MOS capacitance structure can be categorized under two main categories, electrode limited and bulk limited conduction mechanisms. Well known electrode limited conduction mechanism are Fowler-Nordheim (FN) tunneling and Schottky emission (SE). Electrode limited conduction mechanism takes into account the electrical properties at the metal to dielectric interface such as the barrier height at the interface. On the other hand, the bulk limited conduction mechanism takes into account the electrical properties of the dielectric such as traps and ionizing centers within the dielectric. Bulk limited conduction mechanisms includes ohmic conduction, Poole-Frenkel (PF) emission, space-charge limited conduction (SCLC) and ionic conduction [52, 53].

Since the performance of the TSV also very much depends on the leakage performance of the dielectric layer, it is therefore, important to understand and characterize the leakage current mechanism of the dielectric layer. Table 2.3 summarizes the different conduction mechanism in dielectrics, together with its linear expressions.

Table 2.3: Summary of current conduction mechanism in insulators.

Conduction Mechanism	**Expression**	**Linear Expression**
Schottky Emission [54, 55]	$J = A^{*}T^{2}\exp[\frac{-q\emptyset_B - \sqrt{qE/4\pi\varepsilon_r\varepsilon_0}}{kT}]$	$\ln(J) = \left(\frac{q\sqrt{q/4\pi\varepsilon_r\varepsilon_0}}{kT}\sqrt{E}\right) + \ln(A^{*}T^{2}) - \frac{q\emptyset_B}{kT}$
FN Tunneling [55-58]	$J = \frac{q^3E^2}{8\pi hq\emptyset_B}\exp[\frac{-8\pi(2qm_T^*)^{1/2}}{3hE}\emptyset_B^{3/2}]$	$\ln\left(\frac{J}{E^2}\right) = (\frac{-8\pi(2qm_T^*)^{1/2}\emptyset_B^{3/2}}{3h})(\frac{1}{E}) - \ln(\frac{8\pi hq\emptyset_B}{q^3})$
PF Emission [55, 56]	$J = q\mu N_C E\exp[\frac{-q(\emptyset_T - \sqrt{qE/\pi\varepsilon_r\varepsilon_0})}{kT}]$	$\ln\left(\frac{J}{E}\right) = \left(\frac{q\sqrt{q/\pi\varepsilon_r\varepsilon_0}}{kT}\sqrt{E}\right) - \frac{q\emptyset_T}{kT} - \ln(\frac{1}{q\mu N_C})$
Ohmic Conduction [56]	$J = \sigma E = nq\mu E$	$J = \sigma E = nq\mu E$
SCLC [52, 53, 58]	$J_{TFL} = \frac{9}{8}\mu\varepsilon\theta\frac{V^2}{d^3}$ $J_{Child} = \frac{9}{8}\mu\varepsilon\frac{V^2}{d^3}$	$J_{TFL} = \frac{9}{8}\mu\varepsilon\theta\frac{V^2}{d^3}$ $J_{Child} = \frac{9}{8}\mu\varepsilon\frac{V^2}{d^3}$
Ionic Conduction [53]	$J = J_0\exp[-(\frac{q\emptyset_B}{kT} - \frac{Eqd_s}{2kT})]$	$\ln(J) = -\frac{q\emptyset_B}{kT} + \frac{Eqd_s}{2kT} + \ln(J_0)$

J is the current density, E is the electric field across the dielectric, m_T^* is the effective tunneling mass in dielectric, h is the Planck's constant, q is the electronic charge, $\emptyset_B$ is the barrier height, k is the Boltzmann's constant, T is the absolute temperature, ε_r is the optical dielectric constant, ε_0 is the permittivity in vacuum, A^* is the effective Richardson constant, $q\emptyset_T$ is the trap energy level, N_c is the density of states in the conduction band, σ is the electrical conductivity, μ is the electron mobility, n is the number of electrons in the conduction band, J_{TFL} is the trap filled limited current, V is the voltage applied, ε is the static dielectric constant, θ is the ratio between free and total carrier density including trapped carriers, d is the dielectric thickness, d_s is the distance between two defect site, J_0 is the proportional constant.

2.2.4.1 Fowler-Nordheim (FN) Tunneling

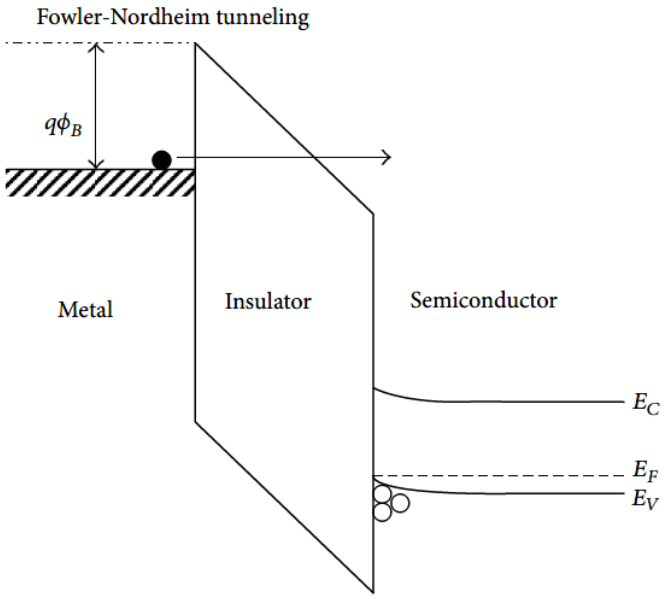

Figure 2.18 Schematic energy band diagram of FN tunneling in MOS structure [53].

In the presence of high electric field, bend bending occurs resulting in an apparent triangular barrier as shown in the schematic energy band diagram in Figure 2.18. When electrons are injected and tunnels through the triangular barrier into the conduction band of the dielectric, FN tunneling occurs. On the other hand, when electrons are injected and tunnels through the entire oxide thickness, direct tunneling occurs.

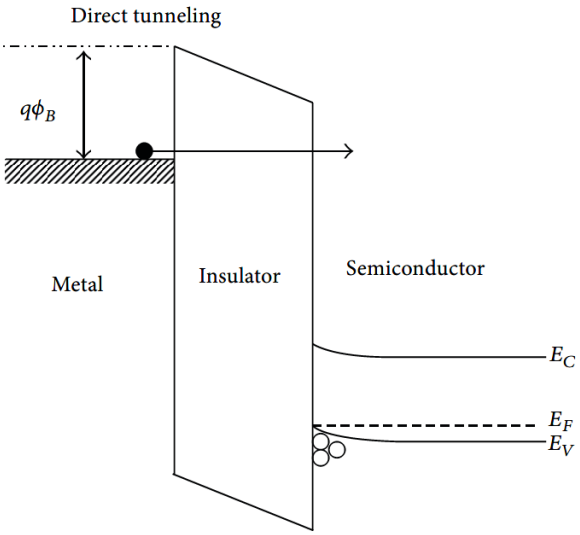

Figure 2.19 Schematic energy band diagram of direct tunneling in MOS structure [53].

Figure 2.19 shows a schematic energy band diagram of direct tunneling. Direct tunneling happens more at lower electric field and for thinner dielectric thickness as compared to FN tunneling. For direct tunneling to be the main conduction mechanism in SiO_2, the thickness of SiO2 is typically in the range of less than 4 to 5 nm. Above 5 nm, FN conduction mechanism typically dominates.

FN tunneling can be expressed linearly in below equation:

$$\ln\left(\frac{J}{E^2}\right) = \left(\frac{-8\pi(2qm_T^*)^{1/2}\emptyset_B^{3/2}}{3h}\right)\left(\frac{1}{E}\right) - \ln\left(\frac{8\pi hq\emptyset_B}{q^3}\right) \qquad (2.1)$$

where J is the current density, E is the electric field across the dielectric, m_T^* is the effective tunneling mass in dielectric, h is the Planck's constant, q is the electronic charge and $Ø_B$ is the barrier height.

As shown from the linear expression, plotting $\ln\left(\frac{J}{E^2}\right)$ vs $\left(\frac{1}{E}\right)$ results in a negative slope and the barrier height can be extracted from the linear regression at the y-intercept. It is also observed that essentially, FN tunneling is dependent on the voltage applied and is independent to temperature. Therefore, FN tunneling current can be measured at low temperature such that other temperature dependent conduction mechanisms can be suppressed without influencing the FN characteristics.

2.2.4.2 Schottky Emission (SE)

When sufficient thermal energy is provided, such that the electrons in the metal are able to overcome and go above the potential barrier of the metal-dielectric interface into the dielectric conduction band, SE occurs. Therefore, SE is a temperature dependent conduction mechanism as current flow is thermally activated. It can be expressed linearly in below equation:

$$\ln(\mathrm{J}) = \left(\frac{\mathrm{q}\sqrt{\mathrm{q}/4\pi\varepsilon_r\varepsilon_0}}{\mathrm{kT}}\sqrt{E}\right) + \ln(\mathrm{A^*T^2}) - \frac{\mathrm{q}\emptyset_\mathrm{B}}{kT} \qquad (2.2)$$

where k is the Boltzmann's constant, T is the absolute temperature, ε_r is the optical dielectric constant, ε_0 is the permittivity in vacuum, and A^* is the effective Richardson constant.

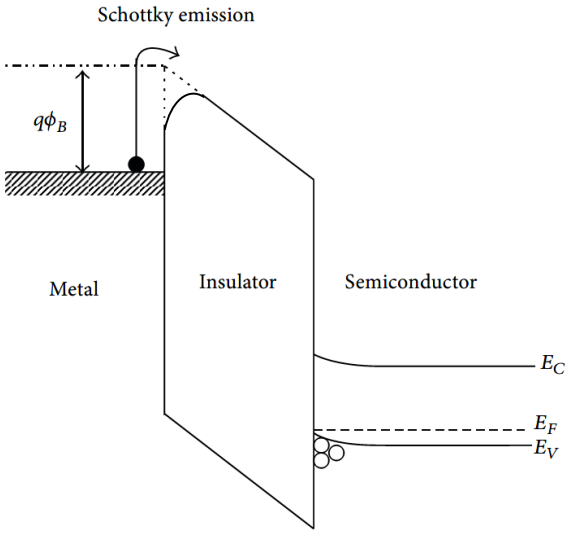

Figure 2.20 Schematic energy band diagram of SE in MOS structure [53].

Figure 2.20 shows the lowering of the energy barrier height at the metal dielectric interface by the image force, which is achieved by applying an appropriate electric field across the metal-insulator-semiconductor (MIS) structure. This is also known as the Schottky effect.

By plotting the linear expression of $\ln(J)$ vs $\left(\sqrt{E}\right)$, the barrier height at the metal-dielectric interface can be calculated and identified by the y-intercept. In addition, the gradient of the slope allows the optical dielectric constant to be calculated which can be used to validate if schottky emission is the main conduction mechanism within the dielectric. The optical dielectric constant of the dielectric layer can be approximated to be the square of the refractive index as:

$$\varepsilon_r = n^2 \qquad (2.3)$$

Where n is the optical refractive index. The optical refractive index can be measured using an optical ellipsometer.

2.2.4.3 Poole-Frenkel (PF) Emission

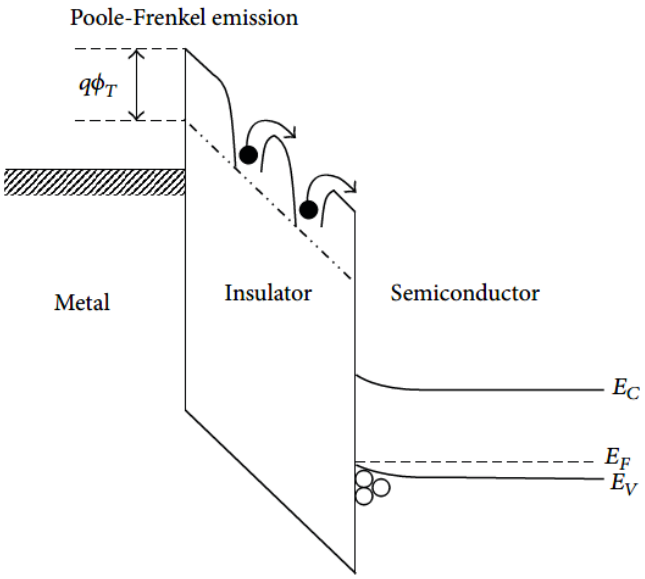

Figure 2.21 Schematic energy band diagram of PF emission in MOS structure [53].

PF is a bulk limited conduction where trapped electrons within the dielectric bulk, gets emitted into the conduction band by thermal excitation. Therefore, PF emission is also sometimes known as the internal SE. Traps within the dielectric can be process or stress induced. When an appropriate *E*-field is applied, the potential barrier of the trapped electrons can be reduced, increasing the probability of thermally emitting the electrons into the conduction band. Larger barrier lowering is usually required for PF as compared to SE. Therefore PF conduction is often observed at high temperature and high *E*-field. Figure 2.21 shows the schematic energy band diagram of a PF emission. PF

emission can also be described in its linear expression as below:

$$\ln\left(\frac{J}{E}\right) = \left(\frac{q\sqrt{q/\pi\varepsilon_r\varepsilon_0}}{kT}\sqrt{E}\right) - \frac{q\emptyset_T}{kT} - \ln\left(\frac{1}{q\mu N_c}\right) \qquad (2.4)$$

where $q\emptyset_T$ is the trap energy level, μ is the electronic drift mobility and N_c is the density of states in the conduction band. From the linear equation, PF conduction can be determined from a straight line plot of a ln (J/E) vs $\sqrt{E}$ curve. Based on the gradient of the straight line, the optical dielectric constant can be extracted and verified experimentally using an optical ellipsometer.

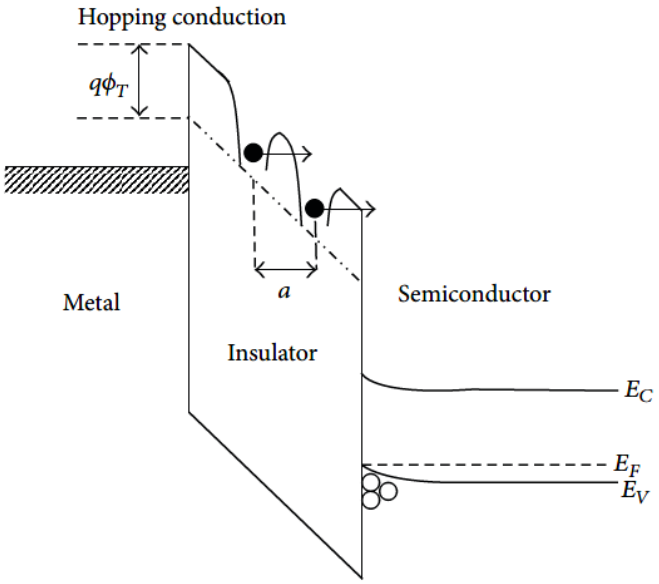

Figure 2.22 Schematic energy band diagram of hopping conduction in MOS structure [53].

When the potential barrier is too high for the carrier to overcome via the thermionic mechanism, tunneling from one trap site to another within the dielectric can take place if the tunneling distance is short, and is known as the hopping mechanism.

However, when the tunneling distance is long or when the electric field is too low for the tunneling effect, PF conduction may dominate through the thermionic mechanism. Figure 2.22 shows the schematic energy band diagram of a hopping mechanism and "a" in the figure represents the mean hopping distance between trap sites.

2.2.4.4 Ohmic Conduction

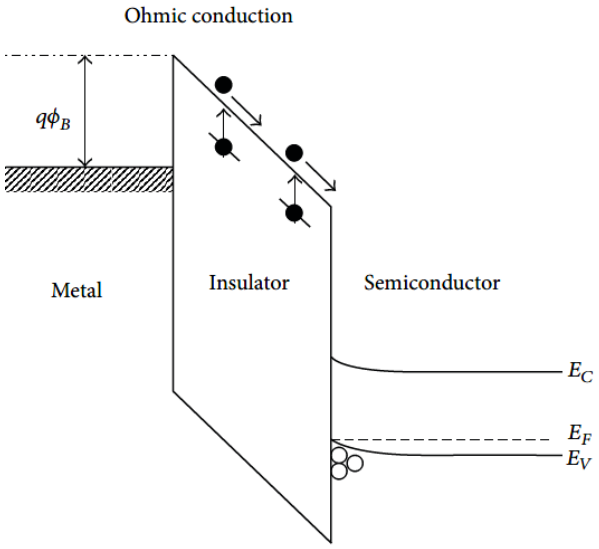

Figure 2.23 Schematic energy band diagram of Ohmic conduction in MOS structure [53].

The ohmic conduction mechanism is due to the flow of mobile electrons and holes in the conduction and valence band respectively. Figure 2.23 shows the schematic energy band diagram of an ohmic conduction mechanism. It has a linear expression which can be expressed as:

$$J = \sigma E = nq\mu E \qquad (2.5)$$

where σ is the electrical conductivity, μ is the electron mobility and n is the number of electrons in the conduction band. The current density is linearly proportional to the electric field. While the energy band gap of a dielectric is large, a small amount of electrons can still be generated and excited into the conduction band from trap states. It is expected that the magnitude of the current is small, therefore, ohmic conduction is usually observed when there are without the influence or contributions of other conduction mechanism. As a result, to prevent the onset of other contributing conduction mechanisms, ohmic conduction is most usually observed at low electric field.

2.2.4.5 Space-Charge Limited Conduction (SCLC)

There are three different carrier injection modes which are weak, strong and very strong injection. Figure 2.24 is a typical current density-voltage plot in log-log scale illustrating the three difference modes.

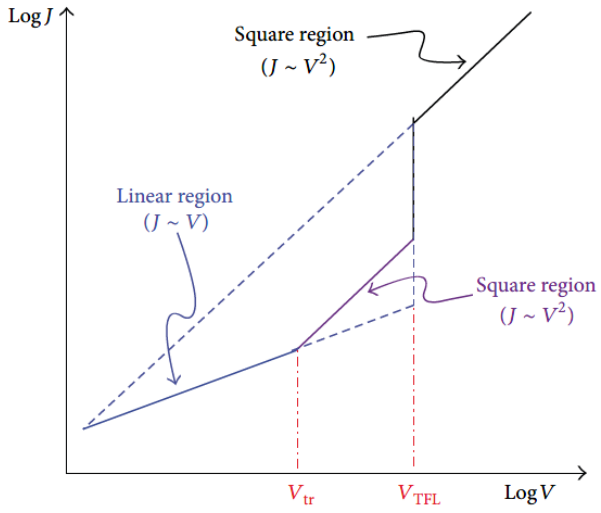

Figure 2.24 A typical Log (J) Vs Log (V) plot of a SCLC leakage current [53].

At low electric field or weak injection, the carrier transit time is larger than the dielectric relaxation time where charges can be redistributed. When the dielectric relaxation time is long, injected carriers have the opportunity to redistribute, maintaining internal charge neutrality. Therefore during weak injection, carriers do not have the chance to travel across the dielectric. However, some charge carriers can still be trapped during weak injection, where ohmic behavior can be observed.

During strong injection where voltage is beyond the transition voltage V_{tr}, the electron transition time is shortened. As a result, a space charge appears as excessive charges are unable to redistribute in time. Traps within the dielectric also starts to be filled up during strong injection. The equation for trap filled limited current is:

$$J_{TFL} = \frac{9}{8}\mu\varepsilon\theta\frac{V^2}{d^3} \qquad (2.6)$$

where J_{TFL} is the trap filled limited current, V is the voltage applied, ε is the static dielectric constant, θ is the ratio between free and total carrier density including trapped carriers and d is the dielectric thickness.

$$J_{Child} = \frac{9}{8}\mu\varepsilon\frac{V^2}{d^3} \qquad (2.7)$$

Traps within the dielectric are continuously being filled, up to a

point where it reaches the trap filled limit (V_{TFL}) at the very strong injection mode. The equation for a trap free SCLC following Child's law is shown in the equation 2.9 above where θ, the ratio between free and total carrier density, including trapped carriers is 1.

Beyond the V_{TFL}, all traps are filled and the space charge is build up resulting in an increase in free electrons, thus increasing the current density. Due to the induced space charge within the dielectric in SCLC, it inhibits the further injection of additional charge carriers into the dielectric. This results in the current density being proportional to the square of the applied voltage, increasing more rapidly as compared to an ohmic conduction. Therefore, when plotted in a log-log scale shown in Figure 2.23, SCLC will result in a gradient of 2 as compared to the ohmic conduction with a gradient of 1.

2.2.4.6 Ionic Conduction

Ionic current flow can be induced by an applied electric field or a gradient in the concentration of mobile ions within the dielectric. In the case of an applied electric field, ionic current flow initially but decreases over time since there is an absence in the constant supply of ions which are neither readily injected nor extracted from the oxide. Under an applied electric field, ions coming from lattice defects within the dielectric may jump from one defect site to another. The movement of ions or ionic conduction can be expressed in its linear form as:

$$\ln(\mathrm{J}) = -\frac{\mathrm{q}\emptyset_{\mathrm{B}}}{\mathrm{kT}} + \frac{\mathrm{Eq}d_s}{2\mathrm{kT}} + \ln(J_0) \qquad (2.8)$$

where, d_s is the distance between two defect site and (J_0) is the proportional constant.

When the electric field is removed, the charge that has been built up initially begins to flow back towards their equilibrium positions. This is similar to a diffusion process where ions diffuses from a region of higher to lower density gradient. As a result, a hysteresis effect can be observed on a typical *I-V* plot.

2.2.5 Time Dependent Dielectric Breakdown (TDDB)

The insulation of a TSV interconnect to the surrounding silicon is its dielectric layer. The use of Cu together with thinner dielectric layers due to the continuous scaling of devices, possess reliability risk which needs to be assessed. Cu diffuses quickly into the dielectric layer causing leakage and device failure. In addition, due to the geometry and construction of a TSV structure, weakness in the corners and roughness on the dielectric side wall during process fabrication, may also introduce reliability risk on the integrity of the dielectric. It is therefore important that the dielectric TDDB performance is assessed.

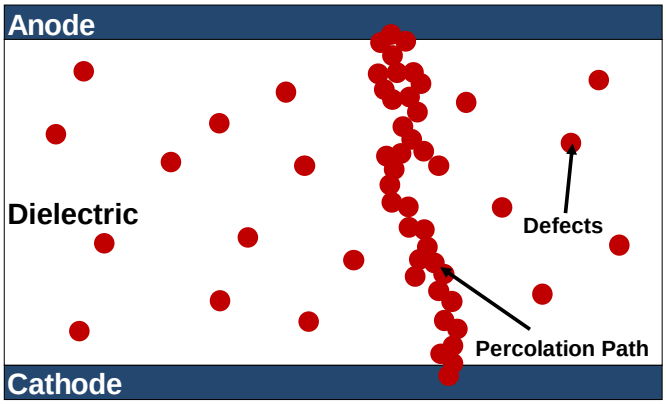

Figure 2.25 Percolation path between the cathode and anode.

TDDB is measured by applying a constant electric field across the dielectric, often higher than its intended design in operation. During the wear out stage, traps are created and built up within the dielectric as electrons tunnels through the dielectric by charge injection mechanism. The destruction of the dielectric layer occurs once there is a critical amount of defect density formed during the wear out process, where a percolation path is formed between the cathode and anode as shown in Figure 2.25. TDDB test is an irreversible test where the dielectric will be permanently damaged.

TDDB test takes a long time, therefore the TDDB model to extrapolate test results to predict actual field life is important. When the time to breakdown is measured, the actual field life can be estimated using TDDB reliability models. Several TDDB models have been proposed over the years and will be described briefly in the subsequent sections.

2.2.5.1 E Model

The E model is a thermochemical model where TDDB takes place due to a field driven thermal bond breakage. The model was introduced by Macpherson et al. to predict the breakdown time of SiO_2 thin film at low electric field. Base on the model, the dielectric time to failure (TTF) can be predicted by the following equation [59]:

$$TTF_{E-Model} = A_0 \exp\left(\frac{Q}{k_B T}\right) \exp(-aE) \qquad (2.9)$$

where A_0 is the material dependent coefficient (varies with different devices), Q is the activation energy and a is the field acceleration parameter.

The E model describes that the applied electric field stretches and weakens the polar molecules, making them susceptible to thermal bond breakage. The continuous generation of defects by the degradation and thermal breakage of the weak chemical bonds of the dielectric material, will eventually forms a percolation path between the cathode and anode where TDDB is observed [60, 61].

2.2.5.2 $\frac{1}{E}$ Model

The 1/E TDDB model that takes into account the current conduction mechanism across the dielectric was first introduced by Chen *et al.* [62] for thin gate oxide. In this model, the FN conduction mechanism is considered.

When electrons are tunneled through the dielectric from the cathode, damages due to impact ionization can be expected in the dielectric layer. In addition, when the electrons reach the anode, the energetic electrons thermalize and generates holes in the anodes. The generated holes are then injected back into the dielectric due to the direction of the applied electric field inducing more damages, since they are more easily trapped, having a greater effective mass as compared to electrons. Overtime, as more positive trapped charges builds up near the cathode, further increasing the electric field for more FN tunneling, leading to an eventual TDDB event. The time to failure according to the 1/E model is expected to show a reciprocal dependence on the electric field due to the FN tunneling current. The equation is described as:

$$TTF_{\frac{1}{E}-Model} = \tau_0(T) \exp\left(\frac{G(T)}{E}\right) \quad (2.10)$$

where $\tau_0(T)$ is a prefactor dependent on temperature, $G(T)$ is a field acceleration parameter dependent on temperature.

2.2.5.3 $\sqrt{E}$ Model

Similar to the 1/E model, the $\sqrt{E}$ model is also based on the leakage current mechanism though the dielectric. The 1/E model assumes a high quality dielectric layer with minimal defects where the dominant current conduction is FN tunneling. However, this will not be the case for a poor quality or degraded dielectric with significant defects and trap density, where the conduction mechanism is likely to become either a SE or PF one. Since both the SE and PF conduction have a $\sqrt{E}$ dependence on leakage current, the time to failure therefore, is also expected to be proportional to the square root of the applied electric field.

$$TTF_{\sqrt{E}-Model} \propto \exp\left(-a\sqrt{E}\right) \quad (2.11)$$

The model was first introduced by Scarpulla et al. [63] on GaAs based metal-insulator-metal (MIM) capacitor, using Si_3N_4 as the dielectric material. Allers K. H. [64] also showed that the $\sqrt{E}$ model is able adequately describe the reliability of a SiN based MIM capacitor with experimental data supporting the model. Subsequently, the $\sqrt{E}$ model was also proposed more recently for

low-k dielectric [65], which have higher leakages as compared to the high quality thermally grown SiO_2. In addition, degraded dielectrics due to Cu ion migration [66] can also be described adequately with the $\sqrt{E}$ model.

2.2.5.4 Lloyd Model

The main idea of the Lloyd model is that an electron, after injection into the dielectric, is accelerated by the electric field and gains enough energy to cause impact damage to the dielectric. Damage to the dielectric depends on the probability of the electrons travelling through the dielectric given a sufficient mean free path, gaining energy higher than the threshold energy for impact damage where a defect will be generated. The accumulation of such defects and traps eventually cause TDDB to occur.

The Lloyd model was proposed by Lloyd et al. [67] and can be described by the following equation:

$$TTF_{LLoyd-Model} = \frac{(N_f - N_0)}{AE} \exp\left(\frac{E_t}{\mu q E} - \gamma\sqrt{E}\right) \qquad (2.12)$$

where N_f is the number of defects, N_0 is the number of pre-existing defects, A and γ are pre-exponential term from the PF function shown in Table 2, μ is the mean free path of electron and E_t is the threshold energy required for defect generation within the dielectric, when the injected electron is accelerated by the electric field.

The Lloyd model is sometimes also known as the impact model or the $(\frac{1}{E} + \sqrt{E})$ model. The first term in the exponential represents the impact damage caused by the electron while the second term represents the leakage current. The model does not take into account the specific mechanism for damage creation leading to breakdown but made some assumptions. Firstly, electrons are injected into the dielectric by the PF conduction mechanism. Secondly, the electrons have sufficient mean free path before a collision. Thirdly, the energy gained and transferred from the electron to the dielectric during the collision is sufficient to cause defects. Lastly, the rate of defects generated will determine the time to breakdown.

2.2.5.5 Power Law Model

The power law model was proposed for ultra thin gate oxides where a voltage driven model is used instead of an electric field driven one. It is mentioned that for ultrathin dielectric of below 5nm, it does not exhibit an Arrhenius temperature dependence anymore [68]. In addition, it was reported that the exponential law will no longer apply leading to two physically impossible results. Firstly the projected lifetime of a thinner oxide would exceed that of a thicker oxide at lower voltage. Secondly, the oxide breakdown distribution violates and is unable to preserve the fundamental Poisson area scaling using the exponential law.

On the other hand, the voltage dependent power law was able to describe TDDB performance of thin oxides as follows:

$$TTF_{Power} \propto {V_{gate}}^{-n} \qquad (2.13)$$

Where V_{gate} is the applied gate voltage and n is the power law exponent which can be derived experimentally. For oxide thickness between 5nm, the exponent is typically in the range between 40 to 48 [61, 69].

2.2.5.6 Uncertainties and Current Status of TDDB Models

There have been a number of TDDB models proposed, with different physics and theories behind each model from past researchers. When fitting the same set of TDDB data to various models as shown in Figure 2.26, it is observed that the prediction of all the models agrees at high electric field and only starts to differ as one extrapolates towards the lower electric field region. When extrapolated to the actual device operating use conditions at lower electric field, the E model will be the most conservative with shortest time to failure prediction as compared to the rest of the models. The $\sqrt{E}$, $\frac{1}{\sqrt{E}}$ and $\frac{1}{E}$ model follows after the E model, with each being more relaxed on the prediction respectively.

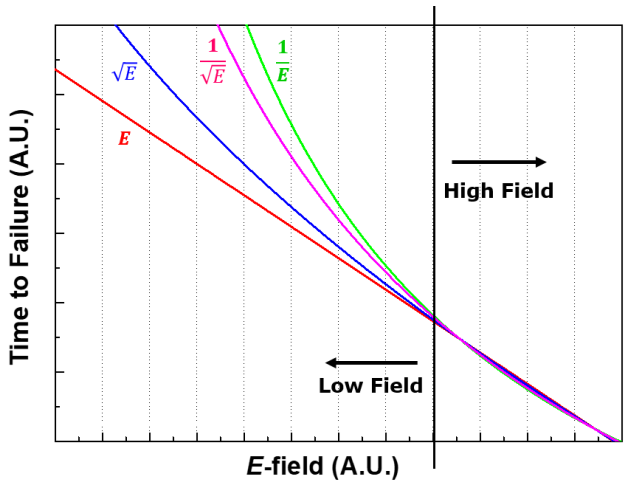

Figure 2.26 Various TDDB model showing divergence at lower *E*-field and convergence at higher *E*-field.

There is at the moment no universal agreement on which is the most appropriate model to use [70]. Lee et al. [71] has consolidated TDDB experimental data from multiple literatures for low-k dielectrics, normalizing and plotting them within the same plot along with various TDDB models. It was observed that despite the efforts from past researchers, there is still no consensus on the most appropriate model to use for extrapolation due to the lack of data at the lower electric field. The problem with TDDB test is that it takes a significantly long time to complete at low electric field. Therefore, it is safe to say that, until data from lower fields are obtained to distinguish the models, the exact physical failure mechanism leading to dielectric breakdown will be unknown.

The models described so far, also did not include extrinsic factors such as Cu migration, where the role of copper in the dielectric layer and its interaction during TDDB is still unclear. More recently, Borja et al. attempted to establish a charge trapping model that describes the interactions between migrated Cu ions, electrons, and intrinsic defects in the dielectric [72]. Chen et al. suggested that there could be a competing role between Cu ions and electron fluence which could modulate dielectric breakdown time under certain extreme conditions [73]. The same authors also observed a difference in the fitting model between a barrier and barrier-less sample following the $\sqrt{E}$ and $\frac{1}{\sqrt{E}}$ model respectively. It is therefore suggested that the $\frac{1}{\sqrt{E}}$ model could be used for samples with potentially large Cu contamination at high stress fields. However, there is at the moment a lack of physics

and understanding to support the model usage. In separate work by Suzumura et al. [66], a $\sqrt{E}$ model was also proposed due to the migration of Cu into the dielectric layer. However this is in disagreement with Zhao et al. [74] and Lloyd et al. [75] who proposed that the $\frac{1}{E}$ and Lloyd model is able to better describe the interaction of Cu presence in the dielectric layer respectively.

While there are still debates on which is the correct TDDB model to use, it is clear that the introduction of Cu into dielectric will affect the dielectric lifetime models. TDDB test which is often used as a reliability indicator for dielectrics, can be affected by the potential interaction between Cu ions and electrons flow within the dielectric. Furthermore, most of the literature on TDDB models are studied on gate oxides, planar and damascene structures. Limited study focus on the influence on how a TSV structure with geometrical differences affects the results and validity of the model. Therefore, for accurate prediction of dielectric lifetime and as for all good reliability study, more work needs to be done to address the exact failure mechanism from experimental data.

2.3 Accelerated Stress Test

The most ideal way to determine the reliability of any component is waiting for a component to fail in its intended field environment meant for its application. However it may take a long time and sometimes impossible to even complete such a test when the product is designed to be highly reliable with long lifetime [76]. Therefore accelerated stress tests are often used in reliability study to accelerate the aging effect for lifetime prediction, and to identify failures mode and mechanism of IC chips in an accelerated stress environment. Different acceleration test induces different types of failure caused by thermomechanical, electrical, environment, chemical or a combination of these mechanisms [77]. The reliability evaluation of wire bonds are often performed by subjecting bonded wires to accelerated stress test such as temperature cycling (TC), high temperature storage life (HTSL) and unbiased highly-accelerated temperature and humidity stress test (uHAST) which is a humidity related stress test.

2.3.1 Temperature Cycling

TC test is performed by alternating between two extreme temperatures at a controlled rate. The alternation between the two temperatures causes expansion and contraction to the entire IC package including material inside such as the bonded wire, lead frame, die attach etc. However, when dissimilar materials with significant CTE mismatch are put together, the different rate of expansion and contraction can lead to stress between the materials and eventually failures associated with thermal fatigue. For copper wire bonding, failures such as cracking on wire neck or micro-cracking between the wire bond and IMC interface, can be observed after TC test [78, 79]. Typical stress conditions according to the JEDEC standard JESD47 [48] for stress driven qualification of integrated circuits is between -55/150 °C up to 1000 cycles and 2000 cycles for automotive standards as stated in the AEC-Q100 revision H [51]. Ramp rate is typically at 15 °C/min as stated in the JESD22-A104E JEDEC standard for

TC [45].

2.3.2 High Temperature Storage Life

HTSL test are usually performed in air environment with temperature high enough to accelerate failure mechanisms that are activated thermally. Common degradation induced on wire bonds by HTSL is the formation and growth of IMC caused by the inter diffusion between the bond-pad interface. Extensive growth in IMC leads to the degradation of electrical performance due to the increase in wire bond contact resistance. The increase in resistance leads to heat generation as current flows, promoting additional IMC formation. IMC growth also leads to formation of cracks [80, 81], voids [82] and are susceptible to corrosion [83], affecting the wire bond reliability. Typical stress conditions according to the JEDEC standard JESD47 [48] for stress driven qualification of integrated circuits is at 150 °C up to 1000 hours and 2000 hours for automotive standards as stated in the AEC-Q100 revision H [51].

2.3.3 Unbiased Highly-Accelerated Temperature and Humidity Stress Test

uHAST is a humidity related stress test for evaluation against moisture related failures. In uHAST, high temperature and relative humidity (RH) levels are the environmental test parameters being defined and controlled for the specified test duration. As moisture plays an important role in the corrosion mechanism, it is expected that higher RH will accelerate corrosion. Therefore in the wire bonding assembly, corrosion is the main failure mechanism reported after such humidity related stress test and will usually take place at the IMC formed between the bond-pad interfaces. The moisture related corrosion can eventually lead to cracks and open failures to the wire bond system [6, 84]. Typical stress conditions according to the JEDEC standard JESD47 [48] for stress driven qualification of integrated circuits is at a temperature of 130 °C or 110 °C with a relative humidity of

85% up to 96 hours or 264 hours respectively. Similar requirement is stated for automotive standards as stated in the AEC-Q100 revision H [51].

2.4 Summary

In this chapter, a detailed literature review was done for Cu wire bonding and Cu TSV interconnect technologies. In the first part, the advantage of the transition from Au to Cu wire is introduced. A brief description of a wire bonding process is illustrated and also some of the challenges faced when transiting from Au to Cu wire bonding in reported works. Various wire bonding evaluation method are described including destructive and non-destructive methods. Their strength and limitations are described including novel methods that were reported by researchers in the past. The advantage of the diode series resistance extraction method used in this research work is also described. In the second part, a brief introduction and advantage of the TSV interconnect technology is introduced. Its fabrication process and its challenges that are reported by past researchers are also described. A general overview of the reliability stress standards and conditions reported by researchers on the study of Cu TSV are also discussed which helped to identify gaps that can be further developed in the field of research. Various leakage current conduction mechanism which can be used to describe the leakage of a TSV structure, which is also seen as a MOS structure, have been discussed. Several TDDB models proposed by past researchers are also described in this chapter. Last but not least, the purpose of an accelerated stress test and some of the commonly performed stress test in the packaging and assembly industry is discussed. Based on the literature, there are opportunities for further reliability studies and to further explore better detection techniques to understand the physics of failure mechanisms.

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Chapter 3
Study of Copper Wire Bonding

3.1 Introduction

Current industrial practice for evaluating the quality of wire bond after the packaging and assembly process can be done either destructively or non-destructively. Destructive assessment such as wire ball pull and shear test may result in loss of critical information on the wire for further investigations and can be resource intensive and time consuming which requires large efforts to execute during mass production. On the other hand, non-destructive methods via electrical testing methods may be limited by silicon real estate to include dedicated test structures. Moreover, FA tools that are able to non-destructively assess the integrity of wire bonds are often limited by its resolution or are often too costly or time consuming to execute. Therefore, current methods available for wire evaluation are limited and may not be efficient to meet production needs. In this work, the degradation of copper wire bond post reliability stress test will be evaluated using a non-destructive method, which is an accurate and quick electrical method to extract series resistance through a power diode [1].

In this chapter, the proposed method will be demonstrated and validated on an actual package for the first time, to extract the series resistance through the package already existing ESD protection diode, for its effectiveness and feasibility study. The extracted series resistance can be used to study the degradation of the entire bonded wire, consisting of both the bond-pad interface and wire span region. Moreover, automotive packages are also starting to transit to use Cu wire as an interconnect option. Automotive quality requirements are often harsher and of prolonged period as compared to packages with consumer requirements. Reliability stress test under harsher and prolonged stress conditions may result in new failure mechanisms which needs further investigation. Therefore, TC stress of automotive grade 0 condition as per AEC-Q100 revision G will be experimented in this chapter to understand the degradation performance. Experimental results will also be compared and verified with conventional destructive wire assessment methods for its effectiveness.

3.2 Experiment Setup

A packaged device with 25um Cu wires thermosonically bonded on a 3.13 um thick NiP/Pd/Au pad, will be used in the study. The package construction consist of the die attached material, the reference and test pins which are the leads of the package and the molding compound. The materials used are the ABLEBOND 3230 from Henkel, Cu with silver plating from Shinko and G700H from Sumitomo respectively. The wires are bonded using optimized bonding parameters and are subjected to TC -65/175 °C reliability stress test. Electrical readouts are taken after 0, 400, 600 and 700 cycles where four point Kelvin measurements are made using the "Keithley 2606A" source meter to eliminate any probe contact resistance before obtaining the desired diode *I-V* characteristics for series resistance extraction. The same unit after electrical measurement is then put back into the TC stress chamber for the next readout, and the steps repeated to determine the change in the extracted Rs for degradation study. The resistor components that are in series with the ESD diode during electrical measurement are as shown in Figure 3.1.

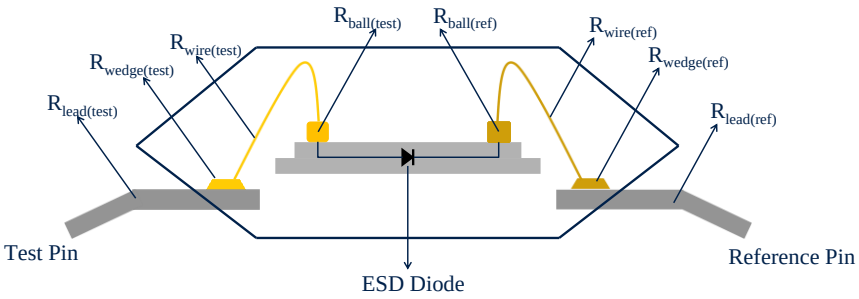


Figure 3.1 Resistor components in current path during electrical measurement.

It can be seen that the total series resistance consist of resistance from two leads and two bonded wires. Each bonded wires will then comprise of three segments, which includes the wedge bond, wire span and ball bond. It is assumed in this study that any resistance change observed from the measurement will not be significantly contributed by the leads, since the size of the leads are much larger as compared to the wire bonds. As the change in resistance after the planned TC stress readouts will be analyzed, all measurements in the experiment will be made with respect to the same reference pin. Any changes in resistance contributed by the reference pin will be consistent across all the measured test pins for accurate

assessment. As a result, any additional differences will have to be contributions coming from the bonded wire of the measured test pins. Therefore, the change in resistance measured due to degradation can be narrowed down to $R_{wedge(test)}$, $R_{wire(test)}$ and $R_{ball(test)}$.

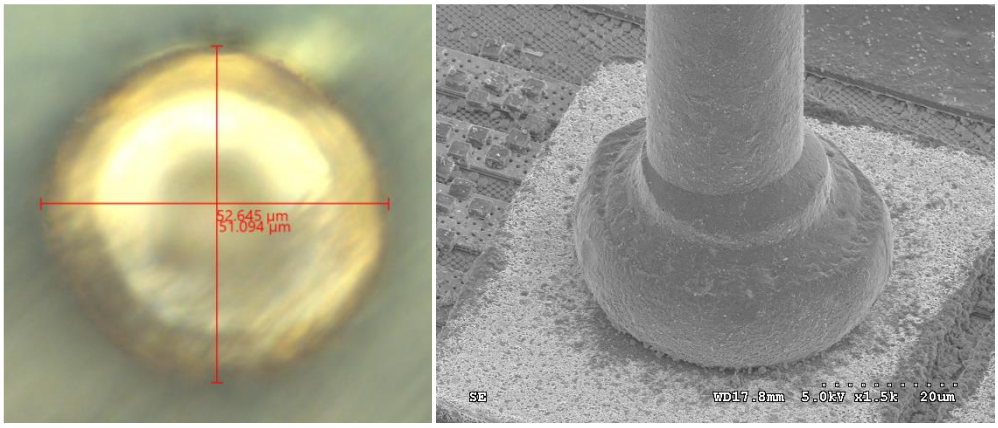


Figure 3.2 Ball bond inspection of an unstressed wire using (a) optical image and (b) SEM image after dry plasma decapsulation.

In order to correlate with conventional destructive method, an optimised dry plasma decapsulation process using the MA3000-151BB microwave plasma system by MUEGGE, in order to preserve the condition of the Cu wire bonds. An optical image measuring the ball bond diameter after plasma decapsulation is shown in Figure 3.2a. It can be observed that the ball bond is preserved without over etching during the decapsulation process and the diameter is close to the target of 55 um. The condition of the wires are also inspected on a "Hitachi SU8010" ultra-high resolution SEM as shown in Figure 3.2b, before any destructive mechanical ball pull and shear test which is performed using the "DAGE 4000plus" wire bond tester. The pull test is performed with the hook positioned as close to the ball bond as possible. A pull speed of 500 um/s was applied with the pull force perpendicular to the bonding surface to avoid any lateral or peeling effect on the wire bond. On the other hand, the shear test is performed where the shear tool is first placed on the same level as the ball bond on the bond pad. The shear height is then calculated from the bond pad surface to the height where the ball bond is sheared. Typically, a shear height of a quarter to half of the bonded ball height is recommended for accurate results. In our

experiment, the shear height is set at 5 um with a targeted ball height of 14 um. The shear speed is set at 500 um/s.

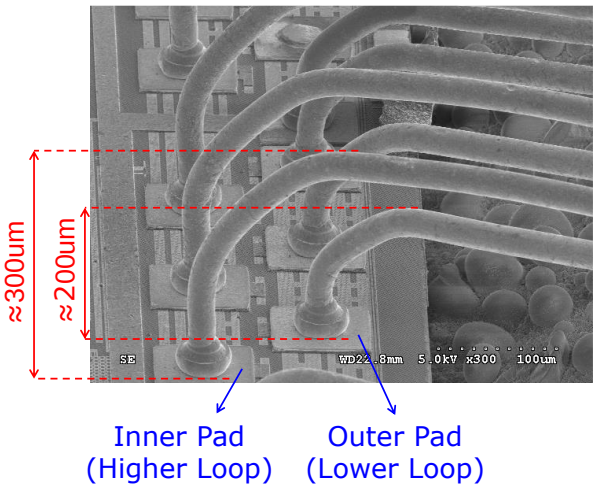


Figure 3.3 Dual pad structure with different loop height.

The device used in this experiment consists of wires with different loop heights due to a dual pad row configuration as shown in Figure 3.3. The inner pads are observed to have a higher loop height as compared to the outer pads and are approximately 300 um and 200 um respectively. It is established that the wire pull strength can be influenced by the difference in loop height as it influences the stress induced on the wires [2]. In addition, the actual break mode after pull test such as wire neck break may also influence analysis since the wire neck region is often the weakest in the entire bonding system due to a larger grain structure from the Heat Affected Zone (HAZ) after Electric Flame Off (EFO) [3]. Hence, subsequent analysis will be separated according to different wire loop height and their break modes.

The confidence bound of a normal distribution curve is used to detect wires that may have degraded more severely with reference to its resistance change values. Since the concern is primarily on a large change in resistance which could potentially reflect a degradation in the bonded wire, only the upper confidence bound is calculated. As such, a confidence level of 99.73% equivalent to most industrial practice of a three-sigma process variation, is used to calculate the upper confidence bound in this work.

3.3 Results and Discussion

The series resistance values at each individual readout are extracted and the change in resistance (ΔR) of the bonded wires with respect to its unstressed condition is used for comparison. 30 individual wire readings were measured per readout and it is observed that the $\Delta R/R$ increases with the number of temperature cycles as shown in Figure 3.4, and it is significant between 600 and 700 cycles with an average percentage increase of more than 100%.

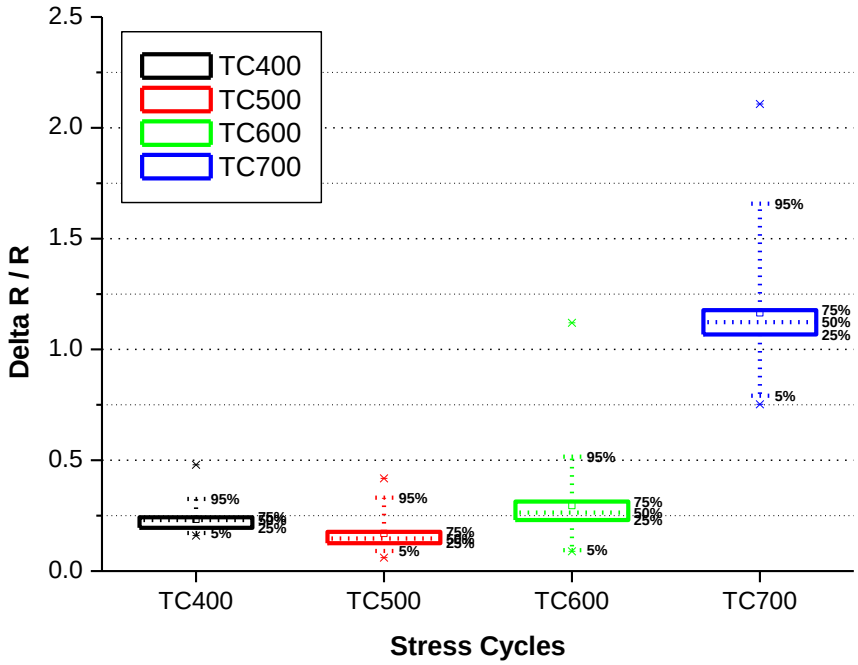


Figure 3.4 Delta R/R vs Stress Cycle plot.

To determine if the measurements at TC 400, 500, 600 and 700 cycles are statistically significant as compared to the as received sample, a 2 tailed student t-test was performed with a significance level of 0.003, indicating that the means of the stressed groups will be considered statistically different when it differs by a three-sigma variation. The t-critical score, t±0.0015, is ±3.09 at a significance level of 0.003 with a degree of freedom of 62. The calculated t-score at the various stress intervals when compared to the as received samples are shown in Figure 3.5. If the t-score is less or more than ±3.09, it is considered to be significantly different. It is observed that the t-score only increases significantly beyond t-critical after 700 cycles. This indicates that after 700 cycles of temperature cycling, there is a significant difference in the measured values.

Stress Interval	t-score
TC 400	1.073540345
TC 500	2.390066463
TC 600	2.264590269
TC 700	38.17746906

Figure 3.5 t-score at various readout for statistical significance

Comparing the SEM micrograph of the wires at different temperature cycles as shown in Figure 3.6, it is observed that the wire after 700 temperature cycles has more cracks as compared to earlier readouts. This explains the significant increase in resistance after 700 cycles of temperature cycling. It is worth noting that the visual inspection on the wires under SEM did not show signs of degradation on the wedge bonds up to 700 temperature cycles while degradation can be observed on the wire ball bond, wire neck and wire span region. As a result, subsequent analysis will be concentrating on these regions of the bonded wires rather than the wedge bond region.

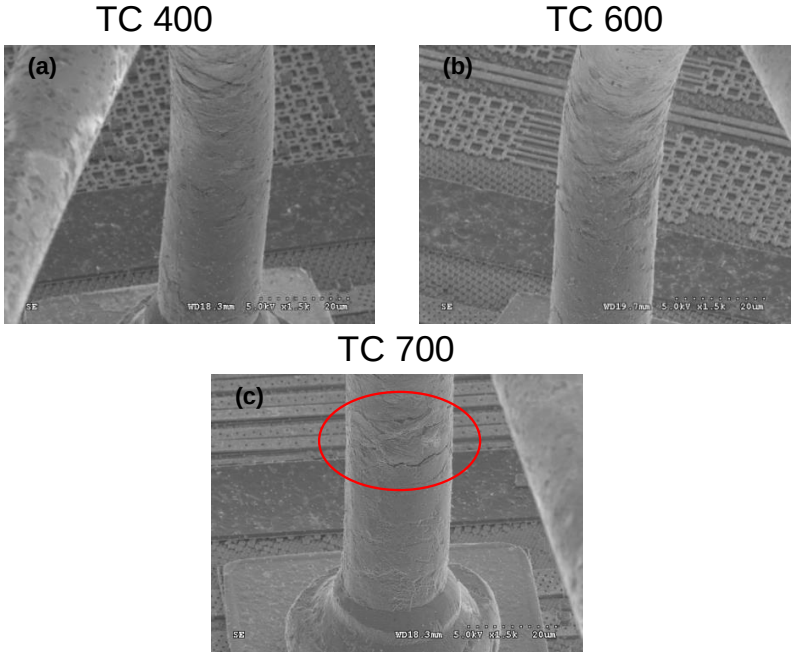


Figure 3.6 SEM micrograph of bonded wires after temperature cycling of (a) 400 cycles; (b) 600 cycles and (c) 700 cycles.

Traditional destructive pull tests for wire assessment are also performed after electrical measurement and it is observed that there is a correlation between ΔR and pull strength as shown in Figure 3.7. It can be observed that pull strength decreases with increasing ΔR at all the different stress cycles. Break modes observed after pull test up to 700 temperature cycles are either at the wire neck region or wire span region which is the region above the neck. Figure 3.8 shows an example of the wire neck and span break mode after wire pull test.

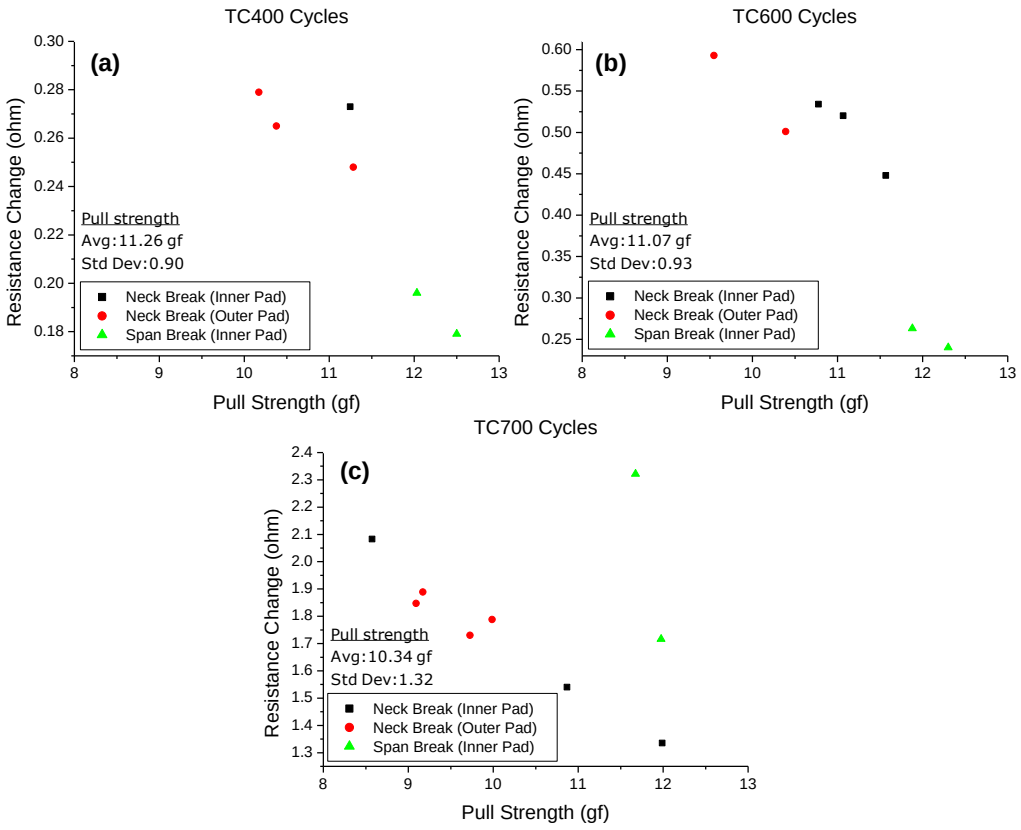


Figure 3.7 Resistance Change Vs Pull Strength plot after temperature cycling of (a) 400 cycles; (b) 600 cycles and (c) 700 cycles.

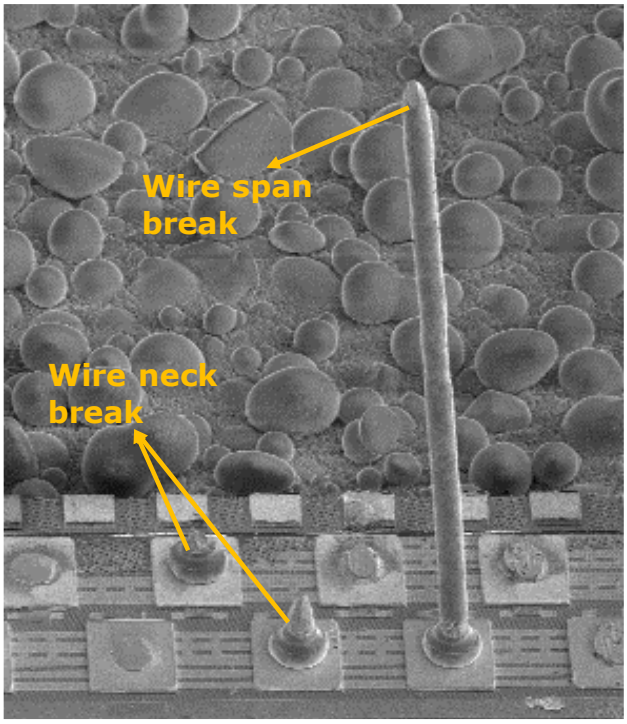


Figure 3.8 Wire neck and span break mode after wire pull test.

Separating wires bonded with different loop height on the inner and outer pad and wires of different break modes, it is observed that wires breaking at the span have higher pull strength as compared to wires breaking at the neck region as shown in Figure 3.9. This is in alignment with existing known theory that the neck region of the bonded wire is often the weakest point due to a larger grain structure at the HAZ after EFO [3]. When the neck region remains strong and wire breaks at the span instead, it can be expected that the pull strength be higher. Comparing wires bonded on the inner and outer pad, results shown are expected again where wires in the inner pad with higher loop height reflects a higher pull strength as compared to outer wire with lower loop height. Next, looking at the rate of change in resistance against the wire pull strength after the various stress cycles, it is observed that the rate of change in resistance to wire pull strength for wires bonded on both the inner and outer die breaking at the neck region are very similar, reflecting a gradient of approximately -1.5. On the other hand, the gradient for wires breaking at span is approximately -4.3 as shown in Figure 3.9. A larger gradient reflects either a smaller change in pull strength or larger change in ΔR over the stress cycles. Considering the larger gradient for wires breaking at span, it suggests that the change in pull strength is less significant as compared to the

change in pull strength for wires breaking at neck over the stress cycles. In other words, a 1 Ω difference in the change of resistance is approximately equivalent to 0.66 gf difference in pull strength for the case of wires breaking at the neck, while it is only equivalent to approximately 0.23 gf difference in pull strength for the case of wires breaking at the span. As a result, the change in pull strength is approximately 3 times less sensitive for wires breaking at span as compared to wires breaking at neck. Therefore, even though there is degradation along the wire span where a large ΔR is measured, conventional pull test may not be sensitive enough to detect the degradation based on its relatively smaller change in pull strength. Due to limited data based on the number of wires pulled, more work is required for verification. However, the results shown indicates its usefulness in the degradation study of bonding wires.

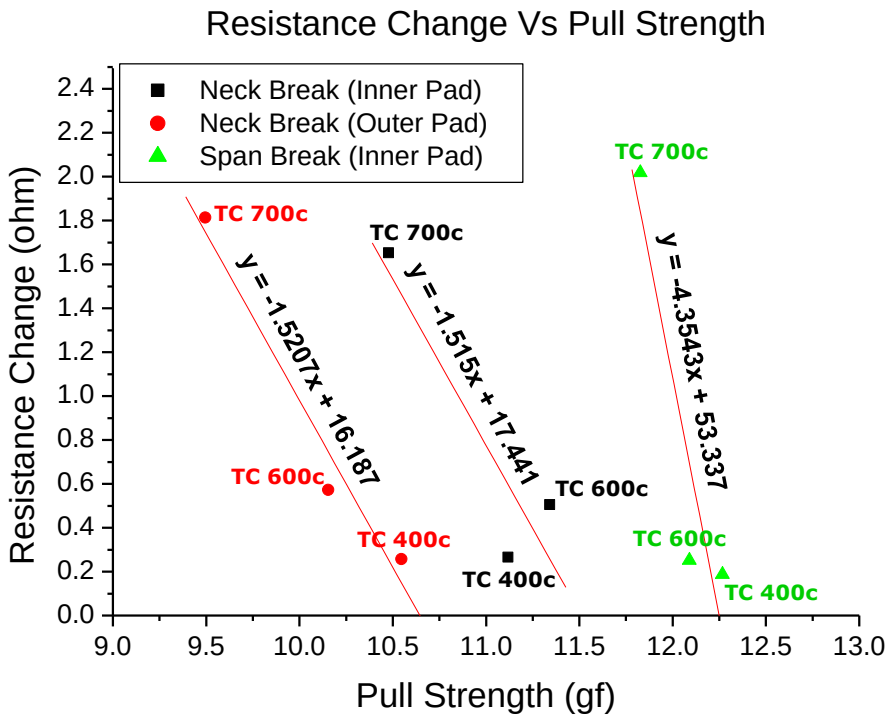


Figure 3.9 Resistance Change Vs Pull Strength plot separating wire loop height and failure mode.

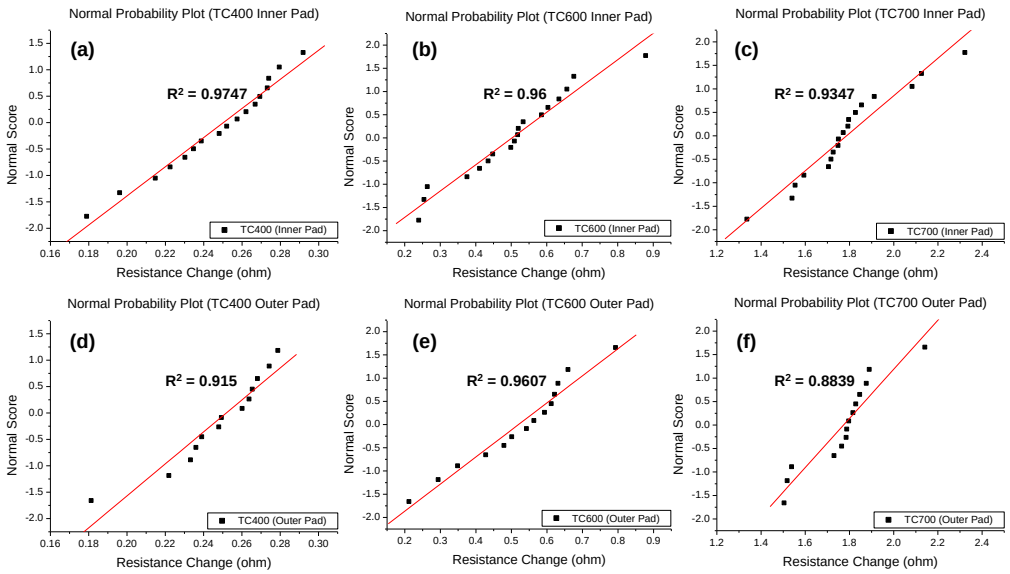
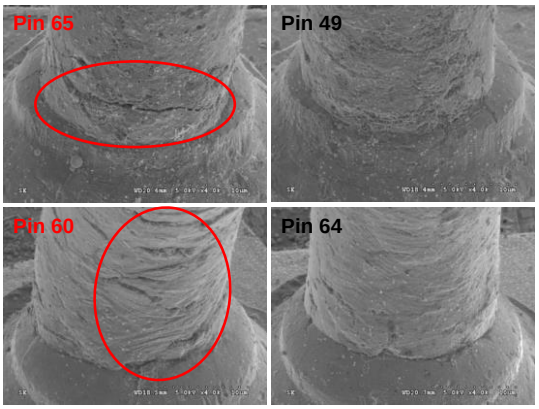


Figure 3.10 Normal probability plot using Benard's median rank method on inner pad wires after temperature cycling of (a) 400 cycles; (b) 600 cycles; (c) 700 cycles; and on outer pad wires after temperature cycling of (d) 400 cycles; (e) 600 cycles and (f) 700 cycles.

The Bernard's median rank method is a method used to estimate the probability from the cumulative distribution function (CDF) of the measured data points, which can be used to plot graphically on a probability plot. If the data points falls nicely within a straight line on a normal probability plot, it can be said that the measured data is following the normal probability distribution. This method thus allows for an accurate and graphical way to check if the measured data belongs to a certain probability distribution. As shown in Figure 3.10, Benard's median rank method is used to prove that the ΔR results are normally distributed with good linear regression. After calculating the upper confidence bound of the normally distributed data, a comparison is made from the SEM micrograph between wires out of the confidence bound and within the confidence bound for different readouts as shown in Figure 3.11. It can be observed in Figure 3.11a that wires out of the confidence bound are observed to have a more severe degradation as compared to wires within the confidence bound after 400 cycles of temperature cycling. Outlier wire pin 65 bonded to the inner pad has hairline crack at the wire neck region while wire pin 49 that is within the confidence bound does not show any sign of cracking. Another outlier wire pin 60 which is bonded to the outer pad

is observed to have accumulated significant damage after temperature cycling with visibly rougher wire surface, which can become potential sites for stress concentration and eventually crack at subsequent temperature cycles.



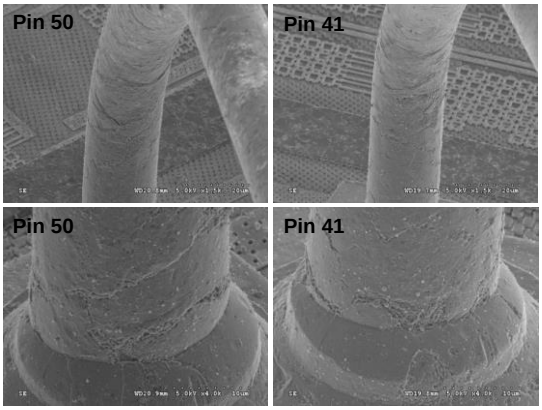
(a)

Inner Wires, ΔR Upper Confidence bound = 0.267Ω

Pin	Pull Strength (gf)	Resistance Change (Ω)	Fail Region
65	11.248	0.273	Neck Break
49	12.032	0.196	Span Break
67	12.502	0.179	Span Break

Outer Wires, ΔR Upper Confidence bound = 0.267Ω

Pin	Pull Strength (gf)	Resistance Change (Ω)	Fail Region
60	10.172	0.279	Neck Break
64	10.378	0.265	Neck Break
36	11.284	0.248	Neck Break



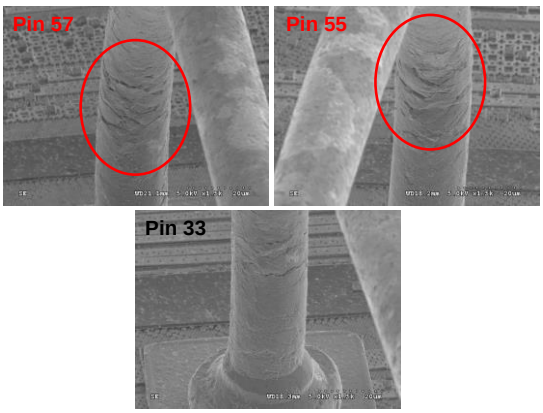
(b)

Inner Pad, ΔR Upper Confidence bound =0.609Ω

Pin	Pull Strength (gf)	Resistance Change (Ω)	Fail Region
55	10.776	0.534	Neck Break
50	11.066	0.520	Neck Break
44	11.567	0.448	Neck Break
37	11.88	0.263	Span Break
41	12.3	0.240	Span Break

Outer Pad, ΔR Upper Confidence bound =0.636Ω

Pin	Pull Strength (gf)	Resistance Change (Ω)	Fail Region
58	8.266	0.563	Neck Break
62	9.549	0.593	Neck Break
48	10.392	0.501	Neck Break



(c)

Inner Pad, ΔR Upper Confidence bound =1.935Ω

Pin	Pull Strength (gf)	Resistance Change (Ω)	Fail Region
57	8.574	2.083	Neck Break
43	10.869	1.540	Neck Break
35	11.989	1.336	Neck Break
55	11.676	2.322	Span Break
33	11.977	1.716	Span Break

Outer Pad, ΔR Upper Confidence bound =1.897Ω

Pin	Pull Strength (gf)	Resistance Change (Ω)	Fail Region
40	9.094	1.847	Neck Break
60	9.171	1.889	Neck Break
48	9.727	1.730	Neck Break
32	9.988	1.788	Neck Break

Figure 3.11 SEM micrograph of wires out of confidence bound and within confidence bound at (a) 400 cycles; (b) 600 cycles and (c) 700 cycles.

As compared to the samples that has gone through 400 cycles of temperature cycling, samples that have gone through 600 cycles of temperature cycle and for wires that were considered for pull test, the distribution does not reflect any wires that are falling out of the confidence bound. As a result, a comparison between their wires as shown in Figure 3.11b between pin 50 and 41, are observed to be similar in terms of degradation after inspecting under the SEM.

Last but not least, Figure 3.11c shows the wires considered for pull test after temperature cycling of 700 cycles. Wires that are falling out of the confidence bound are observing more cracks along the wires as compared to wires that are within the confidence bound. It can also be observed that out of bound wires at their respective readout will always correlates with lower pull strength within their respective break mode. As shown in Figure 3.11c, out of bounds wires pin 57 and pin 55, correlated with having lower pull strength in their respective failure modes. While pin 55 have a higher pull strength as compared to within bound wire at pin 43, comparing them will end up in an inaccurate analysis as their break modes are different. Pin 55 has broken at the wire span which often yields higher pull strength as compared to wire breaking at the neck region. Therefore when compared with pin 33 that is within the confidence bound and has also break mode at the wire span region, out of bound wire at pin 55 reflects a lower pull strength. This further proves that ΔR is more sensitive to the degradation of wire as compared to conventional pull test. Pull strength is not as sensitive to the degradation of wire bonds because breakage at wire span often yields higher pull strength even though ΔR is measured to be large as shown in this experiment. Furthermore, wire pull strength is also largely dependent on its geometrical configuration.

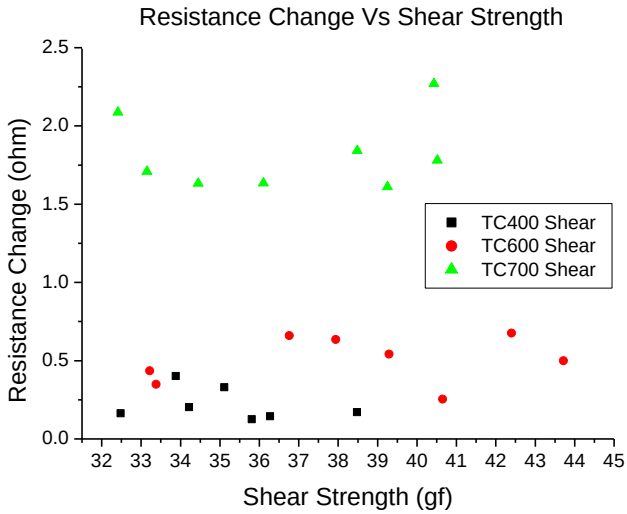


Figure 3.12 Resistance Change Vs Shear Strength plot.

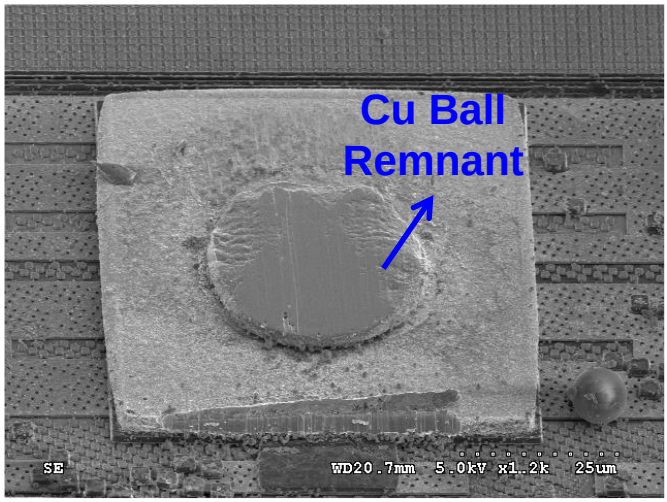


Figure 3.13 SEM micrograph showing Cu ball remnant on pad after shear test.

In addition to ball pull test, ball shear test is also performed for correlation studies with the calculated ΔR. However, no clear trend is observed between the ΔR and shear strength measured as shown in Figure 3.12. By investigating into the failure mode after shear test at their respective readout, up to 700 temperature cycles, Cu ball remnant is revealed to be left on the NiP/Pd/Au pad as shown in Figure 3.13.

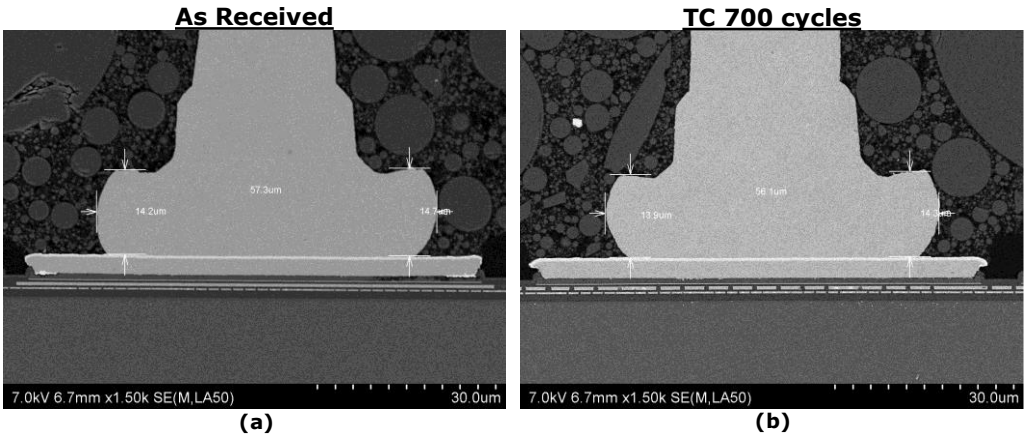


Figure 3.14 SEM cross-sectioned image of (a) as received and (b) post TC 700 cycles ball bond.

The failure mode suggests that there is still a strong bond-pad interface even after temperature cycling of 700 cycles. Figure 3.14a and Figure 3.14b shows a cross-sectioned image of a bonded ball bond as received and after TC 700 cycles, without observable degradation on the bond pad interface. Therefore, degradation at the bond-pad interface is not significant and does not contribute significantly to ΔR. It is the degradation along the wire above the bond-pad interface that has contributed significantly to ΔR. As such, shear test alone is not able to monitor any wire degradation above the bond-pad interface in contrast to the electrical method.

3.4 Summary

In this chapter, the test vehicle and experimental setup for Cu wire bond is described. The degradation of Cu wire bonded on a NiP/Pd/Au bond pad, evaluated using a non-destructive electrical measurement method was proven to be fast and accurate under TC stress. The electrical method is demonstrated to be able to detect degradation of a bonded wire with the measured ΔR values. ΔR is observed to increase with increasing stress cycles and is significant after TC 700 cycles. PFA was performed and SEM micrograph shows signs of cracks on the surface of the wire neck and span region after TC 700 cycles which explains the significant increase in ΔR. A correlation study is performed with conventional mechanical pull test method for wire assessment, and it is observed that ΔR increases with decreasing pull strength. On the other hand, there is no correlation between ΔR and ball shear strength as there is no significant degradation between the bond-pad interfaces up to TC 700 cycles. This is confirmed with the shear break mode where almost 100% of the Cu remnant is found to be left on the pad after shear test indicating a strong bond-pad interface. Therefore, it can be concluded that ΔR is mainly contributed from the degradation of the wire above the bond-pad interface in this study. Outlier wires are identified by using a normal distribution with a confidence level of 99.73%, equivalent to a process variation of three-sigma. Wires that are identified as outliers are found to correlate well with a lower pull strength. In addition, SEM micrographs also showed observable degradation on outlier wires as compared to non-outlier wires. Taking into consideration the looping profile and different break modes after pull test, it is observed that wire pull strength is less sensitive to ΔR for wires breaking at span as compared to wires breaking at the neck region. Experimental results have shown that pull strength can remain high for a wire span break mode even though the degradation detected by ΔR is large. This suggests that traditional wire pull test method may be limited in detecting degradation of the entire wire span due to the inherent weakness in the wire neck induced during the wire bonding process. Furthermore, shear test is not able to monitor degradation of the wire above the bond-pad interface. Therefore conventional methods used to assess bonded wire by destructive and mechanical means may be limited in detecting wire degradation and is insufficient to evaluate the quality and reliability of the entire bonded wire.

On the other hand, the sensitivity of ΔR seems to increase with increasing temperature cycles suggesting its usefulness in the degradation study of bonding wires.

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Chapter 4
Study of Copper TSV

4.1 Introduction

There are numerous factors affecting the reliability of TSV structures which requires more understanding and needs to be well addressed before it can be fully adopted by the semiconductor industry. This work seeks to explore potential implementation of TSV for automotive application, as present studies focused on TSV reliability in less harsh environmental conditions rather than the automotive conditions. More reliability data will be generated in this work under automotive stress test which will be used to evaluate known weaknesses as well as to discover potentially new failure mechanisms for future studies. It is also the motivation of this work to use a non-destructive electrical characterization technique to detect, monitor and control the migration of Cu ions due to a degraded barrier within a Cu blind via structure after an elevated temperature stress testing as part of the reliability assessment.

Ideally, the dielectric layer around the Cu TSV should function as a perfect insulator, free of traps when they are well processed. However, it is almost impossible to achieve a perfect insulator in the manufacturing process. In addition, the introduction of Cu and low-k dielectric material makes things more complicated and needs to be studied as well. In this work, Ti diffusion barrier was deliberately used due to its known degradation mechanism, which reacts with SiO_2 and Cu at 400 °C [1, 2]. According to Hong et al. [1], for a Cu/Ti/SiO_2 structure, Ti reduces SiO_2, producing titanium oxide between the Ti/SiO_2 interfaces and reacts with Cu between the Cu/Ti interfaces to form IMC at a temperature of 400 °C. The reaction product is a Cu_3Ti/CuTi/TiO_x system. The concentration of oxygen in TiO_x will increase overtime up to x = 1.2, and go beyond 1.2 up to x = 2 as Ti out diffuses into Cu which is amongst the competing reactions on the Ti layer. Therefore, to emulate Cu migration into the dielectric in a systematic and controlled manner, samples will be stressed at 400 °C for 30 min in nitrogen (N_2) gas environment to induce degradation to the Ti barrier for characterization study later. As heat will induce a global effect on the entire test structure, any

degradation to the barrier is said to be uniform all around the material interface as compared to deliberately introducing defects to the barrier layer during process fabrication to allow Cu migration, which can be tedious. The approach to this study is also in contrast to fabricating different structures, with and without barrier separately, in order to introduce Cu into the dielectric layer which has been extensively reported [3-5].

Due to aggressive device scaling, advance interconnect technologies often utilizes Cu and low-k dielectric materials in order to fully maximize the benefits of reducing the RC delay for device performance. Cu reduces the resistance and low-k dielectric reduces the capacitance with low permittivity. The assessment of dielectric quality can be done by measuring its leakage current and characterizing its leakage conduction mechanism for process improvement and reliability assessment. The leakage current response will be studied both before and after accelerated reliability stress test for comparison.

4.2 Experiment Setup

All test vehicles in this work were provided by the Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR). Different test structures were chosen for different purpose of the study and can be differentiated by its geometry and bill of material (BOM). All process parameters used to fabricate the test structure has been optimized. A list of test structure used can be found in Table 4.1.

Table 4.1 List of test structures.

Test Structure	Number of blind vias	Material	Stress Condition
Test Structure 1	Single	Copper Via Titanium Barrier PETEOS dielectric Aluminium metal Pad	1) High temperature stress (400 °C - 30min) 2) TC -55/150 °C 3) TC -65/150 °C 4) HTSL 175 °C
Test Structure 2	Array of 200		1) TC -65/150 °C
Test Structure 3	No via	Titanium Barrier PETEOS dielectric Aluminium metal Pad	1) TC -65/150 °C
Test Structure 4	Single	Copper Via Tantalum Barrier PETEOS / Black diamond low-k dielectric without Si_3N_4 Cap	1) TC -55/150 °C 2) HTSL 175 °C 3) HTSL 225 °C
Test Structure 5		Copper Via Tantalum Barrier PETEOS / Black diamond low-k dielectric with Si_3N_4 Cap	1) TC -55/150 °C 2) HTSL 175 °C 3) HTSL 225 °C

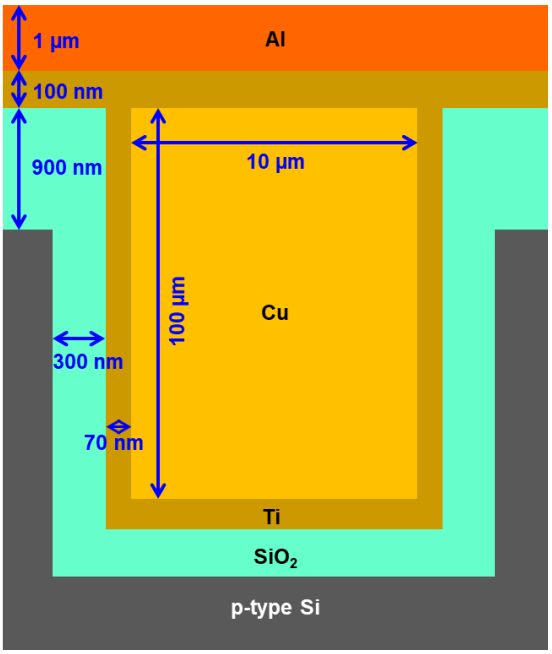


Figure 4.1 Schematic diagram of test structure 1 with blind via.

Test structure 1 used for the non-destructive detection of Cu migration is as shown in Figure 4.1. A single Cu blind via of aspect ratio 10:1 is fabricated on a p-type Si substrate with a depth and width of 100 µm and 10 µm respectively. The deep trench is etched by the BOSCH DRIE process followed by a 300 nm thick plasma-enhanced tetraethylorthosilicate (PETEOS) SiO_2 dielectric layer deposited on the sidewalls using the plasma-enhanced chemical vapor deposition (PECVD) process. Subsequently, a 70 nm thick Ti diffusion barrier and Cu seed layer is deposited using the physical vapor deposition (PVD) process followed by Cu filling of the blind via by electrochemical plating (ECP). An annealing process is carried out at 400 °C with forming gas environment where Cu chemical mechanical polishing (CMP) was used to remove any Cu overburden. Ti and Aluminum (Al) of 100 nm and 1 µm respectively are then deposited and patterned in order to form the probing pads. In addition, an array structure of 200 identical blind via structures which are uniformly spaced with a pitch of 25 um are also fabricated for this research work.

Test structures 4 and 5 were also fabricated to study the response of the blind via to known mechanical stresses and failure modes post accelerated stress test. By

using a 300 nm thick Si_3N_4 deposited by thermal chemical vapor deposition (CVD) above the blind via structure, it emulates a capped TSV such as during stacking. An uncapped blind via structures was also fabricated and studied as a comparison. In addition, black diamond low-k dielectric was also deposited in comparison to PETEOS SiO_2 dielectric. Ta diffusion barrier was used instead of Ti as it is more robust to heat degradation at high temperature. Apart from changes to the structures mentioned above, it also has a slight modification to its geometry where each blind via are 10 um deep with an aspect ratio of 1:1, and the thickness of the dielectric deposited are 200 nm thick.

The fabricated structures are subjected to harsh environmental stress conditions such as HTSL at 175 °C with 250 hours stress out intervals up to 1000 hours, and TC at both -55/150 °C and -65/150 °C with 500 cycles stress out intervals up to 2000 cycles. These conditions are common to the automotive industry defined in the AEC-Q100 (Revision H) standard [6], which defines the qualification requirements and level of quality and reliability of the IC application. Additional stress condition of HTSL 225 °C condition as well as an electrical biasing stress of up to 7 MV/cm were also experimented for its end of life reliability study. These stress test were performed either as individual stress test or as a combination stress test that are performed sequentially.

C-V and *J-E* characteristics were measured and studied after the respective stresses, in order to identify any deviations in their electrical characteristics as a result of degradation post reliability stress test. Current-voltage *(I-V*) and *C-V* characteristics are measured at room temperature after the various stress conditions using a “Keithley 4200-SCS” Parameter Analyzer and a “Cascade Microtec PM8PS” probe station. The cabling, probes and adaptors between the probe station and parameter analyzer may introduce unwanted parasitic inductance and stray capacitance to the measurement. To compensate for such errors, an open and short compensation was performed prior to any measurements for accurate analysis. *C-V* measurements are conducted at a frequency of 100 kHz. A negative *I-V* sweep is measured to exclude the effect of a depletion width in the p-type Si substrate. *J-E* characteristics are then mathematically derived based on the geometry of the test structure and plotted accordingly.

PFA will be performed to evaluate the structural integrity of the Cu blind via test structure as well as the presence of Cu in the dielectric layer before and after reliability stress testing for verification. Precise cross-sections of the test structure at specific area of interest can be achieved by performing a focus ion beam (FIB) cut. Subsequently, the FIB cut allows for further scanning electron microscopy (SEM), transmission electron microscopy (TEM) and energy-dispersive x-ray spectroscopy (EDX) analysis. In addition, in order to achieve accurate EDX analysis, the prepared TEM lamella is then transferred onto a molybdenum grid holder, instead of a Cu grid holder to exclude unwanted Cu stray signals. Last but not least, the refractive index of the dielectric material in the visible range is determined using an optical ellipsometer. The optical dielectric constant can be calculated accordingly which can be used to validate the dominating leakage current conduction mechanism of the test structure used in this study.

4.3 Results and Discussion

4.3.1 Non-destructive Detection of Barrier Degradation

The barrier layer is an important part of a Cu TSV structure as its main purpose is to prevent Cu from migrating into the dielectric layer causing quality and reliability issues. Therefore, any defects in the barrier resulting in its failure to function as its intended purpose needs to be detected. Since Cu diffuses into the dielectric layer rapidly even at room temperature, the quality of a barrier layer can be measured indirectly by detecting traces of Cu in the dielectric layer. It is the motivation of this work to perform the detection in a non-destructive manner by electrical characterization.

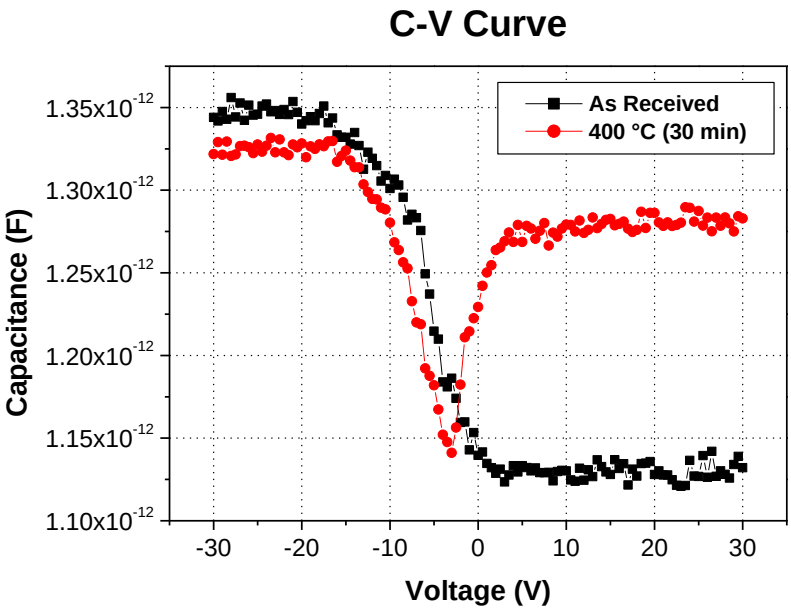


Figure 4.2 *C-V* curve of as received and high temperature stressed samples.

The integrity of the Ti barrier and SiO_2 dielectric layer were deliberately degraded at an elevated temperature of 400 °C which is known to cause a reaction at the Ti interface. The reaction weakens the barrier layer and eventually result in the migration of Cu into the dielectric layer. This method of evaluation by monitoring the presence of Cu directly on a degraded test structure eliminates the effect of any process and geometrical variations. *C-V* measurements of high temperature stressed samples at 400 °C for 30 min in N_2 environment was compared with samples as received as shown in Figure 4.2. It is observed that the inversion capacitance of the stressed sample increases as compared to the as received sample. When the Ti barrier degrades after high temperature stressing, Cu oxidizes to form positively charged Cu ions which then migrate into the dielectric layer. Migrated positively charged Cu ions induces an enhanced electric field which increases the generation of minority carriers within the p-type Si substrate. As a result, an increased inversion capacitance can be observed which is not typical of a 100 KHz *C-V* measurement for a Si substrate. Therefore, such characteristic is a clear indication of a degraded barrier where Cu have migrated out into the dielectric layer.

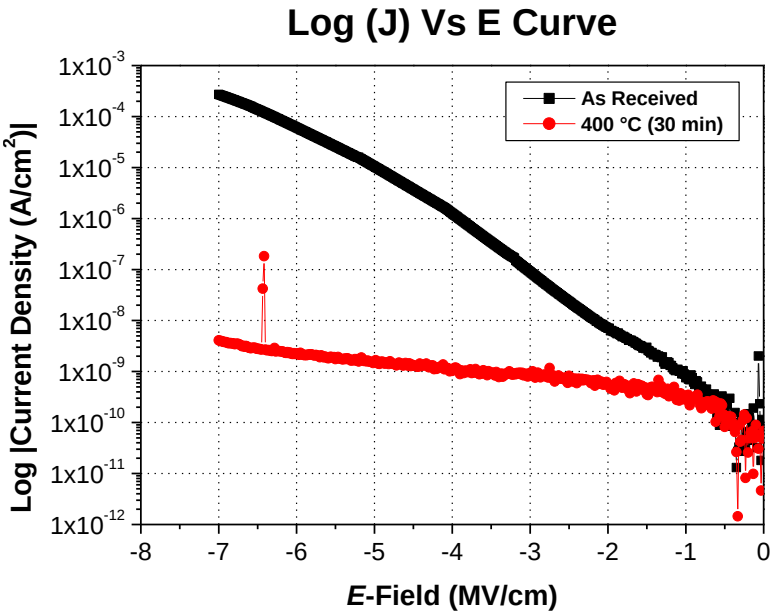


Figure 4.3 *J-E* curve of as received and high temperature stressed samples.

As shown in Figure 4.3, a significant drop in leakage current as compared to as received sample was observed from the *J-E* plot. This is expected as it is known that Ti reacts with Cu to produce a highly resistive IMC and reduces SiO_2 to produce titanium oxide at 400 °C [1, 2]. However, it is unlikely to have caused a significant drop in leakage current even though the interaction at the Ti layer can cause an overall increase in the contact resistance. On the other hand, it has been reported that the presence of Cu in the dielectric layer can cause the leakage current to drop due to electrons trapping by Cu ions [7]. As a result, the significant drop in the leakage current as shown in Figure 4.3 is suspected to be collectively attributed by both the material interaction after heat treatment which increases the overall contact resistance by highly resistive metal oxides and IMC formation, as well as deep traps inhibiting current flow due to the presence of Cu within the dielectric layer.

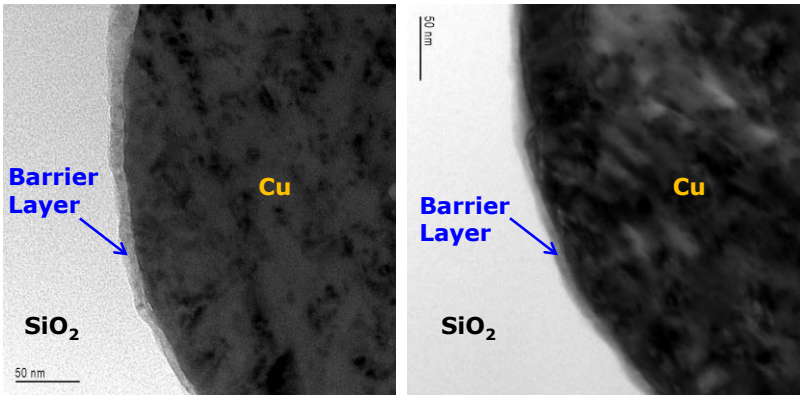


Figure 4.4 TEM micrograph of (a) as received sample and (b) high temperature stressed sample.

PFA was performed on samples after high temperature stressing to validate the presence of Cu in the dielectric due to barrier degradation as detected by the electrical measurement. Comparing TEM micrographs between the stressed and as received samples, the barrier liner was not as distinguishable for the stressed sample in terms of its contrast, which was observed to be less dense or hazy as shown in Figure 4.4b. TEM micrograph of an as received sample is as shown in Figure 4.4a as reference. This indicates that the stress condition of 400 °C for 30 min, caused physical modification to the Ti barrier, where the material interaction between Ti with neighboring Cu and SiO_2 during heat treatment reduces the effective thickness of Ti barrier, making it susceptible for Cu to oxidize and form ions, which may eventually diffuse into the SiO_2 dielectric layer.

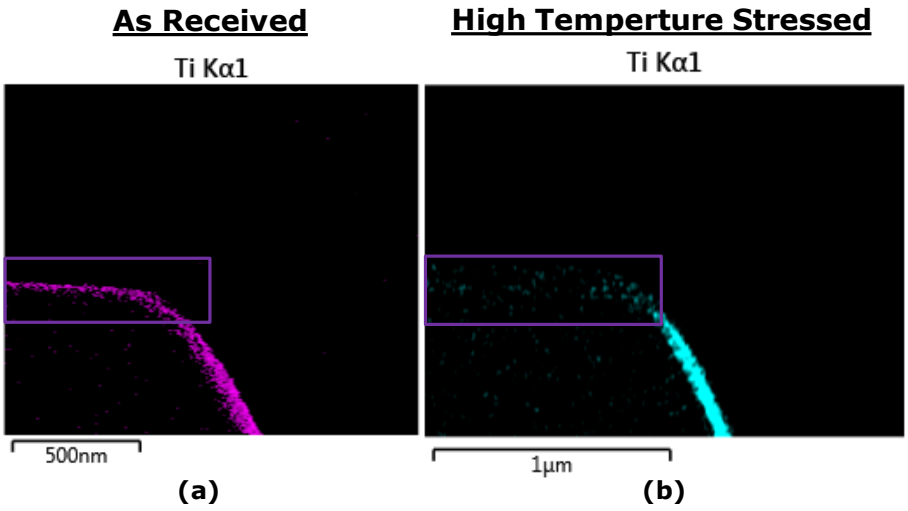


Figure 4.5 TEM-EDX elemental mapping comparing the Ti barrier layer of (a) as received sample and (b) high temperature stressed sample.

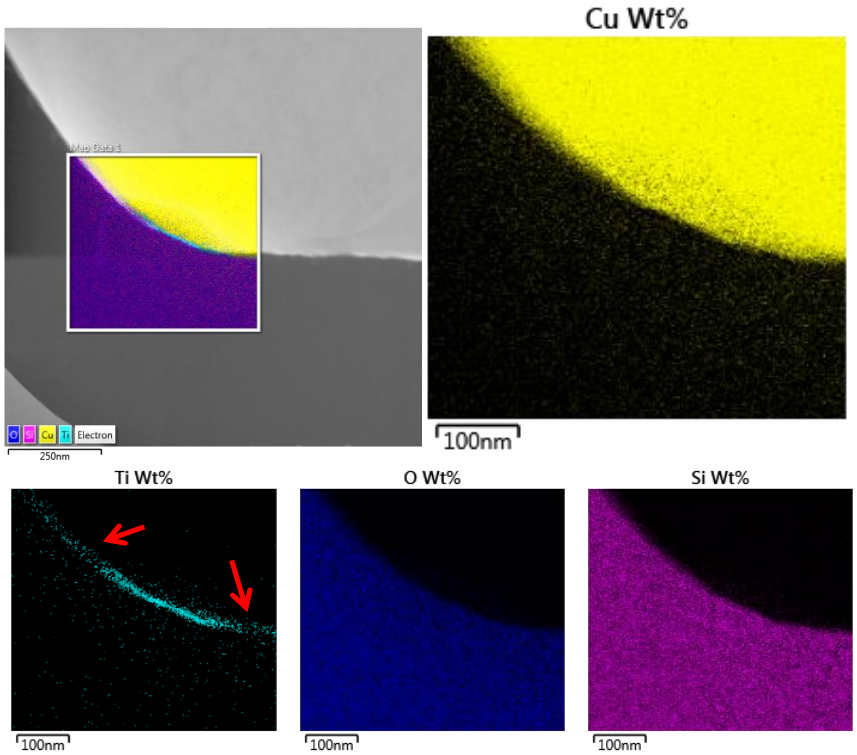


Figure 4.6 TEM-EDX elemental mapping by area scan showing Cu diffusion into the dielectric layer of a high temperature stressed sample.

An area map by TEM-EDX analysis of the Ti barrier also observed depletion of the barrier layer on the high temperature stressed sample as

shown in Figure 4.5b as compared to as received sample as shown in Figure 4.5a. As expected, due to the degraded barrier, Cu was observed to diffuse into the dielectric layer of the high temperature stressed sample as shown in the TEM-EDX area map and line scan analysis as shown in Figure 4.6 and Figure 4.7, respectively. This observation was not made for the as received sample as shown in Figure 4.8.

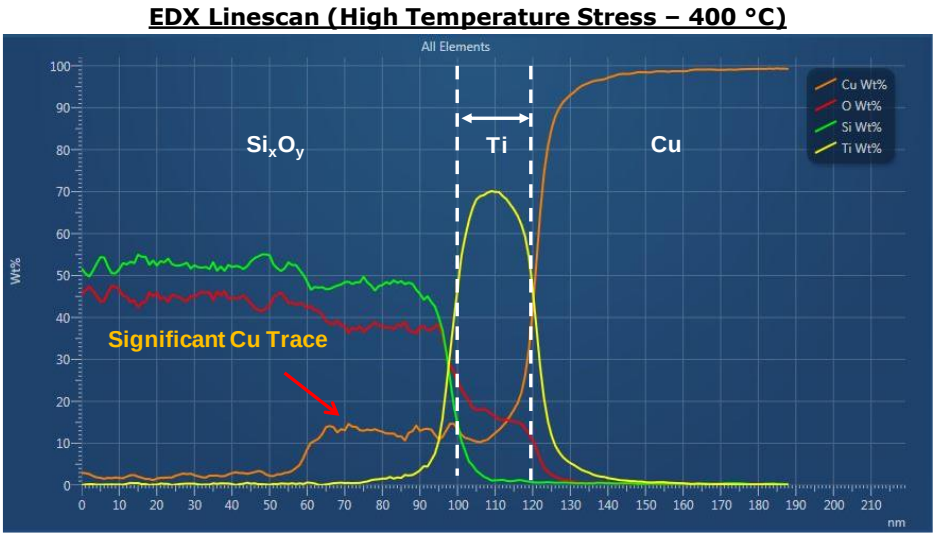


Figure 4.7 TEM-EDX elemental mapping by line scan showing Cu diffusion into the dielectric layer of a high temperature stressed sample.

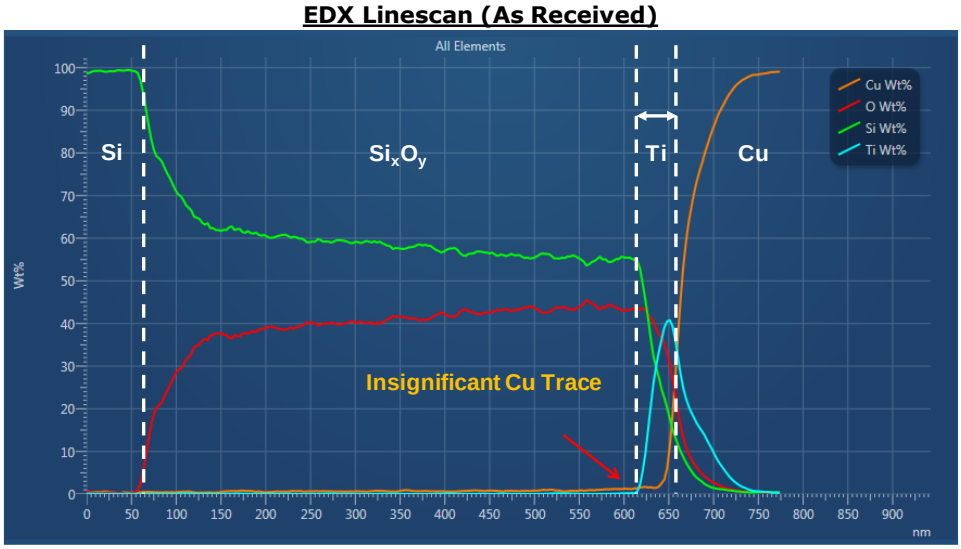


Figure 4.8 TEM-EDX elemental mapping by line scan showing no Cu diffusion into the dielectric layer as received.

During elemental analysis, TEM lamella is placed on a molybdenum grid holder rather than a Cu grid holder to eliminate any possibility of Cu stray signals which may cause an inaccurate analysis. PFA results so far corresponds well with the increased inversion capacitance of a *C-V* curve due to the presence of positively charged Cu ions in the dielectric layer as described in Figure 4.2 previously. With the validation from PFA, the change in the electrical characteristics due to Cu migration will be used as a detection method for reliability assessment post reliability stress test in the following section.

4.3.2 Electrical Characterization Post-Reliability Stress Test

C-V and *J-E* characteristics were analyzed to identify differences in its electrical characteristics before and after the elevated temperature stress on test structure 1. TC -65/150 °C and -55/150 °C up to 2000 cycles was performed on the structures to study the extent of barrier degradation by thermomechanical stress. It is observed from Figure 4.9a and Figure 4.9b that after 2000 cycles, there were insignificant change to their *C-V* curves. Figure 4.10a and Figure 4.10b also showed that there were insignificant changes to the *J-E* curves after TC -65/150 °C and TC -55/150 °C, up to 2000 cycles respectively. Next, HTSL stress at 175 °C up to 1000 hours was performed to study the effects of thermal stress over prolonged duration on the test structure with the intention to induce thermally activated failures to observe any changes to its electrical characteristics. It is observed from Figure 4.9c and Figure 4.10c that there were also insignificant change to the *C-V* and *J-E* curve respectively similar to the observation post TC stress. The relatively unchanged electrical characteristics post HTSL stress could be due to the temperature at 175 °C did not induce the same degradation mechanism as the samples stressed at 400 °C, where Ti interaction with Cu and SiO_2 is promoted. PFA was performed on structures post HTSL stress at 1000 hours, but no significant

degradation on the barrier was observed.

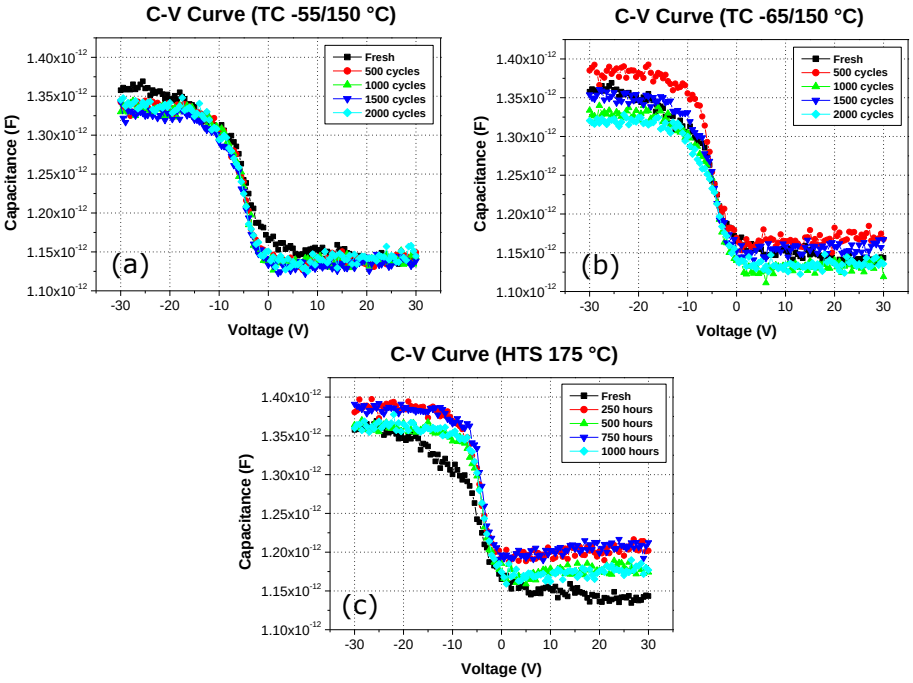


Figure 4.9 Comparison of C-V curves of fresh sample with (a) TC -55/150 °C readout; (b) TC -65/150 °C readout and (c) HTS 175 °C readout.

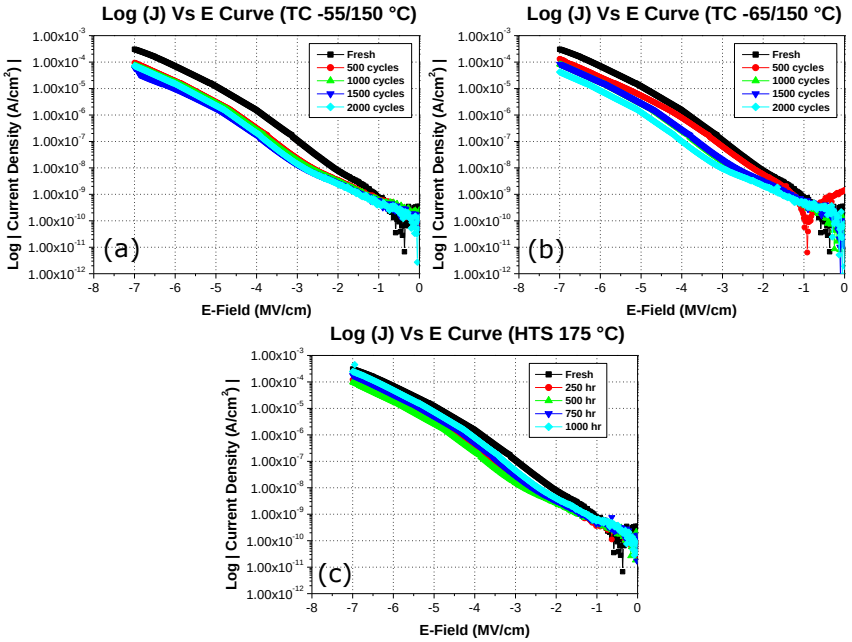


Figure 4.10 Comparison of Log (J) vs E curves of fresh sample with (a) TC -55/150 °C readout; (b) TC -65/150 °C readout and (c) HTSL 175 °C.

The results so far may seem to suggest that the test structure was not significantly degraded after TC and HTSL stress up to 2000 cycles and 1000 hours respectively. However, due to the known CTE mismatch between the Cu blind via and the surrounding Si, the blind via structure is expected to experience some level of stress during accelerated stress testing where cracks have been reported [8, 9]. In addition, during actual device application, current flows within the TSV structure and can experience high electric field. Therefore, in order to ensure that the test structure is truly intact and reliable after accelerated stress test, an electrical field of 7 MV/cm was applied to the test structure with the intention to drive any potentially existing copper ions into the dielectric layer to simulate actual field application. In addition, similar biasing was also performed on both fresh and stressed samples with a similar structures but without any blind vias embedded for comparison.

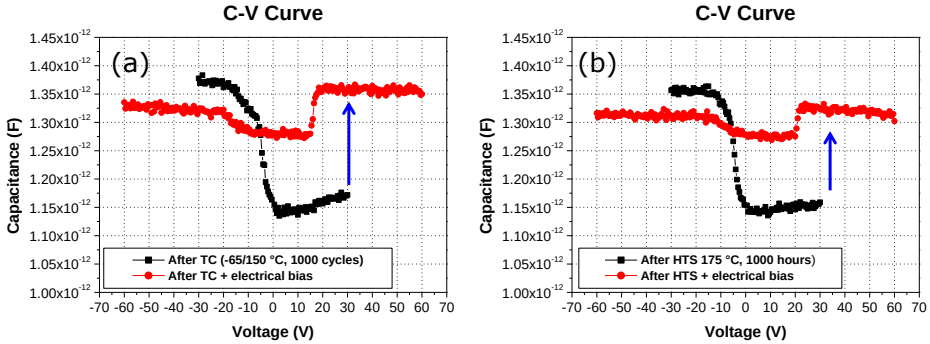


Figure 4.11 Comparing *C-V* curve before and after subsequent electrical bias post (a) TC -65/150 °C 1000 cycles and (b) HTSL 175 °C 1000 hours.

It is observed from Figure 4.11 that after a subsequent electrical bias was applied on a pre-stressed sample after TC and HTSL, an increase in the inversion capacitance was observed in the *C-V* curve again, indicating Cu ions presence in the dielectric layer as described in Figure 4.2 previously. On the other hand, similar increase in inversion capacitance was not observed on a fresh sample when similar *E*-field was applied. Therefore, it is suggested that there are degradation to the structure during the TC and

HTSL stress test and the *E*-field applied resulted in the drift of Cu ions towards the dielectric layer. This resulted in a sufficiently high amount of Cu presence in the dielectric layer, high enough to be detected and reflected by the change in the inversion capacitance.

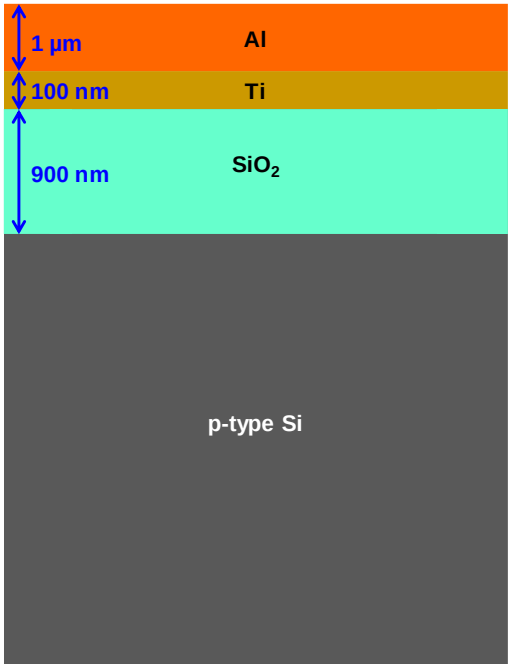


Figure 4.12 Schematic diagram of test structure 3 without blind via.

In order to isolate the stress induced degradation onto the Cu blind via structure, similar stress condition of TC -65/150 °C 1000 cycles with subsequent electrical bias was also applied to a similar structure, but without any blind via embedded for comparison. The schematic of test structure 3 without blind via is shown in Figure 4.12. The resulting *C*-*V* characteristic as shown in Figure 4.13 did not reflect any increase in its inversion capacitance which was observed for structure with blind via. Similar observation was also made for fresh samples without any blind via embedded after electrical bias suggesting that the results are independent to the TC stress. However, a negative flat band shift was observed for structures without blind via, where negative charges could be introduced into the pad oxide during wafer fabrication. The negative flat band shift was not detected for structures with blind via, as the main bulk of the capacitance measured is coming from the MOS structure that is created

between the Cu via and Si substrate as compared to the parasitic capacitance between the Al probe pad and Si substrate. The parasitic capacitance is kept low with a larger oxide thickness of 900 nm as shown in Figure 4.1, for test structure 1 with blind via. Therefore, the relatively unchanged characteristics between bias stress on as-received samples and bias stress after TC -65/150 °C 1000 cycles on structures without blind via embedded as shown in Figure 4.13, suggest that the variation in electrical characteristics where an increased in inversion capacitance was observed for structures with blind via, can be isolated to be a consequence of the degradation on the Cu blind via structure itself.

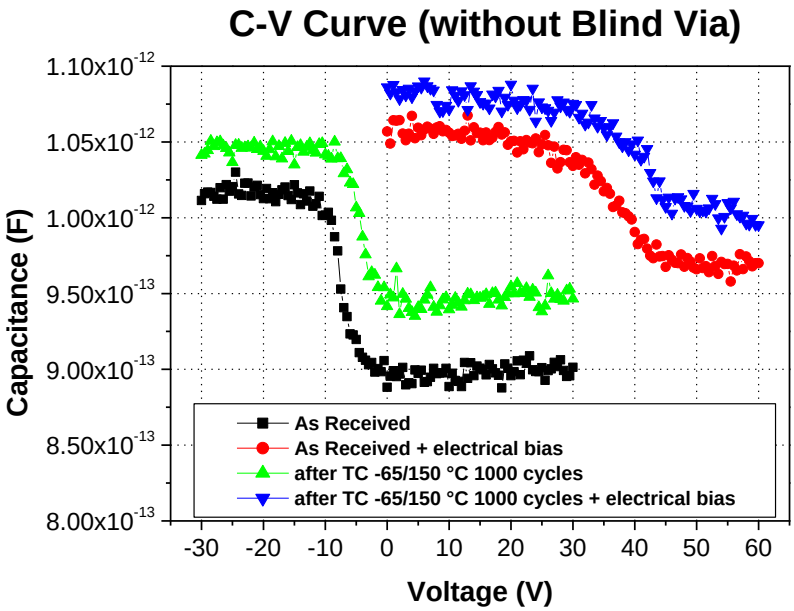


Figure 4.13 Comparing *C-V* curves of structures without blind via when as-received, as-received + electrical bias, TC -65/150 °C 1000 cycles and TC -65/150 °C 1000 cycles + electrical bias.

It is suspected that after TC-65/150 °C at 1000 cycles and HTSL 175 °C at 1000 hours readout interval, Ti barrier and dielectric layer have already been degraded. Furthermore, despite degradation to the barrier and dielectric layer of the Cu blind via, Cu ions did not readily diffuse out into the dielectric layer at room temperature and in the absence of an external driving force. In addition, due to the CTE mismatch between Cu and the

surrounding Si, formation of cracks and its propagation into the Ti barrier layer could have happened especially during TC stress. This can eventually lead to the drift of Cu ions into the dielectric layer under a sufficiently high applied *E*-field, which acts as an external driving force for Cu ions to be able to drive through the degraded barrier and cracks.

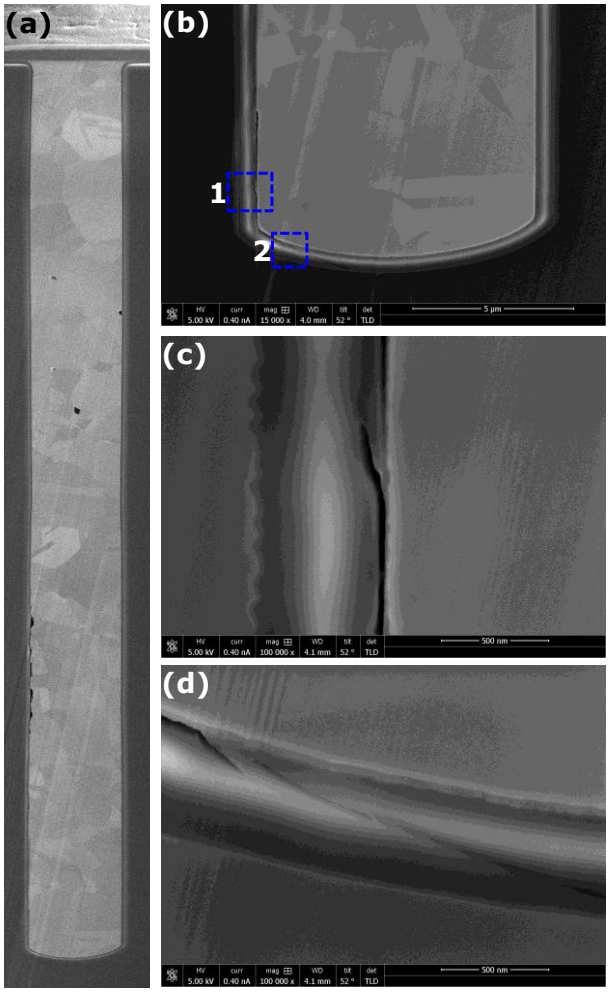


Figure 4.14 X-sect SEM micrographs of blind via structure after TC -65/150 °C, 1000 cycles showing (a) overview; (b) bottom; (c) crack site 1 propagating into dielectric layer; and (d) crack site 2 propagating into dielectric layer.

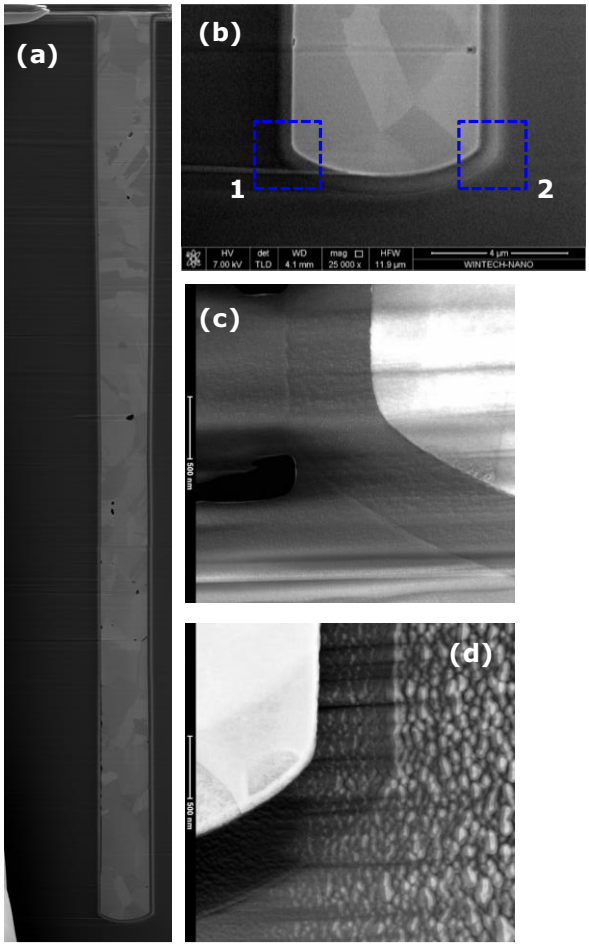
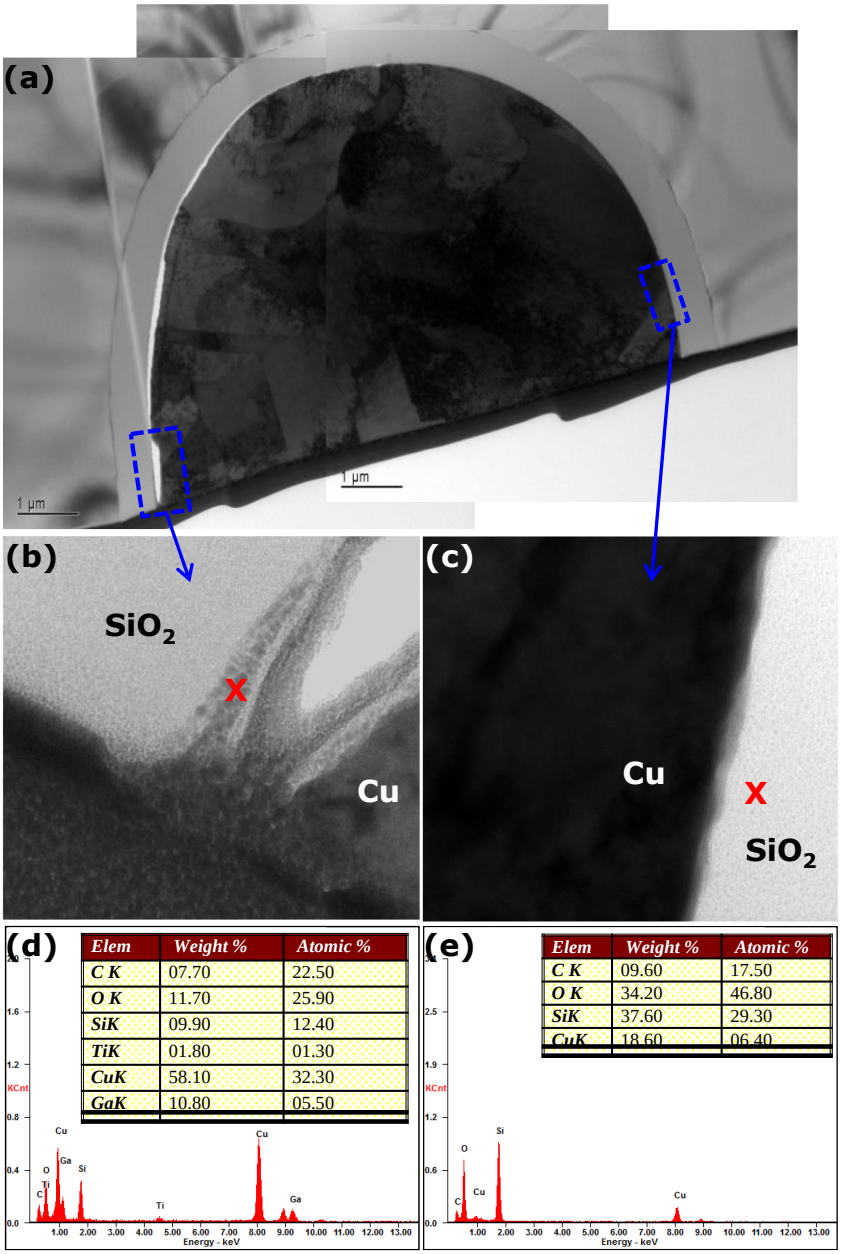


Figure 4.15 X-sect SEM and TEM micrographs of blind via structure as received showing (a) overview; (b) bottom; (c) TEM of site 1; and (d) TEM of site 2.

For a thorough inspection of the entire structure, a cross-sectional analysis using precise FIB cut to reveal the entire 100 µm depth of the blind via structure was performed. As shown in Figure 4.14, SEM micrograph of the cross-sectioned structure after TC -65/150 °C, 1000 cycles showed crack lines at the bottom of the blind via structure propagating into the dielectric layer. A similar cross-section and SEM was performed on an as received sample for comparison, but without any cracks observed as shown in Figure 4.15. It is suspected that the cracks are formed during reliability stress testing of TC -65/150 °C up to 1000 cycles, as a result of the thermomechanical stress induced from the large CTE mismatch between the Cu via and the surrounding Si.



Elem	Weight %	Atomic %
C K	07.70	22.50
O K	11.70	25.90
SiK	09.90	12.40
TiK	01.80	01.30
CuK	58.10	32.30
GaK	10.80	05.50

Elem	Weight %	Atomic %
C K	09.60	17.50
O K	34.20	46.80
SiK	37.60	29.30
CuK	18.60	06.40

Figure 4.16 (a) Overlay of 3 TEM micrographs showing the overview cross-sectioned blind via structure at a crack site; (b) TEM micrograph indicating EDX spot near a crack site; (c) TEM micrograph indicating EDX spot away from a crack site; (d) Energy spectrum of EDX spot in (b); and (e) Energy spectrum of EDX spot in (c).

A TEM lamella was prepared, and is in perpendicular to the blind via cross-sectioned area as shown in Figure 4.14 for further analysis. Furthermore, the preparation was done at the crack site which is the main area of interest for analysis. As shown in Figure 4.16, TEM-EDX on the sample after TC

-65/150 °C, 1000 cycles, performed on a spot within the dielectric layer in close proximity to the crack site, confirmed the presence of Cu. On the other hand, the TEM-EDX performed on an area within the dielectric layer without any cracks observed Cu trace but was not as significant as compared to the crack sites. The results suggests that crack formation induces a localized diffusion path for Cu diffusion into the dielectric layer. Therefore, before detection is possible by electrical measurement, either a sufficiently large crack site within the structure is present which can be induced by reliability stress test, or an external driving force is applied to drive sufficient Cu ions into the dielectric layer after degradation.

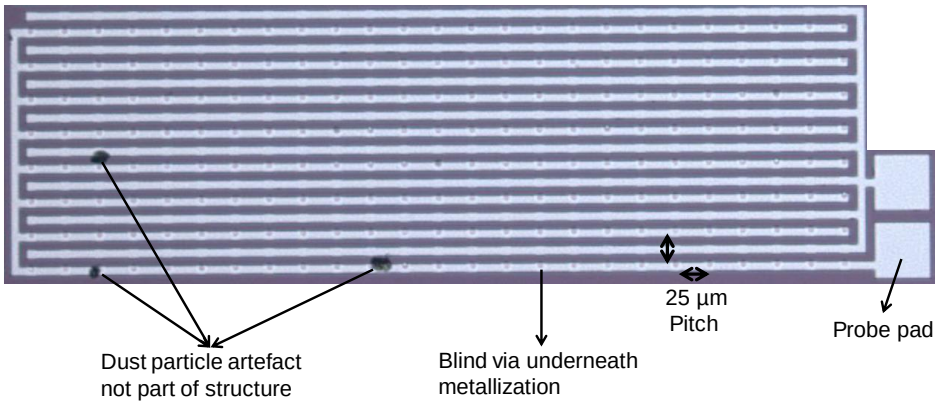


Figure 4.17 Optical image (top view) of test structure 2 with an array of 200 blind vias.

As such, a likely explanation to an unchanged *C-V* characteristics observed before any electrical bias, could be due to an insufficient Cu presence from localized defect sites as compared to a global effect to the entire structure by high temperature stressing at 400 °C as shown in the increase in depletion capacitance in Figure 4.2 previously. Therefore, to increase the statistics of induced defects in a test structure, similar TC stress up to 2000 cycles was applied on an array of 200 similar blind via structures to serve as a comparison to a single blind via structure as shown in Figure 4.17. Each individual blind via will have the same dimensions as shown in Figure 4.1 previously.

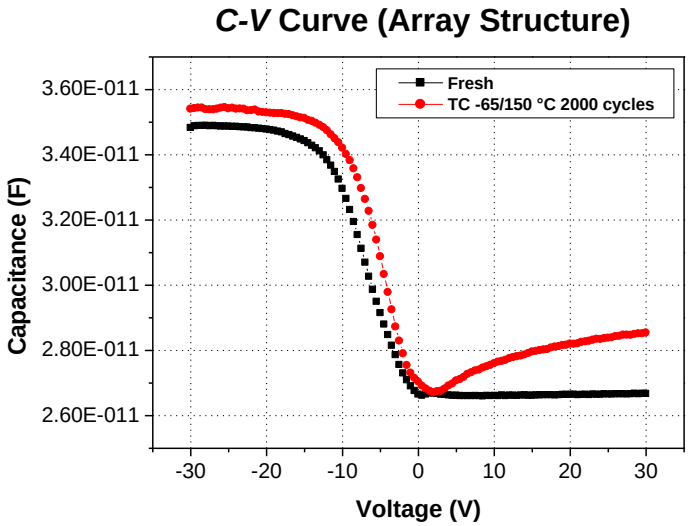


Figure 4.18 *C-V* characteristics of as received and TC -65/150 °C, 2000 cycles post stressed array structure.

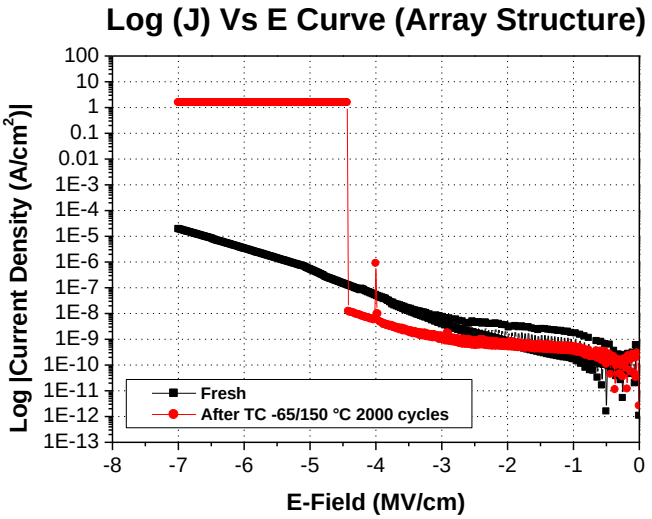


Figure 4.19 Log (J) Vs E characteristics of as received and TC -65/150 °C, 2000 cycles post stressed array structure.

As shown in Figure 4.18, an increase in the inversion capacitance after TC stress was observed on an array structure of 200 similar blind vias before applying any external *E*-field to drive out Cu ions. The result is expected not only due to a statistical increase in the number of blind via structures tested, but also a larger stress that can be possibly induced due to the interaction between blind vias in the array structure. Chakrabarty et al. suggest that the stress interaction between TSV structures is dependent on the designed layout of the TSV structures. TSV positioned in a regular

configuration can result in less stress free zones as compared to TSV positioned in a zig zag configuration [10]. Ryu et al. suggest that stress interaction between TSV structures is dependent on the ratio of the pitch to diameter of the TSV in the array structure. The size of the keep out zone (KOZ) according to Ryu et al. which is an area that should be free of TSV structures based on a criterion of 5% change in the carrier mobility, is reported to increase when the ratio is lesser than 5 [11]. The blind via array test structure fabricated for the purpose of this study has both a regular layout and a pitch to diameter ratio of less than 5 as shown in Figure 4.17. Therefore, stress interaction may be significant and could have possibly resulted in larger defects and a higher defect density. This allows the detection of the increased inversion capacitance in the *C-V* measurement without applying an additional external *E*-field. *J-E* curve was also plotted after TC stress where the catastrophic breakdown observed indicates degradation as shown in Figure 4.19.

4.3.3 Comparison between Dielectric Material

The leakage of two different dielectric material, a black diamond low-k and PETEOS dielectric are investigated post reliability stress test using a more robust Ta barrier layer as compared to a Ti barrier diffusion layer as shown in Figure 4.20.

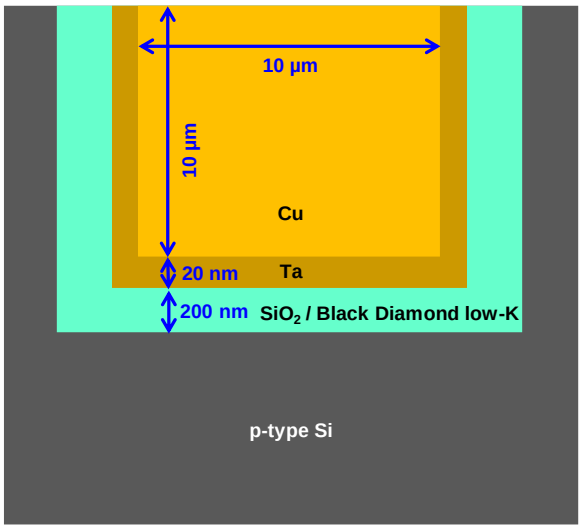


Figure 4.20 Schematic diagram of test structure 4 with Ta diffusion barrier.

Comparing the results from the electrical measurements between the two different dielectric layer materials, blind via structures with low-k liner was revealed to have higher leakage current as compared to blind via structures with PETEOS oxide liner. This is expected due to the higher porosity of low-k dielectric. Figure 4.21 shows the leakage current between the two different dielectric layers after 1000 hours of HTSL at 175 °C, and 2000 cycles of TC at -55/150 °C condition. It is observed that even after harsh accelerated stress testing, no catastrophic failure was observed, such as a dielectric breakdown. The compliance current of the source meter is set at 10 mA.

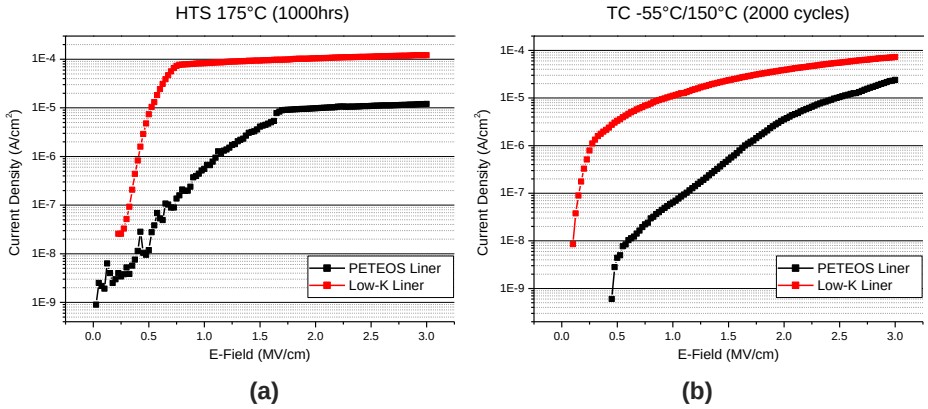


Figure 4.21 Leakage current between PETEOS and low-k liner after (a) 1000 hours of HTSL 175 °C; and (b) 2000 cycles of TC at -55/150 °C.

4.3.4 Comparison between Structure with and without Si_3N_4 Capped Layer

In order to simulate the stress observed in an actual structure during stacking, the blind via test structure as shown in Figure 4.20 was capped with an additional Si_3N_4 layer of 300 nm deposited by the thermal chemical vapor deposition process for comparison as shown in Figure 4.22.

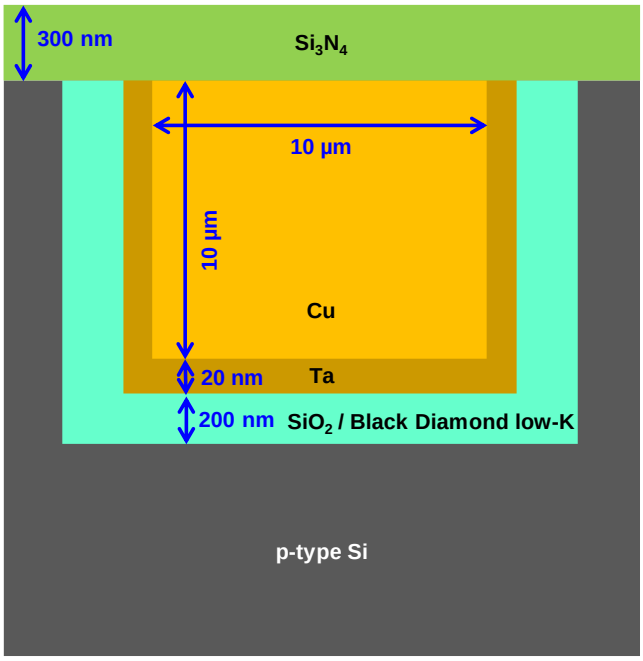


Figure 4.22 Schematic diagram of test structure 5 with Si_3N_4 layer capping.

In this experiment, measurement results showed differences in the leakage current between blind via structures with and without Si_3N_4 after subjecting to an accelerated stress test. Abrupt breakdown can be observed for blind via structures with Si_3N_4 and it happens for PETEOS liner blind via structures at HTS 175 °C and HTS 225 °C after 500 hours. On the other hand, low-k liner blind via structures have abrupt breakdown at HTS 225 °C after 500 hours and TC -55/150 °C after 1000 cycles. An example of breakdown is shown in Figure 4.23 for PETEOS liner blind via after 500 hours of HTS at 225 °C. The breakdown is also shown to be permanent and irrecoverable after three measurements on the same structure as shown in Figure 4.24. While both PETEOS liner blind via and low-k liner blind via have electrical break down at high temperature, low-k liner blind via also have breakdown observed under TC test. This could be due to the weaker thermomechanical properties of low-k dielectrics which tend to be more brittle and likely to crack under thermomechanical stress. No abrupt breakdown was observed for test structures 4 without Si_3N_4 cap layer. It is highly likely that after HTSL stress test, Cu protrusion occurs due to the large CTE mismatch between the Cu via and Si layer of 17.6 ppm/°C and 2.6 ppm/°C respectively [12]. Under normal circumstances, the expansion

of the Cu via is in the vertical upward direction, constrained by the surrounding Si substrate. However, as the blind via are suppressed under a hard Si_3N_4 layer, the stress is unable to be relieved upwards and will have to be relieved by other means, such as through the softer sidewall material of the blind via. The result is a weakened dielectric layer and an electrical breakdown.

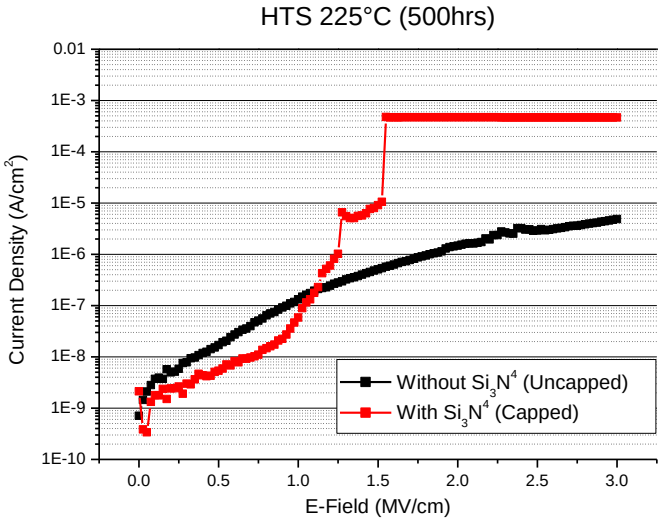


Figure 4.23 Breakdown observed for Si_3N_4 capped structures for PETEOS liner blind via after 500 hours of HTSL 225 °C.

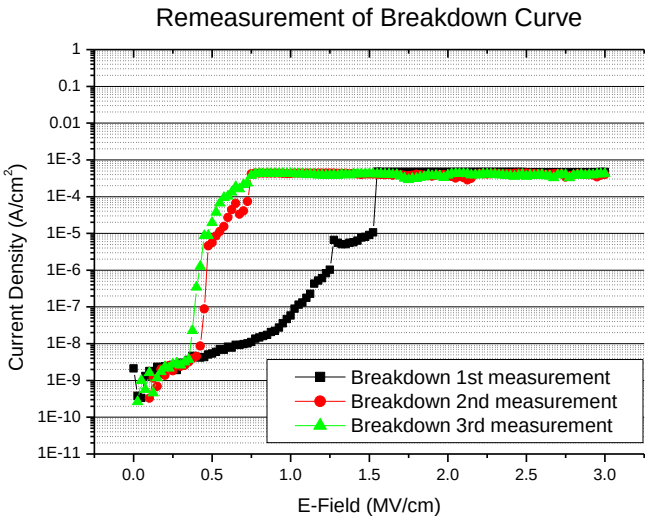


Figure 4.24 Breakdown irrecoverable after three measurements for PETEOS liner blind via after 500 hours of HTSL 225 °C.

4.3.5 Comparison between Stress Condition

While there is an abrupt breakdown observed for PETEOS dielectric structures with Si_3N_4 capped layer, it is observed that structures without Si_3N_4 layer as shown in Figure 4.20, have a leakage current decreasing with stress readout at different duration under HTSL 175 °C and 225 °C up to 1000 hours. On the other hand, for low-k dielectric structures, leakage current increases with stress duration under HTSL 175 °C but decreases with stress duration under HTSL 225 °C. The duration of TC stress did not affect the leakage current for both type of dielectric layer structures, and remain comparable up to 2000 cycles. Figure 4.25 shows the leakage current at different readouts for PETEOS liner blind via at HTSL 225 °C, low-k liner blind via at HTSL 175 °C and PETEOS liner blind via at TC -55/150 °C stress condition.

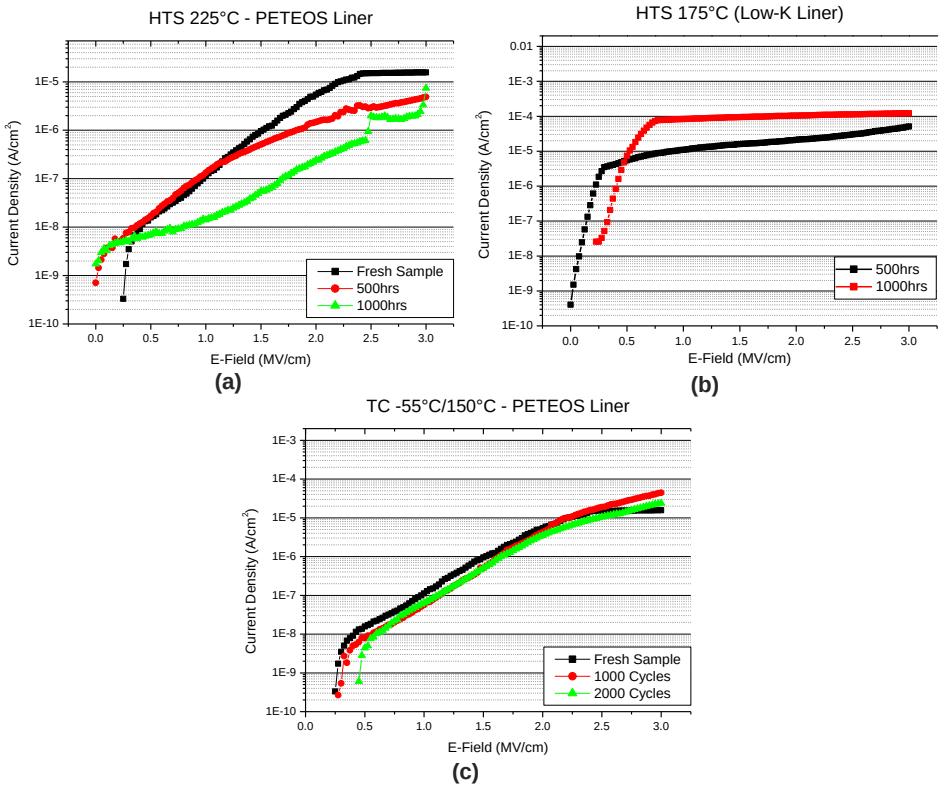


Figure 4.25 Leakage current different readouts for (a) PETEOS liner blind via at HTSL 225 °C; (b) low-k liner blind via at HTSL 175 °C; and (c) PETEOS liner blind via at TC -55/150 °C.

The decreasing trend observed after HTSL could be explained by the excessive Cu protrusion after stress test as shown in SEM micrograph in Figure 4.26a. Excessive Cu protrusion after HTSL test can lead to delamination between the Cu and barrier liner interface and voids within the Cu via, resulting in a poorer electrical connectivity. On the other hand, the protrusion for low-k liner blind via structure was less severe as compared to the PETEOS liner blind via structure as shown in Figure 4.26b. Therefore, the increase in current with stress duration could be due to a prolonged thermal aging on the test structure. Thermally induced stress due to the high thermal mismatch between Cu and Si could result in the formation of voids and cracks and an electrical leakage path within the dielectric layer. There is almost no Cu protrusion observed after TC test as observed in Figure 4.26c. All images are captured with similar magnification and tilt angle, for consistency in comparison.

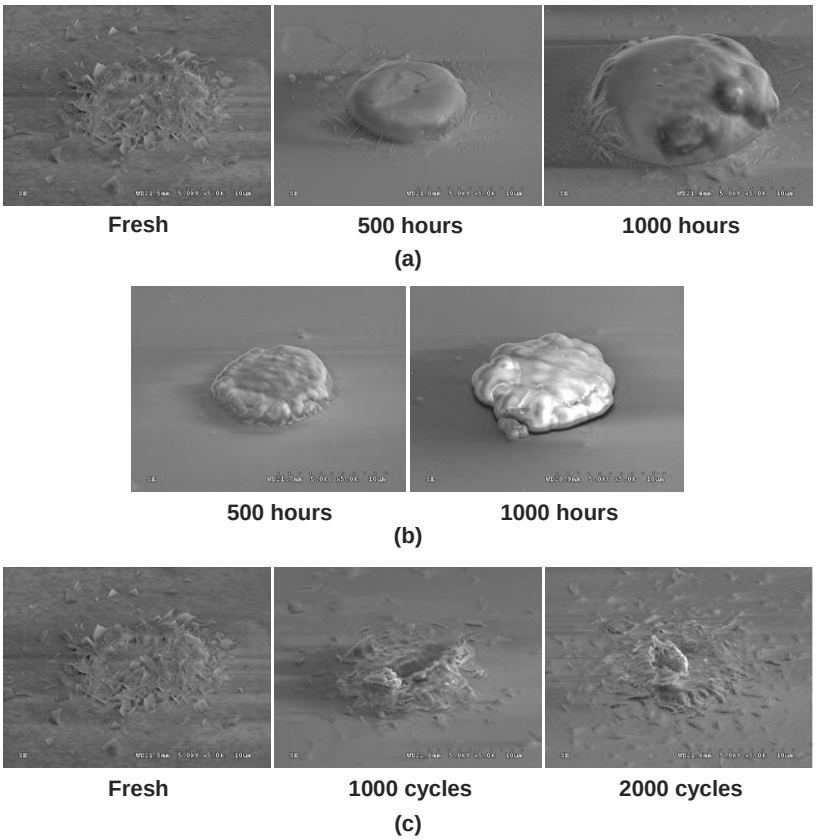


Figure 4.26 SEM micrograph of Cu blind vias for (a) PETEOS liner blind via after HTSL 225 °C; (b) low-k liner blind via after HTSL 175 °C; and (c) PETEOS liner blind via after TC -55/150 °C.

A FIB cross-sectioned SEM micrograph was taken on a PETEOS liner blind via structure after 1000 hours of HTSL 225 °C as shown in Figure 4.27 for further analysis. SEM micrograph revealed that there was severe protrusion measured to be as much as 4.7 um above the wafer surface. As a result of the Cu protrusion, the plastic deformation leads to dimensional changes and induces voids within the Cu via after 1000 hours of HTSL 225 °C stress test. Furthermore, shear stress on the sidewall interface resulted in the delamination between the Cu and PETEOS liner as shown in Figure 4.28. TEM micrographs taken also showed voids within the PETEOS dielectric layer after the stress test as shown in Figure 4.29. Voids and delamination in the Cu blind via results in higher electrical resistance and in the worst case, may result in an electrical open connection. These observations explains the decreasing trend in leakage current.

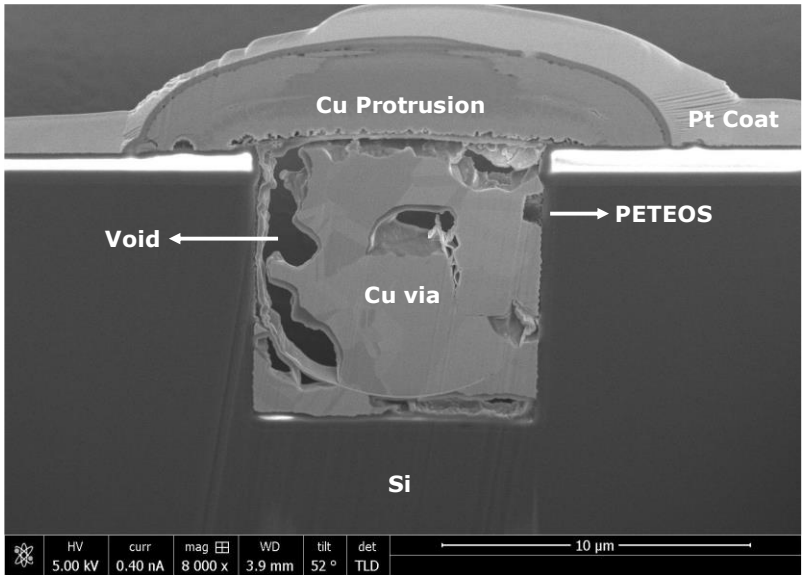


Figure 4.27 Cross-sectioned SEM micrograph of a PETEOS liner blind via after 1000 hours of HTSL 225 °C stress.

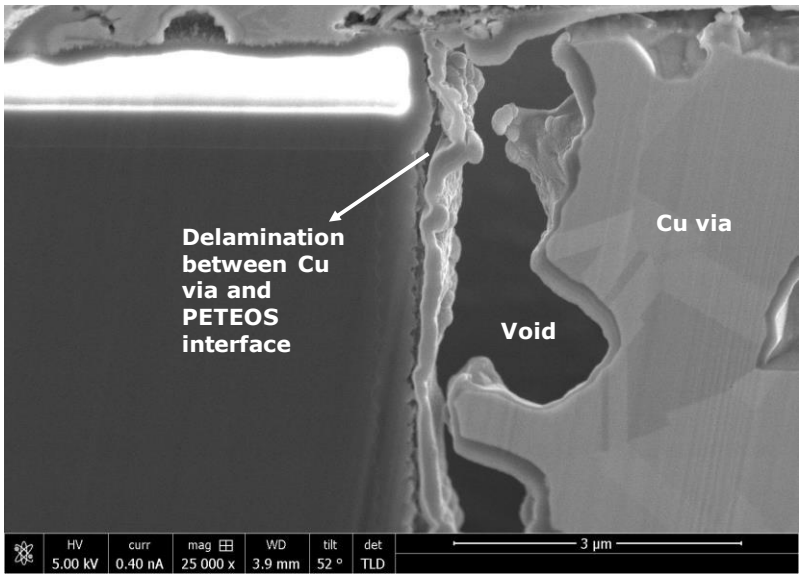


Figure 4.28 Cross-sectioned SEM micrograph showing delamination between Cu and PETEOS liner interface after 1000 hours of HTSL 225 °C stress.

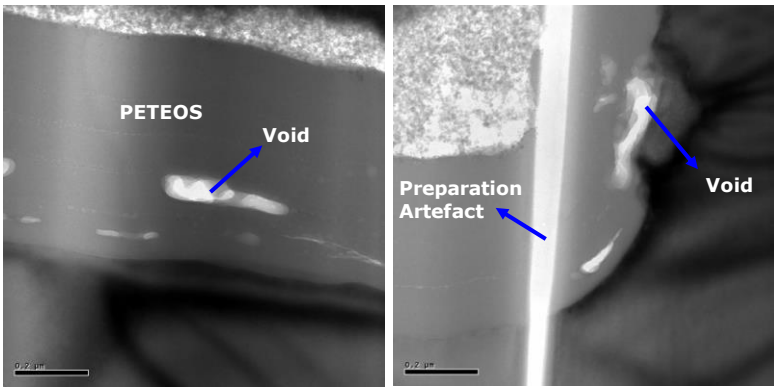


Figure 4.29 TEM micrographs showing voids within the PETEOS dielectric layer at (a) bottom of blind via; and (b) bottom right corner of blind via.

4.3.6 Current Conduction Mechanism

The quality of the dielectric can be characterized and its conduction mechanism determined by fitting measured leakage current to the respective conduction mechanism shown in Table 2.3. In order to better understand the reliability of the blind via structure, knowledge of the

conduction process and its mechanism that leads to the leakage current is important. The structure using Ti barrier that has been stressed at 400 °C will be used to determine its conduction mechanism to understand the influence Cu ions have, on the leakage conduction mechanism. It is worthy to note that in the beginning, for as received samples, the leakage data obtained were unable to reasonably fit to any of the conduction mechanisms across the entire electric field range, suggesting that there is a possibility that several mechanisms is present and could be overlapping simultaneously. In other words, a single conduction mechanism does not adequately describe the leakage current conduction mechanism in the as received state of the blind via structure across the measured *E*-field.

On the other hand, after the structure is stressed at 400 °C where the Ti barrier layer is degraded and Cu expected to migrate into the dielectric layer, there was a clear fitting to the PF conduction mechanism which is known to be a dielectric bulk limited mechanism. Base on the PF equation described in Table 2.3, PF conduction can be determined by fitting a straight line on a ln (J/E) vs $\sqrt{E}$ plot. Looking at the gradient of the fitted straight line, the optical dielectric constant can be extracted and verified experimentally using an optical ellipsometer. The B-spline model was used to fit the measured data by the optical ellipsometer to obtain the refractive index of the dielectric layer. The optical dielectric constant of the dielectric layer can then be approximated to be the square of the refractive index.

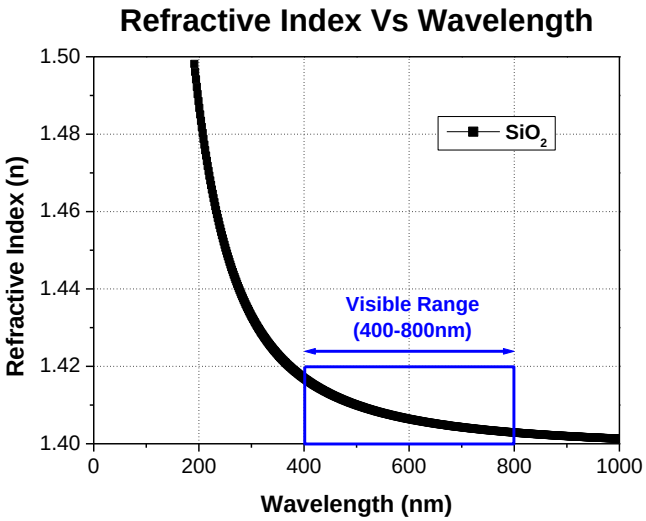


Figure 4.30 Refractive index of fabricated dielectric layer measured from an optical ellipsometer.

Figure 4.30 shows the result of the measured refractive index of the dielectric layer of the fabricated structure, to be approximately between 1.4 and 1.42 within the visible range. Therefore, the dielectric constant can be calculated to be approximately between 1.96 and 2.01 where the values will be used to determine and validate the PF conduction mechanism. The optical dielectric constant was used instead of the static dielectric constant as it is in general, during the electron emission process, electron transit time from trap sites is much shorter as compared to the dielectric relaxation time which results in the dielectric not being able to be polarized [13, 14].

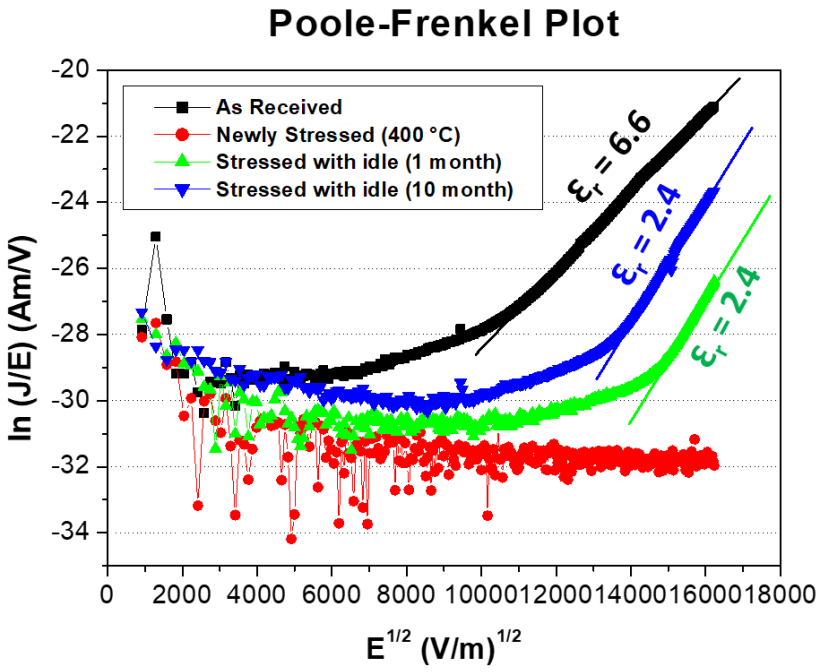


Figure 4.31 Poole-Frenkel plot of samples at various stages.

The ln (J/E) vs $\sqrt{E}$ plots of as received and stressed samples at 400 °C over various time frame were plotted as shown in Figure 4.31. It is observed that not all the plots are able to fit into a straight line and the gradients are observed to be different for newly stressed and as received samples. When the dielectric constants are extracted from the gradient of the plots, only high temperature stressed sample which are left to idle had its dielectric constant match to the measured values between 1.96 and 2.01. This suggests that conduction mechanism changes over time and the dominant conduction mechanism is the PF conduction but only for the high temperature stressed samples that has been left to idle for a period of time. The observation on the change in conduction mechanism towards a PF dominant one will be discussed again in the next chapter where it is observed to be likely related to the change in the oxidation state of Cu ions within the dielectric layer.

4.4 Summary

In this chapter, the test structures and experimental setup for the reliability study of Cu blind vias is described. Harsh automotive stress test conditions up to grade 0 of HTSL 175 °C up to 1000 hours and TC -55/150 °C up to 2000 cycles were used to evaluate its reliability. PETEOS and black diamond low-K dielectric samples were fabricated for the study and did not find any catastrophic failure. On the other hand, severe protrusion was observed post HTSL 225 °C at 500 hours and 1000 hours leading to voiding and delamination resulting in a decreased current performance. However, an increased leakage current and catastrophic dielectric breakdown was observed on a Si_3N_4 suppressed blind via structure likely due to lateral stress. Therefore, an optimized annealing procedure to control excessive protrusion is beneficial to the reliability of TSV structures. A change in the inversion capacitance is observed when Cu is present in the dielectric layer. This is demonstrated on a degraded Ti barrier structure after stressing at 400 °C. An additional electrical bias however, was necessary to be applied to the blind via structure after post reliability stress test in order for the increase in inversion capacitance to be observed. This indicates that even though there are no significant drift in the electrical characteristics, the test structure was already degraded. PFA performed on a blind via structure post TC -65/150 °C at 1000 cycles found cracks in the blind via structure with Cu traces around the crack region. On the other hand, an electrical bias was not necessary for an array of 200 similar blind vias uniformly spaced after similar reliability stress test. This suggests that the concentration of Cu ions migrated might be more significant as compared to a single blind via structure for the change in inversion capacitance to be detected. In addition, it can also be due to the stress interaction between blind vias in the array structure which could induce a larger stress. Various leakage current conduction mechanism were fitted to the blind via structures with and without Cu migration in the dielectric layer. It was found that a single conduction mechanism does not adequately describe blind via structures that are without Cu presence, suggesting that there is a possibility that several mechanisms are present and overlapping simultaneously. On the other hand, blind via structure with Cu ions present in the dielectric layer was found to fit well to a PF conduction mechanism validated with an experimentally measured dielectric constant with the optical

ellipsometer. It is however, dependent on the oxidation state of Cu ions over time which will be discussed in the next chapter. The understanding of the electrical characteristics to detect the presence of Cu in the dielectric layer due to a degraded barrier is useful in the reliability assessment of Cu TSV structures. This makes it suitable for TSV degradation studies in the future. Furthermore, with the ability to detect Cu presence in dielectric layers, the monitoring of its Cu transport and its role on TDDB lifetime can be studied.

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Chapter 5
Effects of Cu Migration on TDDB

5.1 Control and Monitoring of Cu Drifts

Test structure 1 with known degradation to the barrier layer after high temperature stressing at 400 °C, where Cu migrates into the dielectric layer as shown in the TEM-EDX area map and line scan in Figure 4.6 and Figure 4.7 will be used for this study. It is understood that an applied *E*-field can cause Cu ions in the dielectric to drift, and the direction can be well controlled depending on the direction of the applied *E*-field. As such, Cu ions can either drift towards the SiO_2 dielectric layer or Cu via. Therefore, TDDB with the control of Cu ions drift can be investigated [1-3]. In this study, positive and negative bias are applied to the Cu via, grounded at the Si substrate at room temperature, for controlling the drift of Cu ions in the dielectric layer. Positive bias to drive Cu ions into the dielectric layer and negative bias to drive Cu back towards the Cu via will be referred to as a positive drift and negative drift, respectively, from hereon.

As it was previously discussed, when the barrier layer degrades allowing Cu to migrate into the dielectric layer, the presence of Cu ions in the dielectric layer can be observed with the *C*-*V* characteristic curve as shown in Figure 4.2 previously. The presence of positive Cu ions creates an enhanced local *E*-field within the dielectric layer. As a result, more minority carriers are generated in the Si substrate, where the increase in the inversion capacitance from the *C*-*V* characteristics is reflected. Using the same method, the diffusion and drift of Cu ions within the dielectric layer can also be monitored and controlled at room temperature. This can be demonstrated from the corresponding increase and decrease of the inversion capacitance of the *C*-*V* curve, which can be controlled by applying an appropriate *E*-field, allowing dedicated analysis to be carried out with respect to Cu migration and presence within the dielectric layer.

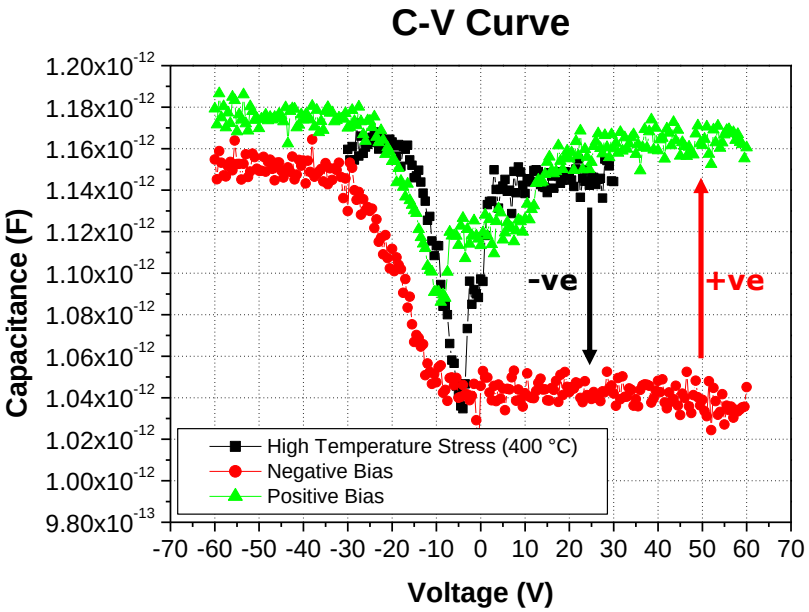

Figure 5.1 *C-V* characteristics after high temperature stressing at 400 °C , negative bias and positive bias sequentially.

When a negative drift equivalent to an *E*-Field of 7 MV/cm was applied for 15 min after high temperature stressing, the inversion capacitance decreases as shown in Figure 5.1. As a result of the applied negative bias, existing Cu ions in the dielectric drift and accumulate back towards the core of the Cu via. Since the negative drift depletes the presence of Cu ions within the dielectric layer, the enhanced *E*-field diminishes. Consequently, the inversion capacitance decreases and reverts back to a typical high frequency *C-V* curve which will be reflected for an as received structure without degradation. On the other hand, when a positive drift of similar *E*-field was applied, to drive the Cu ions out into the dielectric layer, the inversion capacitance increased again. This observation is repeatable and not influenced by the sequence of the applied *E*-field. Therefore, even when beginning with a positive followed by a negative drift, similar characteristics can be observed. This suggest that it is possible to calibrate the ions towards the Cu via at any point in the experiment, with the assumption that there will be no degradation to other parts of the test structure. This will be referred to as the "restored state" from hereon. A lower *E*-field with shorter biasing duration was also experimented for evaluation. It was found that at room temperature, an *E*-field of at least 3 MV/cm is required for Cu ions to drift with a biasing duration of

5 min. As 5 min was a reasonable test time, a shorter stress duration was not experimented. It might be possible that a shorter duration will be sufficient to drive Cu ions transport. In addition, there is also a possibility that an *E*-field lower than 3 MV/cm is sufficient to drive Cu ions transport, if a longer biasing time is applied.

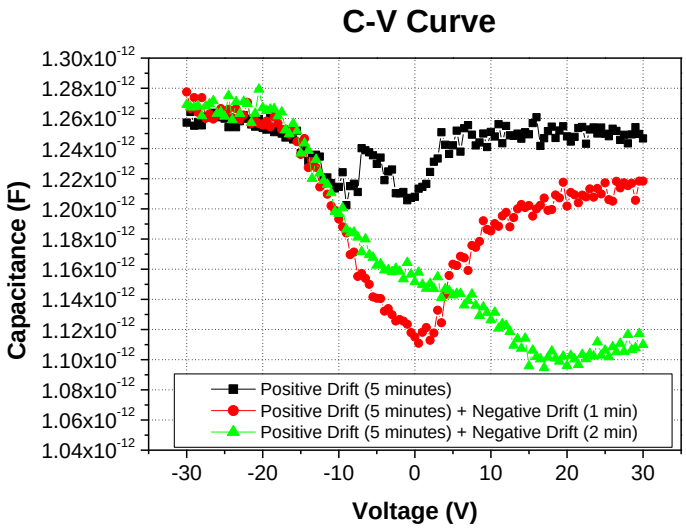

Figure 5.2 *C-V* characteristics of a high temperature stressed sample with different biasing sequence and duration.

Attempts were made to observe the *C-V* characteristics progressively before the full biasing duration of 5 min is reached. This was done by first applying a positive drift of 5 MV/cm to the Cu via for 5 min. At this moment, Cu ions are already driven out into the dielectric layer and would indicate an increased inversion capacitance as demonstrated previously. A subsequent negative drift of similar *E*-field but of shorter duration is then applied and measured again to observe for any changes. Figure 5.2 showed that the inversion capacitance gradually decreases reflected at different levels, as the duration of the negative drift increases. This suggests that it is possible to monitor and control qualitatively, the amount of Cu ions present in the dielectric layer by adjusting the biasing duration accordingly.

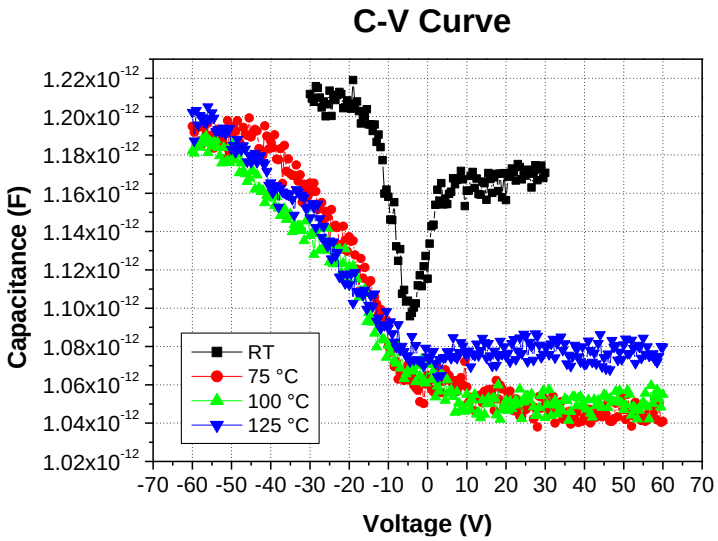

Figure 5.3 *C-V* characteristics of high temperature stressed samples measured at various elevated temperature after negative *I-V* sweep.

Experiments were also performed at elevated temperature up to 125 °C to evaluate Cu transport in the SiO_2 dielectric layer by the diffusion process. As shown in Figure 5.3, it is observed that the inversion region of the *C-V* curve decreased at 75 °C, 100 °C, and 125 °C. However, this is unlikely the result of back diffusion of Cu ions towards the Cu via since it has higher Cu concentration as compared to the dielectric layer. The decrease in the inversion capacitance observed in this case, is the consequence of a negative *I-V* sweep performed at the elevated temperature similar to the temperature used to obtain the C-V curve in Figure 5.3. A negative *I-V* sweep is done so as to exclude the effect of the depletion width in the p-type Si substrate, up to an *E*-field of 7 MV/cm, prior to the *C-V* measurement. The result therefore, suggest that biasing at elevated temperatures can accelerate the drift of Cu ions at short durations. Furthermore, the depletion portion of the curve was observed to stretch out in the *C-V* curve, indicating trapped charges between the SiO_2 and Si interface after the negative *I-V* sweep. Similar characteristics were not observed when electrical bias was applied at room temperature as shown in Figure 5.1 previously.

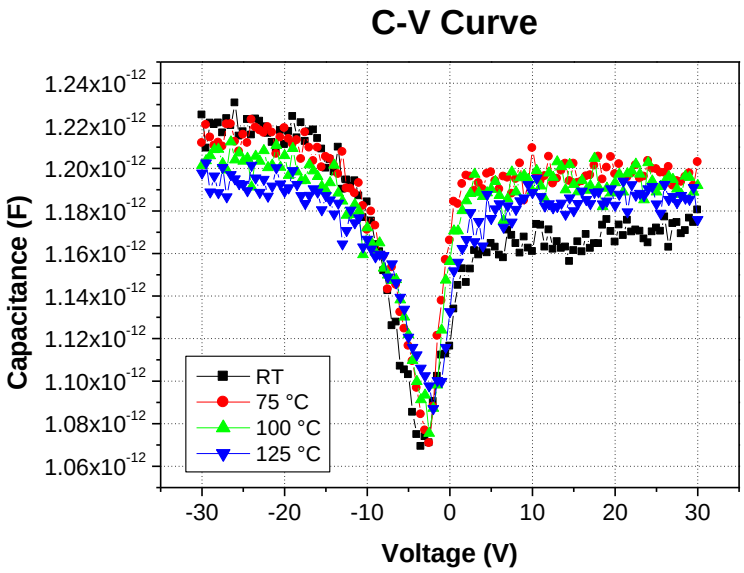

Figure 5.4 *C-V* characteristics of high temperature stressed samples measured at various elevated temperature without negative *I-V* sweep.

A separate experiment on a similar structure and subjected to similar elevated temperature *C-V* measurements without any prior *I-V* curve sweep, did not result in a decrease in the inversion capacitance as shown in Figure 5.4. It is observed that the *C-V* curve remains relatively unchanged when measured at an elevated temperature, suggesting that back diffusion of Cu ions is insignificant. This is important in the subsequent sections where the influence of Cu diffusion is desired to be kept to a minimum in order for accurate analysis. The ability to monitor and control the diffusion and drift of Cu ions within the dielectric layer as demonstrated in the experiment will be useful for subsequent TDDB investigations. As a result, the potential effect on the presence of Cu ions within the dielectric layer on TDDB can be studied and will be discussed in the next section.

5.2 Influence of Copper on TDDB Lifetime

Diffusion barriers can be indirectly assessed by measuring the TDDB lifetime of the test structure. However, the role and impact Cu ions have on TDDB lifetime is still not fully understood. Moreover, the influence of the presence of Cu ions in the dielectric is made more complex, taking into considering the dynamic drift of Cu ions under high electric field. The review on the uncertainties and current status of TDDB model to be used is written in section 2.2.5.6.

Based on the electrical characteristics and FA observation on the presence of Cu ions detected in the dielectric as discussed in the previous section, TDDB lifetime experiments can be performed to understand the influence of Cu on TDDB lifetime estimation. TDDB lifetime experiment is performed with various *E*-field and temperature to understand its influence on the breakdown mechanism. In this study, a catastrophic breakdown is defined as a sharp and abrupt increase in leakage current by a magnitude of at least 3 orders or a measured leakage current of above 1 mA. Structures tested are either pre-biased or without any pre-bias. Pre-biased samples were subjected to a positive and negative Cu drift, to drive Cu ions towards the dielectric and towards the Cu via respectively. The *E*-field applied during pre-bias to drive Cu ions was performed at 5 MV/cm for 5 min in room temperature. TDDB is performed at various *E*-field up to 7 MV/cm and temperatures up to 175 ºC.

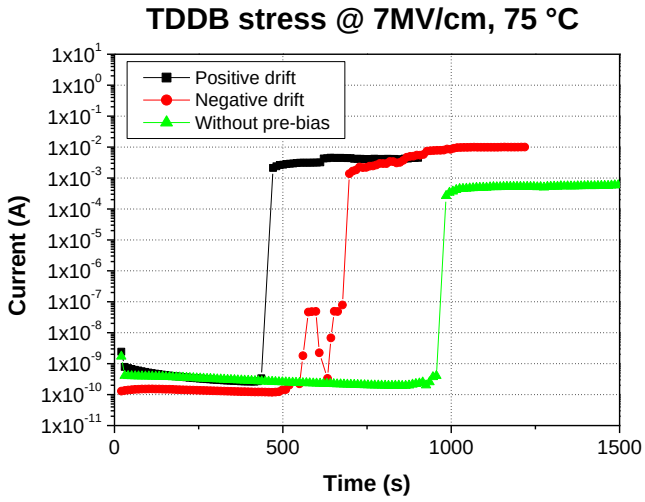

Figure 5.5 TDDB comparison of samples between positive drift, negative drift and without pre-stress at 7 MV/cm, 75 °C.

Figure 5.5 shows the result of a TDDB stress performed at an *E*-field of 7 MV/cm and temperature of 75 ºC on three structures after positive drift, negative drift and without any pre-bias. It is observed that with a positive drift, its TDDB lifetime is shorter at 436 seconds as compared to the TDDB lifetime of 677 seconds with a negative drift applied. This is expected as it has been widely reported that the presence of Cu ions in dielectric will cause early failure as Cu ions accumulates and form clusters within the dielectric layer, which eventually form a conduction path leading to an electrical short [4]. In addition, Cu ions are also reported to have encouraged leakage current flow [5]. The unstressed samples on the other hand, was observed to have the longest TDDB lifetime of 984 seconds. This could be due to the drift of Cu ions causing some degradation to the dielectric layer by ionic movement. As a result, samples with pre-bias where Cu ions are driven within the dielectric layer by an applied *E*-field cannot be directly compared with samples without pre-bias.

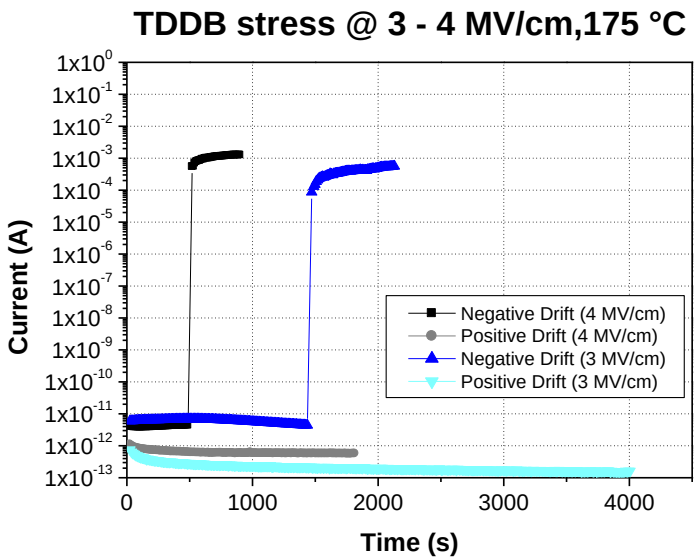

Figure 5.6 TDDB comparison of samples between negative drift and positive drift at 3-4 MV/cm, 175 °C.

TDDB stress was also performed at an *E*-field of 3 and 4 MV/cm and temperature of 175 °C. Figure 5.6 shows that after the TDDB stress, the structure with positive drift do not report any TDDB up to 4005 seconds and 1813 seconds for 3 and 4 MV/cm respectively before the experiment is stopped. On the other hand, structure with negative drift reported a shorter TDDB lifetime of 1488 seconds and 520 secs

for 3 and 4 MV/cm respectively. The results is in contrast to the previous experiment performed at 7 MV/cm and temperature of 75 °C as shown in Figure 5.5. This observation suggests that there might be a different breakdown mechanism that prolongs the TDDB lifetime and could be related to the interaction between electrons and Cu ions. It is reported that the Cu ions serve as an active trap to electrons, which may have reduced leakage current transport. Furthermore, the presence of Cu ions may also serve as scattering centers, which reduces impact generated defects caused by high energy electrons [6].

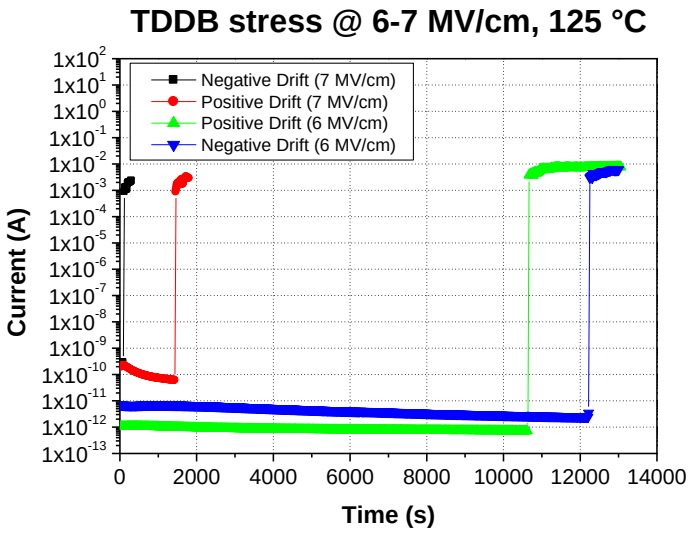

Figure 5.7 TDDB comparison of samples between negative drift and positive drift at 6-7 MV/cm, 125 °C.

TDDB test at *E*-field of 7 MV/cm and temperature of 175 ºC were also experimented but the time to breakdown reported was too short, in the range of 10s of seconds, to differentiate their TDDB performance in the analysis. This suggest that the condition might be too harsh for the experiment. As a result, a lower temperature of 125 ºC was experimented with an *E*-field of 6 and 7 MV/cm. Figure 5.7 shows that at 7 MV/cm, the failure sequence corresponded with the experiment performed at 175 ºC as shown in Figure 5.6, where positive drift results in a longer dielectric lifetime. On the other hand, at lower *E*-field of 6 MV/cm and 125 ºC condition, the failure sequence corresponded with the experiment performed at 75 ºC as shown in Figure 5.5 where positive drift results in a shorter dielectric lifetime.

It is evident that dielectric lifetime is influenced by the presence of Cu ions. However, given that different response were observed from TDDB evaluations performed at different conditions, it is suggested that the breakdown mechanism has a dependence on the applied *E*-field and temperature of the TDDB stress conditions which could have somehow activated the different roles of Cu ions in the dielectric and needs further investigation. This suggests that TDDB is not a simple parametric test where proper understanding of the different mechanisms induced by the presence of Cu in the dielectric layer is necessary for accurate lifetime analysis.

It is worth stating that at an elevated temperature, movement of Cu may take place by the diffusion process, altering the breakdown mechanism. To ensure that insignificant diffusion of Cu ions take place during the TDDB stress duration, a control structure close to the actual test site was utilized as a monitoring reference. The control structure has a prior negative drift applied and is measured again after the TDDB stress test to observe for any increase in the inversion capacitance due to out diffusion of Cu into the dielectric layer. The monitoring is performed for all TDDB experiments discussed in this work, to ensure insignificant variation due to contributions by the diffusion process.

5.2.1 Oxidation state of Cu ions

A positive bias is applied to the Cu via with respect to the Si substrate during TDDB experiment. The oxidation state of the Cu ions formed in the dielectric layer was observed to play a significant role which may alter TDDB lifetime. This was first discovered when an increasing and decreasing slope was observed during TDDB stress, comparing as received samples, newly stressed samples at 400 °C, stressed samples at 400 °C that were left to idle in room temperature for an extended period and pre-biased samples.

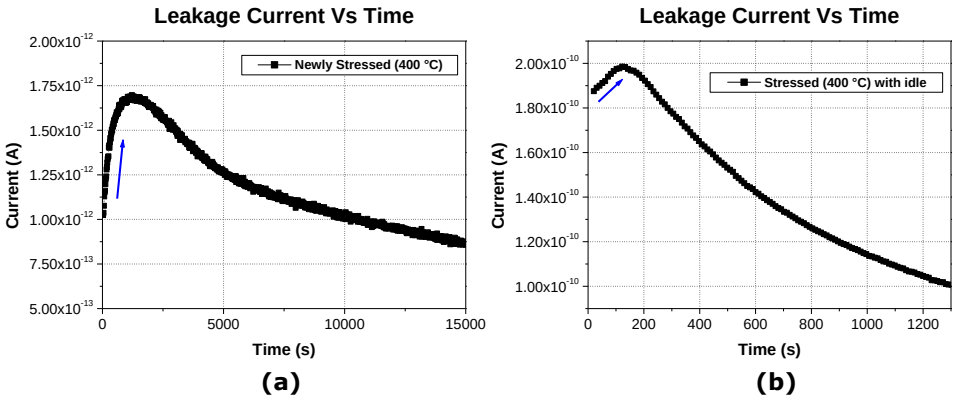

Figure 5.8 Leakage current profile of samples that are (a) newly stressed at 400 °C and (b) stressed at 400 °C with a period of idle.

The increasing slope indicates Cu drifting into the dielectric while the decreasing slope after a period of time indicates electron trapping as Cu is known to form deep traps within the dielectric layer. Figure 5.8a and Figure 5.8b shows the current leakage curve of a newly stressed sample and a stressed sample that have been left to idle during TDDB stress, respectively. As expected, an increasing slope was observed for the newly stressed sample at the initial stage of the TDDB stress. On the other hand, a slight increase over a short period of time was observed for the stressed samples that have been left to idle at room temperature, indicating that over time, Cu have diffused out into the dielectric layer before TDDB stress was performed. As received samples on the other hand, reflected an initial decrease during TDDB stress, as no Cu ions drift is expected to be present.

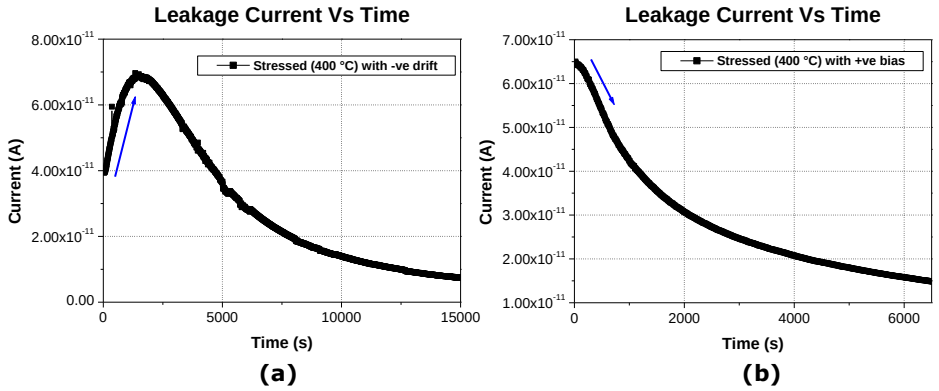

Figure 5.9 Leakage current profile of stressed samples with (a) negative drift and (b) positive drift.

With an appropriate applied *E*-field, the control of Cu ions movement was possible as demonstrated in the previous section. This allows for the study of the influence Cu have on TDDB lifetime performance. When a negative drift is applied prior to the TDDB stress, Cu ions will drift towards the Cu via. Subsequently when the TDDB stress is applied, an initial increase in slope as shown in Figure 5.9a was observed due to a positive drift of Cu ions into the dielectric layer during TDDB stress. On the other hand, as shown in Figure 5.9b, the slope decreased when a positive drift was applied prior to TDDB stress where Cu ions are drifting out into the dielectric layer. As a result, subsequent TDDB stress no longer result in a significant amount of Cu drift into the dielectric layer which would have been reflected by an increasing slope as described previously. Instead, a decreasing slope was observed due to the presence of Cu which is known to form deep traps for electrons causing the current to drop. This suggests that the amount of Cu ions present after high temperature stressing could be limited and more ions was not significantly introduced during TDDB stress test.

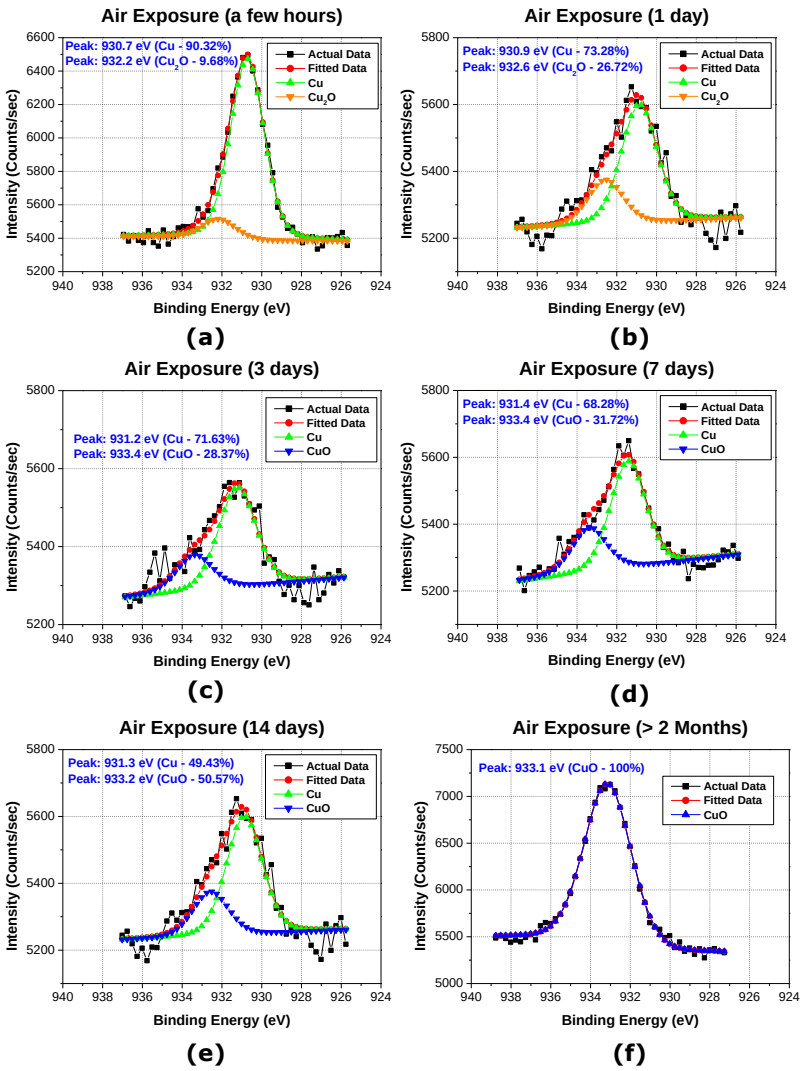

Figure 5.10 De-convoluted peaks showing different Cu oxidation states after exposure to (a) a few hours, (b) 1 day, (c) 3 days, (d) 7 days, (e) 14 days and (f) more than 2 months in air.

Since a difference in electrical characteristics was observed between newly stressed samples and stressed samples with idle time, the oxidation state of the Cu was investigated using XPS analysis. As it is difficult to determine the oxidation state of Cu within the dielectric layer due to limitations on available FA tools, the entire Cu via is etched from the top and exposed in ambient condition for XPS analysis instead. The peaks of Cu sub-oxides can be determined by de-convoluting the acquired scans after exposing the high temperature stressed samples at different timeframe as shown in Figure 5.10. The de-convoluted peaks suggest that the oxidation state of Cu changes over time from Cu_2O to CuO. Hence, while

it is generally known that the presence of Cu ions affects the TDDB lifetime, in depth understanding on the oxidation state of Cu ions is important to determine if it will accelerate or prolong failure.

It is hypothesized that for newly stressed samples at 400 °C, Cu_2O are more likely to form over CuO. This is due to the high influx of Cu migration into the dielectric layer at the beginning, where oxygen is the limiting reagent. On the other hand, for high temperature stressed samples that are left to idle for a period of time, Cu diffuses further into the dielectric layer where oxygen is no longer limited in the reaction to form CuO. With clear understanding on the behavior of the change in Cu oxidation state over time, TDDB lifetime influence by Cu presence in the dielectric layer can be studied. Experiments can be carried out by applying an appropriate *E*-field to known condition of the test structure, in order to understand if it accelerate or prolong failure.

Taking into considering the change in current conduction mechanism, where a high temperature stressed sample if left to idle will reveal a conduction mechanism that is PF dominant as discussed in section 4.3.6 previously. Together with the change in oxidation state of Cu ions over time observed from the XPS analysis in Figure 5.10, the behavior in TDDB performance between high temperature stressed samples with and without a period of idle can be compared and described.

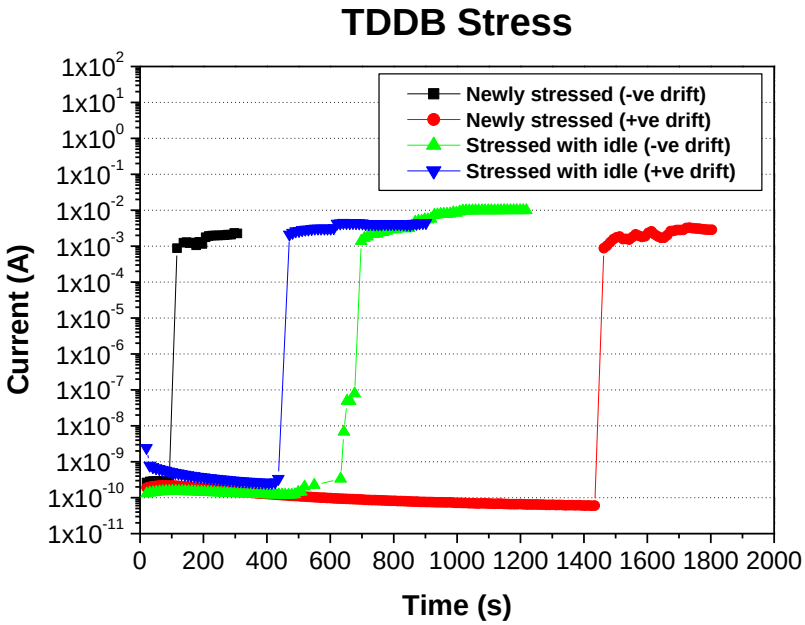

Figure 5.11 TDDB lifetime comparison after negative and positive drift on newly stressed (400 °C) and stressed (400 °C) samples with a period of idle.

As shown in Figure 5.11, a positive drift was observed to have an earlier failure as compared to a negative drift for high temperature stressed samples with a period of idle. On the other hand, it is found that Cu presence will delay the failure for samples that are newly stressed at 400 °C, in contrast to data from most reported works. This is in agreement with findings from previous section where the change in oxidation state from Cu^{+} to Cu^{2+} over time, have altered its current leakage conduction mechanism towards a PF dominant mechanism.

As the Cu ions are in the Cu^{2+} state after a period of idle, it promotes PF conduction when electrons are injected into the dielectric layer. PF conduction increases the flow of the energetic electrons allowed to be injected into the dielectric which may further cause electron scattering and as a result, generate more defects and traps within the dielectric layer leading to TDDB. On the other hand for newly stressed samples at 400 °C, Cu ions are mainly in the Cu^{+} state, which does not promote PF conduction as readily as in the Cu^{2+} state. Therefore, the presence of Cu^{+} ions in the dielectric after positive drift does not accelerate failure. For a newly stressed sample at 400 °C, an earlier occurrence of a TDDB event can be observed after a negative drift where Cu^{+} ions are accumulated at the Cu bulk. This is because, when high temperature and *E*-field is applied during

TDDB after a negative drift, the high thermal and electrical energy may convert Cu ions from Cu^{+} to Cu^{2+} which promotes PF conduction as the ions are driven out. This is unlikely to happen at lower temperature and electrical energy during a negative drift at room temperature. Another possible reason is that the drift of Cu ions within the dielectric layer during TDDB stress have resulted in some degradation. The dielectric may be weakened due to bond breakage generating new defects and traps causing early failures.

5.2.2 Extension of TDDB lifetime

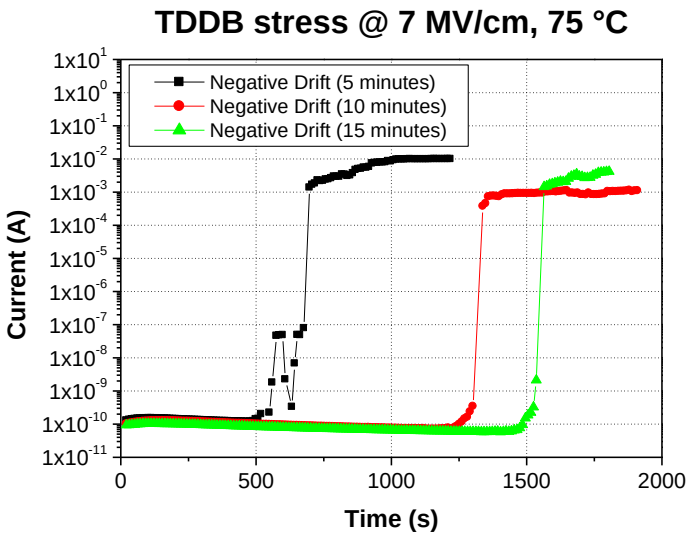

Figure 5.12 TDDB comparison of samples with negative drift of different durations at 7 MV/cm, 75 °C.

Based on the information established on the breakdown mechanism from the TDDB evaluation in section 5.2, the extension of TDDB lifetime can be demonstrated. This can be achieved by taking into consideration the TDDB stress condition that is subjected on the test structure, as well as the applied pre-bias duration and condition for Cu drift. An example is as shown in Figure 5.12, that as we increase the duration of negative drift, TDDB lifetime can be increased under a TDDB stress condition of 7 MV/cm and 75 ºC where its breakdown mechanism is said to be enhanced by the presence of Cu ions as demonstrated in Figure 5.5 previously.

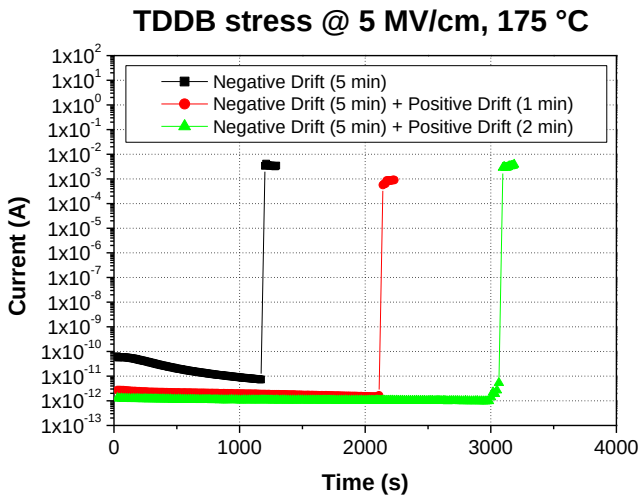

Figure 5.13 TDDB comparison of samples with various drift sequence at 5 MV/cm, 175 °C.

Similarly, the extension of TDDB lifetime can also be observed on a newly stressed sample taking into consideration the oxidation state of the migrated Cu ions. For a newly stressed sample at 400 °C, a positive drift is expected to increase its lifetime where it can be controlled and extended with the application of a positive drift of different durations after calibrating to a restored state using a negative drift as shown in Figure 5.13, where a TDDB stress of 5MV/cm at 175 ºC condition was applied. Likewise, structures can also be first calibrated with a positive drift of similar duration, followed by a negative drift of different duration, resulting in a similar outcome. The interesting attempt to observe the changes to the *C-V* curve during calibration and after biasing of different duration, was observed in Figure 5.2 as shown in section 5.1 previously. It is observed that the inversion capacitance of the *C-V* curve decreases gradually up to different levels as the intended applied negative drift duration increases. These observations suggest that it is possible to monitor and control the presence of Cu ions within the dielectric qualitatively which correlates with TDDB lifetime after the correct failure mechanism is identified.

5.3 TDDB Modelling

A comprehensive TDDB model is still not fully understood although there have been several studies with different prediction models for SiO_2, either with and without the influence of Cu reported in the literature. Therefore, a common agreement amongst researchers are still not achieved, and it is still debatable as to which TDDB model would be the most suitable to be used for an accurate TDDB lifetime prediction.

Actual experimental data from TDDB study using a degraded structure post high temperature stress, was collected from a wide range of *E*-field. The same set of data were fitted to various reported TDDB models such as the E, $\frac{1}{E}$, $\sqrt{E}$ and $\frac{1}{\sqrt{E}}$ model, to determine the most appropriate TDDB model to be used for a PETEOS dielectric layer with the influence of Cu ions migration due to a degraded barrier. In order to achieve accurate modeling, TDDB data were obtained experimentally at lower *E*-field for curve fitting as opposed to extrapolating the results from higher *E*-field.

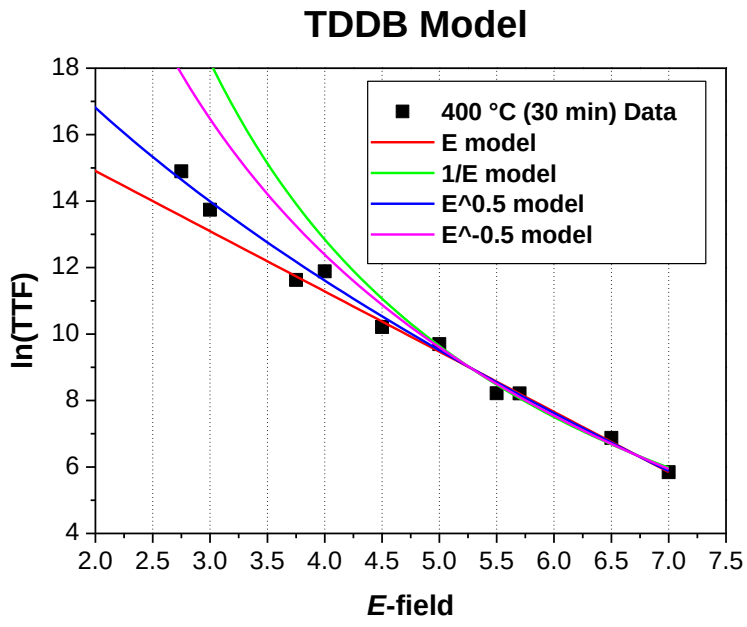

Figure 5.14 TDDB model of a degraded sample after high temperature stress.

Figure 5.14 shows the experimental data of a high temperature stressed structure at 400 °C for 30 min with degraded barriers, fitted to various TDDB models.

Based on the r-square goodness of fit, the best fitting model observed from Figure 5.14 is the $\sqrt{E}$ model, which is a widely used extrinsic TDDB model that takes into consideration on the effect of Cu migration. This is aligned with previous published work by Chen *et al*., who similarly described the $\sqrt{E}$ model as appropriate for a damascene comb structure and a Ta based diffusion barrier [7]. The results from Figure 5.14 compliments the findings from Chen et al., who extrapolated the TDDB data from high *E*-field. Therefore, based on experimental results so far, using the E model will be overly conservative which underestimates TDDB lifetime, while using the $\frac{1}{E}$ and $\frac{1}{\sqrt{E}}$ model will be overly optimistic which overestimating the TDDB lifetime at low *E*-field.

While the $\sqrt{E}$ model provides the best prediction in this work, the other models reported should not be totally eliminated as there could be other underlying variations and mechanisms that may not be well understood and represented in the study. Some variations from other reported works could be in the form of a different material and test structure used which need to be studied thoroughly as there could be potential contributions to the deviation in TDDB model. Other factors include TDDB stress conditions, amount of Cu introduced into the dielectric system, structures that are processed with barrier and without barrier, as well as the oxidation state of Cu which changes over time as discussed in section 5.2.1 previously.

5.4 Summary

In this chapter, the possibility to control and monitor the transport of Cu ions was demonstrated. When an appropriate direction of *E*-field is applied to either drive Cu ions towards the dielectric layer or Cu blind via, the inversion capacitance can be observed to increase and decrease accordingly. This observation facilitated the study of the influence of Cu ions on TDDB lifetime and is revealed to be dependent on the applied *E*-field, temperature and also the oxidation state of the Cu ions. With understanding of the failure mechanism, TDDB lifetime can be extended accordingly. It is observed that the oxidation state of Cu to switch from Cu_2O to CuO over a period of time as verified by the XPS. The change in the oxidation state over time correlates well with a PF dominant conduction mechanism which also explains how it impacts the TDDB lifetime negatively through a higher probability of defect and traps formation. Therefore, this suggests that TDDB is not a simple parametric test where proper understanding of the different mechanisms induced by the presence of Cu in the dielectric layer is necessary for accurate lifetime analysis. As a result, it could be the reason for various TDDB models proposed by different researchers to date. TDDB lifetime models were fitted experimentally on a degraded structure with Cu presence in the dielectric layer and is found to be in good agreement to the $\sqrt{E}$ model. The $\sqrt{E}$ model was verified experimentally by measuring the time to failure at low *E*-field, rather than extrapolating data from high *E*-field.

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Chapter 6
Conclusion and Future Work

6.1 Conclusion

The reliability study of two interconnect technology namely Cu wire bonding and Cu TSV have been discussed. The reliability of Cu wire bond was evaluated using a non-destructive electrical method and was proven to be fast and accurate under TC stress. The series resistance extracted from the diode method found significant change in resistance, by more than 300% increase, between 600 to 700 cycles at TC -65/175 °C condition. Bernards's median rank method was used to prove that the extracted ΔR are normally distributed and is used to identify outliers with a confidence level of 99.73%, equivalent to most industrial practice of a three-sigma process variation. A correlation study between the extracted resistance and wire pull strength found that the wire looping profile as well as the break mode of the destructive wire pull test needs to be taken into consideration for reasonable analysis. The analysis demonstrated that there is a good correlation between the two methods and it is demonstrated that the series extraction method can be more sensitive as compared to conventional pull test. Results shows that even though a large ΔR was measured, it does not translate to a large difference in wire pull strength. In addition, wire pull test with failure mode breaking in the wire span is approximately 3 times less sensitive as compared to wires breaking at the neck region. SEM images which are taken to assess the condition of the wire before destructive wire pull test is performed, also correlates well with the results of the measured ΔR. Ball shear test which is also a destructive conventional wire assessment method, found that there were Cu remnant on the bond pad after ball shear test, suggesting a strong wire ball to pad interface and does not contribute significantly to the measured ΔR. Therefore, the series extraction method is proven to be accurate, which makes it suitable for future wire bond degradation studies focusing on a failure mechanism based approach.

Another interconnect technology in Cu TSV is studied for its reliability assessment with various test structures and material fabricated to emulate actual application scenarios to study its structural integrity. A PETEOS and black

diamond low-k dielectric layer were studied and compared after post reliability stress test with low-k dielectric layer having a higher leakage, expected due to its higher porosity. The difference is approximately 1 order of magnitude after HTSL 175 °C for 1000 hours and TC -55/150 °C for 2000 cycles, under an electric field of 1.5 MV/cm. Comparing structures with and without a layer of Si_3N_4 suppressing the blind via structure to emulate stacked chips, catastrophic breakdown failure can be observed post HTSL 225 °C at 500 hours for structure with Si_3N_4 layer. On the other hand, no breakdown was observed for blind via structures without Si_3N_4 layer. Instead, a decreased leakage current between 500 hours and 1000 hours was observed. Failure analysis performed post HTSL 225 °C at 1000 hours found severe Cu protrusion as much as 4.7 um above the wafer surface, leading to voiding and delamination. Therefore, an optimized annealing procedure to control excessive protrusion is beneficial to the reliability of TSV structures.

The impact of Cu migration in a blind via structure and its impact on its reliability and electrical characteristics were studied. A Ti barrier was deliberately used for this study as it is known that Ti reacts with Cu and SiO_2 at an elevated temperature of 400 °C, weakening the barrier layer causing Cu to migrate. It was found that the inversion capacitance increases when there is presence of Cu in the dielectric layer, validated with PFA results. On the other hand, post reliability stress test alone at HTSL 175 °C up to 1000 hours and TC -65/150 °C up to 2000 cycles did not seem to have any impact to the electrical characteristics initially. When an additional electrical bias was applied to drive Cu ions into the dielectric layer, the increase in the minimum deletion capacitance was observed suggesting that degradation to the blind via structure has already taken place during the stress test causing Cu ions to migrate into the dielectric layer. Expectedly, PFA performed on a test structure post TC -65/150 °C at 1000 cycles found cracks in the blind via structure with Cu traces around the crack region. On the other hand, an electrical bias was not necessary for an array of 200 similar blind vias uniformly spaced after similar reliability stress test. This suggests that the concentration of Cu ions migrated might be more significant as compared to a single blind via structure for the change in inversion capacitance to be detected. In addition, it can also be due to the stress interaction between blind vias in the array structure which could have

induced a larger stress.

The electrical characteristics observed on the increase in the inversion capacitance from Cu presence in the dielectric together where an additional electrical bias was required for single structure post stress test, suggest that it was possible to monitor and control the transport of Cu ions using an appropriate *E*-field. When an appropriate direction of *E*-field is applied to either drive Cu ions towards the dielectric layer or Cu blind via, the inversion capacitance can be observed to increase and decrease accordingly. The ability to control and monitor Cu ions within the dielectric layer, facilitated the study of the influence that Cu have on the leakage current conduction mechanism and TDDB lifetime.

Various leakage current conduction mechanism were fitted to the blind via structures with and without Cu migration in the dielectric layer, to determine the best fit for the most dominant conduction mechanism. It was found that a single conduction mechanism does not adequately describe blind via structure that are without Cu presence, suggesting that there is a possibility that several mechanisms are present and overlapping simultaneously. However the blind via structure with Cu ions present in the dielectric layer after degradation was found to fit well with a PF conduction mechanism validated with experimentally measured optical dielectric constant, using the optical ellipsometer. It was also interesting to observe that the leakage current conduction is dependent on the oxidation state of the migrated Cu ions where the PF mechanism is dominant only when the oxidation state of Cu ions is in the CuO form. XPS analysis suggest that the oxidations state of Cu changes over time from Cu_2O to CuO.

Cu ions play different roles in the dielectric layer which can accelerate and decelerate TDDB lifetime, which is influenced by the applied E-field, temperature and also the oxidation state of the Cu ions. With understanding of the failure mechanism, TDDB lifetime can be extended accordingly. This suggests that TDDB is not a simple parametric test where proper understanding of the different mechanisms induced by the presence of Cu in the dielectric layer is necessary for accurate lifetime analysis. As a result, it could be the reason for various TDDB models proposed by different researchers to date. TDDB lifetime models were

fitted experimentally and is found to be in good agreement to the $\sqrt{E}$ model. The $\sqrt{E}$ model was verified experimentally by measuring the time to failure at low *E*-field, rather than extrapolating data from high *E*-field.

6.2 Future Work

The present work explores the reliability performance of interconnect technology in the form of Cu wire bond and Cu blind via, after reliability stress test up to the automotive grade 0 requirements. Degradation study post stress test using a non-destructive electrical characterization method for Cu wire bonding has been explored and is proven to be effective with results correlating with actual PFA. This has open up room and opportunity for further research work to look more deeply into a failure mechanism based degradation study approach, considering the bill of material. Another aspect can be to focus on the end of life reliability assessment where new failure modes and mechanisms may start to surface and needs to be identified. The influence of multiple failure modes and mechanisms may result in a more complex analysis, especially to differentiate them which needs further investigations. In addition, the early detection of the onset of failures induced by other commonly applied acceleration stress tests in the microelectronics industry such as HTSL and uHAST can also be explored as the failure modes and mechanism induced, can be totally different. At present, the measured ΔR has contributions coming from all the three different sections of the entire wire bond, which consist of the ball bond, wire span and wedge bond. Therefore, further development work can focus on how the electrical characterization method can be segmented separately into the three different sections of the wire, for a more dedicated and specific assessment.

The present work on Cu blind vias as a simulation for TSV interconnect technology reliability revealed failures such as Cu protrusion that can be further improved by process optimization. Therefore, it can be the scope of future work to look into process optimization such as annealing, to control the severity of Cu protrusion after reliability stress test which will otherwise lead to catastrophic electrical failures. In addition, for a more accurate analysis, actual device with stacked dies can be used for assessment. Electrical characterization on Cu migration was studied where it was demonstrated that a general sense of control and monitoring of the transport of Cu ions within the dielectric for reliability evaluation was possible. However, more understanding is required on the correlation between the sensitivity of the electrical characteristics to the

concentration of Cu ions present in the dielectric layer. A possibility is to perform an in-situ biasing and imaging of Cu migration under TEM, which may provide some insights to determine the point where detection becomes possible. The difference in sensitivity was observed from the comparison between a single blind via and an array of 200 blind via structures after post reliability stress test. Furthermore, with the continuous scaling and introduction of low-k dielectrics for higher performance, it is expected that this method of reliability evaluation will be even more sensitive. This is because thinner dielectric and low-k dielectric will result in an increased capacitance and easier transport of Cu ions within the dielectric respectively. Low-k dielectric material was not considered for Cu migration in this present study due to differences in test structure, layout and the availability of samples. While it is clear that the presence of Cu in the dielectric influence TDDB lifetime, the failure mechanism on how different TDDB stress test conditions could affect its TDDB lifetime performance is still not fully understood. Full understanding may influence how TDDB test will be performed in the future. Last but not least, more TDDB data can be collected especially at lower *E*-field for more accurate TDDB modeling.

List of Achievement and Publications

Achievement / Award:

[1] Recipient of CPMT/ECTC Student Travel Award for 2017 IEEE 67th Electronic Components and Technology Conference.

Journal Papers:

[1] J. M. Chan, C. M. Tan, K. C. Lee, C. S. Tan, "Non-Destructive Degradation Study of Copper Wire Bond for Its Temperature Cycling Reliability Evaluation", *Microelectronics Reliability*, vol. 61, pp. 56-63, Jun. 2016.

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International Conferences:

[1] J. M. Chan, C. M. Tan, K. C. Lee, C. S. Tan, "Non-Destructive Degradation Study of Copper Wire Bond for Its Temperature Cycling Reliability Evaluation", in *8th International Conference on Materials for Advanced Technologies (ICMAT)*, Singapore, 28 Jun – 03 Jul 2015.

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