Analysis and Design of

Audio Class D Amplifiers

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Summary

This Ph.D. research program pertains to the analysis and design of Class D Amplifiers (CDAs) for 'next-generation' devices embodying CDAs with substantially improved specifications over the state-of-the-art, including Total Harmonic Distortion (THD), Intermodulation Distortion (IMD), Power Supply Rejection Ratio (PSRR) and power-efficiency. Said analysis and design are on the basis of analytical investigations (into the mechanisms of and the circuit parameters affecting the various specifications of CDAs) and on the basis of a monolithic realization of CDA prototypes (embodying novel architectures and/or circuits). The specific CDA architectures of interest are the somewhat esoteric ultra-low-power Bang-bang Control CDAs and the ubiquitous Pulse-Width-Modulation (PWM) CDAs. The former and latter CDA architectures are appropriate for ultra-power-critical portable devices and high-quality multimedia devices respectively.

To improve the linearity of Bang-bang control CDAs, their IMD is investigated to ascertain the mechanisms thereof and to derive analytical expressions to comprehensively model said IMD mechanisms. It is interesting that despite its imperativeness, the IMD of Bang-bang control CDAs remains unreported/uninvestigated in literature. From our analysis, we observe the interesting phenomenon of the presence of even-order IMD that is usually negligible/unreported in CDAs and in linear amplifiers; as expected, odd-order IMD is present. We show that in some practical scenarios, the even-order IMD is unexpectedly dominant over the odd-order IMD. The derived analytical expressions for the IMD are verified by simulations and on the basis of measurements on a physical Bang-bang control CDA. This analysis is insightful and useful as it provides an analytical basis to model (and to predict the magnitude of) the IMD of Bang-bang control CDAs,

and delineates the possible trade-offs in relation to other imperative parameters (e.g. PSRR) to mitigate the IMD.

To improve both the linearity and the supply noise immunity of PWM CDAs, a novel PWM CDA is proposed, designed and monolithically realized in 65nm CMOS. The proposed design, embodying a novel carrier generator and the first-ever 'phase-error-free' PWM modulator, circumvents the otherwise undesirable trade-offs involving linearity, noise-immunity, power-efficiency and electromagnetic interference in conventional designs. On the basis of measurements on the prototype CDA ICs, the proposed design achieves not only the highest PSRR reported to-date, but also the highest (two) Figures-of-Merit when benchmarked against reported state-of-the-art CDAs.

We identify that the ground-bounce in CDAs can drastically degrade the linearity and reliability of CDAs, including Bang-bang control and PWM CDAs. Interestingly, this phenomenon in CDAs has yet to be analytically investigated in literature, and the generally accepted means for its mitigation are largely empirical and intuitive. We complete the first-ever analytical investigation to ascertain the mechanisms of and the circuit parameters affecting the ground bounce, and its ensuing effects on CDAs. We show that the generally accepted practices for mitigating ground bounce may unexpectedly exacerbate the ground bounce, thereby degrading the linearity of CDAs. On the basis of this investigation, we propose a systematic design methodology to reduce the ground-bounce and its effects on CDAs. The efficacy of the proposed design methodology is verified by means of simulations. For example, a PWM CDA optimized with said methodology features significantly higher linearity (4x lower THD) compared to the same CDA without said optimization.

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Nomenclature

BJT	Bipolar Junction Transistor
BTL	Bridged Tied Load
CMOS	Complementary Metal Oxide Semiconductor
EMI	Electromagnetic Interference
IMD	InterModulation Distortion
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	*n*-type MOSFET
PMOS	*p*-type MOSFET
PS-IMD	Power Supply induced InterModulation Distortion
PSRR	Power Supply Rejection Ratio
PWM	Pulse Width Modulation
SNR	Signal to Noise Ratio
THD+N	Total Harmonic Distortion plus Noise
ΣΔ	Sigma Delta

Chapter 1 Introduction

1.1 Motivation

Audio power amplifiers are ubiquitous electronic circuits and at this juncture, the design art thereto is mature. Audio power amplifiers functionally serve to amplify electronic signals within the audio frequency range (20 Hz to 20 kHz), ideally with perfect linearity and perfect power-efficiency. The linearity of an audio power amplifier is generally qualified by its distortions, and the commonly quoted parameters include Total Harmonic Distortion plus Noise (THD+N) [1, 2] and Intermodulation Distortion (IMD) [1, 2]. Power-efficiency [3], on the other hand, is defined by the ratio of the useful power (delivered to the load, typically a loudspeaker) to the total power (drawn by the amplifier). An ideal audio power amplifier features zero distortion and 100% power-efficiency.

A commonality in virtually all portable electronic devices, such as smart devices (including smartphones and tablets), is the need for small-form-factor, thereby requiring the embedding of many complex circuits (e.g. power management, digital signal processor, audio amplifier, etc.) into an SoC (System-on-Chip) or an SiP (System-in-Package). In the SoCs or SiPs, these complex circuits are placed in close proximity to each other and they often share the same power supply rail. In such embodiments, these

different complex circuits often interfere with each other. For example, in smart devices embodying GSM transceivers, the radio frequency transmitter therein injects substantial noise at 217 Hz into the supply rail [4, 5], and this was a major issue in early audio amplifiers. The usual solutions involve employing DC-DC converters and/or LDOs (Low Dropout regulators) to provide a noise-suppressed supply for the audio amplifiers. The cost penalty, however, is expensive in terms of added hardware (and lower power-efficiency) and the ensuing larger form-factor. To accommodate this noisy power supply issue, an ideal audio power amplifier embodied in the SoC or SiP of electronic devices (portable and otherwise) should additionally feature infinitely-high supply-noise immunity. Supply-noise immunity is often qualified by Power-Supply-Rejection-Ratio (PSRR) [1, 2] and Power-Supply-induced-Intermodulation-Distortion (PS-IMD) [6, 7].

In short, an ideal audio power amplifier should collectively feature not only zero distortion, 100% power-efficiency, but also infinitely-high supply-noise immunity. The power-efficiency is of particular importance for portable electronic devices for two reasons. First, a power-*in*efficient amplifier wastes a significant portion of its operating power and this in turn reduces the battery lifetime of portable devices. Second, said wasted power is dissipated in the form of heat, which often requires a heat-sink to dissipate to avoid over-heating. Heat-sinks are typically bulky and are incompatible in small-form-factor portable devices.

Present-day audio power amplifiers can be categorised into two categories according to the topology of their output stage design: linear amplifiers (for instance Class A or Class AB amplifiers) and switching amplifiers (that are primarily Class D amplifiers

(CDAs) and sometimes known as 'digital' amplifiers; arguably a misnomer). The output stage of linear power amplifiers typically adopt linear topologies where the output power transistors therein are idiosyncratically biased in the saturation region (for Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)) or in the active region (for Bipolar Junction Transistors (BJTs)) [8]. This modus operandi is power-*in*efficient (typically < 30%, see Figure 1-1), because a large amount of power is wasted by the ensuing biasing current flowing (directly from supply to ground) through the output power transistors even when little or no useful power is delivered to the load. Due to the low power-efficiency of the linear amplifiers, they are now largely replaced by CDAs in portable electronic devices. For completeness, it is interesting to note that power amplifiers for earphone and headphone loudspeakers nevertheless are typically linear Class AB because of their relatively low output noise, and because their power is small (~100 mW), their low power-efficiency is largely of little consequence (from a system perspective).

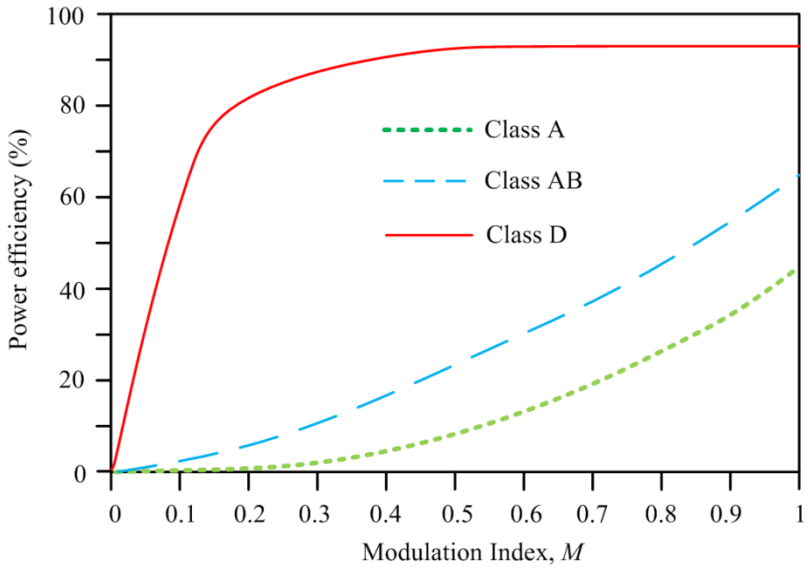


Figure 1-1 Power Efficiency of audio amplifiers versus Modulation Index [9]

CDAs typically feature high power-efficiency [2] – their efficiency can be as high as >90% over a large range of the output power [3] and as depicted in Figure 1-1, is substantially higher than their linear counterparts. The high power-efficiency of CDAs is primarily due to the switching operation of their output stage. Specifically, the output transistors of CDAs are biased in either the cut-off or the triode regions (vis-à-vis saturated/linear region), thereby respectively functioning as switches with either high off-resistance or low on-resistance. Hence, there is no wasted constant biasing current required in linear amplifiers. From a portable device design perspective, their high power-efficiency is particularly advantageous as the battery lifetime of portable devices is desirably extended, and they offer a small-form-factor solution due to the absence of a heat-sink.

In the evolution of CDAs, the early CDAs [10-13] were inferior to their linear counterparts, typically with poorer linearity (e.g. higher THD+N) and lower noise-immunity (e.g. lower PSRR). With the maturing of CDA technology over the last decade, due to the advancement of process technology and concerted effort by the CDA design community, the design art thereto have somewhat matured with the performance of CDAs having improved significantly. For instance, many present-day commercial CDAs feature relatively low THD+N (e.g. THD+N < 0.1%) and high PSRR (e.g. PSRR > 60 dB) [14-17] – this level of performance is arguably sufficient for many applications. In a few state-of-the-art high-performance CDAs, their performance is rather impressive in the sense that their performance often surpasses that of linear amplifiers – achieving very-low THD+N (e.g. THD+N < 0.01%) and very-high PSRR (e.g. PSRR > 80 dB) [18-20], yet retaining

their high power-efficiency advantage. Not unexpectedly, CDAs are now widely and increasingly accepted as the amplifier of choice in a plethora of electronic devices, including portable devices.

Despite the availability of relatively high-performance CDAs, there is a growing demand for '*next-generation*' CDAs in some fast-evolving and emerging applications. At this juncture, this demand is apparently evident for two applications – high-quality multimedia devices embodied in high-end smart devices (e.g. smartphones and tablets), and ultra-power-critical audio applications such as hearing instruments (hearing aids).

In the former, the high-end smart devices are now evolving to include functionality as the primary entertainment and communication device for their users, and are therefore expected to feature improved user-experience including better audio fidelity; although it can be argued that the fidelity of ultra-high fidelity CDAs significantly exceeds that of present-day loudspeakers, there is substantial effort within the transducer industry and community to realize loudspeakers with significantly improved fidelity. This in turn requires the *next-generation* CDAs in the high-end smart devices to feature commensurably higher linearity (e.g. THD+N << 0.01%) and improved noise-immunity (e.g. PSRR >> 80 dB). In addition, low Electromagnetic Interference (EMI) of CDAs [21-24] is also desired for portable devices. Specifically, as the switching operation of the CDA output stage may generate considerable EMI which interferes with the operation of other circuits in close proximity, EMI is an important design consideration in small-form-factor devices (see section 2.1.3 later).

In the latter ultra-power-critical applications, such as hearing instruments where the battery is sub-miniature (with ~100 *m*AHr energy capacity), the power-efficiency of the CDA therein is expected to be higher than conventional CDAs. It is because conventional (general-purpose) CDAs typically dissipate a few milli-Amperes (mA) of quiescent current. This is intolerably large because the total quiescent current of ultra-power-critical hearing instruments is typically expected to be <1 mA (not accounting for acoustical power output); reported CDAs in hearing aids typically feature relatively poor THD+N (e.g. 0.3%) and/or poor PSRR (e.g. 45 dB) [25]. Put simply, the *next-generation* CDAs therein would need to feature very-high power-efficiency (and very-low quiescent current), while maintaining sufficient fidelity (e.g. THD+N < 0.1%) and high PSRR (e.g. >60 dB); see Section 3.1 later.

CDAs are often categorized [5, 9, 26] according to their modulation scheme. In view of the aforesaid applications and their respective requirements for CDAs, the two categories of CDAs that are of particular interest herein are the Bang-bang Control (Bang-bang) and the Pulse-Width-Modulation (PWM) CDAs; these two categories (and other modulation schemes) will be comprehensively reviewed in Chapter 2. Of the two categories, PWM CDAs are most prevalent, largely due to their easy realization, relatively good linearity (e.g. THD+N < 0.05%) and for being able to accommodate more than one channel (for example a stereo audio signal comprising left channel and right channel signals) [4, 20, 24] due to the synchronized clocking between two or more channels; see Chapter 2 later. On the other hand, as the Bang-bang CDAs are arguably the most hardware-simplistic and the most power-efficient [6, 27], they are arguably most

appropriate for the ultra-power-critical devices (with a single channel output such as hearing instruments).

Interestingly, at this juncture, the performance of state-of-the-art Bang-bang and PWM CDAs remains insufficient for the *next-generation* CDAs. Not unexpectedly, there is significant interest within the CDA design community to address the shortcomings of present-day CDAs (relative to the envisioned *next-generation* CDAs). Some aspects of the design efforts by the CDA design community will now be described.

To design the *next-generation* Bang-bang CDAs for ultra-power-critical devices, it is imperative to comprehend and appreciate the mechanisms of and the circuit parameters affecting their linearity and power-efficiency. Some aspects of their linearity (and noise-immunity) have been reported but are largely limited to THD [27] – the technological know-how is incomplete. Specifically, IMD, an imperative parameter that qualifies linearity, remains unreported, and the mechanisms of and the circuit parameters affecting the IMD of Bang-bang CDAs are largely unknown. For instance, it is not known that if even-order IMD components exist in Bang-bang CDAs and if they do exist, their magnitude and effects are unknown. Further, although it is well-established [28] that the odd-order IMD is the dominant IMD component in linear amplifiers, it is not known if this is true for Bang-bang CDAs and how it varies at different operating conditions. Perhaps most imperatively, design methods to minimize the IMD in Bang-bang CDAs are largely unknown, including the potential trade-offs with other parameters. Simply put, at this juncture, designers design Bang-bang CDAs largely based on intuition (and experience), and an analytical basis for their designs for the IMD is apparently lacking.

Consider now the *next-generation* PWM CDAs. As they are presently the most prevalent CDAs, their designs have been extensively researched and reported in literature. Their design art is relatively mature and the analytical investigations thereto are largely complete [7, 28-33]. For example, it is well-established that conventional PWM CDA designs inevitably incur trade-offs between critical specifications including THD+N, PSRR, power-efficiency and EMI. Said trade-offs are largely due to the distortion mechanisms of (closed-loop) PWM CDAs. Specifically, the mechanisms for the distortions of PWM CDAs are well-established – open-loop PWM CDA error reduced by feedback (loop gain+1; see Section 2.2 later), and duty-cycle error and phase error; the phenomena of duty-cycle and phase errors were discovered by the NTU CDA group [33]. It was reported that, unlike classical linear feedback theory for the design of analog circuits, the phase error distortion is largely non-linear and cannot be mitigated by negative feedback [20, 33]. Conversely, the conventional (and intuitive) method to increase the loop-gain to improve CDA performance could instead have adverse effects (see Chapter 2 later)!

At this juncture, there is no reported method to eliminate the phase error; employing higher switching frequency only reduces the phase-error to some extent. However, higher switching frequency is generally undesirable because the penalty can be expensive in terms of higher switching power dissipation and the ensuing lower power-efficiency (and potentially more severe EMI). A number of design attempts have been reported to achieve better performance PWM CDAs [4, 20, 26], but without fundamentally addressing the aforementioned (non-linear) distortion mechanisms and the ensuing trade-offs, said attempts (designs) fall short in one or more specifications of *next-generation*

CDAs for high-quality multimedia devices; see details later in Section 2.2. In other words, at this juncture, there is no viable architecture/method to enable an 'across-the-board' improvement of all imperative specifications of PWM CDAs. Hence, there is a real need to design novel ('out-of-the-box') PWM CDA architectures and pertinent circuits that are fundamentally different from conventional designs, particularly not solely relying on the negative feedback – by implementing said novel designs, thereby achieving the performance required by the *next-generation* PWM CDAs.

In addition to the aforementioned issues with 'system' optimization (i.e. lack of analytical basis for Bang-bang CDAs) and with architecture design (i.e. the need for novel architecture for PWM CDAs), there are also practical implementation issues that could impede and/or complicate the realization of *next-generation* CDAs. Amongst these practical issues, the ground-bounce is probably the most serious and pervasive. The ground-bounce is voltage-spikes (and 'ringing') largely induced on the parasitic inductance in the supply rails by the switching operation of digital (or digital-like) circuits [34]. The ground-bounce noise exists in virtually all practical CDAs, and it could drastically interfere with the operation of sensitive analog signal processing circuits in CDAs. Interestingly, although the ground-bounce has been extensively studied in the perspective of digital circuits [34-37], the ground-bounce in CDAs remains largely uninvestigated. Further, its effect is largely unknown, for instance if ground-bounce affects specific imperative parameters such as THD+N.

Specifically, at this juncture, the mechanisms of and the circuit parameters affecting the ground-bounce in CDAs are largely unreported. Further, there is no established or

rigorous mitigation technique to reduce the ground-bounce and its effects. Nevertheless, although there are empirical (and intuitive) mitigation techniques (adopted by practicing designers within CDA design community) for the ground-bounce in CDAs, it is unestablished if these empirical methods would reduce the ground-bounce at different operating conditions or conversely, possibly exacerbating the ground-bounce. Put simply, without a method to adequately reduce the ground-bounce and/or to mitigate its effects on CDAs, the ground-bounce issue could seriously impede the practical realization of *next-generation* CDAs (in monolithic embodiments).

In summary, there are compelling motivations to improve the performance of Bang-bang and PWM CDAs for the *next-generation* applications. For Bang-bang CDAs, there is a need for an effort to complete analytical investigations, for example an analytical investigation to ascertain the mechanisms of and the circuit parameters affecting the IMD of *next-generation* CDAs for ultra-power-critical devices. For PWM CDAs, there is a need for an effort to design novel PWM CDA architectures/circuits to achieve the performance required for *next-generation* CDAs in high-quality multimedia portable devices. In addition, for the ground-bounce, a practical implementation issue in the monolithic realization of CDAs, there is a need for an effort to analytically investigate and to derive analytical means for CDA designers to mitigate the ground-bounce in CDAs.

1.2 Objectives

In view of aforementioned motivations, the broad objective of this Ph.D. program pertains to the analysis and practical design of Bang-bang and PWM CDAs for ultra-power-critical devices and high-quality multimedia devices respectively. The specific objectives are:

(i) To analytically investigate the IMD of Bang-bang CDAs for ultra-power-critical portable devices. This includes ascertaining the mechanisms of and the circuit parameters affecting the IMD, and to provide an analytical basis for the optimization (minimization) of the IMD, including the potential trade-offs with other parameters to mitigate the IMD;

(ii) To propose novel PWM CDA architectures and/or circuits to reduce (or eliminate) the phase error and to circumvent trade-offs between imperative specifications. This includes the design of PWM CDAs embodying novel architectures/circuits to simultaneously achieve high linearity (low THD+N), high noise-immunity (high PSRR), high power-efficiency and low EMI;

(iii) Further to (ii), to practically realize monolithic prototypes of the proposed CDA designs in (ii) using a standard CMOS process. Furthermore, on the basis of physical measurements on said prototypes, to verify the efficacy of the proposed architectures and circuits, thereby demonstrating the substantially improved performance of the proposed PWM CDAs;

(iv) To analytically investigate the ground-bounce in CDAs to ascertain the mechanisms of and circuit parameters affecting the ground-bounce and its effect on CDAs. This includes the derivation of analytical expressions of the ground-bounce noise in CDAs;

(v) Further to (iv), on the basis of said investigation in (iv), to propose a practical design methodology to minimize the ground-bounce in CDAs, thereby mitigating its effects thereto. This also includes demonstrating the preciseness of the derived analytical expressions and the efficacy of the proposed design methodology.

1.3 Contributions

A number of contributions are made in this Ph.D. program and they are largely reported in our technology disclosures and ensuing patents [38-40], and journal [41-43] and conference publications [44-47]. To the best of the author's knowledge, all contributions delineated herein are novel and unreported in literature. These contributions are now summarized, congruous to the aforementioned objectives.

The contributions pertaining to the objective (i) include:

(a) An analytical investigation into the mechanisms of the IMD of Bang-bang CDAs – the first ever investigation into the IMD of Bang-bang CDAs. The investigation ascertained the mechanisms of and circuit parameters affecting the odd-order IMD (the IMD type commonly-seen in CDAs and in linear amplifiers) and somewhat

unexpectedly, the even-order IMD. The contributions herein included the derivations of analytical expressions for both the odd-order and even-order IMDs in Bang-bang CDAs. This analysis is particularly useful as it offers insights into optimization for the mitigation of IMD, including the potential trade-offs with other imperative specifications.

The contributions pertaining to the objectives (ii) and (iii) include:

(b) The proposal of two inventions that are phase-error-free PWM modulator and input-modulated carrier generator. These two inventions, individually and collectively, largely eliminated the phase error and circumvented the aforementioned undesirable trade-offs (that are otherwise inevitable in conventional PWM CDAs). Further, a PWM CDA design embodying said inventions is designed that simultaneously achieved low distortion, high noise-immunity and high power-efficiency, yet with reduced EMI (compared to the conventional PWM CDAs).

(c) Further to (b), CDA prototypes embodying the proposed design in (b) are realized using a commercial 65 nm CMOS process. On the basis of physical measurements on said prototypes, the proposed CDA featured a THD+N of 0.0027% when delivering ~500mW, and a PSRR of 101 dB; this PSRR is the highest reported to-date, and the efficiency is a high 94%.

On the basis a reported Figure-of-Merit (and a proposed Figure-of-Merit), the proposed CDA is overall the ‘best’ design amongst all reported state-of-the-art CDAs.

The contributions pertaining to the objectives (iv) and (v) include:

(d) An analytical investigation into the ground-bounce in CDAs. The investigation included the identification of two distinctive mechanisms of the ground-bounce and the associated circuit parameters. Analytical expressions of the ground-bounce in CDAs are derived and subsequently verified by means of simulations.

(e) Further to (d), on the basis of said derived expressions, a practical design methodology to minimize the ground-bounce and to mitigate its effects on CDAs is proposed – this is the first-ever systematic and rigorous design methodology reported. Interestingly, it is ascertained that some empirical and intuitive methods to minimize the ground-bounce may conversely have adverse effects. The efficacy of the proposed methodology is subsequently verified – a CDA optimized with said methodology featured approximately four times lower THD compared with the same CDA without said optimization.

1.4 Organizations of the thesis

The subsequent chapters of this thesis are organized in the following manner.

In Chapter 2, a comprehensive literature review on CDAs is provided. The fundamental building blocks of CDAs and their design considerations are reviewed, followed by a review of commonly used modulation techniques, the design of CDA output stages, and the design of filterless CDAs. An in-depth review of state-of-the-art

PWM and Bang-bang CDAs and the associated design considerations thereto are subsequently reviewed, including the associated design challenges.

In Chapter 3, the IMD of Bang-bang CDAs is investigated – this is the first-ever investigation into the IMD of Bang-bang CDAs. This chapter commences with an investigation of the IMD of ideal Bang-bang CDAs and this serves as a preamble to the following investigation into the IMD of practical Bang-bang CDAs; said practical CDAs include non-idealities such as comparator offsets and/or supply mismatch. The analytical expressions for the IMD of Bang-bang CDAs, both ideal and practical, are derived and subsequently verified by means of simulations and on the basis of physical measurements on prototype CDAs.

In Chapter 4, a novel PWM CDA that embodies an input-modulated carrier generator and a first-ever phase-error-free PWM modulator is proposed. This chapter commences with a discussion on the design challenges of conventional PWM CDAs, particularly the undesirable and inevitable trade-offs between imperative specifications. To circumvent the trade-offs, two innovations (said carrier generator and modulator) are proposed and their operation mechanisms discussed. The design of other important building blocks is also delineated. The design of the prototype ICs embodying said innovations is presented. The measurements thereto are thereafter benchmarked against reported state-of-the-art designs. The benchmarking demonstrates the significant improvements of the proposed CDA over reported state-of-the-art designs. Particularly, the prototype CDA features the highest PSRR and highest (two) Figures-of-Merit of all reported designs to-date.

In Chapter 5, the ground-bounce in CDAs is analytically investigated. This chapter commences with a discussion on the mechanisms of and the circuit parameters affecting the ground-bounce in CDAs, followed by the effects of the ground-bounce on the reliability and performance (particularly the linearity) of CDAs. The analytical expressions of the ground-bounce are thereafter derived. On the basis of said investigations, a practical design methodology to minimize the effects of the ground-bounce on CDAs is proposed. The efficacy of the proposed methodology is demonstrated by simulations, where a PWM CDA optimized using said methodology features 4x THD improvement over the same CDA without said optimizations.

In Chapter 6, conclusions of this research program are drawn and recommendations for further work presented.

Chapter 2 Literature Review

This chapter provides a comprehensive review of CDAs and it serves as a preamble to the contributions delineated in the following chapters.

In general, CDAs can be categorized as either analog CDAs or digital CDAs [29, 48, 49], and they are sometimes collectively called 'switching amplifiers'. Analog CDAs (and their linear amplifier counterparts, such as the prevalent Class AB linear amplifiers) typically accept an analog (continuous-time) signal as their input signal (from their preceding circuits such as an audio Digital-to-Analog Converter), and the signal processing (including modulation) is carried out in the analog domain. The digital CDAs, on the other hand, accept digital signals as their input signals, and the signal processing is carried out digitally.

The CDAs of interest in this Ph.D. program are the analog CDAs. Section 2.1 provides a comprehensive review of CDAs, including the fundamental building blocks thereof and their basic operating mechanisms, followed by the review of the commonly-used modulation schemes, the output stage designs, and filterless CDA design issues. In Section 2.2, a more in-depth review of PWM and Bang-bang CDAs is provided, with

emphasis on state-of-the-art design techniques and where pertinent, analytical investigations. A conclusion is drawn in Section 2.3.

2.1 A Review of Class D Amplifiers

The first concept of a CDA can probably be attributed to A. H. Reeves [2] in the 1950s. In early CDAs, their linearity was relatively poor compared to their linear counterparts. Thanks to the advances in process technology and the concerted efforts by the CDA design community, the performance of present-day CDAs has improved considerably. At this juncture, CDAs are widely adopted in numerous audio-related devices including the smartphones, tablets, TVs [5, 26], etc.

A CDA typically comprises a modulator, an output stage and a load (typically a loudspeaker and possibly a preceding lowpass filter), as shown in Figure 2-1.

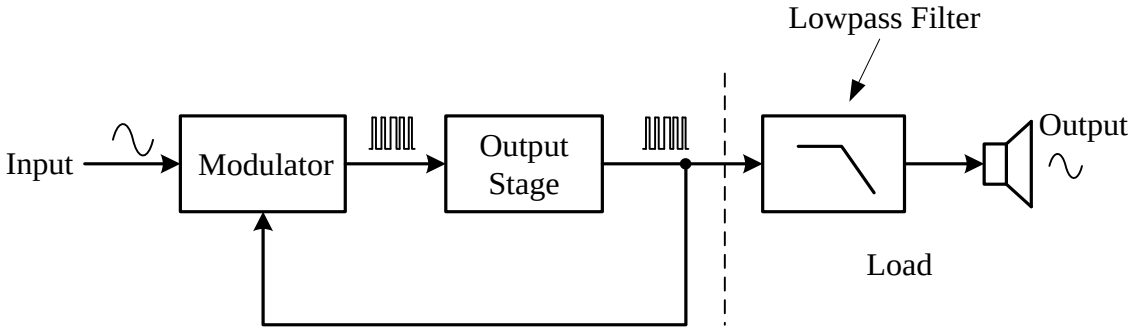


Figure 2-1 Block diagram of a CDA

Modulator

The modulator modulates the analog input signal into a digital-like pulse signal, which serves as the control signal to the output stage. CDAs are commonly categorized according to their modulation scheme. The commonly-used modulation schemes include (i) PWM [7, 16, 20, 26, 33, 50], (ii) Sigma-Delta [18, 51, 52], (iii) Bang-bang Control [6], and (iv) Self-oscillating [53-55]. As each said modulation scheme has its merits and drawbacks in terms of linearity, noise-immunity, power-efficiency, cost and form-factor, it is hence important for designers to judiciously select an appropriate modulation scheme for their targeted application. We will review the aforementioned modulation schemes in turn in section 2.1.1.

Output Stage

The output stage in CDAs serves to provide sufficient driving capability to drive the loudspeaker load, typically of low-impedance. The resistance of the load is often 4 Ω or 8 Ω for general purpose loudspeaker, and is typically 64 Ω or 128 Ω (or even higher, e.g. 400 Ω) for some micropower applications, such as hearing instruments (hearing aids) [9]. The output stage can be configured as either singled-ended (also known as half-bridged) or differential (also known as Bridged-Tied-Load (BTL)), as depicted in Figure 2-2 and Figure 2-3 respectively. Each configuration has its merits and drawbacks. For instance, a BTL output stage can support twice the voltage swing on the load compared to a single-ended output stage from the same voltage supply, hence four times the output power. Nevertheless, the drawback is that the IC area (of said BTL output stage) is doubled and the cost likewise increased. The BTL output stage is generally more commonly-used, and

it is largely due to its higher output power and its higher PSRR – the PSRR of a BTL output stage is about 6 dB higher than its single-ended counterpart.

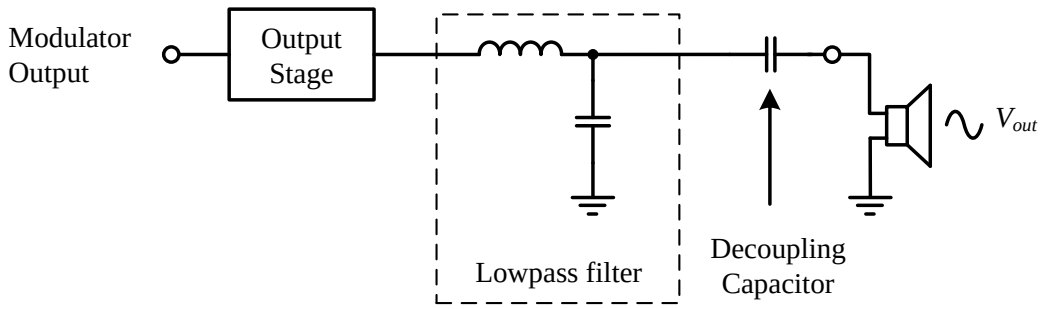


Figure 2-2 Schematic of a single-ended CDA output stage with a load

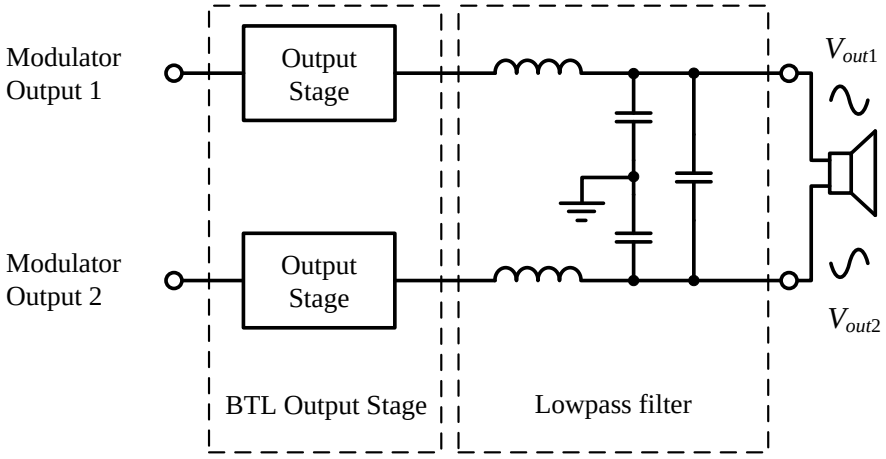


Figure 2-3 Schematic of a BTL CDA output stage with a load

The output stage design is also critical due to its sheer size and power – for a CDA that drives a typical loudspeaker load (whose resistance typically ranges from 4 Ω to 32 Ω), the output stage therein often occupies over 50% of the total active IC area and dissipates over 90% of the total power (including the power delivered to the load via the

output stage) [9]. We will provide a detailed review of the output stage design and pertinent design considerations thereto, including the power-efficiency optimization and the dead-time control circuit design in the next section.

2.1.1 Class D Amplifier Modulation Schemes

2.1.1.1 PWM Class D Amplifiers

PWM CDAs are arguably the most prevalent type of CDAs and this is largely due to their relatively simple hardware, low switching frequency and good performance – it has been demonstrated recently that the PWM CDA can achieve very-low THD+N and very-high PSRR [20]. PWM CDAs can be categorized according to their feedback topology: open-loop (no feedback), single-feedback and double-feedback. Triple or more feedback (paths) topology could possibly be realized, but they are nevertheless not commonly used due to their potential stability issue and often penalizing hardware and power overheads [4].

Figure 2-4 depicts the schematic of an open-loop PWM CDA. It comprises a PWM modulator (which comprises a carrier generator and a comparator), an output stage and a load with a lowpass filter. The operation of the open-loop PWM CDA is very simple. The PWM modulator generates a PWM signal by comparing the analog input signal against an internally generated carrier signal (that is often a triangular wave signal or a saw-tooth signal). The output stage buffers the aforementioned PWM signal and drives the load. The

lowpass filter removes high-frequency switching components and recovers the amplified input signal on the load.

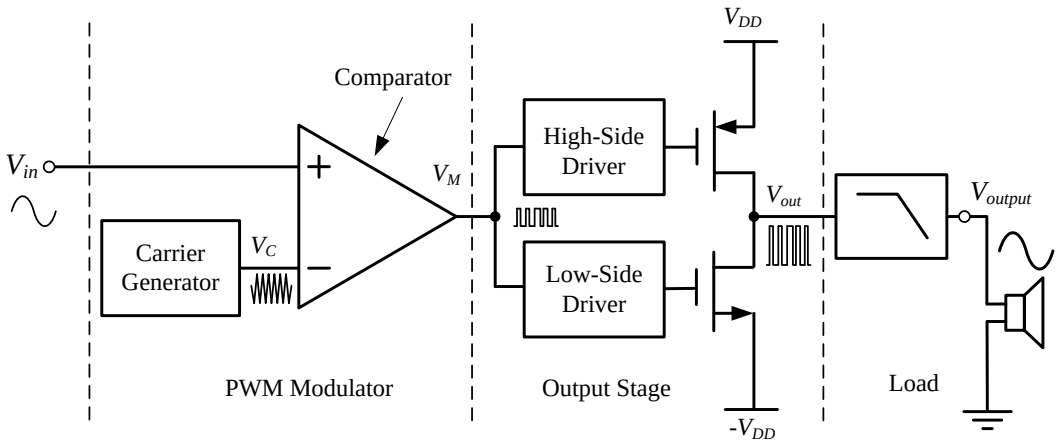


Figure 2-4 Schematic of an open-loop PWM CDA

The analysis of PWM signals is well-established. The spectrum of an ideal PWM signal can be analytically derived using a double-Fourier method [50]:

$$\frac{V_{out}}{V_{DD}} = M\cos(2\pi f_{in}t) + 4\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{J_n\left(\frac{m\pi M}{2}\right)}{m\pi}\cos(4m\pi f_{sw}t + 4n\pi f_{in}t)\sin\left(\frac{m+n}{2}\pi\right) \quad (2.1)$$

where V_{DD} is the supply voltage,

M is the modulation index,

f_{in} is the input frequency,

f_{sw} is the carrier (switching) frequency, and

$J_n()$ is the Bessel function of the first kind with order n.

It can be seen from eqn. (2.1) that the ideal PWM signal has no distortion or noise, and the unwanted components are at the carrier frequency and its harmonics. Given that the carrier signal frequency is typically much higher (e.g. >10 times) than the input signal, the lowpass filter can largely remove the unwanted carrier components from the output signal. In short, an ideal PWM CDA does not introduce any (audible) distortion or noise to the output signal. As aforementioned, distortions[+] are often qualified by THD that can be defined as eqn. (2.2) [1]. An ideal PWM CDA would therefore feature zero THD.

$$\text{THD} = \frac{1}{V_{out}(f_{in})}\sqrt{\sum_{n=2}^{\infty} V_{out}(nf_{in})^2} \times 100\% \tag{2.2}$$

Nevertheless, practical open-loop PWM CDAs suffer from severe distortions and noise, or high THD+N. Their high THD+N largely arises from non-ideal building blocks such as the non-ideal carrier generator or the non-ideal output stage [10, 56, 57]. It is therefore quite difficult, if not impossible, to realize a practical open-loop CDA that features low THD+N. It is because that the distortions and noise introduced by non-ideal circuit blocks therein will directly (i.e. without any suppression) appear on the output signal. Furthermore, some non-ideality is necessary for the CDA operation and is intentionally introduced in practical designs. For instance, the dead-time that is intentionally introduced into the output stage to improve the power-efficiency and reliability of the CDA [58]. In addition, open-loop PWM CDAs are very susceptible to supply noise, i.e. their PSRR is insufficiently high. A noisy supply would consequently exacerbate the noise of an open-loop PWM CDA. In general, because of their high

+ Other common distortions and non-idealities include IMD, output noise, supply-induced noise and PS-IMD.

THD+N and low PSRR, open-loop PWM CDAs are not generally accepted or widely adopted.

To improve the THD+N and PSRR of open-loop PWM CDAs, the usual approach of negative feedback was adopted – closed-loop PWM CDAs. Figure 2-5 depicts the schematic of a single-feedback PWM CDA. It comprises an integrator, an open-loop PWM CDA, a feedback network of R_1 and R_{fb1}, and a load with a lowpass filter. On the basis of classical negative feedback theory, the distortions and noise introduced by the open-loop PWM CDA can be largely attenuated by the loop-gain of the feedback loop. Hence the THD+N and PSRR of closed-loop PWM CDAs are significantly improved over their open-loop counterparts. As a result of said improvements, closed-loop PWM CDAs are well accepted and widely adopted for various applications.

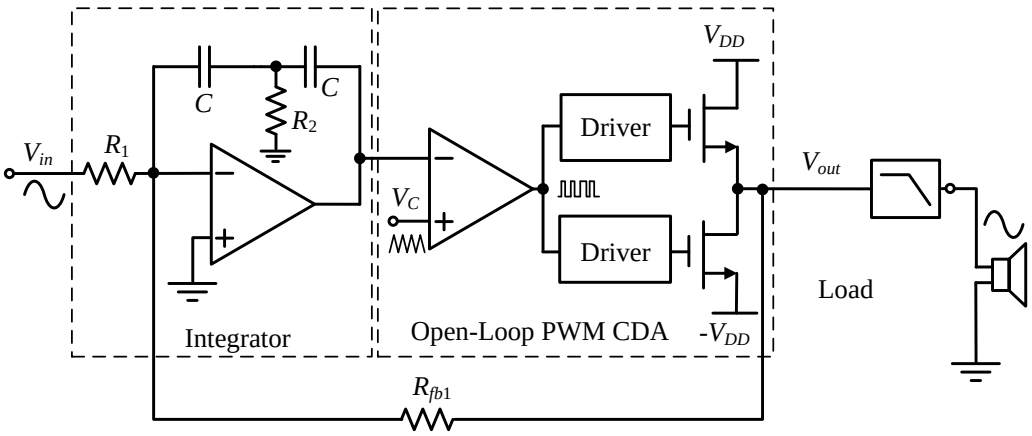


Figure 2-5 Schematic of a single-feedback PWM CDA

The mechanisms of the THD of single-feedback PWM CDAs are well-established [7, 32, 33, 59, 60]. Specifically, its THD mainly arises from three distinctive mechanisms:

(i) distortions introduced by the open-loop PWM CDA, (ii) duty-cycle error, and (iii) phase error. The THD due to (i) can be considerably attenuated by a factor of $LG+1$ (where LG is the loop-gain of the closed-loop PWM CDA). On the other hand, the THD due to (ii) and (iii) arise from the feedback of the PWM signal and the ensuing residual (not fully attenuated) switching component at the PWM modulator input – the intermodulation between the residual switching component and the carrier results in systematic distortions. These distortions exist even if all the building blocks are ideal, and they are largely affected by some design parameters such as loop-gain and switching frequency.

The mechanism of the PSRR of closed-loop PWM CDAs is also well-established and its mechanisms reported in literature [7, 61] – the supply noise is primarily injected via the output stage and can be considerably attenuated by the loop-gain.

In short, closed-loop PWM CDAs feature considerable improvements over their open-loop counterparts in terms of THD+N and PSRR, and said improvements can be largely attributed to the employment of negative feedback. Nevertheless, an in-depth review in the next section will show that the conventional closed-loop PWM CDAs incur some inevitable limitations/trade-offs that have potentially impeded their further improvements.

2.1.1.2 Sigma-Delta Class D amplifiers

Sigma-Delta (ΣΔ) modulation is another commonly-used modulation scheme in CDAs [18, 19, 51, 62]. The advantages of ΣΔ CDAs include their relatively lower output noise and higher linearity. For instance, a recently reported ΣΔ CDA achieved an integrated noise of 7.2 μV and a THD+N of 0.003% [19], considerably lesser than that of typical PWM CDAs whose noise and THD+N are often >30 μV and >0.01% respectively [4, 14, 15].

Arguably, the drawbacks of ΣΔ CDAs are their relatively complex hardware and high switching frequency, and the ensuing high quiescent power consumption. This is largely because a high-order, high clock-rate (switching frequency) ΣΔ modulator is typically desired for ΣΔ CDAs to achieve good linearity and low noise.

The ΣΔ CDAs can be categorized as synchronous and asynchronous, according to their ΣΔ modulator design. We will now review these two categories in turn.

Synchronous Sigma-Delta CDAs

The schematic of a first-order synchronous ΣΔ CDA is depicted in Figure 2-6. It comprises an integrator, a quantizer (including a comparator and a D flip-flop), a feedback network, an output stage and a load. The integrator integrates the difference between the input signal and the output signal, and shapes the quantization noise (that arises from the sampling with a finite sampling rate) to a frequency range that is out of the frequency band of interest (typically the audio frequency range). The output signal of the integrator is subsequently fed to the comparator. The comparator generates a digital-like signal by comparing the integrator output against a predetermined reference voltage. The D flip-

flop samples the comparator output at the clock rate (or sampling frequency). The output of the D flip-flop is a Pulse Density Modulated (PDM) signal that is the input to the output stage. The desired amplified analog signal is recovered at the output after the lowpass filter.

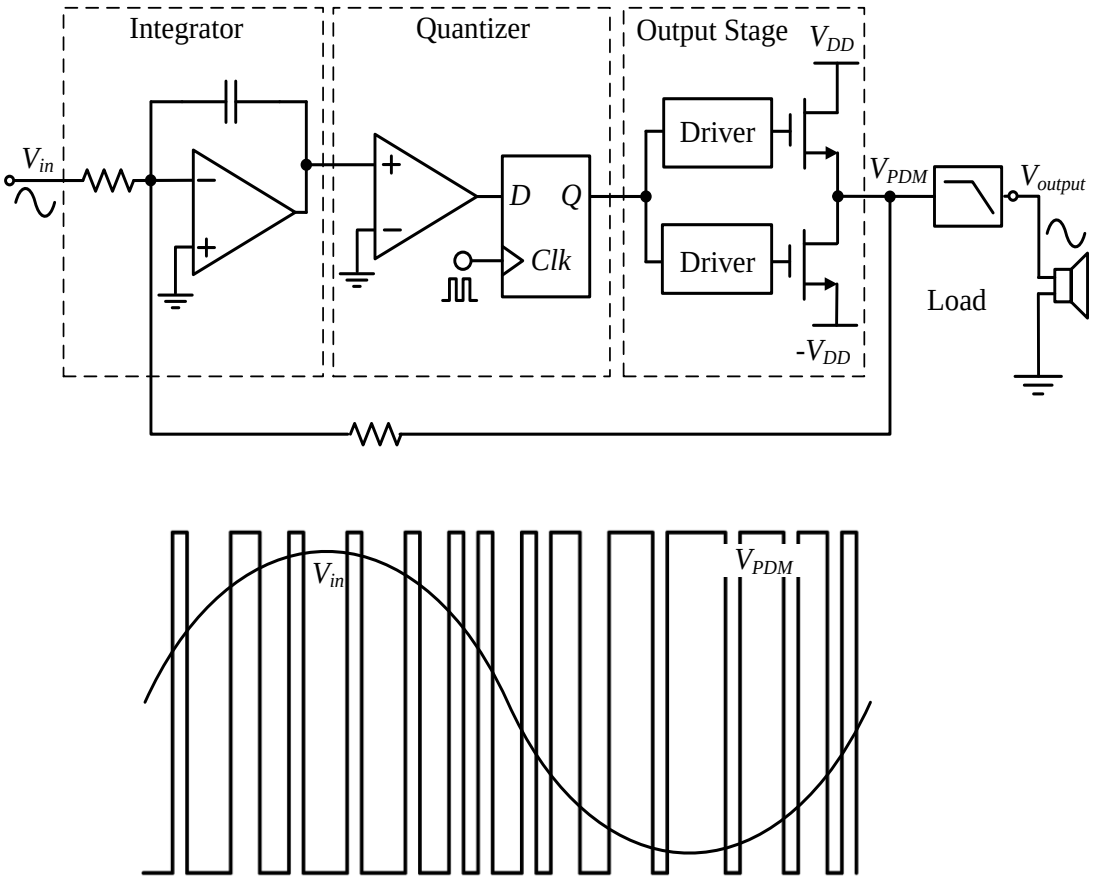


Figure 2-6 Schematic of a first-order synchronous ΣΔ CDA and its waveforms

The signal waveforms of a synchronous ΣΔ amplifier are also depicted in Figure 2-6. Congruous to the PDM signal, the instantaneous switching frequency of the ΣΔ CDA

varies with the magnitude of the input signal. This is in contrast with the PWM CDA whose switching frequency is independent of the input signal.

The high linearity and the low noise of synchronous ΣΔ CDAs have been demonstrated – a number of studies (and commercial products) have shown that the THD+N of some synchronous ΣΔ CDAs can be as low as ~0.003% [18].

Asynchronous Sigma-Delta CDAs

The schematic of an asynchronous ΣΔ CDA is depicted in Figure 2-7, and it is somewhat similar to its synchronous counterpart. The difference is that the quantizer of the ΣΔ CDA is now not controlled by an external clock but is instead controlled by the switching of a hysteresis comparator. The advantage of the asynchronous design is that its quantization noise is theoretically zero [63] because the sampling is now controlled by a continuous-time comparator. Similar to its synchronous counterpart, the output signal of the asynchronous ΣΔ CDA is also PDM. On the other hand, different to its synchronous counterpart whose switching operation can be synchronized by a clock, the switching operation of an asynchronous ΣΔ CDA is largely signal-dependent. This is potentially problematic because the signal-dependent switching components might intermodulate with other signals, for example if more than one channel (stereo comprising two audio channels) is accommodated on a single IC. This intermodulation may result in 'clock-beating', which can potentially lead to drastic fidelity degradation in terms of contaminated noise.

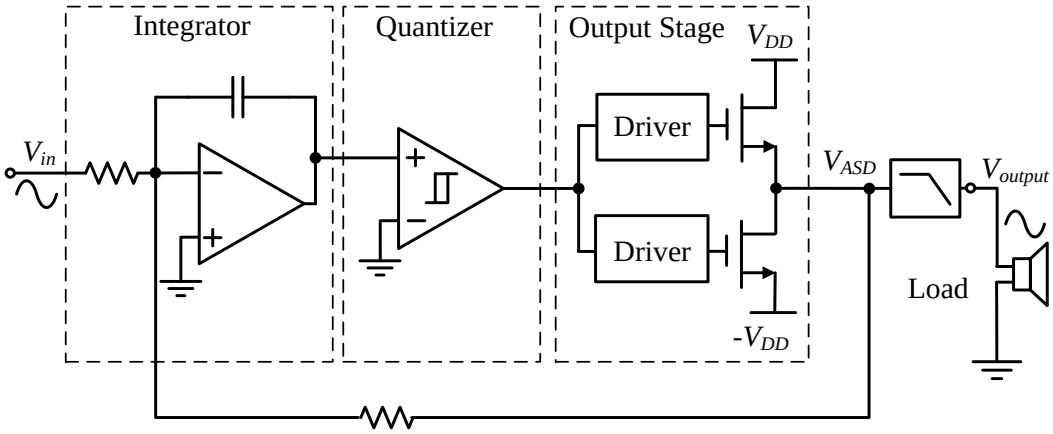


Figure 2-7 Schematic of a first-order asynchronous ΣΔ CDA

2.1.1.3 Bang-bang control Class D Amplifiers

Bang-bang control (Bang-bang) CDAs are less prevalent compared to PWM and ΣΔ CDAs and this is due to their relatively higher distortion and noise. Nevertheless, Bang-bang CDAs arguably feature the most simplistic hardware and the lowest quiescent power dissipation. Because of these attributes, there is growing interest for Bang-bang CDAs in some power-critical applications, including the hearing instruments (hearing aids) and the emerging wearable electronics [6, 9, 27].

The block diagram of a Bang-bang CDA is depicted in Figure 2-8. It comprises a Bang-bang Controller (realized by a hysteresis comparator), an output stage, a load with a lowpass filter and a feedback network. The feedback network feeds the noise-shaped output signal back to the input stage. The resultant signal, V_{error}, is the error between the desired output signal and the actual output signal. The Bang-bang controller compares the error signal against a predetermined hysteresis. The controller output changes (switches)

if the error signal exceeds the boundaries (i.e. upper and lower limits) of the hysteresis. The output of the controller is fed to the output stage. The Bang-bang modulated signal is PDM-like – similar to the modulated signal in the asynchronous ΣΔ CDA. As in other CDAs, the amplified input signal is recovered at the load after the lowpass filter.

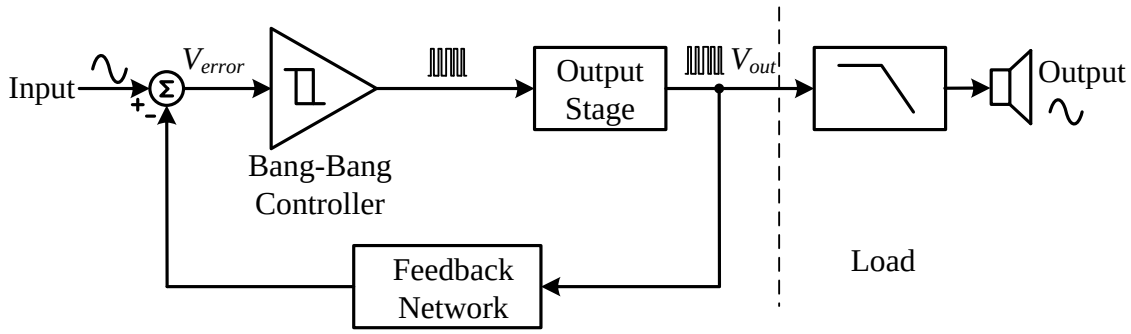


Figure 2-8 Block diagram of a Bang-bang CDA

It can be seen from a comparison between Figure 2-8 and Figure 2-5 that the Bang-bang CDA features much simpler hardware compared to PWM CDAs; ΣΔ CDAs are more complex than both. Specifically, the carrier generator and the integrator that are needed in PWM CDAs are not required in Bang-bang CDAs. The ensuing low quiescent power dissipation is imperative to improve the power-efficiency in some power-critical applications such as hearing instruments [44].

The linearity and the noise-immunity of Bang-bang CDAs have been reported in literature, including the analytical expressions of both THD and PSRR (and PS-IMD) [27]. The analysis and design of Bang-bang CDAs will be discussed in detail in section 2.2.2.

2.1.1.4 Self-Oscillating Class D amplifiers

In addition to the aforementioned modulation schemes, self-oscillating is another modulation scheme employed in CDAs [30, 64-66]. Figure 2-9 depicts the block diagram of a self-oscillating CDA.

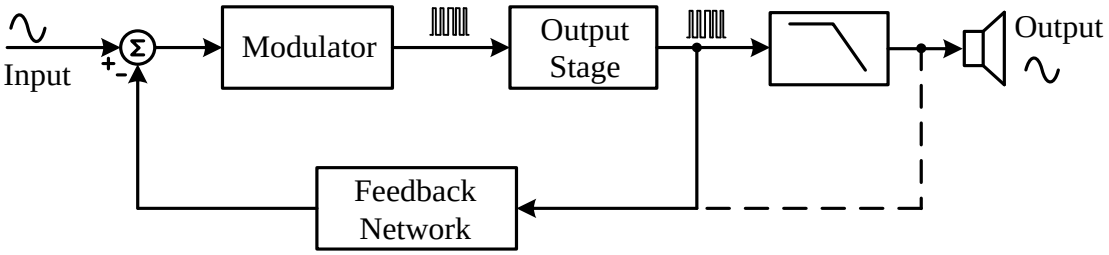


Figure 2-9 Block diagram of a self-oscillating CDA

The modus operandi of a self-oscillating CDA is very similar to that of an oscillator. The oscillation occurs at the frequency where the total phase shift in the feedback loop (that comprises the modulator, the output stage and the feedback network; sometimes the lowpass filter is also included) is 180 degrees. Arguably, one advantage of the self-oscillating CDA is that there is no stability concern as the CDA is (designed) intrinsically unstable.

Recent monolithic implementations of self-oscillating CDAs have demonstrated that, with some clever circuit techniques, self-oscillating CDAs can achieve relatively good linearity and noise-immunity. For instance, a recently reported [54] CMOS self-oscillating CDA features a THD+N of 0.02% and a PSRR of 82 dB. Nevertheless, there are a few drawbacks thereto that prevent wide adoption of self-oscillating CDAs in mobile

applications. For instance, the need to tab the feedback after the lowpass filter undesirably increases the pin count of the monolithic IC, which in turn potentially increases the form factor (as a larger package of a higher pin count may be required).

2.1.2 Class D Amplifier Output Stage

As discussed earlier, the output stage is a critical part in any CDA because it not only occupies a large silicon area but also consumes a significant portion of the total power. For instance, in a reported CDA [49] that drives an 8 Ω loudspeaker load, the output stage therein occupies over 70% of all active area and consumes over 90% of the total power.

In principle, the design of the output stage in CDAs is relatively simple [3] compared to that of modulators. The block diagram of a typical output stage design is depicted in Figure 2-10. The output stage consists of output power transistors, their corresponding drivers, a dead-time circuit, a control circuit and a protection circuit [67] (such as the overcurrent protection circuit). Interestingly, despite the simple schematic design of the output stage, because of its sheer size and power dissipation, it has appreciable effects on various specifications of CDAs. For instance, the dead-time circuit has a marked and direct effect on the reliability and linearity of CDAs [58, 68]. We will now review design techniques and considerations pertaining to the functional blocks in the output stage.

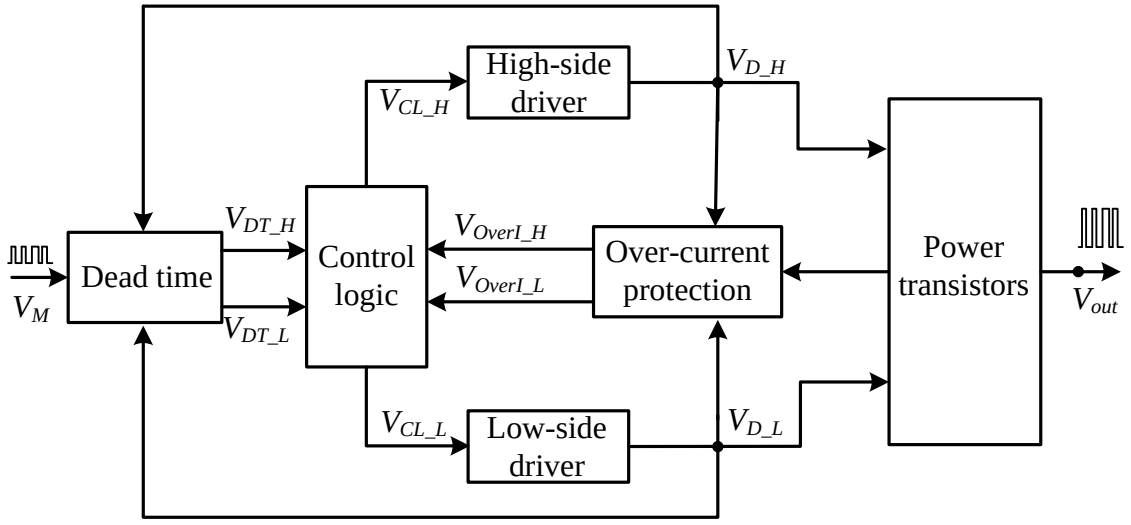


Figure 2-10 Block diagram of a Class D output stage

The Design of Power Transistors and Drivers

The power transistors and their corresponding drivers are normally configured in either *p*-channel-cum-*n*-channel inverter configuration or *n*-channel totem-pole configuration, as depicted in Figure 2-11 (a) and Figure 2-11 (b) respectively.

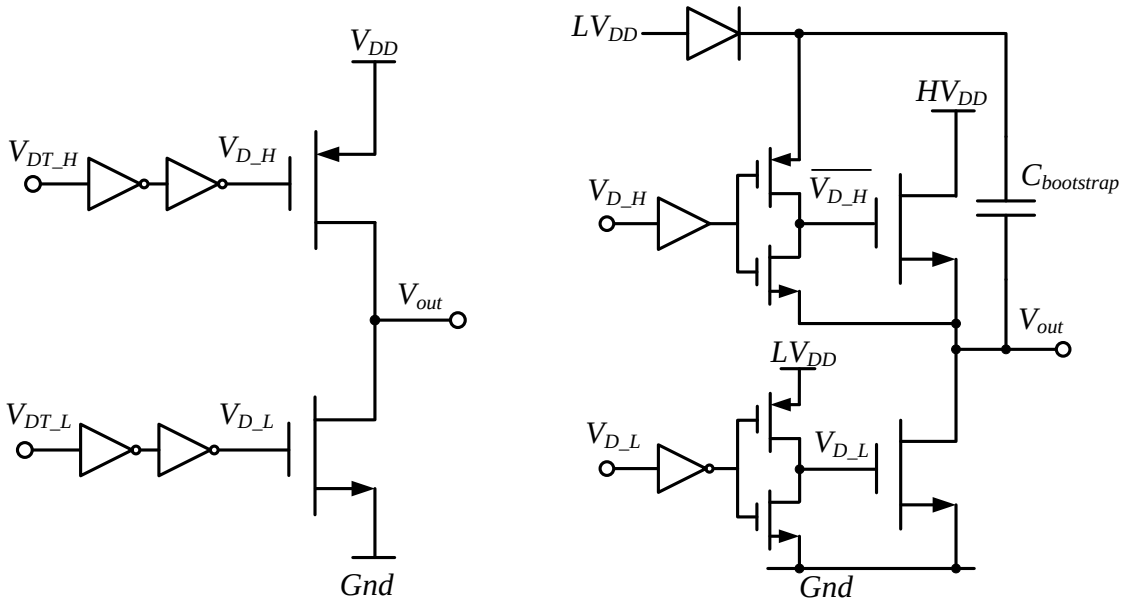


Figure 2-11 Schematic of power transistors and their drivers: (a) *p*-channel-cum-*n*-channel inverter configuration, and (b) *n*-channel totem-pole configuration

Each configuration has its own merits and drawbacks, and they are equally prevalent in particular applications. The primary advantage of the *p*-channel-cum-*n*-channel inverter configuration is its easy implementation and not requiring external components. Its drawbacks, on the other hand, include relatively higher switching power dissipation as the driver signals are in full swing (from *Gnd* to V_{DD}) [4, 20, 69]. Hence, this configuration is often employed in low-to-medium output power (e.g. the output power is less than a few Watts) CDAs where the supply voltage, V_{DD}, is relatively low (e.g. 3.6V). It is therefore appropriate for mobile applications where the supply voltage is low and the form-factor is desired to be small.

On the other hand, the primary advantage of the *n*-channel totem-pole configuration is its lower switching power dissipation when the supply voltage, HV_{DD}, is high (e.g. HV_{DD} = 24 V) in order to deliver larger output power (e.g. the output power is a few tens of Watts or even higher) [70-72]. The lower switching power dissipation is because *n*-type transistors, whose on-impedance is typically 2~3 times lower than *p*-type transistors of the same size, are used for both low-side and high-side power transistors, hence smaller parasitic capacitance. It is also due to the driver signals are not in full swing. Another advantage of the *n*-channel totem-pole configuration is that the size of the output stage is smaller as *p*-type transistors are now replaced with *n*-type, hence a smaller size (width/length of the transistor) is needed to achieve the same on-impedance. Nevertheless, its main drawback is its need of external components.

In view of the merits and drawbacks of said two output stage configurations, and considering the interest of this Ph.D. program that is pertinent to portable electronic devices, the *p*-channel-cum-*n*-channel inverter configuration is adopted. The power dissipation mechanism of this configuration has been reported in literature [3] and the primary power dissipation mechanisms are the on-resistance of the power transistors and the switching power dissipation of the drivers. The design art thereto is also well-established with reported analytical expressions to ascertain the power dissipation and a systematic design/optimization methodology [3].

Dead-time Circuit

The dead-time circuit serves to introduce a small time interval into the output stage control signal to ensure that the two complementary output power transistors (high-side and low-side) will not simultaneously be switched on. This is critical because the on-resistance of said power transistors is so small (e.g. typically in the order of ~0.1 Ω for an 8 Ω load) that, if simultaneously switched on, a low resistance path is formed between the supply and the ground. The consequence is drastic – the ensuing large current is so large that it would not only degrade the power-efficiency, but also potentially damage the output transistors thereat, resulting in an outright device failure. Hence, it is imperative that a dead-time circuit be employed.

An output signal with a dead-time is very similar to that of a non-overlapping clock and its waveform is depicted in Figure 2-12.

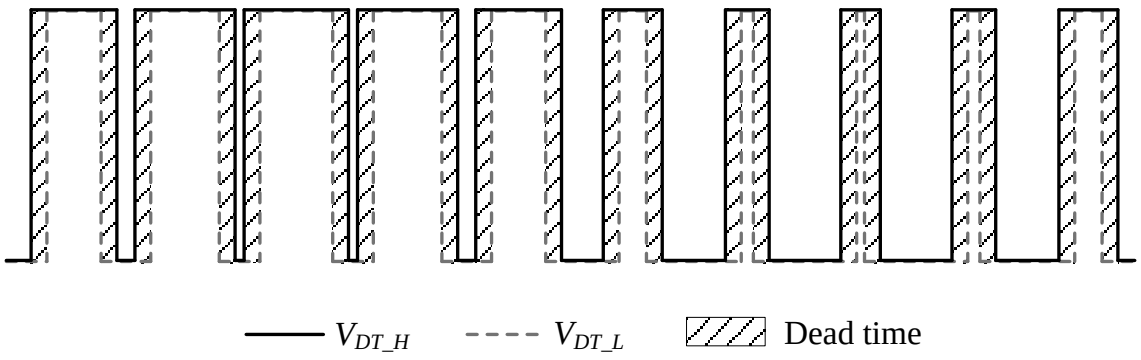


Figure 2-12 Output waveforms of a dead time circuit

The most robust method to introduce the dead-time is probably the non-overlapping logic method (similar to the method of generating a non-overlapping clock signal) [73].

The schematic of said dead-time circuit is depicted in Figure 2-13. The robustness of this design is due to the feedback mechanism thereof – the feedback control circuit ensures that the high-side (or low-side) output power transistor can only be switched on after the low-side (or high-side) power transistor is switched off.

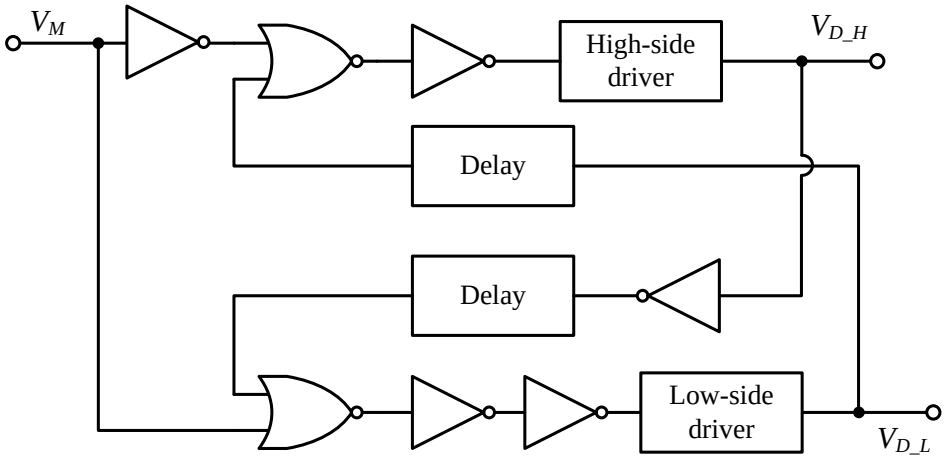


Figure 2-13 Schematic of a dead-time circuit using non-overlapping logic method

For completeness, there are other reported methods to introduce the dead-time into the output stage signal, such as controlling the slewing rate of both the high-side and low-side drivers [74]. Nevertheless, these methods have their individual drawbacks. For instance, said method of controlling the slew rate is sensitive to circuit parameter variances, and therefore are somewhat inappropriate for monolithic realizations.

Protection Circuit

The protection circuit is imperative to the reliability of the output stage. An overcurrent protection circuit is particularly pertinent for CDA output stages as

overcurrent is probably the most common cause of CDA failures – a short-circuit in the connections or an unexpected out-of-range load (or signal) would cause the output transistors conducting a current beyond their safe operating region [67, 75]. Without the overcurrent protection, said output transistors would be damaged, resulting in an outright device failure.

One of the most straightforward methods to realize an overcurrent protection for output power transistors is resistor-based current sensing, as depicted in Figure 2-14 [67]. The modus operandi is very simple – if the current of the power transistors exceeds a predetermined value, $V_{ref}/R_{L(\mathrm{H})}$, an overcurrent signal is generated by the comparator and is sent to the control logic, which would turn off the corresponding overcurrent power transistor.

This design has two drawbacks. First, the resistor therein is in series with the output power transistor. This increases the effective on-resistance of the output stage, which in turn reduces the power-efficiency of the CDA. Second, the accuracy of the current sensing partly depends on the accuracy of the resistance. Integrated resistors typically feature >10% variance, which would compromise the sensing accuracy.

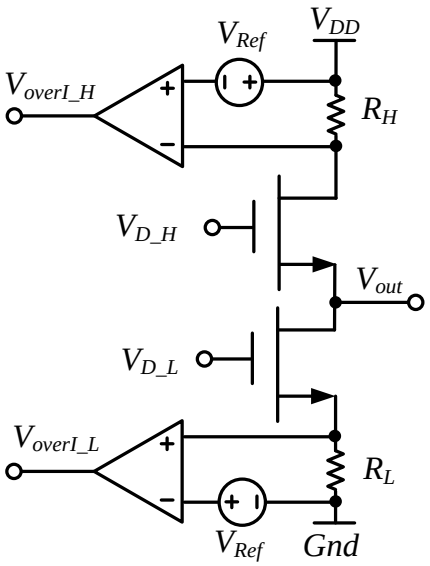


Figure 2-14 Schematic of an overcurrent protection circuit using series resistors [67]

A number of alternative protection circuit designs based current-mirror sensing have been reported in literature [67]. Figure 2-15 depicts the schematic of one of the current-mirror based protection circuits. The primary advantage of this design is its current-mirror based sensing where no additional resistance is introduced into the output power transistors. Hence their operation and efficiency are unaffected. The accuracy of the sensing largely depends on the matching ratio of the current mirrors. The smaller the ratio, the better the matching is, but the cost is slightly larger IC area of the output stage and a more complex layout.

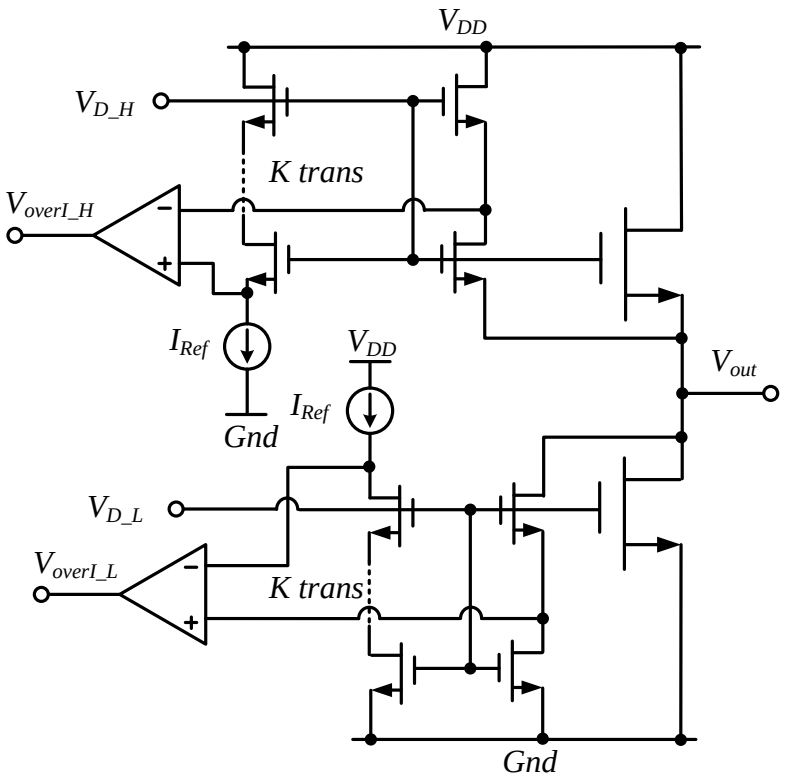


Figure 2-15 Schematic of a current-mirror based overcurrent protection circuit [67]

It is interesting and perhaps not unexpected that the design of overcurrent protection circuits has largely focused on high-power high-voltage applications, and its design for the relatively low-power and micro-power applications are largely based on the same design. The effect of the overcurrent protection circuit on the efficiency of CDAs is largely unreported. To this end, we have found that [44] in some power-critical applications, the power dissipation of the overcurrent protection circuit is very pertinent to the overall power budget and the power-efficiency may be consequently compromised.

2.1.3 Filterless Class D Amplifiers

As discussed earlier, the lowpass filter in the CDAs is typically an *LC* filter comprising an inductor, *L*, and a capacitor, *C*. The filter serves to present high impedance at high frequencies, particularly at the switching frequency and its harmonics, to the output of the CDA, thereby removing the high frequency components from the load. In general, because of the cost of the *LC* filter and the space required (large form-factor) on the Printed-Circuit-Board (PCB), the lowpass filter is undesirable; the inductor-capacitor lowpass filter potentially accounts for ~30% of the cost and ~75% of the PCB area.

To this end, the *filterless* CDAs are now increasingly adopted where their output(s) is directly connected to the load (typically a loudspeaker) without a preceding lowpass filter [76]. Filterless CDAs rely on the parasitic inductance of the loudspeaker (typical dynamic loudspeakers embody some inductance at high frequencies, for instance, an 8 Ω loudspeaker typically embodies an inductance of a few tens of μH) to achieve the same function as a conventional lowpass *LC* filter. Another advantage of the filterless CDA over its filtered counterpart is its potentially higher linearity. It is because the inductor is not perfectly linear, and this slight non-linearity introduces distortion into the output signal. Further, as the inductor(s) is typically not within the feedback loop (for instance, see Figure 2-5 and Figure 2-6), said distortion is not attenuated [76] by negative feedback. Figure 2-21 and Figure 2-22 respectively depict a BTL CDA output stage driving a loudspeaker with an *LC* filter and in a filterless fashion.

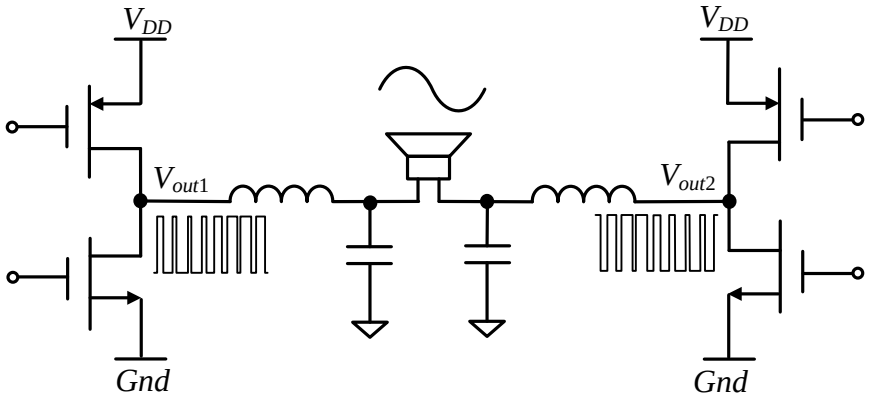


Figure 2-16 A BTL output stage driving a loudspeaker with a conventional lowpass filter

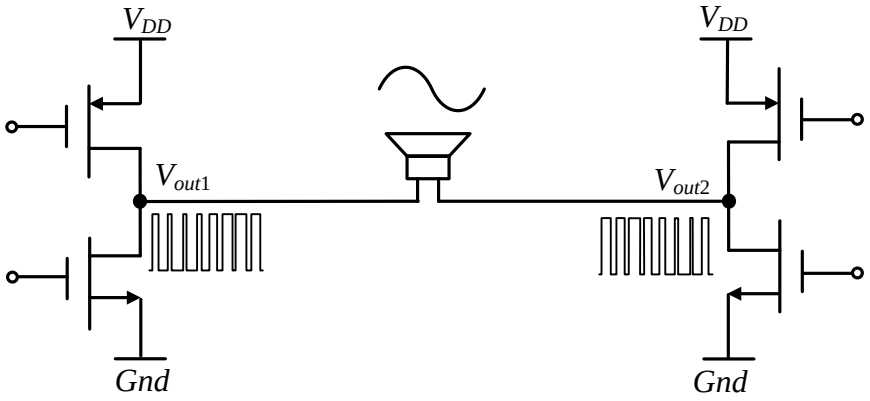


Figure 2-17 A BTL output stage driving a loudspeaker without filter (filterless)

The PWM signals of a filterless BTL CDA are BD modulated [26, 59, 77]. BD modulated PWM signals are also called 3-state (PWM signals), i.e. the differential switching signal across the load has three levels, as depicted in Figure 2-18 (b) where the three levels of the differential signal, $V_{out2} - V_{out1}$, are $+V_{DD}$, *Gnd* (zero) and $-V_{DD}$. On the other hand, the PWM signals of a filtered BTL CDA can be either BD modulated or AD modulated. AD modulated is also called 2-state [26, 59], i.e. the differential switching

signal across the load has two levels, as depicted in Figure 2-18 (a) where the two levels of the differential signal, $V_{out2} - V_{out1}$, are $+V_{DD}$ and $-V_{DD}$. In both AD and BD modulations, the same (low frequency) audio signal is recovered on the load.

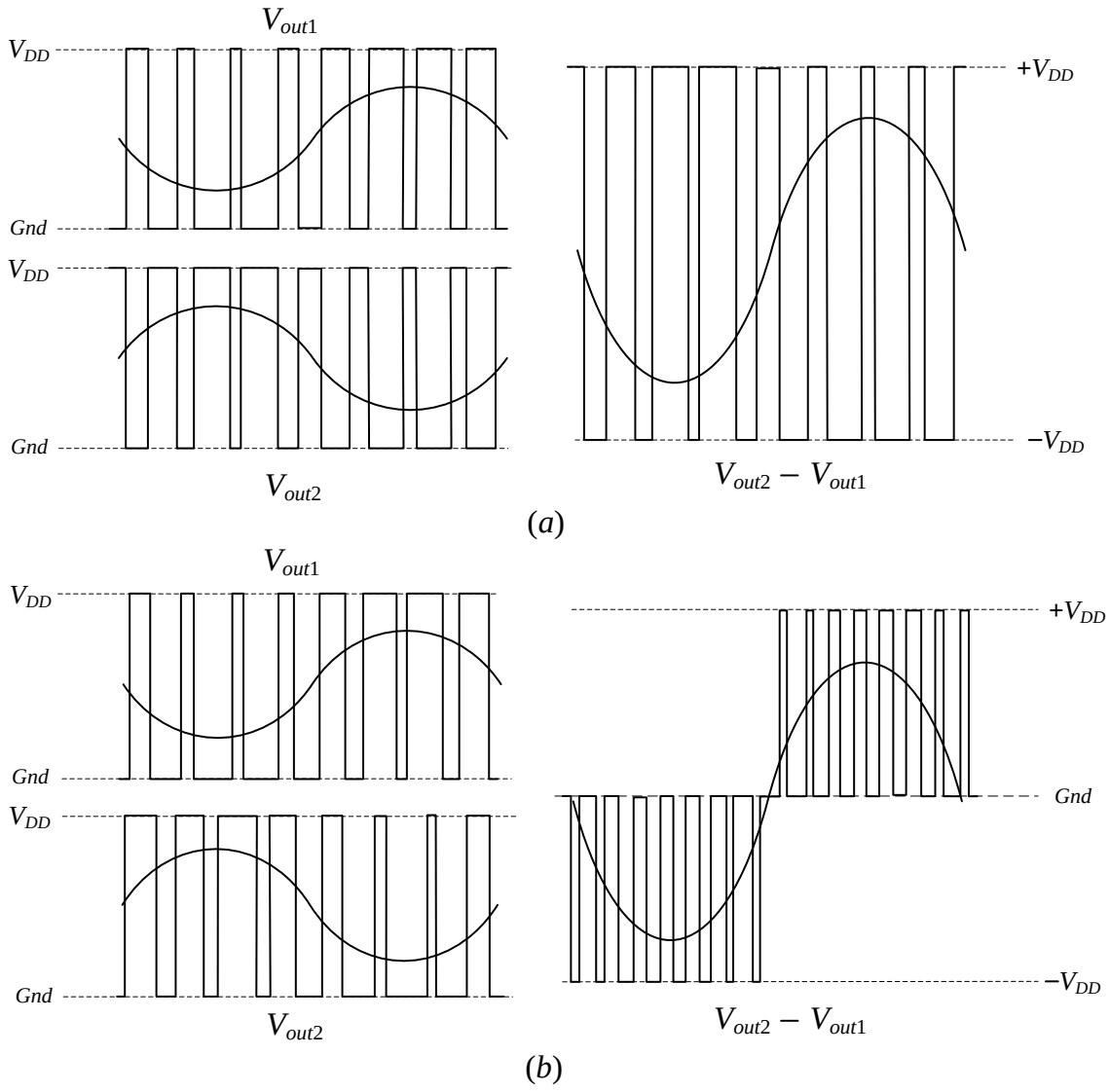


Figure 2-18 PWM output signals with (a) AD modulation and (b) BD modulation

The advantage of using the BD modulation is that the magnitude of the differential switching signal is only half of that in AD modulated PWM signal while the effective switching frequency is doubled, as depicted in Figure 2-18. Put differently, the differential switching component is reduced in magnitude and pushed to a higher frequency. Consequently, the filtering by the parasitic inductance of the loudspeaker would be sufficient.

2.1.3.1 EMI control for filterless Class D Amplifiers

As mentioned earlier, the filterless CDAs, due to their small form-factor and low cost, are now widely and increasingly adopted in portable electronic devices [5, 26, 59]. Nevertheless, the (radiated) EMI of filterless CDAs is probably more severe compared to their filtered counterparts. It is because the EMI arises from the switching operation of the CDA output signal that comprises high frequency components. For CDAs with a filter, said high frequency components are largely attenuated by the filter. However, for filterless CDAs, these high frequency components, despite attenuated by the BD modulation (and inaudible), are still relatively large in magnitude, and they may propagate through the wires and/or PCB traces that connect the CDA output to the loudspeaker. Said connections could inadvertently function as antennas and emit said high frequency components. The emission, or EMI, potentially affects sensitive circuits in the proximity, such as radio frequency low noise amplifiers. It is therefore important for filterless CDAs to limit their EMI emission to a sufficiently low level [21, 24, 69, 78].

There are generally four categories of EMI control techniques for filterless CDAs:

(i) EMI-aware PCB design

To reduce the EMI, the PCB traces and the wires (connecting the CDA outputs and the loudspeaker) should be designed as short as possible [79, 80]. Minimizing the length of the 'antenna' would have some ensuing mitigation effects on the EMI.

(ii) EMI suppression components

Ferrite beads are commonly used for EMI suppression [69]. They can be connected in series between CDA outputs and the loudspeaker, and preferably near to the CDA outputs (ideally right at the output pins). Ferrite beads typically feature very high impedance at high frequency and negligibly small impedance at low frequency, thereby respectively blocking high frequency components propagating in the 'antenna' and not affecting the desired audio-range signal.

(iii) Slew rate control

Unlike (i) and (ii), the slew rate control [80] does not require additional off-chip components or PCB design constraints. It is instead a design technique employed as part of the overall monolithic CDA designs. Specifically, this technique deliberately slows down the switching operation of the output power transistors, typically by using a driver with smaller driving capability (reduced slew rate). Consequently, the output signal will have a substantially smoother transition – the smoother the transition, the lesser the high frequency component – and EMI is therefore reduced.

Nevertheless, this method has two potential drawbacks. First, the slowed transition requires a longer dead-time to avoid short-circuit current, which in turn deteriorates the linearity of the CDA. Second, the slew rate is sensitive to the supply voltage and process variations. It is therefore challenging to precisely control the slew rate in applications, where supply voltage variance is large (for instance in portable electronic applications), and particularly if the CDA is connected directly to the battery terminals (for system design simplicity and for increased power-efficiency).

(iv) Spread-spectrum modulation

Similar to (iii), the spread-spectrum modulation [21] technique is also a design technique employed as part of the overall monolithic CDA designs. This technique modulates the carrier signal (in PWM CDAs) in a way such that the switching frequency of the CDA is not fixed but is instead spread over a relatively wide frequency band. In this manner, the peak emission (due to switching) power is reduced compared to that in the case of the fixed switching frequency where the power is concentrated only at the harmonics of the fixed switching frequency. The effect of the spread-spectrum can be illustrated by Figure 2-19.

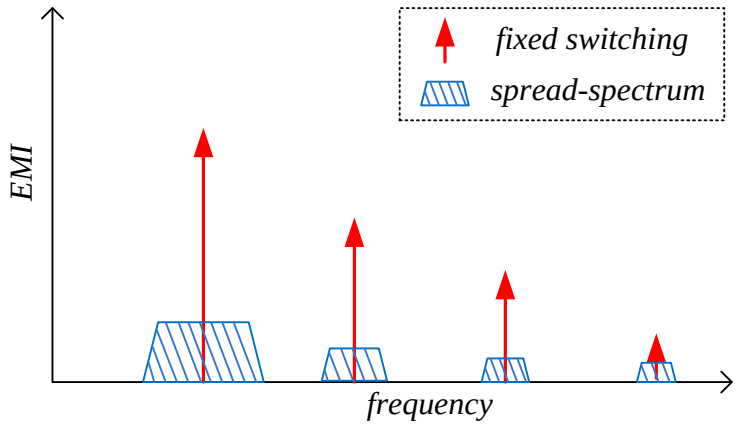


Figure 2-19 EMI of fixed switching and spread-spectrum CDAs

For completeness, the spread-spectrum modulation has its potential drawbacks. The varying switching frequency is essentially a carrier with purposely-introduced jitter noise. If not properly designed, said noise could fold back into the audio band, thereby deteriorating the audio performance, particularly exacerbating the imperative THD+N.

In summary, filterless CDAs are largely preferred due to their smaller footprint and lower cost. Nevertheless, their EMI could potentially interfere with sensitive circuits in their proximity. EMI-aware PCB designs, EMI suppression components, slew rate control and spread-spectrum techniques can, individually and collectively, reduce the EMI of filterless CDAs.

2.2 Analysis and Design of state-of-the-art PWM and Bang-bang Class D Amplifiers

In Section 2.1, a broad review of CDAs was provided and critical functional circuit blocks therein delineated. In view of the interest of this Ph.D. research program, a more in-depth review of the analysis and design of PWM and Bang-bang CDAs, including a number of reported state-of-the-art designs, will now be provided. It would lend some insights into the challenges for the analysis and design of state-of-the-art (and beyond) CDAs, thereby providing a preamble to the contributions delineated in the following chapters.

2.2.1 Analysis and Design of PWM Class D Amplifiers

As mentioned earlier, the next-generation PWM CDAs are expected to feature substantially improved performance including very-low THD+N (e.g. THD+N << 0.01%), very-high PSRR (e.g. PSRR >>80 dB), high power-efficiency (e.g. power-efficiency >90%) and low EMI. There are a number of reported designs that attempt to achieve said improvements.

As a preamble to the discussion of said state-of-the-art designs, that conventional PWM CDAs cannot achieve 'across-the-board' improvements will first be reviewed. The inability to achieve said improvements is largely because some specifications are competing – the improvement of one specification may result in the degradation of

another (for instance, the PSRR and THD can be competing specifications in terms of the loop-gain; see later).

The block diagram of a conventional PWM CDA is depicted in Figure 2-20. It comprises a loop filter, a modulator and a carrier generator, an output stage and a feedback network. The carrier generator therein generates the carrier signal, whose frequency is the switching frequency of the CDA, and it is typically a triangular wave signal of a few hundred kHz. The loop filter, together with the feedback network, determines the loop-gain (i.e. the frequency response) of the closed-loop of the CDA. The selection and design of these two design parameters, the loop-gain and the switching frequency, are of paramount importance because they directly and markedly affect the aforementioned specifications of PWM CDAs. These will now be reviewed in turn.

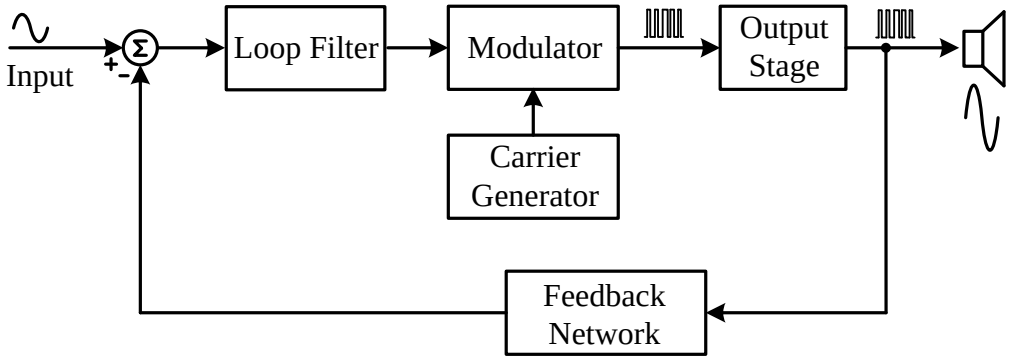


Figure 2-20 Block diagram of a typical PWM CDA

Loop-gain

The effect of loop-gain, *LG*, on the PSRR of CDA is well-established [7, 61] and is relatively straightforward on the basis of the classical negative feedback theory. The

noise injected via the output stage can largely be suppressed by the loop-gain, or specifically, be attenuated by the factor of $1+LG$. To improve the PSRR of CDAs, it is desired to design the loop-gain to be as high as possible.

The effect of the loop-gain on THD, on the other hand, is not as straightforward. As previously mentioned, the THD of PWM CDAs arises from three distinctive mechanisms (open-loop CDA, duty-cycle error and phase error), and the effects of the loop-gain thereto are different and sometimes converse [33, 59]. While the loop-gain can suppress the distortion arising from the open-loop CDA – higher loop-gain results in smaller distortions introduced by the open-loop CDA – the loop gain may have converse effects on the other two mechanisms. Specifically, a higher loop-gain inevitably reduces the attenuation of the switching components in the modulator input signals, and the residual (i.e. not fully attenuated) switching components therein intermodulate with the carrier, thereby causing distortions. Hence, an increased loop-gain might inadvertently increase the THD arising from said duty-cycle error and phase error.

In short, the design considerations for the loop-gain pertaining to THD and PSRR are somewhat competing – opposing high in-band (at the audio frequencies) and high out-of-band (at switching frequencies) attenuation are simultaneously desired. These opposing features are what practical filter designs cannot accommodate without increasing the order of the loop-design, and yet higher-order loop design undesirably increases the hardware complexity and the quiescent power dissipation thereof. In addition, higher order filters potentially incur stability issues and are more susceptible to process variations, and this in turn reduces the manufacturability (lower yields) of the design.

Switching frequency

As mentioned earlier, the switching frequency of PWM CDAs is determined by its carrier generator and its effect on the various specifications of PWM CDAs (including the PSRR, THD, power-efficiency and EMI) are well documented in literature [5, 20, 21, 32, 33, 59]. In generally, a high switching frequency is desired as it leads to lower THD, largely because a higher switching frequency results in larger attenuation of the switching components. However, the higher switching frequency comes with several penalties. This includes the increased switching power dissipation and hence reduced overall power-efficiency, and potentially higher EMI.

In summary, conventional PWM CDA designs involve trade-offs between PSRR, THD, power-efficiency and EMI specifications, and hence the design optimization of loop-gain and switching frequency inevitably incur trade-offs between said specifications. A number of PWM CDA designs that attempt to achieve said optimizations will now be reviewed.

2.2.1.1 A PWM CDA embodying high order loop filter

As aforementioned, one method to simultaneously increase the loop-gain (hence improving the PSRR) and the attenuation of switching components is to use a high order (and often complex) loop filter design. A PWM CDA embodying this method was reported recently and its schematic is depicted in Figure 2-21 [4].

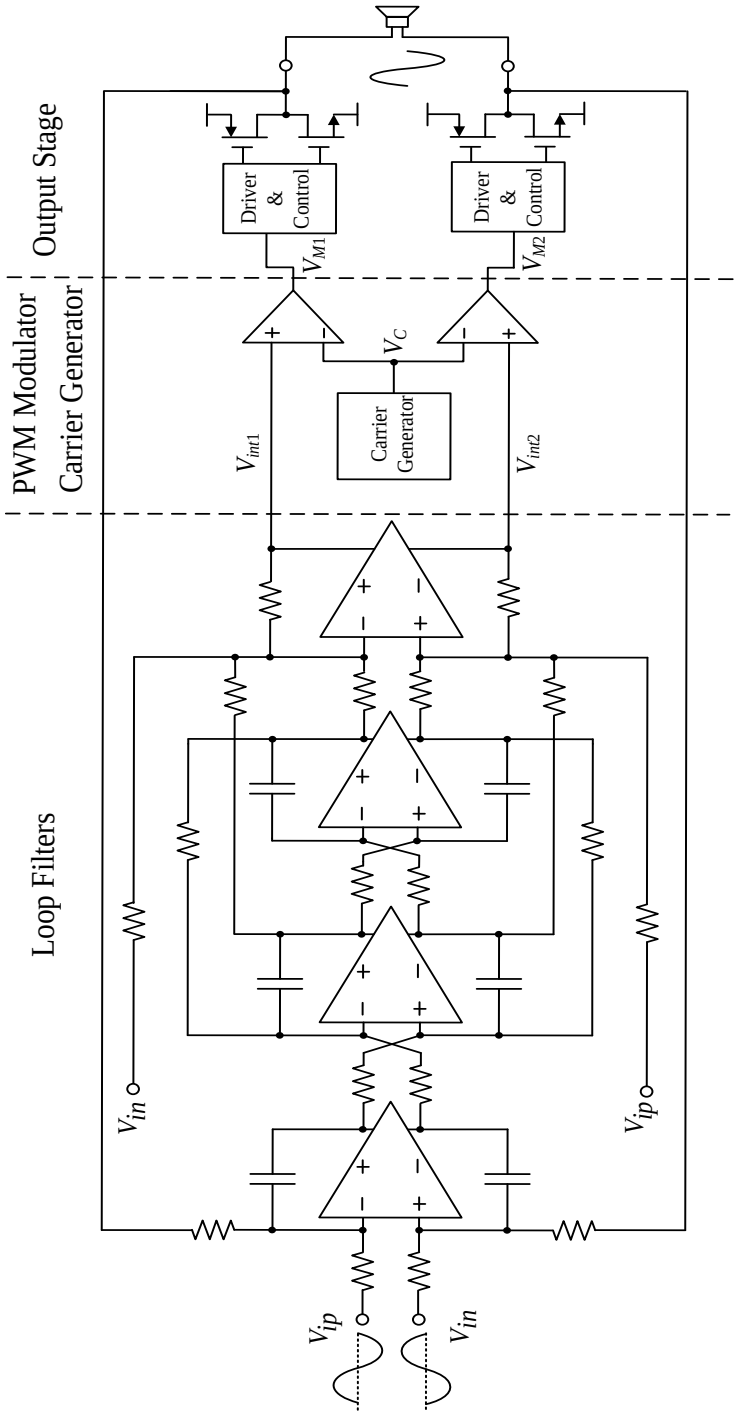


Figure 2-21 Schematic of a PWM CDA embodying high-order loop filters [4]

The loop filter comprises both feedforward and feedback paths, and it is designed to simultaneously achieve high in-band gain and high out-of-band attenuation. Consequently, the CDA embodying this design achieves a high 88 dB PSRR (at 217 Hz) and a low THD+N of 0.018%, with a relatively low switching frequency of 320 kHz. Nevertheless, despite its rather complex loop filter design, it can be argued that there is the inevitable trade-off between the in-band gain and out-of-band attenuation. For example, despite the high loop-gain, the achieved THD+N is 0.018% – insufficiently low to meet the THD+N << 0.01% expected of the *next-generation* PWM CDAs. Moreover, the complex loop filter design is probably susceptible to process variations, as a large number of capacitors and resistors therein makes this design sensitive to the matching (as well as absolute variances) thereof.

2.2.1.2 A PWM CDA with high switching frequency

As reviewed earlier, a high switching frequency is desired to achieve high PSRR and low THD. The potential drawbacks, nevertheless, include increased switching power dissipation of the output stage (due to the parasitic capacitance of drivers and output power transistors therein) and the increased EMI [21] because of the more frequent switching of the output stage.

Higher switching frequency is attractive for CDAs employing small technology nodes (with reduced minimum feature size). Specifically, the shrinking size of CMOS transistors significantly reduces said parasitic capacitors, hence allowing the use of higher

switching frequency without incurring excessive switching losses due to capacitance. In some cases, the switching frequency exceeds 1 MHz. Figure 2-22 depicts the schematic of a (uniform-sampling) PWM CDA with a switching frequency of 1 MHz [20].

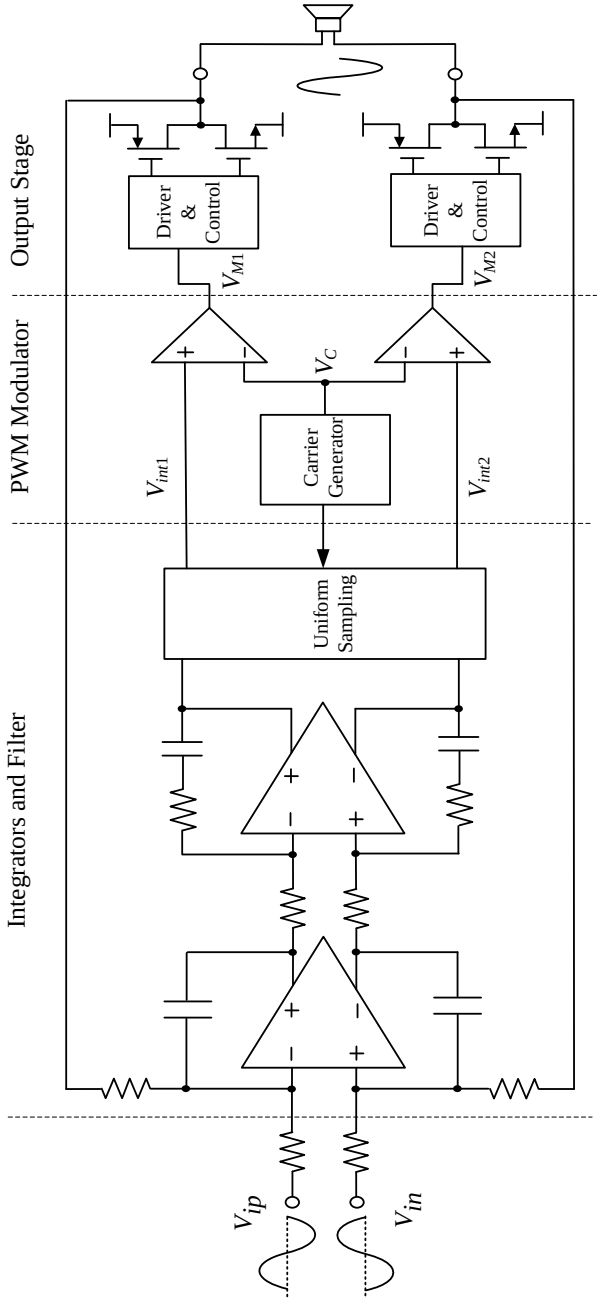


Figure 2-22 Schematic of a PWM CDA of 1 MHz switching frequency [20]

The loop-filter herein is designed to feature very-high gain at low frequencies (in-band frequencies) by cascading two integrators in series. The penalty is reduced attenuation at high frequencies. To achieve sufficiently high attenuation of the switching components at the integrator outputs, two methods were adopted. First, a high switching frequency (1 MHz) is employed – the higher the frequency, the larger is the attenuation because the loop filter gain is more attenuated at higher frequency. Second, a uniform-sampling PWM method is employed, whereby the integrator outputs are sampled at the clocked rate, f_{clk}, thereby creating a notch filtering effect at the $2 \cdot f_{clk}$. As the dominant switching components are also at $2 \cdot f_{clk}$, the attenuation is significantly increased.

This reported CDA design achieves very good performance, featuring a THD+N of 0.0012% and a PSRR of 96 dB while delivering 1.1 W output power to the load. Nevertheless, the high switching frequency inevitably increases the switching power dissipation of the output stage, hence increasing the overall quiescent power dissipation – the total quiescent power is a relatively high 14.4 mW (for V_{DD} = 3.6 V). In addition, the high switching frequency may exacerbate the EMI, which potentially requires EMI suppression components and imposes constraints on the PCB design and layout.

2.2.1.3 A PWM CDA embodying a spread-spectrum carrier generator

The spread-spectrum PWM modulation can be used to reduce the EMI of filterless CDAs, but it could potentially deteriorate THD+N due to the sometimes inadvertent folding back of the noise (of the carrier) into the audio band. Hence it is imperative to

design the carrier generator circuit that simultaneously achieves the spread-spectrum and with minimum noise folding-back.

Figure 2-23 depicts the schematic of a PWM clock modulating circuit, a 5-bit programmable delay line (with another fixed bit) [69]. The CDA embodying this clock modulating circuit achieves a ~11 dB reduction of high frequency spurs, without affecting the audio noise. The idle (with input grounded) integrated noise is a relatively low 28 μV_{rms} (A-weighted) and the maximum Signal-to-Noise Ratio (SNR) is 104 dB, sufficient for general purpose applications. Nevertheless, the potential drawback of this design is its relatively higher THD+N = 0.027% (at 1.1 W). This high THD+N may possibly be due to the varying switching frequency.

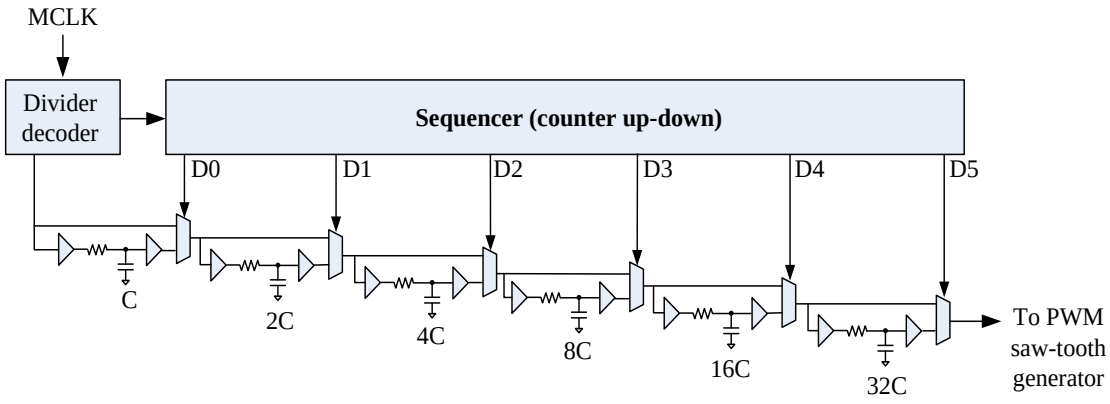


Figure 2-23 Schematic of a 5-bit programmable delay line for clock modulation [69]

In summary, there are a number of reported PWM CDA architectures and design techniques that attempt to improve the imperative specifications of PWM CDAs. However, due to the said inevitable design trade-offs between the various specifications, a

simultaneous improvement of all specifications has not yet been reported. Put simply, a CDA featuring a THD << 0.01% and PSRR >> 80 dB, yet with high power-efficiency and low EMI remains unreported – this is despite these specifications required of *next-generation* electronic devices.

2.2.2 Analysis and Design of Bang-bang Class D Amplifiers

Bang-bang CDAs are somewhat esoteric compared to their PWM counterparts. Unlike PWM CDAs whose analytical investigations reported in literature are largely complete, the analysis of Bang-bang CDAs remains somewhat incomplete. To-date, reported investigations have only analytically investigated two imperative specifications of Bang-bang CDAs, their THD and PSRR [6, 27]. Interestingly, an imperative specification, IMD, remains uninvestigated, including the mechanisms thereof and the circuit parameters affecting the IMD of Bang-bang CDAs.

In general, the performance of the Bang-bang CDA is somewhat inferior to the competing PWM CDA, specifically in terms of the linearity (THD+N) and the noise-immunity (PSRR). Nevertheless, it was reported [27] that in some micropower applications where a high-gain high-bandwidth operational amplifier is not viable due to its typical (relatively) high power consumption, the Bang-bang CDA features a better THD+N and a higher PSRR compared to the PWM CDA. In other words, the Bang-bang CDAs are potentially superior to PWM CDAs with an ultra-low power dissipation

constraint, and are therefore more appropriate for devices and applications with a stringent power budget.

For the design of Bang-bang CDAs, there remain a number of limitations and unknowns. For instance, at this juncture, there is no filterless Bang-bang CDA architecture reported; reported BTL Bang-bang CDAs typically adopt an AD modulation that requires a lowpass filter; see Section 2.1.3 earlier.

In summary, at this juncture, the analysis of Bang-bang CDA remains incomplete, and the design art thereto is relatively nascent compared to its PWM counterparts.

2.3 Conclusions

In this chapter, audio CDAs have been reviewed, including their modus operandi and their fundamental building blocks. Of specific interest, the in-depth review was largely focused on the PWM and Bang-bang CDAs, and it provided an overview of the current design challenges and unknown/unreported mechanisms of imperative specifications. On the basis of this review, it is found that despite the art of CDA design is relatively mature and the analytical investigations largely complete, there remain a number of ambiguities/unknowns and unresolved fundamental design limitations; and some of them will be addressed in Chapters 3-5 in this thesis.

Chapter 3 Bang-bang Class D Amplifiers: Intermodulation Distortion

3.1 Introduction

A large portion of this chapter has been published in IEEE Transactions on Power Electronics [41].

As previously discussed in Chapter 2, the Bang-bang CDA is arguably the most advantageous in power-critical low voltage applications due to its sheer hardware simplicity and the ensuing low power dissipation. Table 3-1 [27] benchmarks the performance of a Bang-bang CDA and a PWM CDA, both designed for the same power-critical low voltage hearing instrument application. It is apparent from this table that compared to the competing PWM CDAs designed for micropower low voltage applications, Bang-bang CDAs feature higher power-efficiency, comparable THD and superior PSRR and PS-IMD.

Table 3-1 Comparison [27] of the Bang-bang CDA and PWM CDA at M=0.15

	Bang-bang CDA*	PWM CDA+
Power-efficiency	50%	35%
THD	0.06%	0.02%
PSRR	60dB	44dB
PS-IMD	-75dB	-45dB

* measurement results + simulation results

The parameters for both CDAs in Table 3-1 are based on the nominal operating conditions, including nominal modulation index, M=0.15, and receiver (typical subminiature loudspeaker) load, R_L=200Ω. The nominal modulation index is relatively low because this is the average signal level in a practical amplifier due to the crest factor of speech and music, and to allow sufficient signal swing overhead margin to avoid signal clipping (otherwise leading to intolerable severe distortion); most reported works conversely report parameters at the maximum modulation index. At M=0.15, the power-efficiency is not unexpectedly lower than for high M, for example M=0.95. In view of the aforesaid and the intended applications, the Bang-bang CDA is the amplifier of interest in this chapter.

Interestingly, at this juncture, unlike the competing PWM CDAs, the nonlinearities of Bang-bang CDAs have yet to be thoroughly investigated. Specifically, to the best of our knowledge, the intermodulation distortion, IMD (eqn. (3.1) below) of Bang-bang CDAs remains uninvestigated/unreported and the mechanisms thereof are unknown – as universally accepted and specified by AES [81], IMD is an important parameter and is typically quoted in specifications pertaining to high-fidelity. As the modulation involved in Bang-bang CDAs is different from PWM CDAs [28], the mechanisms of IMD are as

expected different; see later.

IMD is a distortion measure for an input signal comprising two or more frequency components, defined by the Society of Motion Picture and Television Engineers (SMPTE) [1] as:

$$\%\text{IMD} = \frac{\sqrt{\sum_{n=1}^{\infty}\sum_{m=1}^{\infty}[V_o(mf_1 + nf_2) + V_o(mf_1 - nf_2)]^2}}{V_o(f_2)} \times 100\% \quad (3.1)$$

where the ideal output voltage is $V_o(f_1) = 4V_o(f_2)$ at input frequencies f_1 =60Hz and f_2 = 7kHz.

In this chapter, we will investigate the IMD of Bang-bang CDAs and derive the analytical expressions thereto. These expressions are useful and significant as they not only depict the mechanisms of IMD but also provide insights to the design of Bang-bang CDAs, including compromises and trade-off of other parameters with respect to IMD. Of specific interest, the derivations show that the even-order IMD (particularly 2nd-order, i.e. m=1 and n=1 in eqn. (3.1)) may be dominant in some operating conditions vis-à-vis only 3rd-order IMD components (i.e. m=2, n=1 or m=1, n=2 in eqn. (3.1)) in reported CDAs and linear amps. These findings are interesting and somewhat unexpected because the even-order IMD is usually insignificant/unreported in amplifier designs. The analytical work herein is verified by HSPICE simulations and on the basis of measurements on a physical Bang-bang CDA embodying an output stage IC.

The chapter is organized as the following manner. In section 3.2, the operation of an ideal Bang-bang CDA is described and the IMD expressions thereof derived. In section

3.3, the non-idealities of a practical Bang-bang CDA are investigated and the ensuing analytical expressions for odd-order and even-order IMD are derived and discussed. In section 3.4, the derived expressions are verified by HSPICE simulations and on the basis of measurements on a physical Bang-bang CDA. Finally, the conclusions are drawn in section 3.5.

3.2 IMD of an ideal Bang-bang CDA

In this section, the IMD of an ideal Bang-bang CDA is investigated and this serves as a preamble for the investigation into the IMD of practical Bang-bang CDAs in the next section. In this section, mathematical expressions for the IMD of the ideal Bang-bang CDA will be derived in Section 3.2.1. The interpretation of derived expressions and investigations on IMD will be delineated in Section 3.2.2. Readers can skip the derivations (section 3.2.2) if his/her interests are primarily on the amplifier designs and optimizations.

Figure 3-1 depicts the block diagram of a Bang-bang CDA – the hardware is very simple, comprising a Bang-bang controller (a hysteresis comparator), an output stage, a feedback network (realized by a simple *RC* network comprising $R_{in,}$ R_{fb} and C) and a load with a preceding low pass L_LC_L filter. The hysteresis comparator compares the 'error' signal V_e at its inverting input terminal against the predetermined hysteresis ($\pm V_h$), and generates a switching signal, V_B, to the output stage. The output stage provides current to drive the load (typically the subminiature loudspeaker (receiver) in a hearing aid). The

output stage comprises a driver stage (that comprises a chain of inverters with increasing aspect ratios) and a pair of output transistors.

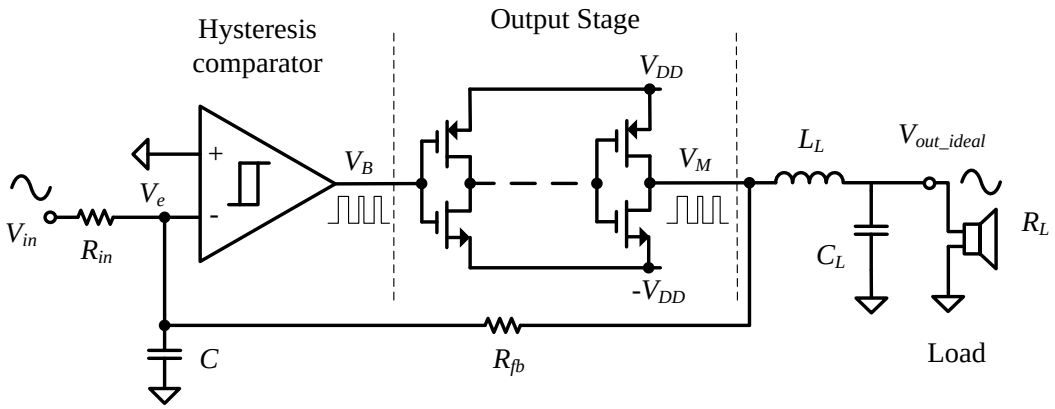


Figure 3-1 Block diagram of the Bang-bang CDA

The 'ideal' Bang-bang CDA assumes that all building blocks therein are ideal, including the hysteresis comparator whose delay t_D=0s, and the output stage whose output on-resistance R_{on}=0Ω. To investigate the IMD, we will now derive the expression for the output of the ideal Bang-bang CDA when the input V_{in} comprising two frequency components at f_1 and f_2, and hence the expression for IMD. For the following derivations, we assume that the input is constant within each switching cycle. This approximation barely compromises the accuracy of the ensuing derivations because the switching frequency is typically >10~20 times higher than maximum input signal frequency.

3.2.1Modeling and Derivations for the IMD of an ideal Bang-bang CDA

For an ideal Bang-bang CDA, an input V_{in} comprising two frequency components at

f_1 and f_2 can be expressed as:

$$V_{in}(t) = -\frac{R_{in}}{R_{fb}}(M_1 \sin(2\pi f_1 t) + M_2 \sin(2\pi f_2 t))V_{DD} \tag{3.2}$$

where M_1 and M_2 are the respective modulation index of the input signal whose frequencies are f_1 and f_2 – the modulation index of a signal is its normalized output amplitude with respect to the supply voltage. The representation of the input as eqn. (3.2) is to facilitate the following analysis.

In each switching cycle, we define t_{on} is the "on" time interval when output is V_{DD}, and t_{off} is the "off" time interval when output is $-V_{DD}$. Note that t_{on} and t_{off} are dependent on the input signals within each switching cycle. The input signals are changing in the time domain and are functions of time. Hence, t_{on} and t_{off} are functions of time. On the basis of Figure 3-1, t_{on} is also the time interval during which V_e increases from $-V_h$ to $+V_h$. By deriving the expressions of V_e when t=0 and V_e=$-V_h$ and when t= t_{on} and V_e=$+V_h$, the following equation can be derived.

$$V_h = \frac{1}{\omega_p}\left(\frac{V_{in}}{R_{in}C} + \frac{V_{DD}}{R_{fb}C}\right) - e^{-\omega_p t_{on}}\left[V_h + \frac{1}{\omega_p}\left(\frac{V_{in}}{R_{in}C} + \frac{V_{DD}}{R_{fb}C}\right)\right] \tag{3.3}$$

where ω_p is the corner frequency of the *RC* feedback network; see eqn. (3.12f) later .t_{off} is the time interval during which V_e decreases from $+V_h$ to $-V_h$, and the following equation can be derived:

$$-V_h = \frac{1}{\omega_p}\left(\frac{V_{in}}{R_{in}C} - \frac{V_{DD}}{R_{fb}C}\right) - e^{-\omega_p t_{off}}\left[-V_h + \frac{1}{\omega_p}\left(\frac{V_{in}}{R_{in}C} - \frac{V_{DD}}{R_{fb}C}\right)\right] \tag{3.4}$$

Within a switching cycle (comprising a t_{off} and a t_{on}) that starts at $t=t_n$ and ends at $t=t_{n+1}$, we assume that the input signal is constant and is $V_{in}(t_n)$. Hence, by substituting eqn. (3.2) into eqns. (3.3) and (3.4), $t_{on,n}$ and $t_{off,n}$ in this switching cycle (between $t=t_n$ and $t=t_{n+1}$) can be expressed as:

$$t_{on,n} = \frac{1}{\omega_p} ln\left[\frac{V_{DD} + GV_{in}(t_n) + V_{DD}(1+G)h}{V_{DD} + GV_{in}(t_n) - V_{DD}(1+G)h}\right] \tag{3.5a}$$

$$t_{off,n} = \frac{1}{\omega_p} ln\left[\frac{V_{DD} - GV_{in}(t_n) + V_{DD}(1+G)h}{V_{DD} - GV_{in}(t_n) - V_{DD}(1+G)h}\right] \tag{3.5b}$$

Based on the assumption that each switching cycle is infinitesimal in time, the series of discreet t_{on} and t_{off} time intervals can be approximated as continuous-time signals, as shown in eqns. (3.6a) and (3.6b):

$$\begin{aligned} t_{on} &= \frac{1}{\omega_p} ln\left[\frac{V_{DD} + GV_{in}(t) + V_{DD}(1+G)h}{V_{DD} + GV_{in}(t) - V_{DD}(1+G)h}\right] \\ &= \frac{1}{\omega_p} ln\left[\frac{1 - (m_1+m_2) + (1+G)h}{1 - (m_1+m_2) - (1+G)h}\right] \end{aligned} \tag{3.6a}$$

$$\begin{aligned} t_{off} &= \frac{1}{\omega_p} ln\left[\frac{V_{DD} - GV_{in}(t) + V_{DD}(1+G)h}{V_{DD} - GV_{in}(t) - V_{DD}(1+G)h}\right] \\ &= \frac{1}{\omega_p} ln\left[\frac{1 + (m_1+m_2) + (1+G)h}{1 + (m_1+m_2) - (1+G)h}\right] \end{aligned} \tag{3.6b}$$

$$m_1 = M_1 \sin(2\pi f_1 t) \tag{3.7a}$$

$$m_2 = M_2 \sin(2\pi f_2 t) \tag{3.7b}$$

where $h=V_h/V_{DD}$ is the normalized hysteresis of the hysteresis comparator, $G=R_{fb}/R_{in}$ the closed-loop gain of the Bang-bang CDA. M_1 and M_2 is the respective modulation index of the signals m_1 and m_2.

The output signal of the ideal Bang-bang CDA, V_{out_ideal}, can be derived by taking the average signal over one switching period. Based on eqns. (3.5)-(3.7) and Taylor expansion of t_{on} and t_{off}, V_{out_ideal} can be derived as:

$$V_{out_{ideal}} = \frac{t_{on} - t_{off}}{t_{on} + t_{off}} V_{DD} \tag{3.8a}$$

Based on Taylor Expansion, t_{on} can be expressed as:

$$t_{on} = \frac{1}{\omega_p} \times 2 \left\{ \left[\frac{1}{1} \left(\frac{(1+G)h}{1-(m_1+m_2)} \right)^1 \right] + \left[\frac{1}{3} \left(\frac{(1+G)h}{1-(m_1+m_2)} \right)^3 \right] + \left[\frac{1}{5} \left(\frac{(1+G)h}{1-(m_1+m_2)} \right)^5 \right] + \left[\frac{1}{7} \left(\frac{(1+G)h}{1-(m_1+m_2)} \right)^7 \right] + \cdots \right\} \tag{3.8b}$$

$$t_{on} \approx \frac{2}{\omega_p} \times \left\{ \left[\frac{1}{1} \left(\frac{(1+G)h}{1-(m_1+m_2)} \right)^1 \right] + \left[\frac{1}{3} \left(\frac{(1+G)h}{1-(m_1+m_2)} \right)^3 \right] \right\} \tag{3.8c}$$

As shown in eqns. (3.8b) and (3.8c), the higher order terms from the 5th-order onwards have been truncated in expansions of t_{on}. Similarly, t_{off} can be approximated as:

$$t_{off} \approx \frac{2}{\omega_p} \times \left\{ \left[\frac{1}{1} \left(\frac{(1+G)h}{1+(m_1+m_2)} \right)^1 \right] + \left[\frac{1}{3} \left(\frac{(1+G)h}{1+(m_1+m_2)} \right)^3 \right] \right\} \tag{3.8d}$$

Substitute the eqn. (3.8c) and (3.8d) into eqn. (3.8a), we have:

$$V_{out_{ideal}}/V_{DD}$$

$$\approx \frac{\left[\frac{(1+G)h}{1-(m_1+m_2)} + \frac{1}{3} \left(\frac{(1+G)h}{1-(m_1+m_2)} \right)^3 \right] - \left[\frac{(1+G)h}{1+(m_1+m_2)} + \frac{1}{3} \left(\frac{(1+G)h}{1+(m_1+m_2)} \right)^3 \right]}{\left[\frac{(1+G)h}{1-(m_1+m_2)} + \frac{1}{3} \left(\frac{(1+G)h}{1-(m_1+m_2)} \right)^3 \right] + \left[\frac{(1+G)h}{1+(m_1+m_2)} + \frac{1}{3} \left(\frac{(1+G)h}{1+(m_1+m_2)} \right)^3 \right]} \tag{3.8e}$$

After some algebraic manipulations, the output signal can be approximated as eqn. (3.8f):

$$V_{out_{ideal}} \cong \left\{ (m_1+m_2) + \frac{2[(1+G)h]^2}{3} \sum_{k=0}^{+\infty} [(m_1+m_2)]^{2k+1} \right\} V_{DD} \tag{3.8f}$$

$$= (m_1+m_2)V_{DD} + V_{m\pm n}\, sin(2\pi(mf_1 \pm nf_2)t) + V_{THD} \tag{3.8g}$$

where in eqn. (3.8g) the first item is the desired output, the second item is the IMD component and V_{THD} is the THD. $V_{m\pm n}$ the magnitude of $(m+n)^{th}$-order IMD component at $mf_1 \pm nf_2$ for m,n =1,2,3… Note that eqns. (3.8f) and (3.8g) comprise all non-linearities (including the IMD), and the IMDs can be extracted therefrom. Specifically, the IMD includes all the terms comprising both m_1^m and m_2^n. Hence, from eqns. (3.8f) and (3.8g), and considering the filtering effects of both the load filter and the feedback networks on high-frequency components, the IMD in eqn. (3.8g) can be further expressed as in eqn. (3.9):

$$V_{m\pm n}\, sin(2\pi(mf_1 \pm nf_2)t)$$

$$= \frac{2}{3}[(1+G)h]^2 \sum_{i=1}^{\infty} \sum_{j=2}^{j=i+1} \binom{2i+1}{j} {m_1}^{2i+1-j} {m_2}^{j} H(f)F(f)\, V_{DD} \tag{3.9}$$

where f is the frequency, and $H(f)$ and $F(f)$ the respective magnitudes of the frequency response of the low pass filter and feedback network; see eqns. (3.12d) and (3.12e) later.

Using the trigonometric functions and multinomial expansion, each IMD component can be derived individually. Only 3rd-order IMD is derived in eqns. (3.10a), (3.10b) & (3.11) as higher order IMD components are insignificant compared to 3rd-order IMD component. It is because the magnitude of the IMD component exponentially decreases as its order increases. For instance, when M=0.15, 5th-order IMD component is over 30dB smaller than 3rd-order IMD component.

$$V_3(2f_1 \pm f_2) = \frac{2}{3}[(1+G)h]^2 H(2f_1 \pm f_2)F(2f_1 \pm f_2)C_{oeff}V_{DD} \tag{3.10a}$$

where

$$C_{oeff}$$

$$= \sum_{\substack{coefficient\ of \\ \sin(2f_1 \pm f_2)}} \sum_{i=1}^{\infty} \sum_{j=2}^{j=i+1} \left[\binom{2i+1}{j} (M_1\, sin(2\pi f_1 t))^{2i+1-j} (M_2\, sin(2\pi f_2 t))^{j} \right] \tag{3.10b}$$

C_{oeff} is the sum of all the coefficients of the terms comprising $\sin(2f_1 \pm f_2)$ in eqn. (3.10b), and can therefore be derived based on polynomial expansions of eqn. (3.10b):

$$C_{oeff} = \sum_{i=1}^{\infty}\sum_{j=2}^{i+1}\left[\left(\frac{1}{2}\right)^{2i}\binom{2i+1-j}{j-2}\binom{2i+3-2j}{i+1-j}\binom{2i+1}{j}{M_1}^{2j-2}{M_2}^{2i+3-2j}\right] \quad (3.11)$$

The IMD component $V_3(f_1+2f_2)$ can be similarly derived.

3.2.2IMD of an ideal Bang-bang CDA

Based on the derivation methods delineated above, the analytical expression for the 3rd-order IMD of an ideal Bang-bang CDA can be derived as:

$$\begin{aligned} &V_{3^{rd}\text{IMD,ideal}}(t) \\ &= V_3(2f_1+f_2)\sin(2\pi(2f_1+f_2)t) + V_3(2f_1-f_2)\sin(2\pi(2f_1-f_2)t) + \\ &\quad V_3(f_2+2f_1)\sin(2\pi(f_2+2f_1)t) + V_3(f_2-2f_1)\sin(2\pi(f_2-2f_1)t) \end{aligned} \quad (3.12a)$$

where

$$\begin{aligned} &V_3(2f_1 \pm f_2) \\ &= \frac{2}{3}[h(1+G)]^2 F(2f_1 \pm f_2)H(2f_1 \pm f_2)V_{DD} \\ &\times \sum_{i=1}^{\infty}\sum_{j=2}^{i+1}\left(\frac{1}{2}\right)^{2i}\binom{2i+1}{j}\binom{2i+1-j}{j-2}\binom{2i+3-2j}{i+1-j}{M_1}^{2j-2}{M_2}^{2i+3-2j} \end{aligned} \quad (3.12b)$$

$$V_3(f_1 \pm 2f_2)$$

$$= \frac{2}{3}[h(1+G)]^2 F(f_1 \pm 2f_2) H(f_1 \pm 2f_2) V_{DD} \times \sum_{i=1}^{\infty} \sum_{j=2}^{i+1} \left(\frac{1}{2}\right)^{2i} \binom{2i+1}{j} \binom{2i+1-j}{j-2} \binom{2i+3-2j}{i+1-j} {M_2}^{2j-2} {M_1}^{2i+3-2j} \quad (3.12c)$$

$$F(f) = \left|1 + j2\pi \frac{f}{\omega_p}\right| \quad (3.12d)$$

$$H(f) = \left|\frac{1}{1 + j2\pi f \frac{L_L}{R_L} - 4\pi^2 L_L C_L f^2}\right| \quad (3.12e)$$

$$\omega_p = \left(\frac{R_{in} R_{fb}}{R_{in} + R_{fb}} C\right)^{-1} \quad (3.12f)$$

Note that only odd-order IMD components exist, that is there is no even-order IMD component; this is expected as this phenomenon is likewise observed in PWM CDA and other amps.

From eqns. (3.12a)-(3.12f), it can be observed that the primary parameters that affect the odd-order IMD include the modulation indexes (M_1 and M_2), hysteresis (h), closed-loop gain (G) and the corner frequency (ω_p) of the feedback network. The effect of these parameters will now be delineated in turn.

(i) Modulation Indexes, M_1 and M_2

If either (or both) the modulation index, M_1 and M_2, increases, the IMD increases. This observation is similar to that observed for PWM CDAs and for linear amps.

(ii) Hysteresis, *h*

The lower the hysteresis, the lower is the IMD – eqns. (3.12a)-(3.12c) show that *h* has a quadratic effect on IMD. This is primarily because *h* determines V_e, the 'error' signal which is the difference between the input signal and the output signal. Specifically, the lower the *h*, the smaller is the V_e, (thereby a lower IMD), and the converse is true. For example, it will be shown later in Figure 3-5 that by reducing *h* from 0.05 to 0.025, the IMD is reduced very significantly – by ~75% over the entire modulation index range. However, from a practical perspective, the ensuing cost is increased power dissipation in the output stage due to increased switching frequency. Nevertheless, despite the increased switching frequency, it has been shown that for micropower low voltage applications, the power dissipation of the Bang-bang CDA remains substantially lower than other amps, including the PWM CDAs.

(iii) Closed-loop gain, *G*

Similar to *h*, a smaller *G* results in a lower IMD. For example, it will be shown later in Figure 3-6 that reducing *G* from 2 to 1 leads to a significant ~50% IMD reduction. However, as in aforesaid (ii), there are practical considerations. For example, reducing *G* to <1 is not recommended as the maximum modulation index is reduced (before signal clipping), thereby limiting the maximum output power of the Bang-bang CDA. In our experience, *G*=1 is a good tradeoff. For completeness, if a higher overall gain of the Bang-bang CDA is desired (for a given *G*), a pre-amp may be employed at the cost of increased hardware complexity and power dissipation.

(iv) Corner frequency, ω_p

The effect of ω_p on the IMD is largely insignificant. Nevertheless, from an overall design perspective, ω_p affects the switching frequency of the Bang-bang CDA and other linearities, including THD, PS-IMD, PSRR; the zero-input switching frequency is given later in eqn. (5.15d). In our experience, ω_p set to between the bandwidth (BW) to 1.5BW of the Bang-bang CDA is a good compromise.

In summary, only the odd-order IMD is present in ideal Bang-bang CDAs, and the even-order IMD is zero. To obtain a low IMD, it is recommended that both h and G be low, and in the perspective of overall CDA parameters, G=1 and BW<ω_p<1.5BW are a good compromise.

3.3 IMD of a Practical Bang-bang CDA

Following the analysis of the IMD of the ideal Bang-bang CDA, in this section, the IMD of a practical Bang-bang CDA will now be investigated and analytical expressions thereof derived. Figure 3-2 depicts a practical Bang-bang CDA with the following non-ideal circuit parameters:

(i) Non-zero t_D, the delay time of the hysteresis comparator;

(ii) Non-zero R_{on}, the output on-resistance of the output stage;

(iii) Hysteresis mismatch h_{OS}, the normalized hysteresis mismatch ($h_{OS}=V_{OS}/V_{DD}$) arising from the input DC offset V_{OS} of the hysteresis comparator; and

(iv) Power supply mismatch k, the non-zero power supply mismatch coefficient where the positive supply is $(1+k)V_{DD}$ and negative supply is $-V_{DD}$; $k<<1$.

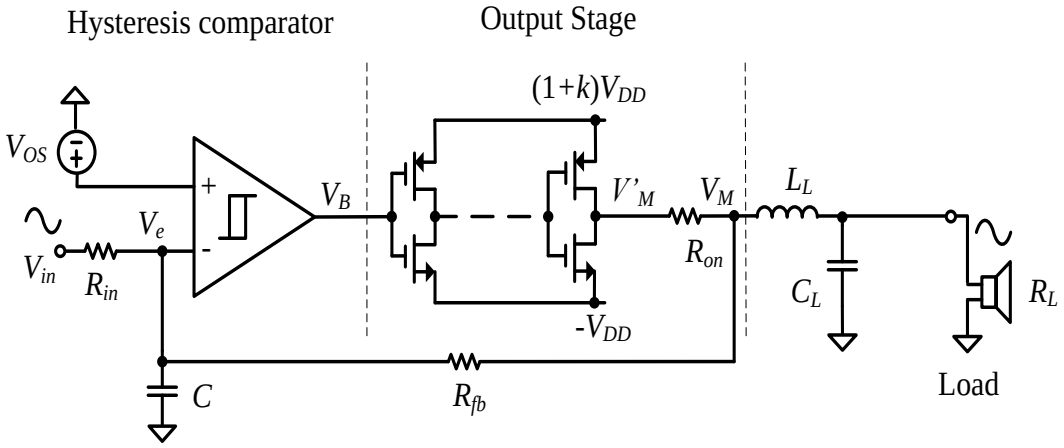


Figure 3-2 Block diagram of the practical Bang-Bang CDA

Unlike the ideal Bang-bang CDA, the IMD of the practical Bang-bang CDA comprises two distinct order-types, odd-order IMD and even-order IMD. The mechanism of odd-order IMD of the practical Bang-bang CDA is as that delineated for the ideal Bang-bang CDA, and we will later show that the magnitude of the odd-order IMD is affected by the t_D and R_{on} non-idealities and that the non-idealities of mismatch has no effect thereto. The mechanisms of the even-order IMD, on the other hand, are the mismatch h_{OS} and k non-idealities that are inherent in the practical Bang-bang CDA; the magnitude of even-order IMD is also affected by the t_D and R_{on} non-idealities – as the case of the odd-order IMD. We now investigate the effect of aforesaid non-idealities (i)-(iv) on the practical Bang-bang CDA and derive analytical expressions for the ensuing IMD.

As a consequence of the aforesaid non-idealities (i)-(iv), the 'error' signal V_e that

was earlier confined to within $\pm V_h$ in the ideal Bang-bang CDA, now swings in an extended region – between upper bound V_{h+} and lower bound V_{h-}. This is depicted in Figure 3-3. We derive the expressions for V_{h+} and V_{h-}:

$$V_{h+} = (V_h + V_{OS})e^{-t_D\omega_p} + \frac{V_{DD}}{1+G}(1 - e^{-t_D\omega_p})\left[1 + k - \left(1 + \frac{R_{on}}{R_L}\right)(M_1 \sin(2\pi f_1 t) + M_2 \sin(2\pi f_2 t))\right] \quad (3.13a)$$

$$V_{h-} = -(V_h - V_{OS})e^{-t_D\omega_p} - \frac{V_{DD}}{1+G}(1 - e^{-t_D\omega_p})\left[1 + \left(1 + \frac{R_{on}}{R_L}\right)(M_1 \sin(2\pi f_1 t) + M_2 \sin(2\pi f_2 t))\right] \quad (3.13b)$$

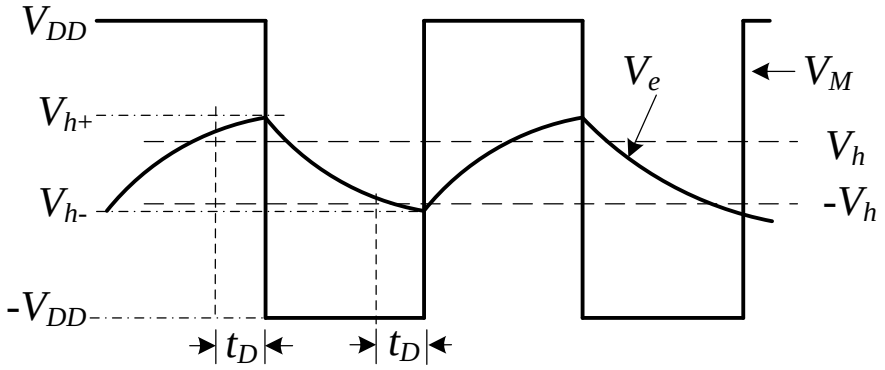


Figure 3-3 Waveforms of a practical Bang-bang CDA

Using the eqns. (3.13a) and (3.13b) and the same derivation method for the ideal Bang-bang CDA delineated earlier, we derive the analytical expressions for the IMD of the practical Bang-bang CDA:

$$V_{\mathrm{IMD},prac} = \left[V_{3^{rd}\mathrm{IMD},prac}(t) + V_{5^{th}\mathrm{IMD},prac}(t) + \cdots\right] + \left[V_{2^{nd}\mathrm{IMD},prac}(t) + V_{4^{th}\mathrm{IMD},prac}(t) + \cdots\right] \tag{3.14}$$

where the terms within the first parenthesis are the odd-order (3rd, 5th, 7th, …) IMD components and the terms within the second parenthesis are the even-order (2nd, 4th, 6th, …) IMD components.

Of the odd-order IMD components of the practical Bang-bang CDA in eqn. (14), the dominant component is the 3rd-order, and the higher odd-order terms are insignificant and can hence be neglected; this is as in the case of the ideal Bang-bang CDA. The 3rd-order IMD of the practical Bang-bang CDA can be expressed as:

$$V_{3^{rd}\mathrm{IMD},prac}(t) = V_{3prac}(2f_1 \pm f_2)\sin(2\pi(2f_1 \pm f_2)t) + V_{3prac}(f_2 \pm 2f_1)\sin(2\pi(f_2 \pm 2f_1)t) \tag{3.15a}$$

where

$$V_{3prac}(2f_1 \pm f_2) \cong \frac{2}{3}(1 + 8t_D f_0)[h(1+G)]^2 F(2f_1 \pm f_2) H(2f_1 \pm f_2) V_{DD} \times \sum_{i=1}^{\infty}\sum_{j=2}^{i+1}\left[\left(\frac{1}{2}\right)^{2i}\binom{2i+1}{j}\binom{2i+1-j}{j-2}\binom{2i+3-2j}{i+1-j} \times M_1^{p\,2j-2} M_2^{p\,2i+3-2j}\right] \tag{3.15b}$$

$$V_{3prac}(f_1 \pm 2f_2) \cong \frac{2}{3}(1 + 8t_D f_0)[h(1+G)]^2 F(f_1 \pm 2f_2) H(f_1 \pm 2f_2) V_{DD} \tag{3.15c}$$

$$\times \sum_{i=1}^{\infty} \sum_{j=2}^{i+1} \left[\left(\frac{1}{2}\right)^{2i} \binom{2i+1}{j} \binom{2i+1-j}{j-2} \binom{2i+3-2j}{i+1-j} \times M_2^{p\,2j-2} M_1^{p\,2i+3-2j} \right]$$

$$f_0 = \frac{\omega_p}{4(1+G)h} \tag{3.15d}$$

$$M_{1,2}^{p} = \left(1 + \frac{R_{on}}{R_L}\right) M_{1,2} \tag{3.15e}$$

where f_0 is the zero-input switching frequency of the ideal Bang-bang CDA.

In the case of the even-order IMD, the dominant component is the 2nd-order and the higher even-order terms are negligible and can hence be neglected. The 2nd-order IMD of the practical Bang-bang CDA can be expressed as:

$$\begin{aligned} V_{2^{nd}\mathrm{IMD},prac}(t) &= V_{2prac}(f_1 + f_2)\sin(2\pi(f_1 + f_2)t) \\ &+ V_{2prac}(f_1 - f_2)\sin(2\pi(f_1 - f_2)t) \end{aligned} \tag{3.16a}$$

where

$$V_{2prac}(f_1 \pm f_2) \cong \frac{2}{3} \frac{(1 + 8t_D f_0)\left((1+G)h\right)^2}{1 + \frac{k}{2}} F(f_1 \pm f_2) H(f_1 \pm f_2) V_{DD} \times$$

$$\sum_{i=1}^{\infty}\sum_{j=1}^{i}\sum_{q=1}^{j}\left[\frac{\left((1+G)h_{os}-\frac{k}{2}\right)^{2i+1-2j}}{\left(1+\frac{k}{2}\right)^{2i+1}}\right.$$

$$\left.\times\left(\frac{1}{2}\right)^{2j-1}\binom{2i+1}{2j}\binom{2j}{q}\binom{2j-q}{q-1}\binom{2j+1-2q}{j+1-q}M_1^{p\,2q-1}M_2^{p\,2i+1-2j}\right] \tag{3.16b}$$

For ease of interpretation, the 2nd-order IMD components in eqn. (3.16a) can be classified into two groups, according to the mechanisms thereof – the first is due to the h_{OS}, and the second is due to k. For the former, the 2nd-order IMD is given in eqn. (3.17a) and for the latter, the 2nd-order IMD is given in eqn. (3.18a) below:

$$\begin{aligned} V_{2^{nd}\mathrm{IMD},h_{OS}}(t) &= V_{2,h_{OS}}(f_1+f_2)\sin(2\pi(f_1+f_2)t) \\ &+ V_{2,h_{OS}}(f_1-f_2)\sin(2\pi(f_1-f_2)t) \end{aligned} \tag{3.17a}$$

where

$$V_{2,h_{OS}}(f_1\pm f_2)\cong\frac{2}{3}(1+8t_Df_0)\big((1+G)h\big)^2F(f_1\pm f_2)H(f_1\pm f_2)V_{DD}\times$$

$$\sum_{i=1}^{\infty}\sum_{j=1}^{j}\sum_{q=1}^{j}\left[\left((1+G)h_{OS}\right)^{2i+1-2j}\left(\frac{1}{2}\right)^{2j-1}\right. \tag{3.17b}$$

$$\left.\times\binom{2i+1}{2j}\binom{2j}{q}\binom{2j-q}{q-1}\binom{2j+1-q}{j+1-q}M_1^{p\,2j-1}M_2^{P\,2i+1-2j}\right]$$

$$V_{2^{nd}\mathrm{IMD},k}(t) = V_{2,k}(f_1+f_2)\sin(2\pi(f_1+f_2)t) + V_{2,k}(f_1-f_2)\sin(2\pi(f_1-f_2)t) \tag{3.18a}$$

where

$$V_{2,k}(f_1 \pm f_2) \cong \frac{2}{3}\frac{(1+8t_D f_0)\big((1+G)h\big)^2}{1+\frac{k}{2}}\, F(f_1 \pm f_2)H(f_1 \pm f_2)V_{DD}$$

$$\times \sum_{i=1}^{\infty}\sum_{j=1}^{i}\sum_{q=1}^{j}\left[\left(\frac{1}{2}\right)^{2j-1}\frac{\left(-\frac{k}{2}\right)^{2i+1-2j}}{\left(1+\frac{k}{2}\right)^{2i+1}}\right. \tag{3.18b}$$

$$\left. \times \binom{2i+1}{2j}\binom{2j}{q}\binom{2j-q}{q-1}\binom{2j+1-2q}{j+1-q} M_1^{p\,2q-1} M_2^{p\,2j+1-2q}\right]$$

We will now interpret eqns. (3.15a)-(3.18a) to delineate the aforesaid non-idealities (i)-(iv) and other circuit parameters, and their effects on the IMDs of the practical Bang-bang CDA.

i) Modulation Indexes (M_1 and M_2), hysteresis (h), closed-loop gain (G) and corner frequency (ω_p) of the feedback network

The effect of these parameters on the IMD of the practical Bang-bang CDA is the same as that on the IMD of the ideal Bang-bang CDA delineated earlier. Specifically, the higher the value of these parameters (save for ω_p), the higher is the IMD. It is true for both odd-order and even-order IMDs.

ii) Delay, t_D

From eqns. (3.15a) and (3.16a), it can be seen that for the practical Bang-bang CDA, a non-zero t_D increases both the odd-order and even-order IMDs by $(1+8t_Df_0)$

times compared to a Bang-bang CDA with zero t_D. Nevertheless, from a practical perspective, the delay-induced increase in IMD is usually inconsequential because the switching frequency of the Bang-bang CDA is typically low (relative-wise) which in turn corroborates with the need for low power dissipation; for completeness, it is interesting to note that for the Bang-bang CDA, the effect of t_D to IMD is similar to that of THD. As a case in point, for a typical practical Bang-bang CDA whose zero-input switching frequency, f_0=250kHz, a large t_D=50ns increases the IMD by a mere 10% compared to the case when t_D=0s. Practically, a t_D as short as ~10ns can be readily designed for the hysteresis comparator with low power dissipation [82], and the ensuing IMD increase of 2% is largely inconsequential. In short, a hysteresis comparator with a relatively relaxed delay is recommended for the sake of low power dissipation, yet without appreciably compromising the IMD.

iii) On-resistance, R_{on}

Like t_D, the effect of R_{on} on the odd-order and even-order IMDs of a practical Bang-bang CDA is the same – a non-zero R_{on} in the practical Bang-bang CDA results in an increased IMD compared to a Bang-bang CDA with zero R_{on}, and the higher the R_{on}, the higher is the IMD. This is because the effect of non-zero R_{on} is akin to an effective increase in the modulation index by a factor of R_{on}/R_L (eqn. (3.15e)). For instance, for the condition at high modulation index, M=0.7, and R_L=200Ω (a typical load resistance in hearing instruments), an R_{on}=2.9Ω (hence R_{on}/R_L=1.45%) results in 10% increase in IMD compared to the ideal case of R_{on}=0Ω. When R_{on} is increased to R_{on}=12.9Ω (R_{on}/R_L=6.45%), the IMD increase is a dramatic 62%.

Put simply, to obtain a low IMD, it is imperative that R_{on} be low. In the context of practical designs, the need for low R_{on} corroborates with good design practice for CDA designs – a low R_{on} is necessary to obtain a design with high power-efficiency. The cost, nevertheless, is a larger IC area and hence ensuing higher cost.

iv) Hysteresis mismatch, h_{OS}

From eqns. (3.15a)-(3.15c), it can be seen that h_{OS} does not affect the odd-order IMD of the practical Bang-bang CDA. On the other hand, from eqns. (3.17a) and (3.17b), it can be seen that even-order IMD arises from h_{OS} and, the higher the h_{OS}, the larger is the even-order IMD.

From a design perspective, V_{OS} ($h_{OS}=V_{OS}/V_{DD}$ is the normalized hysteresis mismatch) is largely due to the variance and mismatch in the manufacturing process [83] and, V_{OS}=10mV is not atypical. We will show later in Figure 3-7 that an increase of h_{OS} from 10mV to 20mV approximately doubles the even-order IMD over the entire modulation index range.

v) Power supply mismatch, k

From eqns. (3.15a)-(3.15c), it can be seen that k has little effect on the odd-order IMD of the practical Bang-bang CDA. On the other hand, from eqns. (3.18a) and (3.18b), it can be observed the even-order IMD arises from k, where the higher the k, the larger is the even-order IMD. For instance, a supply mismatch k=5% results in an even-order IMD of ~0.18%, and when the supply mismatch increases to k=20% the even-order IMD increases to nearly 1.0%. From a practical perspective, the power supply variance is common in real-life, particularly in power amplifiers

where the large current being delivered can easily induce V_{DD} variance through ohmic and inductive parasitics. This is somewhat corroborated by ITRS's specification that ±10% V_{DD} variance (equivalent to k=10%) as a testing condition [84].

vi) Combined h_{OS} and k mismatch

From the eqns. (3.16a) and (3.16b), it can be seen that the combined effect of h_{OS} and k is not simply an addition of the two individual mismatches. Specifically, the even-order IMD of the practical Bang-bang CDA depends on the polarities of the individual mismatch, V_{OS} and k. For example, when V_{OS} k>0 (i.e. V_{OS}>0 and k>0, or V_{OS}<0 and k<0), the IMD is lower than the case when only either V_{OS} or k of the same magnitude exists (see Fig. 8 later). This is because for V_{OS}>0 and k>0 (or V_{OS}<0 and k<0), the individual mismatch has opposing effect on the magnitude of the output signal and consequently, their effect on the IMD cancels each other. In contrast, when V_{OS} k<0, the IMD is higher than the case when only either V_{OS} or k of the same magnitude exists; see Figure 3-7 later.

From a practical perspective, the magnitude and polarity of mismatches V_{OS} and k are difficult to control but good design practice (e.g. centroid layout, etc.) does nevertheless mitigates the magnitude of V_{OS} and k. In short, as the aforesaid cancelling effect is difficult to realize, we recommend that the mismatches V_{OS} and k be designed to be as low as possible.

In summary, in the practical Bang-bang CDA, the only pertinent IMDs are the 2nd-order even and 3rd-order odd IMDs. To obtain a low IMD for the practical Bang-bang

CDA, we recommend that $R_{on,}$ V_{OS} and k be designed to be as low as practically possible, h be low (e.g. h=0.025), and as a good overall design compromise, G=1, and BW<ω_{p-} <1.5BW. A relaxed delay is largely acceptable as it has little effect on the IMD, and allows a hysteresis comparator design with lower power dissipation, thereby improving overall power-efficiency.

3.4 Verification and Measurements Results

In this section, the pertinent 2nd-order and 3rd-order IMD analytically predicted by eqns. (3.15a) and (3.16a) respectively are verified against HSPICE simulations and on the basis of practical measurements [85] on a physical Bang-bang CDA embodying an output stage IC. The microphotograph of the IC is shown in Figure 3-4.

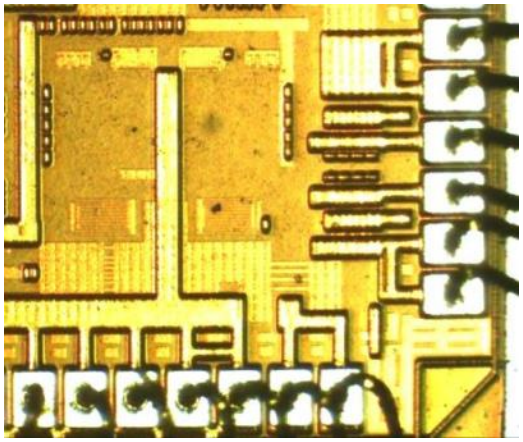


Figure 3-4 Microphotograph of the Class D output stage IC

To delineate the effect of the various IMD mechanisms and circuit parameters of Bang-bang CDAs, several Bang-bang CDA designs with different circuit parameters are tabulated in Table 3-2 and Table 3-3. The testing scenarios in Table 3-2 assume that there are no mismatches, hence the even-order IMD therein is insignificant and this serves to verify the odd-order IMD eqn. (3.15a). The test scenarios in Table 3-3, on the other hand, include the mismatch, hence both odd-order and even-order IMDs are present. The scenarios in Table 3-3 are hence more realistic; and serve to verify the derived even-order IMD equation given in (3.16a).

Table 3-2 Circuit Parameters of the Bang-bang CDA for odd-order IMD

Parameter	Value			
	Case 1	Case 2	Case 3	Case 4
h	0.025	0.05	0.025	0.025
f_0(kHz)	250	125	250	250
t_D(ns)	50	50	50	100
G	1	1	2	1
R_{in}(kΩ)	10	10	10	10
R_{fb}(kΩ)	10	10	20	10
R_{on}(Ω)	2.9	2.9	2.9	2.9
C(nF)	4	4	3	4
ω_p(Hz)	—— $2\pi\times8$k (for all cases) ——			
R_L(Ω)	—— 200 (for all cases) ——			

The measurements herein adhere to the SMPTE standards, including that for IMD where the input signal comprises a low frequency component f_1=60Hz and a high frequency component f_2 =7kHz, and that $V(f_1) = 4V(f_2)$. The range of the modulation indexes of the two input frequency components is from M_1=0.1 to M_1=0.7 and M_2 (=M_1/4) from 0.025 to 0.175; note that if the input comprises only one frequency component, the

maximum modulation index would be M=0.9, after which the output signal clips. The V_{DD} is set to 1.5V in all test scenarios.

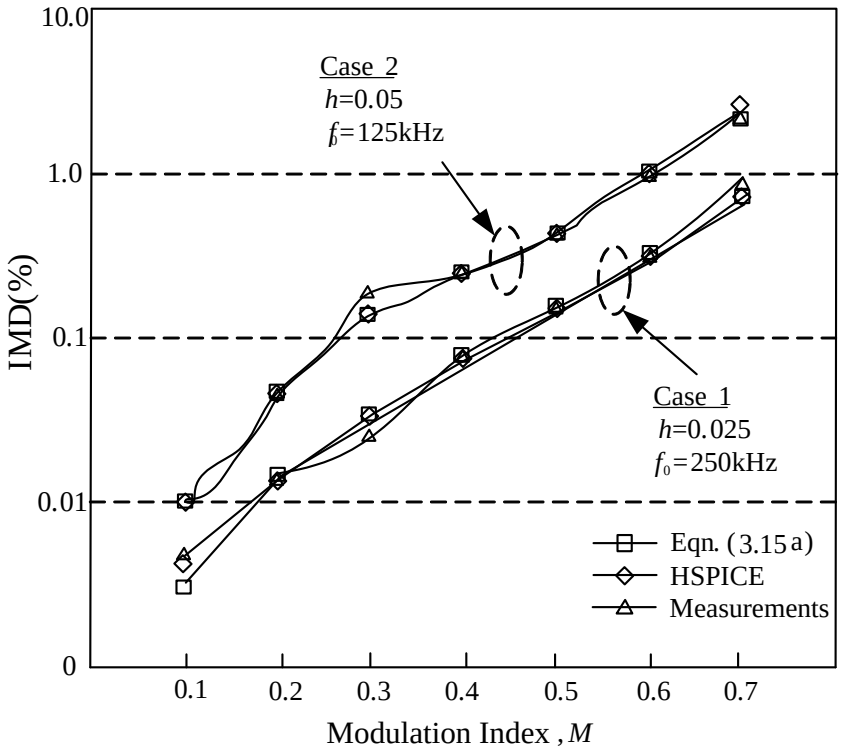


Figure 3-5 Cases 1 and 2: 3rd-order IMD versus modulation index

First consider the effect of the hysteresis, h, on the odd-order IMD for Cases 1 and 2 in Table 3-2. Figure 3-5 summarizes the IMD (odd-order; even-order IMD is absent) versus modulation index of the Bang-bang CDA, obtained analytically by eqn. (3.15a), by simulation and measurements.

It can be seen from Figure 3-5 that the IMD obtained analytically from eqn. (3.15a) agrees well with the simulations and measurements, thereby verifying the said derived equation. As expected, the IMD increases as M increases. A comparison of Cases 1 and 2 shows that a lower hysteresis results in a lower IMD, but this is at the cost of higher

switching frequency. A higher switching frequency is in general undesirable as this increases the switching power, for example, doubling the switching frequency inevitably leads to a 2x switching power dissipation.

Consider now the effect of the closed-loop gain, G, and the delay, t_D, on the IMD of Bang-bang CDAs, specifically for the Cases 1, 3, and 4 in Table 3-2. Figure 3-6 summarizes the IMD obtained analytically (eqn. (3.15a)), by simulations and on the basis of measurements.

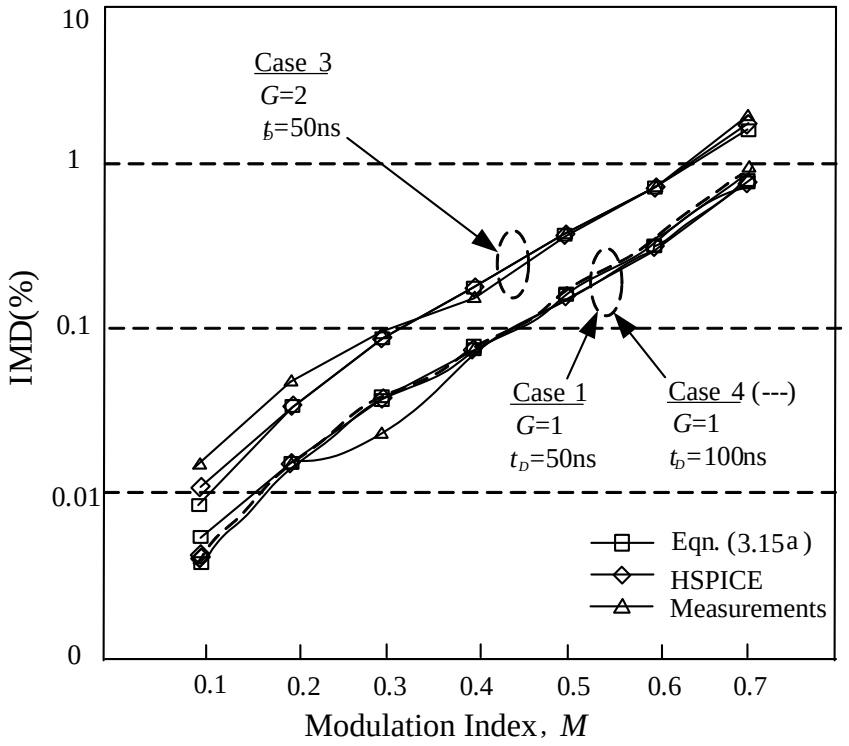


Figure 3-6 Cases 1, 3 and 4: 3rd-order IMD versus modulation index

The analytical results as before agree well with simulation and measurements, thereby verifying eqn. (3.15a). As predicted, G has a strong effect on the odd-order IMD

and this can be observed by comparing Case 1 where G=1 and Case 3 where G=2, both having the same t_D=50ns. As expected, a lower G leads to a lower IMD. Note that the modulation index is referred to the output, hence a larger G equals to a smaller input at the same output power.

For the sake of completeness, note that the plots for Case 4 was obtained from simulations as it is difficult to adjust t_D experimentally.

Consider now the effect of the even-order IMD mechanisms and other circuit parameters on the even-order IMD. Table 3-3 tabulates Cases 5-10 for the different conditions, and note that the 3rd-order IMDs of the Bang-bang CDA for Cases 5-10 are the same as that of Case 1 in Table 3-2. The choice for this condition is justified because as delineated earlier, the input DC offset of the hysteresis comparator and power supply mismatch have little effect on the 3rd-order IMD. Also note that as V_{OS} is difficult to control experimentally, the results of the cases involving V_{OS} (Cases 5, 6, 9 and 10) are that obtained analytically and by means of SPICE simulations. The summary of the even-order IMD for Cases 5-10 are plotted in Figure 3-7 and Figure 3-8.

Table 3-3 Circuit Parameters of the Bang-bang CDA for even-order IMD

Parameter	Value					
	Case 5	Case 6	Case 7	Case 8	Case 9	Case 10
H	0.025	0.025	0.025	0.025	0.025	0.025
f_0(kHz)	250	250	250	250	250	250
V_{OS}(mV)	-10	-20	0	0	-20	20
G	1	1	1	1	1	1
R_{in}(kΩ)	10	10	10	10	10	10
R_{fb}(kΩ)	10	10	20	10	10	10
R_{on}(Ω)	2.9	2.9	2.9	2.9	2.9	2.9
C(nF)	4	4	4	4	4	4
K	0	0	0.07	0.15	0.07	0.07
ω_p(Hz)	—— $2\pi\times8$k (for all cases) ——					
R_L(Ω)	—— 200 (for all cases) ——					

To delineate the effect of V_{OS} on the even-order IMD, consider the even-order IMD of Cases 5 and 6 whose V_{OS}=-10mV and V_{OS}=-20mV respectively, and where k=0 for both cases. It can be seen from Figure 3-7 that IMD obtained analytically from eqn. (3.16a) agrees well with that obtained by means of SPICE simulations, thereby verifying eqn. (3.16a).

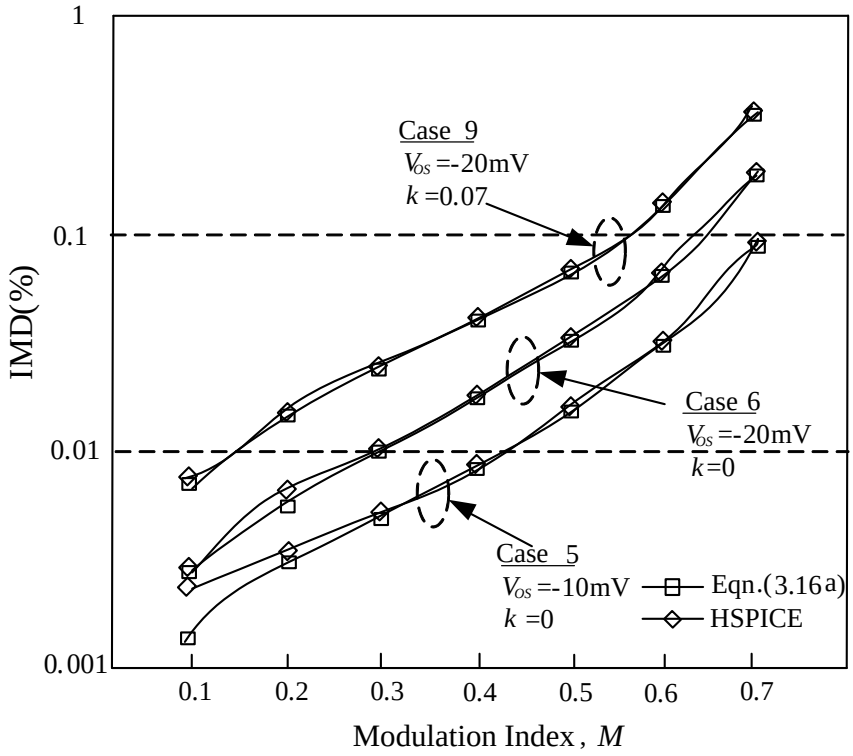


Figure 3-7 Cases 5, 6 and 9: 2nd-order IMD of Bang-bang CDA versus modulation index

It can be seen that V_{OS} has a marked effect on even-order IMD. Specifically, as predicted by eqn. (3.16a), a doubling of V_{OS} increases the even-order IMD by an approximate factor of 2.

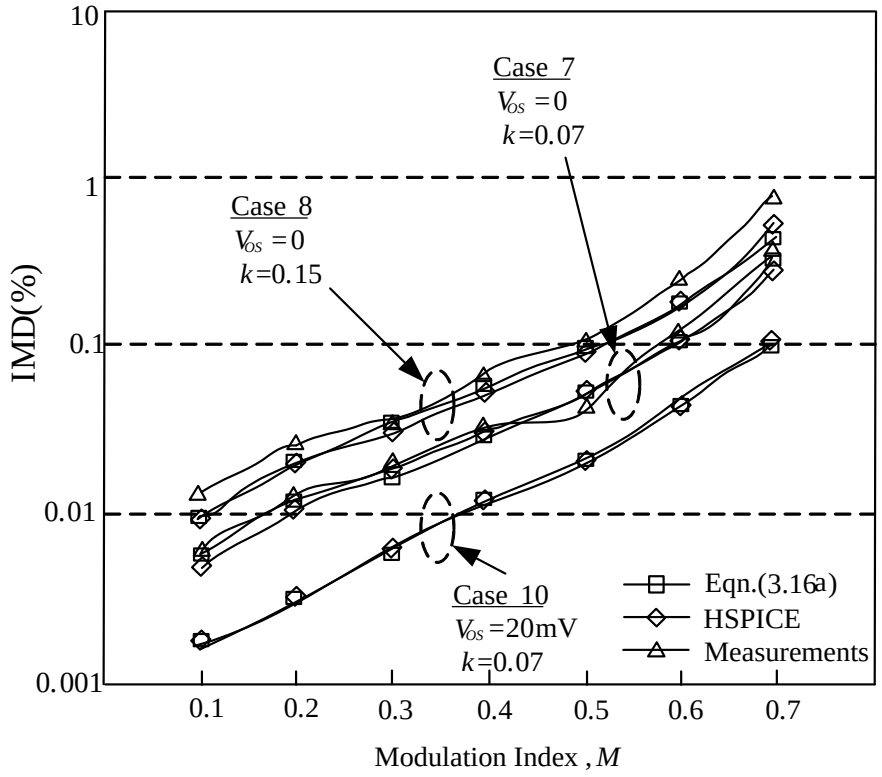


Figure 3-8 Cases 7, 8 and 10: 2nd-order IMD of Bang-bang CDA versus modulation index

To delineate the effect of k on the even-order IMD, consider the even-order IMD plotted in Figure 3-8 for Cases 7 and 8 whose k=0.07 and k=0.15 respectively, and where V_{OS}=0 for both cases. It can be seen from Figure 3-8 that the analytical predictions agree well with the simulations and measurements, thereby verifying eqn. (3.16a). It can also be seen that a lower power supply mismatch, k, results in a lower 2nd-order IMD.

Consider now the combined effect of V_{OS} and k, specifically noting the polarities of V_{OS} and k as delineated earlier. In Figure 3-7, consider Cases 6 and 9 whose k=0 and k=0.07 respectively, and V_{OS}=-20mV for both cases. The 2nd-order IMD of Case 9 is

higher than that of Case 6. This corroborates the analytical prediction by eqn. (16a) that IMD is increased in the case of two mismatches, V_{OS} łk<0 (V_{OS} =-20mV and k=0.07 for Case 9), compared with the case where only one mismatch of the same magnitude (V_{OS} =-20mV and k=0 for Case 6).

In another example, consider Cases 7 and 10 depicted in Figure 3-8 whose V_{OS}=0 and V_{OS}=20mV respectively, and k=0.07 in both cases. The 2nd-order IMD of Case 7 is perhaps somewhat surprisingly higher than that of Case 10. This, as before, corroborates the analytical prediction by eqn. (16a) that IMD is decreased in the case of two mismatches, V_{OS} łk>0 (V_{OS} =20mV and k=0.07 for Case 10), compared with the case where only one mismatch of the same magnitude (V_{OS} =0 and k=0.07 for Case 7).

Finally, to depict the overall perspective of the magnitudes of even-order and odd-order IMD of a practical Bang-bang CDA (Case 9), Figure 3-9 depicts these IMDs as a function of modulation index. It can be seen from Figure 3-9 in this Bang-bang CDA design, the 2nd-order IMD is higher than the 3rd-order IMD for M<0.2. This is perhaps unexpected as even-order IMD is usually insignificant compared to odd-order IMD in CDAs and in linear amps. Considering that M=0.15 (<0.2) is the nominal condition of Bang-bang CDAs, the even-order IMD may arguably be more detrimental. For M>0.2, the 3rd-order IMD is the larger of the two IMDs.

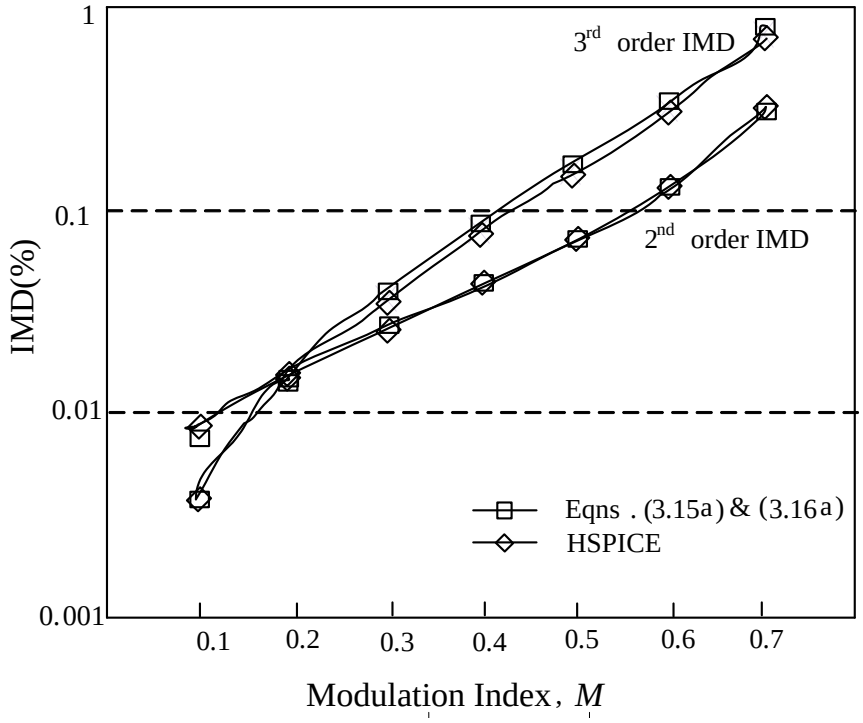


Figure 3-9 Case 9: Comparison of 2nd-order and 3rd-order IMDs versus modulation index

In summary, on the basis of HSPICE simulations and measurements, the derived analytical expressions for the 2nd-order and 3rd-order IMDs are verified. The derived analytical expressions provide good insights into the mechanisms of even- and odd- order IMD and the effect of these mechanisms and other circuit parameters on IMD. Of specific interest, the even-order IMD of a practical Bang-bang CDA can be dominant at lower modulation index range, and the odd-order IMD dominates at higher modulation index range.

3.5 Conclusions

IMD, an unreported measure of fidelity for Bang-bang CDAs, has been investigated. Analytical expressions for the IMD of the Bang-bang CDA have been derived and verified against HSPICE simulations and the measurements of a prototype Bang-bang CDA. On the basis of the derived analytical expressions, the mechanisms for IMD and other circuit parameters that affect the odd-order IMDs have been ascertained and investigated. It has been shown that the even-order IMD that is usually negligible/unreported in other Class D and linear amplifiers, is significant in Bang-bang CDAs, particularly when the modulation index is low. Odd-order IMD on the other hand, is dominant when the modulation index is high. The analytical expressions provide insights into the design of the Bang-bang CDA and on how various circuit parameters can be traded-off to improve the IMD of Bang-bang CDAs.

Chapter 4 An Ultra-High PSRR Ultra-Low Distortion PWM Class D Amplifier

4.1 Introduction

A large portion of this chapter has been published as a US provisional patent [38] and published in IEEE Journal of Solid State Circuits [42].

Smart mobile devices, including smartphones and tablets, continue to evolve with increased data communication rate, improved visual (screen/display) resolution and increased auditory (audio/sound) fidelity. In case of audio fidelity, several present-day smart mobile devices claim very high fidelity because they incorporate a 24-bit 192 kHz digital-to-analog converter, possibly with Signal-to-Noise Ratio, SNR>100 dB, Dynamic Range>100 dB and THD+N of the order of 0.002% [49, 86, 87]. To ensure that these smart devices retain their overall (system) audio fidelity, the audio amplifier embodied therein would likewise need to feature commensurable high fidelity, including THD+N of the same order. Further, due to the inevitable noise coupling between different modules (including said digital-to-analog converter) in the audio CODEC System-on-Chip, said audio amplifier therein would need to feature very high tolerance to noise in the supply

rail (qualified by high PSRR), for example PSRR>90 dB, and low PS-IMD, for example PS-IMD<-90 dB), and low EMI. Yet further, in view of the limited power resources in these mobile smart devices, it is highly desirable that said amplifier features high power-efficiency, for example power-efficiency, η>90%. Virtually all present-day smart mobile devices embody a CDA as the driver to the primary ('speakerphone') loudspeaker. Nevertheless, as discussed earlier in Chapter 1, at this juncture, CDAs are largely deficient in fidelity and noise immunity (to power supply noise); for example, only very few CDAs feature THD+N <0.01% and PSRR >90 dB, and none featuring PSRR>100 dB; see Table 4-1 later.

Reported methods [4, 19, 20] to improve these imperative fidelity and noise immunity parameters include employing a high switching frequency (e.g. f_{sw} > 500 kHz), and/or complex multiple feedback loops. However, these reported methods incur compromises and penalties. Specifically, the former not only increases the power dissipation (hence compromising the power-efficiency) but also potentially increases the EMI. The latter, on the other hand, penalizes both the hardware complexity (hence higher IC area and cost) and the quiescent power dissipation (hence reducing the power-efficiency), and may render the CDA non-fully-integrated if external components are required.

To circumvent said undesirable compromises and ensuing penalties, yet obtaining high power-efficiency and without resorting to a high switching frequency, we propose a novel CDA design that embodies an input-modulated carrier generator and a phase-error-free PWM modulator; we previously showed that the primary mechanisms of THD are

duty-cycle and phase errors [33]. Arguably, this is the first-ever CDA to feature a design with zero phase-error. The prototype CDA, fabricated using a commercial 65 nm CMOS process, features a very-low THD+N of 0.0027% (when delivering 500 mW to an 8 Ω load) and the highest PSRR to-date, PSRR=101 dB at 217 Hz, yet with a relatively low switching frequency, f_{sw}=~320 kHz at nominal operating conditions. Furthermore, the prototype CDA is highly versatile in terms of operating supply voltages, ranging from 1.2 V to 4 V, thereby allowing operation from a rechargeable single-cell (1.2 V) to standard smartphone operation (3.7 V). In addition, as the switching frequency is input-modulated, hence varying, the ensuing EMI is reduced compared to conventional CDAs whose switching frequency is fixed. The proposed CDA features the highest Figures-Of-Merit (FOMs) compared with state-of-art designs; see benchmark Table 4-1 later. For completeness, the ~0.6 mm^2 (active area) prototype CDA is (for cost reasons) integrated with other (unrelated) designs on a large 3x3 mm^2 die and packaged in a large 6x6 mm^2 lead-frame package. Should the prototype CDA be diced to an individual (hence smaller) die and packaged either into a smaller package (e.g. 3x3 mm^2) or with wafer-level packaging, the THD+N, on the basis of simulations, would improve by ~6 dB, from 0.0027% to 0.0015%.

This chapter is organized as follows. Section 4.2 discusses the system-level design. In Section 4.3, circuit realizations are delineated in detail. Section 4.4 presents the measurement results and the benchmarking of the proposed CDA against state-of-the-art CDAs. Finally, conclusions are drawn in Section 4.5.

4.2 System Level Design

Pulse-Width-Modulation (PWM) is the most prevalent CDA modulation scheme at this juncture. Open-loop PWM CDAs were initially used largely for their hardware simplicity, but are now largely discarded due to their poor linearity and low PSRR. Closed-loop CDAs are now ubiquitous because of their improved performance; largely by the means of negative feedbacks. Figure 4-1 depicts a prevalent closed-loop design, a single-feedback 2nd-order integrator PWM CDA.

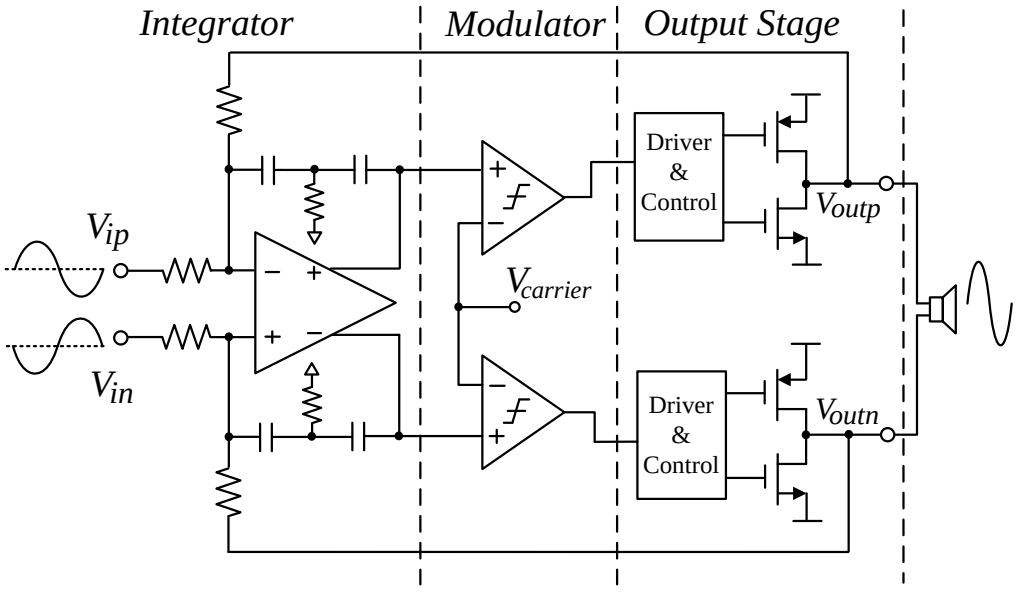


Figure 4-1 Schematic of a single-feedback 2nd-order integrator PWM CDA

The amplifier outputs (V_{outp} and V_{outn}) are fed (back) to the integrator which integrates these signals with the input signals (V_{ip} and V_{in}), forming a closed-loop. The loop-gain of the closed-loop is a fundamental design parameter for closed-loop CDAs

because it directly and markedly affects two imperative specifications of CDAs – THD and PSRR:

(i) A high loop-gain results in a large in-band (at audio frequencies) gain. This in turn leads to high PSRR (and reduced (improved) PS-IMD) as the large gain suppresses the (audio frequency) supply noise introduced at the output stage of the CDA.

(ii) Unlike linear amplifiers, a high loop-gain may conversely and inadvertently exacerbate the distortions in the CDA. It is because a high loop-gain inevitably results in reduced out-of-band attenuation (at high frequencies, particularly at the switching frequency) of the switching signal component. The residual switching signal component intermodulates with the carrier during the PWM modulation process, thereby introducing distortions.

(iii) Following (ii), we have shown that these distortions are "duty-cycle error" and "phase-error" according to their different mechanisms. Particularly, the phase-error distortion arises because the time delay between the center of the PWM signal and the center of the carrier is signal-dependent, and this distortion cannot be suppressed by the in-band loop-gain. In other words, the phase-error distortion may undesirably increase as the loop-gain increases.

In short, there is an inevitable trade-off between PSRR and linearity when designing the loop-gain – a large loop-gain improves the PSRR while potentially exacerbating distortions. Furthermore, a large loop-gain may limit the dynamic range of the CDA. This is because a large loop-gain results in a large (less attenuated) switching signal component at the integrator output (see Figure 4-2 later), which takes away part of the headroom for

the signal swing. The limited signal swing at the integrator output in turn limits the maximum output signal swing of the CDA. Although a very high switching frequency could theoretically resolve said issues, it is nevertheless not desirable for the reasons delineated earlier.

To circumvent said undesirable trade-offs, we propose a novel PWM CDA architecture that, as depicted in Figure 4-2, embodies an input-modulated carrier generator and a phase-error-free PWM modulator (see Figure 4-5 (a) later). We will now discuss the mechanisms and efficacies of these two blocks in relation to the performance of the CDA.

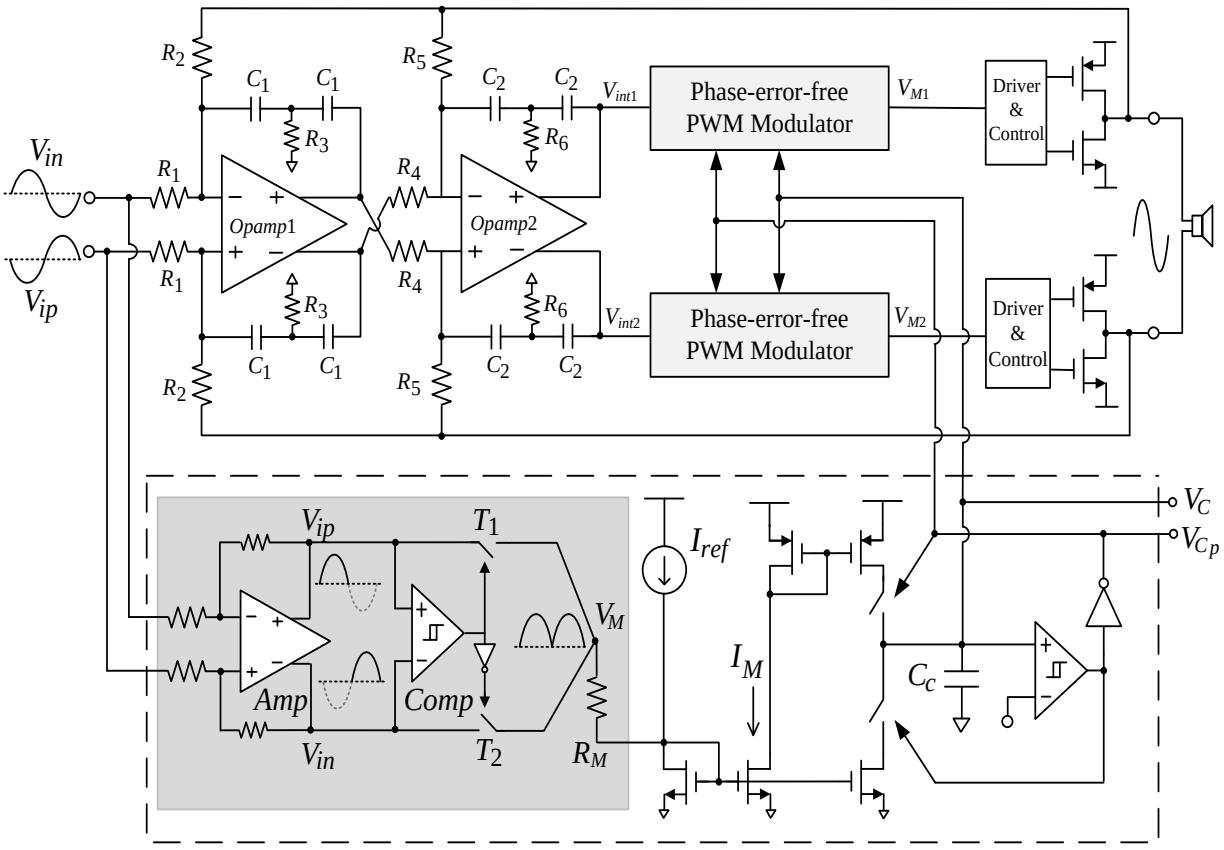


Figure 4-2 Schematic of the proposed CDA

The input-modulated carrier generator (depicted in the dashed-box at the bottom of Figure 4-2) takes the input signals, V_{in} and V_{ip}, of the CDA as the modulating signal to vary the frequency of the carrier. Specifically, when the magnitude of the input signal increases, the carrier switching frequency increases accordingly; and vice versa. In this manner, the switching frequency at nominal operating conditions remains low, which reduces switching power dissipation and generates less ground-bounce noise. Of specific interest, the switching frequency increases to its maximum when the magnitude of the input signal is at its maximum. This desirably leads to increased attenuation of the switching component as the switching is now at a higher frequency. Consequently, the potential signal-clipping is mitigated, thereby maintaining high dynamic range, and the ensuing distortions reduced. The detailed operation of this proposed carrier generator will be delineated in the next section. We will show that, compared to conventional carrier generators, the hardware and the quiescent power overheads of the proposed generator are negligible.

The phase-error-free PWM modulator is also depicted in Figure 4-2, the detailed schematic thereof is depicted in Figure 4-2. This novel modulator is intrinsically phase-error free. As abovementioned, the phase error in conventional PWM arises because the time delay between the center of the PWM signal and the center of the carrier is signal-dependent, and this distortion cannot be suppressed by the in-band loop-gain. To eliminate the phase error, our proposed PWM modulator is designed in a fashion such that the center of the PWM signal is aligned to the center of the carrier signal. With this modulator, a large loop-gain can be employed, without potentially compromising

(increasing) the distortions due to phase-errors. The detailed schematic and operation of the proposed modulator will be delineated in the next section.

The proposed input-modulated carrier generator and the phase-error-free PWM modulator, individually and collectively, allow the employment of a very large loop-gain, without compromising the dynamic range and/or the linearity of the CDA. The high loop-gain is realized by the double-feedback 2nd-integrator loop-filter design depicted in Figure 4-2. The design of the loop-filter and its potential stability issues will now be delineated in detail.

4.3 Circuits Level Design

In this section, we will discuss the circuit design of the critical functional blocks embodied in the proposed CDA.

4.3.1 Loop-filter design

The proposed CDA depicted in Figure 4-2 adopts a double-feedback topology with a 2nd-order integrator for each feedback loop. The equivalent block diagram model of the CDA is depicted in Figure 4-3, where β_{fb1} and β_{fb2} are respectively the feedback factor for the first (inner) feedback loop, $Loop_1$, and second (outer) feedback loop, $Loop_2$. $Loop_1$, depicted within the shaded box, is essentially a closed-loop single-feedback CDA, and is

encompassed within the forward path of $Loop_2$. The transfer functions (or gains) of the first and second integrators are also depicted.

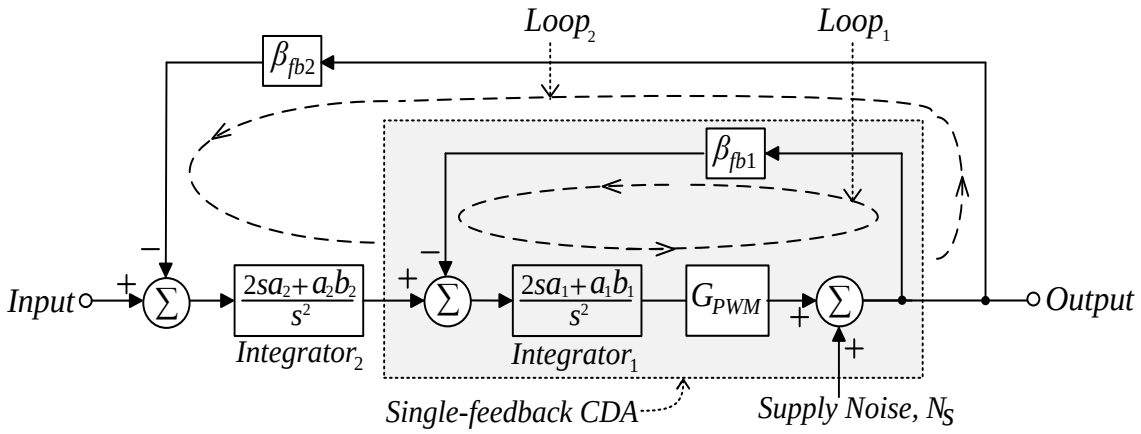


Figure 4-3 Block diagram of the proposed double-feedback CDA

The imperativeness of high loop-gain was delineated in the last section. From Figure 4-3, the effective loop-gain, G_{EL}, of the CDA that suppresses the supply noise (and the output stage distortions) can be derived as follows:

$$G_{EL} = 1 + \left(\frac{2sa_2 + a_2b_2}{s^2}\right)\beta_{fb2}\left(\frac{2sa_1 + a_1b_1}{s^2}\right)G_{PWM} + \left(\frac{2sa_2 + a_2b_2}{s^2}\right)\beta_{fb1}G_{PWM} \quad (4.1)$$

It is apparent from eqn. (4.1) that a high loop-gain can easily be achieved by increasing the integrator(s) gain (terms within parentheses). These gains, however, cannot be arbitrarily increased, in part because the double-feedback CDA is not unconditionally stable; and it is stable only if both feedback loops are stable. Amongst the two loops,

Loop$_1$ (with a 2nd-order integrator) is unconditionally stable. On the other hand, *Loop*$_2$ is only conditionally stable, and its stability largely depends on three parameters: the poles/zeros of *Integrator*$_2$, β_{fb2} and the single-feedback CDA.

It can be seen that the frequency response, G_{lp2}, of *Loop*$_2$ is:

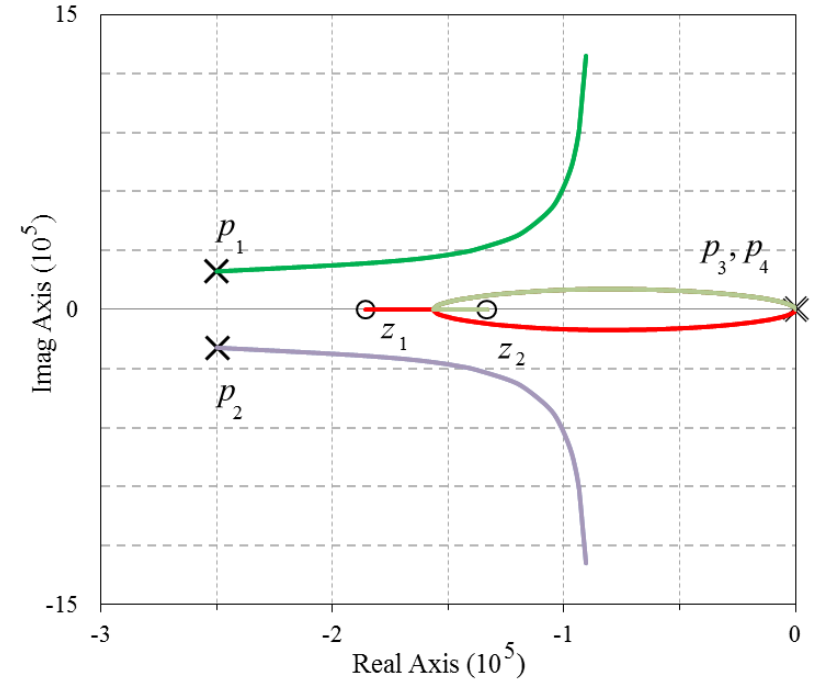
$$G_{lp2} = \frac{G_{op2}}{1 + \beta_{fb2} G_{op2}} \tag{4.2}$$

where G_{op2} is the forward path gain of *Loop*$_2$, which can be expressed as:

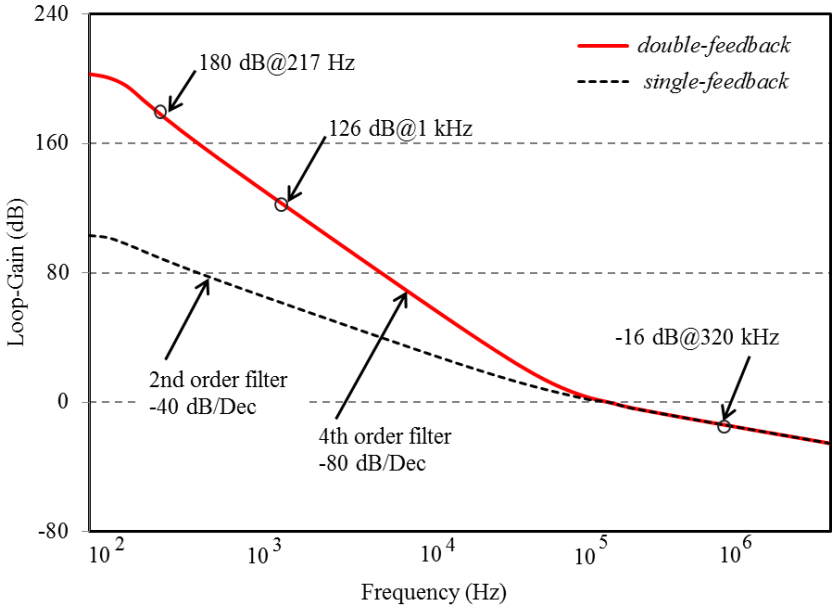
$$G_{op2} = \left(\frac{2sa_2 + a_2 b_2}{s^2}\right)\left(\frac{2a_1 s + a_1 b_1}{s^2 + 2a_1 G_{PWM}\beta_{fb1} s + 4a_1 b_1 \beta_{fb1}}\right) \tag{4.3}$$

The root-locus of G_{lp2} is depicted in Figure 4-4 (a). To ensure stability, we design the CDA loop filter in the following fashion. The closed-loop poles of the single-feedback CDA, p_1 and p_2, are placed on the left hand side of the two zeros, z_1 and z_2, introduced by the two integrators. In this manner, all the poles of G_{lp2} will reside in the left-hand plane, thereby achieving a stable loop.

The loop-gain, G_{EL}, of the ensuing filter-loop design (embodying four poles and two zeros) is plotted in Figure 4-4 (b). It can be seen that it simultaneously achieves very large in-band loop gain (180 dB and 126 dB at 217 Hz and 1 kHz respectively) and high out-of-band attenuation (-16 dB at ~320 kHz).



(a)



(b)

Figure 4-4 (a) Root-locus of G_{lp2}, and (b) the loop-gain of double-feedback and single-feedback CDA

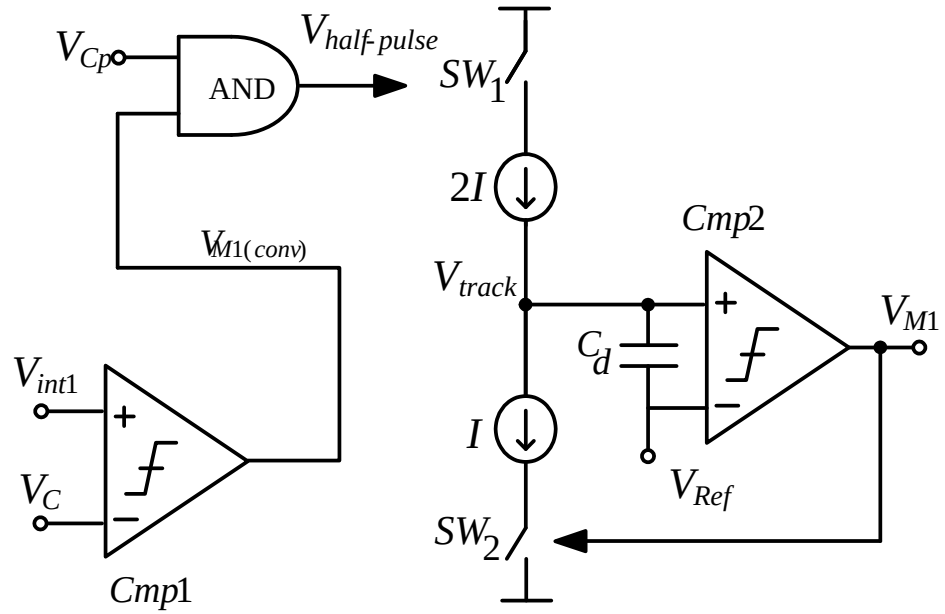
4.3.2 Proposed phase-error-free PWM modulator

The schematic of the proposed phase-error-free PWM modulator and its waveforms are depicted in Figure 4-5 (a) and (b) respectively. For completeness, the proposed modulator is embodied in both differential branches as depicted in Figure 4-2. For brevity, we will only delineate the operation of the modulator in the upper branch thereof.

The proposed modulator operates as follows. The first comparator, *Cmp*1, compares the integrator output signal, V_{int1}, against the triangular carrier signal, V_C, to generate a conventional PWM signal, $V_{M1(conv)}$. An "AND" gate generates the 'half-pulse', $V_{half\text{-}pulse}$, by combining the pulse signal of the carrier (V_{Cp}) with $V_{M1(conv)}$. This 'half-pulse' is essentially one half of a complete PWM pulse that is the input to the output stage, and is phase-error-free. Subsequently, $V_{half\text{-}pulse}$ turns on the 2*I* current source and capacitor C_d commences to charge from its original value. The voltage at the positive input of *Cmp*2, V_{track}, commences to ramp up and triggers comparator *Cmp*2 to change state. This in turn closes switch SW_2 and the lower side current source commences to sink a current *I*. Hence, for the 'half-pulse' period, capacitor C_d is effectively being charged by a current of *I*. At the end of the 'half-pulse' period, SW_1 opens while SW_2 remains closed, and the lower-side current source continues to discharge capacitor C_d with current *I*. Subsequently, V_{track} ramps down until it reaches its initial voltage, and it triggers *Cmp*2 to open T_2. In this manner, the width of the final PWM pulse, V_{M1}, is twice of $V_{half\text{-}pulse}$.

The pertinent waveforms are depicted in Figure 4-5 (b). It can be seen that the center of the final PWM signal V_{M1} is synchronized with the center of the carrier signal,

and is independent of the input signal. Hence the V_{M1} has zero phase error, i.e. phase-error-free. Further, as its rising edge coincides with that of the conventional natural-sampling PWM signal, the sampling is not synchronized by any clock signals, hence the sampling is natural sampling.



(a)

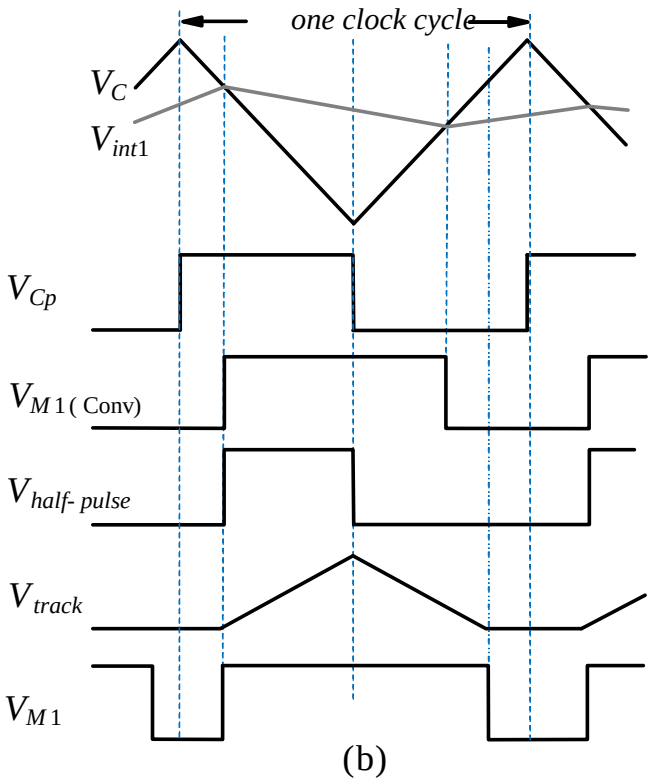


Figure 4-5 (a) Schematic of the proposed phase-error-free PWM modulator and (b) its waveforms

4.3.3 Proposed input-modulated carrier generator

As delineated in the section 4.2, the switching frequency, f_{sw}, of the proposed carrier generator is not fixed as conventional designs. It is instead input-modulated and hence varying. The schematic of the proposed input-modulated carrier generator was depicted earlier in the dashed box at the lower half of Figure 4-2.

Its operation is as follows. The proposed carrier generator generates a triangular carrier, V_C, whose switching frequency varies with the signal swing. This is obtained by employing a varying current (vis-à-vis a constant current in conventional designs), I_M, whose magnitude is input-related, to charge and discharge capacitor C_C to generate the carrier. The varying I_M is generated as follows. The differential input signals, V_{in} and V_{ip}, are first buffered by op-amp *Amp*, whose outputs are subsequently compared by comparator *Comp*. When $V_{ip}>V_{in}$ (i.e. V_{ip} is positive with respective to the input common-mode voltage and V_{in} is negative), switch T_1 is closed and V_M connected to V_{ip}. Conversely, when $V_{in}>V_{ip}$, switch T_2 is closed and V_M is connected to V_{in}. In this fashion, V_M is always positive (with respect to the common-mode) as depicted in the waveforms in Figure 4-2. Resistor R_M consequently converts V_M to current I_M.

The hardware overhead (shaded area in Figure 4-2) and power overhead of the proposed carrier generator over the conventional carrier generator are, in the context of the entire CDA, largely negligible. This is because the specifications of op-amp *Amp* and comparator *Comp* are relaxed, and the output stage dominates the power-dissipation and IC area. Specifically, for the former, the gain-bandwidth of *Amp* is about 1 MHz (with a resistive load of >100 kΩ), and the delay and resolution of *Comp* are >0.05 μs and >10 mV respectively. The other added hardware overheads are negligible – two switches and a few resistors, all integrated.

In addition to the higher attenuation of the switching component when the input signal is large, another advantage of generating the carrier in this manner is that the ensuing switching of the output stage is not fixed at a single frequency (as in conventional

designs) but is instead spread over a relatively large range of spectrum. Consequently, the EMI of the CDA is significantly reduced.

4.3.4 Operational amplifiers

Figure 4-6 depicts the schematic of the operational amplifiers (op-amps), $Opamp_1$ and $Opamp_2$ depicted in Figure 4-2. The op-amps are employed in the integrators ($Integrator_1$ and $Integrator_2$) in the loop-filter, and to ensure the integrators function as designed, the op-amp therein must feature a high DC gain (~100 dB) and a relatively wide bandwidth (~15 MHz). This is because the desired high in-band gain of the integrator(s) is directly determined by the gain of the op-amp therein, and because the desired frequency response (which is largely determined by *RC* values) of the integrators can only be realized if the bandwidth of the op-amp is higher than the cut-off frequency of the integrator. Of specific interest, as the input-referred noise of $Opamp_1$ directly contributes to the overall input-referred noise of the CDA, hence affecting the noise floor and the SNR of the CDA, the input transistors of $Opamp_1$ are designed to be very large to reduce flicker noise.

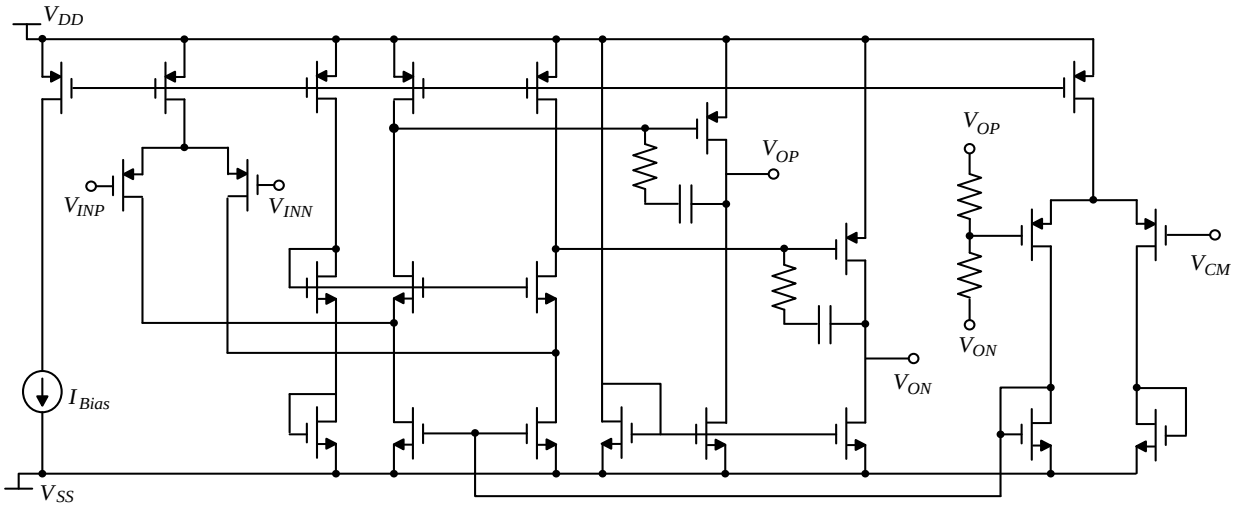


Figure 4-6 Schematic of the operational amplifiers, $Opamp_1$ and $Opamp_2$

4.3.5 Output stage design

The output stage of the CDA is a Bridged-Tied-Load topology to drive the load differentially. Figure 4-7 depicts the schematic of one branch of the differential output stage; the other branch is identical. The output power transistors therein adopts a standard CMOS inverter topology where the upper-side transistor, M_p, is PMOS and the lower-side transistor, M_n, is NMOS. The output transistors are designed to feature a low on-impedance to achieve high power-efficiency. Specifically, the width (W) of M_n and M_p is W=2.4 mm and W=5 mm respectively, with length L=320 nm.

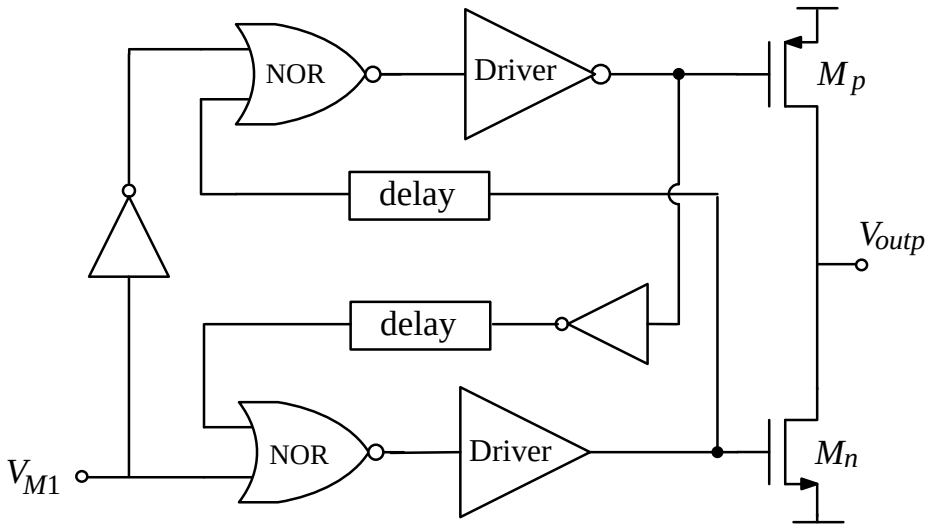


Figure 4-7 Schematic of the output stage (a half-bridge of the differential output stage)

Due to the relatively low switching frequency of the proposed CDA, a relatively large dead-time, >5 ns, can be accommodated, largely without affecting the linearity of the CDA. A long dead-time in turn improves the robustness of the output stage. The driver circuit is designed with a relatively large tapering ratio (the ratio of the size of the driving inverter to that of the inverter being driven), thereby resulting in relatively slow switching of the output transistors. This in turn reduces the ground-bounce generated by the output stage, and hence improves the overall performance of the CDA.

4.4 Measurement Results

The prototype CDA IC is fabricated using a commercial 65 nm CMOS process and for cost reasons, integrated with other (unrelated) designs on a 3x3 mm^2 die (the active area is ~0.6 mm^2). The microphotographs of the CDA chip and its placement in a standard 6x6 mm^2 QFN package are shown in Figure 4-8.

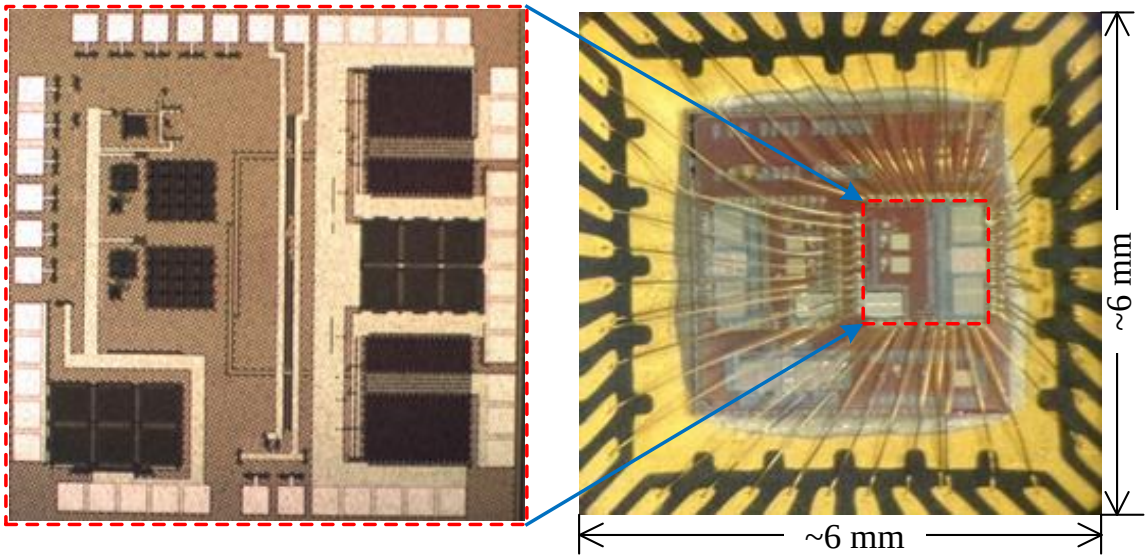


Figure 4-8 Microphotograph of the CDA IC prototype and its placement in the QFN package

A single-rail supply V_{DD} = 3.6 V and an 8 Ω load, unless specified otherwise, are used. Measurements are obtained by means of the *Rohde* & *Schwarz* UPV Audio analyzer. The measured bandwidth of the prototype CDA is from 20 Hz to 20 kHz. The measurements setup complies with the CDA testing settings described in a well-established application note [88]. To ascertain the PSRR and PS-IMD parameters, a

power supply that is able to superimpose a sinusoidal wave on a DC voltage is used to inject the noise in the supply voltage.

Figure 4-9 depicts the spectrum of the output signal, V_{out} = 2 V_{rms} at f_{out} = 1 kHz. The dominant 3rd-order harmonics is >94 dB lower than the 1 kHz fundamental component, and the measured THD+N and SNR are 0.0028% and ~96 dB respectively.

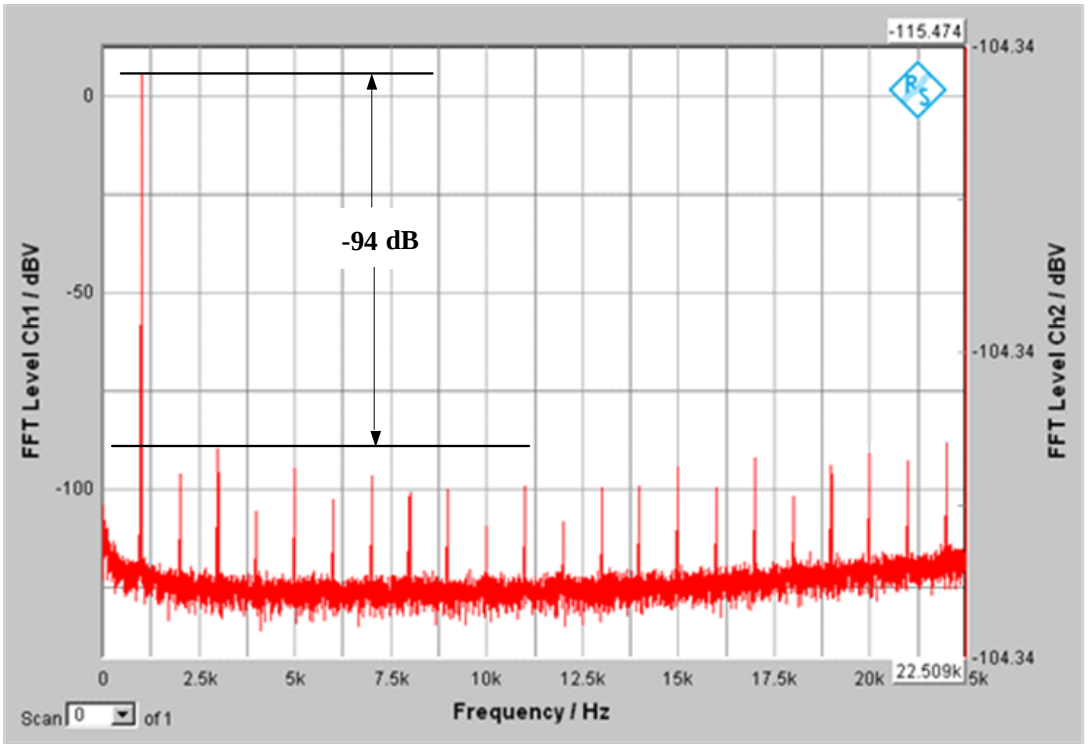


Figure 4-9 Spectrum of the output signal, V_{out} = 2 V_{rms} at 1 kHz

Figure 4-10 depicts the THD+N (%) versus the output power under different supply voltages. At nominal V_{DD} = 3.6 V, the minimum THD+N is a very low 0.0027% at 500 mW. When the output power increases to slightly over 800 mW, the THD+N remains very low, <0.01%.

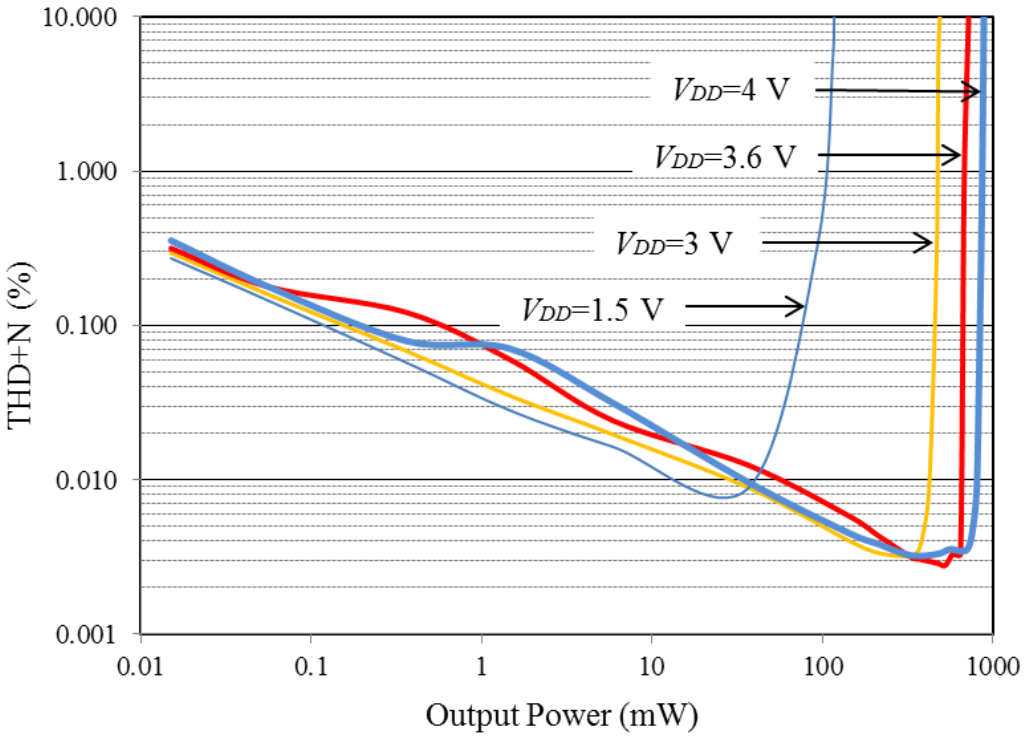


Figure 4-10 THD+N (%) versus output power (mW) at different voltage supplies when driving an 8 Ω load at f_{in} = 1 kHz

As designed, the CDA can operate over a large range of supply voltages, ranging from 1.2 V to 4 V. This versatility is important in one of our intended applications – devices powered by a rechargeable 1.2 V single-cell and for meeting stringent power requirements where there is no voltage regulation (also see PSRR later).

Figure 4-11 depicts the THD+N (%) versus the input signal frequency when delivering 500 mW to an 8 Ω load from V_{DD} = 3.6 V. The prototype CDA features excellent THD+N performance over a wide range of input frequencies, including THD+N = 0.0022% at 100 Hz and THD+N = 0.0027% at 1 kHz.

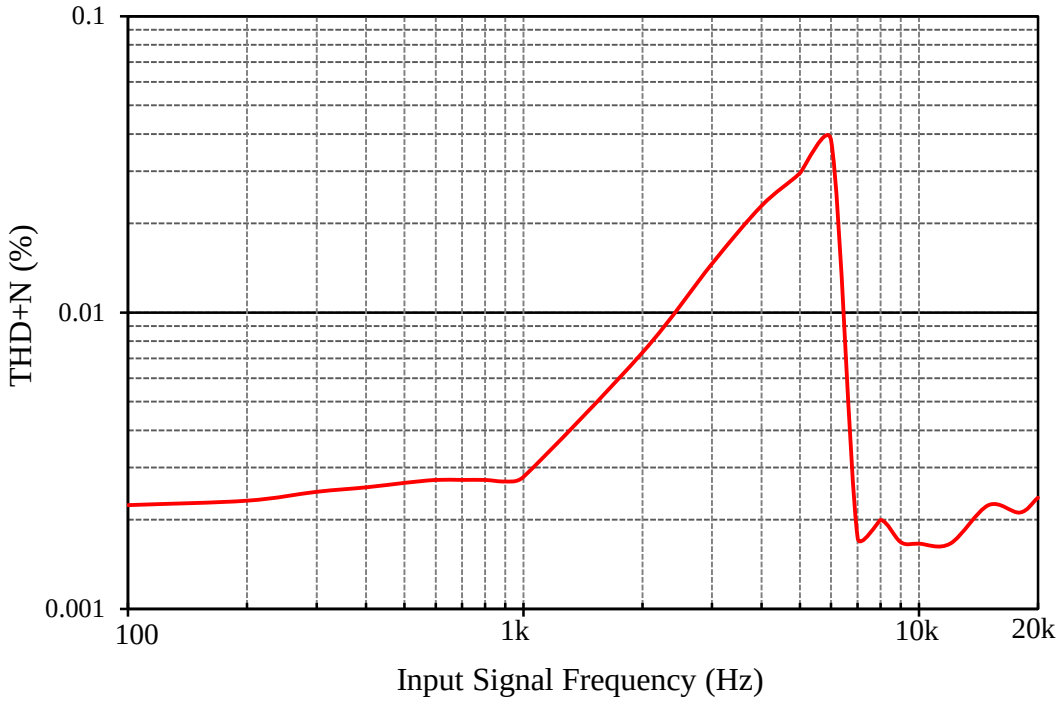


Figure 4-11 THD+N (%) versus input signal frequency (Hz) when delivering 500 mW to an 8 Ω load from V_{DD} = 3.6 V

For PSRR measurements, a noise signal, V_{ripple} = 200 mV_{pp}, at different frequencies is superimposed on V_{DD} = 3.6 V, and the input of the CDA is either grounded or floating. Figure 4-12 depicts the PSRR of the prototype CDA against the frequency of the supply noise. Of specific interest, the PSRR is very high at 217 Hz and 1 kHz, respectively PSRR = ~101 dB and PSRR = -90 dB, and the PSRR is largely dependent of whether the input is grounded or floating. The PSRR at these two frequencies are particularly pertinent for mobile applications as the radio frequency power amplifier in mobile devices may induce large magnitude supply noise at 217 Hz and 1 kHz when transmitting GSM and LTE signals respectively.

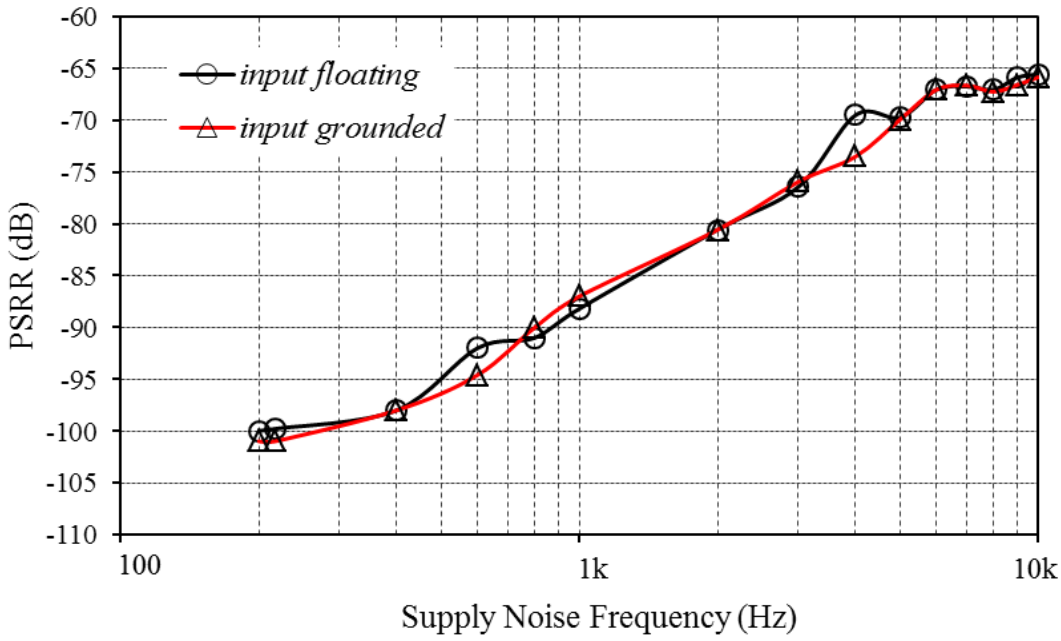


Figure 4-12 PSRR versus supply noise frequency (V_{DD} = 3.6 V and V_{ripple} = 200 mV_{pp})

In addition to PSRR, PS-IMD is another important parameter to qualify the supply noise rejection attributes of CDAs. Figure 4-13 depicts the spectrum of the output signal, V_{out} = 1 V_{rms} at 1 kHz when V_{DD} = 3.6 V and V_{ripple} = 200 mV_{pp} (-23 dBV_{rms}) at 217 Hz. The PS-IMDs with respect to the output signal and the noise are very low, -106.5 dB and -83.5 dB respectively. To ascertain the PSRR for a practical case, the PSRR is measured for V_{out} = 1 V_{rms}, and the PSRR remains a high 96.8 dB.

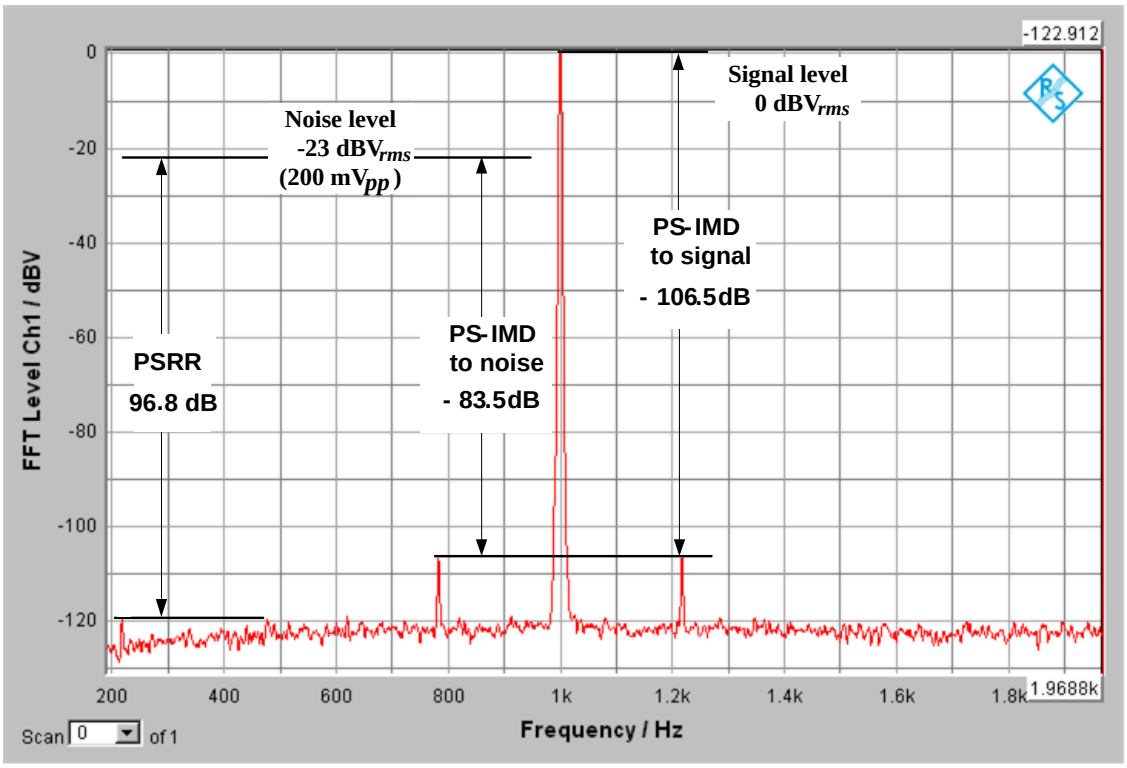


Figure 4-13 Spectrum of the output signal of V_{out} = 1 V_{rms} at 1 kHz when V_{DD}=3.6 V and V_{ripple} = 200 mV_{pp} (-23 dBV_{rms}) at 217 Hz

Figure 4-14 depicts the power-efficiency of the prototype CDA when driving different loads with V_{DD} = 3.6 V. The power-efficiency is a high 94% when delivering ~0.9 W output power to an 8 Ω load. With a 4 Ω load, the efficiency remains a high 85% when delivering ~1.8 W output power. In Figure 4-14, the maximum output power is defined when THD+N = 10%.

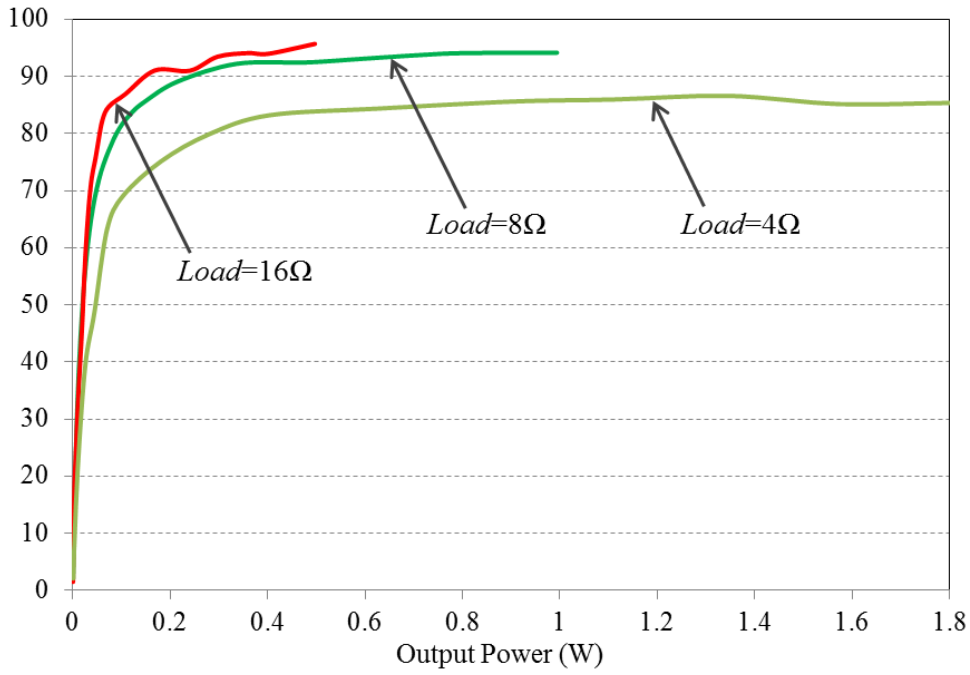


Figure 4-14 Efficiency (%) versus output power (W) when driving different loads from a 3.6 V supply (maximum output power is at THD+N = 10%)

Figure 4-15 depicts the spectrum of the output signal, V_{out} = 1 mV_{rms} at f_{out} = 1 kHz. It can be seen that the noise floor of the prototype CDA is low; and the A-weighted integrated noise from 20 Hz to 20 kHz is ~35 μV.

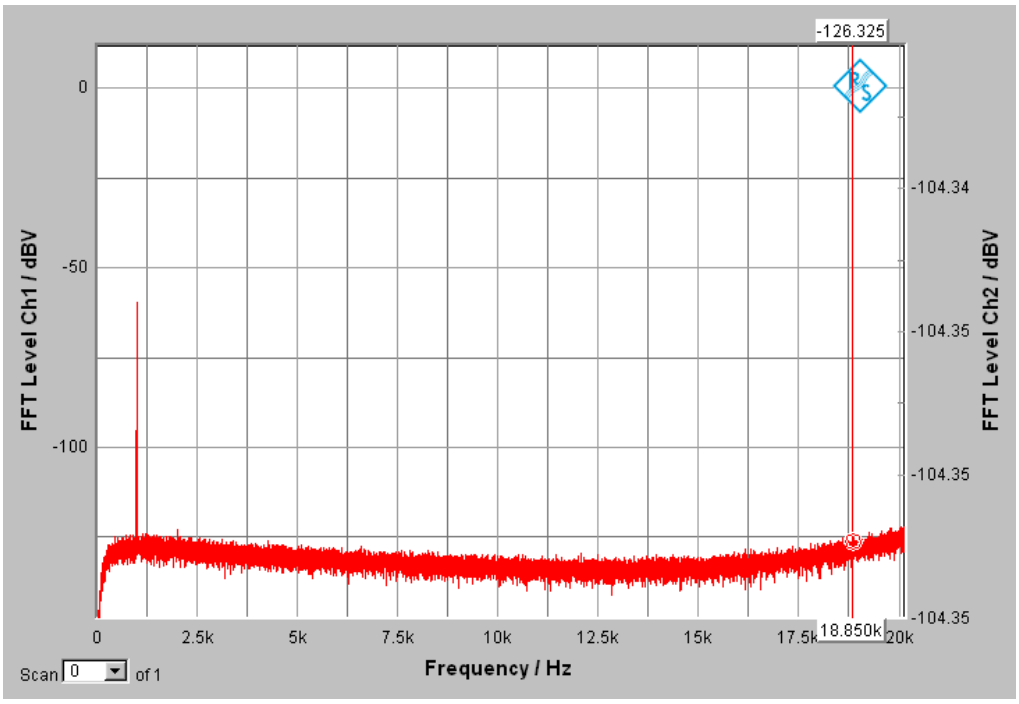


Figure 4-15 Spectrum of the output signal of V_{out} = 1 mV_{rms} at 1 kHz

The measurements of the prototype CDA are consolidated in Table 4-1, and are benchmarked against several state-of-the-art designs; for completeness other imperative parameters are also included thereto. The state-of-the-art designs are grouped according to their packaging types – lead-frame packages (QFN, QFP) and non-lead-frame-packages (wafer-level CSP) – CDAs in the two right-most columns are commercial CDAs.

Table 4-1 Performance benchmarking with reported state-of-the-art CDAs

References	this work	[53]	[4]	[55]	[19]	[20]	[89]	[16]	[18]
Package Type	Lead-Frame					Wafer-Level CSP			
PSRR@217 Hz	101	77	88	82	70	96	72.2	82	66
THD+N@1 kHz (%)	0.0027	0.02	0.018	0.02	0.0012	0.0012	0.028	0.04	0.004
SNR	97	94	92	100	116.5	103	97.5	103	103
Efficiency %	94	89	85.5	84	84.5	93	90.9	93	93
Pout max (W) @ THD+N=1% (8Ω)	0.85	0.25	1.15	0.35	1.45	3.6	0.725	1.8	1.84
Supply (V)	1.2-4	2.7	2.7-4.9	2.7	5	2.5-5.5	2.7-5.2	2.5-5.5	2.2-5.5
Single Cell (1.2V) Operation	Yes	No	No	No	No	No	No	No	No
I_q (mA)	3.1	0.25	3.02	0.55	24*	4	2	1.5	3.2
Load (Ω)	8	8	8	8	8	4 or 8	8	4	4
Architecture#	PWM	SMC	PWM	SMC	SMC	UPWM	PWM	PWM	ΔΣ
Switching (kHz)	320	450	320	380	600	1000	420	300	280
Process	65nm	0.5μm	0.18μm	0.5μm	0.7μm	0.25μm	0.18μm	-	-
Area (mm^2)	1.69	1.49	1.01	1.65	6	1.44	1.14	1.41	2.2
Package	QFN	QFP	LQFP	DIP	QFP	WLCSP	WLCSP	WLCSP	WLCSP
FOM_1 [9]	1260	126	40	96	9	1222	7	20	14
FOM_2	184.2	16.4	5.8	13.3	1.1	122.2	0.9	2.9	2.2

From Table 4-1, it can be seen that the prototype CDA features the highest PSRR of all benchmarked CDAs. Its THD+N is a low 0.0027% (when delivering 500 mW output power) and is much lower compared to all but two CDAs benchmarked. The power-efficiency is a high 94% and is the highest of all designs benchmarked. Of specific

interest, the prototype CDA is the only CDA that can operate with a supply voltage as low as 1.2 V and hence is able to operate from a single rechargeable cell.

To qualify the overall performance of all CDAs benchmarked, a previously reported [4, 20] Figure-Of-Merit (FOM), FOM_1, defined in eqn. (4.4) below is employed:

$$\mathrm{FOM}_1 = \frac{\eta}{I_q * (\mathrm{THD+N}) * \mathrm{PSRR} * 10^6} \tag{4.4}$$

where η and I_q are respectively the maximum efficiency (%) and the quiescent current (in mA) of the CDA. On the basis of this FOM_1, the prototype CDA features substantially higher FOM than all other CDAs packaged in the same lead-frame package. When compared against CDAs packaged in wafer-level CSP, it still features the highest FOM_1, although only slightly above one CDA.

It can be argued that because the reported FOM_1 does not take account of the EMI, an imperative specification for mobile devices, the FOM_1 is incomplete. To account for the EMI, we propose an alternative FOM, coined FOM_2, to include the EMI, which can partly be inferred from the switching frequency. As the EMI is only inferred, and to provide a balanced and meaningful FOM, the alternative FOM_2 is defined in eqn. (4.5), where the contribution of the switching frequency is a cube root:

$$\mathrm{FOM}_2 = \frac{\eta}{I_q * (\mathrm{THD+N}) * \mathrm{PSRR} * 10^6 * \sqrt[3]{f_{sw}}} \tag{4.5}$$

where f_{sw} is the switching frequency (in kHz) of the CDA. On the basis of FOM_2 and from Table I, the prototype CDA features significantly higher FOM than all benchmarked CDAs, independent of packaging.

In conclusion, the prototype CDA, on the basis of both the reported FOM_1 and the alternative FOM_2, is superior over the benchmarked state-of-the-art CDAs.

4.5 Conclusions

A very-high fidelity and very-high noise-immunity PWM CDA with low (and varying) switching frequency has been proposed. The proposed CDA featured said attributes without resorting to high switching frequency and/or complex multiple feedback loops by means of a novel input-modulated carrier generator and a novel phase-error-free modulator. Collectively these novelties permit the employment of very-high loop-gain, yet without compromising linearity/dynamic-range.

The prototype CDA, realized in 65 nm CMOS, and with V_{DD} = 3.6 V, achieved a THD+N of 0.0027% and a power-efficiency of 94% when delivering a 500 mW to an 8 Ω load. The PSRR of the prototype CDA was 101 dB @ 217 Hz and 90 dB @ 1 kHz, and the switching frequency was input-modulated with relatively low nominal ~320 kHz. The prototype CDA also featured a versatile supply voltage operating range with functionality for V_{DD} ranging from rechargeable single-cell of 1.2 V to standard smart device voltage of 4 V. Overall, on the basis of benchmarking against state-of-the-art CDAs, the prototype

CDA featured the highest PSRR, highest power-efficiency, very-low THD+N, wide V_{DD} operating voltage range, and highest Figures-of-Merit (FOM_1 and FOM_2).

Chapter 5 Fundamental Investigation into Ground-Bounce and Optimization

5.1 Introduction

A large portion of this chapter has been published as a US provisional patent [39], and submitted to IEEE Transactions on Power Electronics [43].

As aforementioned in Chapter 2 and as shown in Figure 5-2 (see later), a CDA typically comprises signal-processing analog circuits (including an integrator, a modulator, a carrier generator and a feedback network) and an output stage. The integrator provides high loop-gain to suppress unwanted noise and distortions. The modulator modulates the output of the integrator to a digital-like pulse signal. The output stage buffers the pulse signal and drives the loudspeaker load by turning on and off its output transistors. The feedback network feeds the output back to the integrator to form a closed-loop, thereby improving the linearity of the CDA by means of negative feedback. The modulation techniques include PWM, Bang-Bang, Sigma-Delta modulation and Self-Oscillation control. Yet irrespective of the modulation techniques, a congruity in the design of CDAs is the ground-bounce due to the switching operation of the CDA output stage. The ground-bounce is the large voltage spikes on the otherwise clean supply rails, potentially

resulting in significant reliability degradation and compromising the linearity of the CDA. Figures 5-1 (a) and (b) respectively depict the ideal and practical switching waveform of the output stage of the CDA. In the latter, the ground-bounce occurring immediately after the rise and fall of the waveform is apparent.

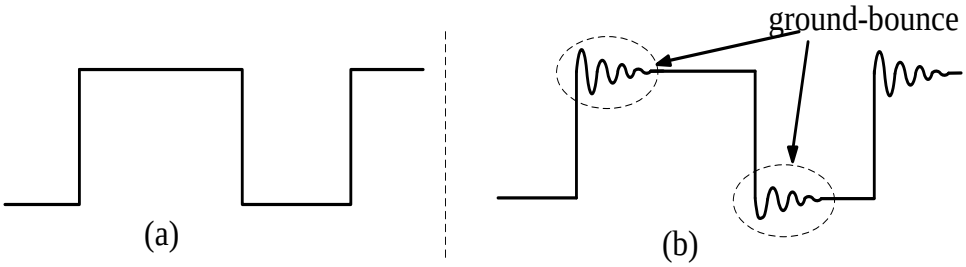


Figure 5-1 CDA output waveforms: (a) ideal, and (b) practical

The ground-bounce has been previously reported in the context of digital circuit designs [34, 36, 37, 90, 91]. Interestingly, despite the significance of the ground-bounce issues in CDAs, an investigation thereof is unreported in literature. Moreover, as the mechanisms of the ground-bounce in CDAs and its effects are very different from that in digital circuits, the design considerations for digital circuits may not be applicable for CDAs. Furthermore, at this juncture, the design methodologies to mitigate the effects of the ground-bounce in CDAs are lacking, save for some empirical methods, such as employing large decoupling capacitors (which could undesirably consume a large IC area). Surprisingly, some of these empirical methods may conversely and undesirably have adverse effects – for instance, we will show herein that a larger capacitance (to a certain point) may inadvertently exacerbate the ground-bounce and degrades the linearity of the CDA, qualified by Total Harmonic Distortion, THD.

In this chapter, we investigate the mechanisms of the ground-bounce in analog CDAs. The investigation includes the identification of the ground-bounce mechanisms, and derivation of analytical expressions to model the ground-bounce on power supply rails; to the best of our knowledge, this is the first-ever analytical investigation of the ground-bounce in CDAs. Based on these investigations, we show that although the ground-bounce on the supplies (V_{DD}) is usually larger than (or at least comparable to) that on the grounds (V_{GND}), the effect of the latter is dominant on the linearity of the CDA. In other words, to improve the linearity of the CDA, it is imperative that the ground-bounce on V_{GND} is mitigated. We further propose a 'ground-bounce-aware' design methodology – a systematic design methodology to minimize the ground-bounce and its effects on the linearity of the CDA. By means of a practical CDA design example, we show that the THD of a non-optimized CDA design can be reduced by 400% when the same CDA is optimized by our proposed 'ground-bounce-aware' methodology. The theoretical analyses derived herein are verified by HSPICE simulations using a commercial 65nm CMOS process.

This chapter is organized as follows. In Section 5.2, an overview of the ground-bounce in CDAs is provided, followed by a delineation of its detrimental effects on the CDA performance, including reliability and linearity. In Section 5.3, the mechanisms of the ground-bounce are investigated and identified, and their analytical expressions thereafter derived. In Section 5.4, we propose the 'ground-bounce-aware' design methodology to mitigate the detrimental effects of ground-bounce. In Section 5.5, the

analytical results are verified by HSPICE simulations, and conclusions are drawn in Section 5.6.

5.2 Effects of Ground-Bounce

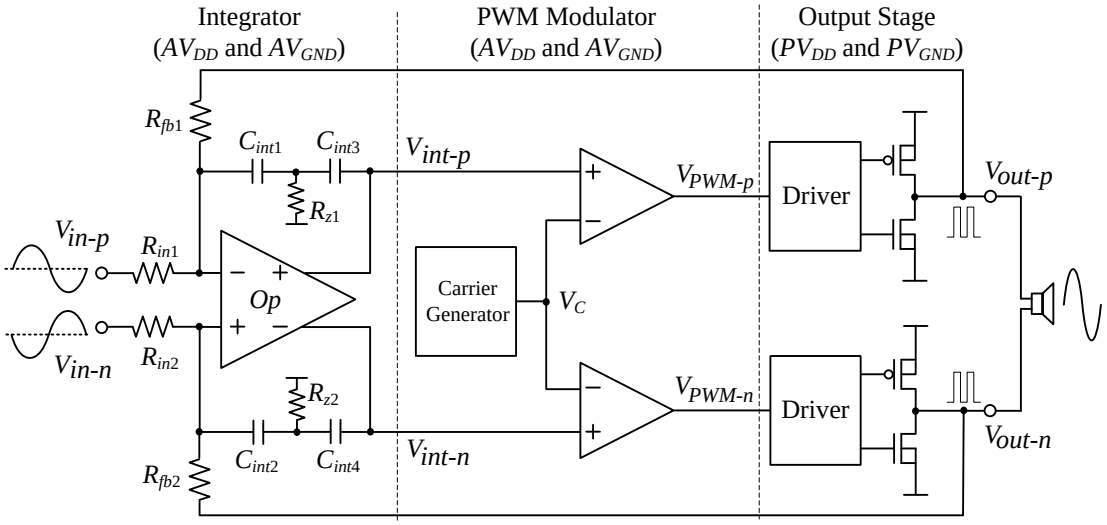
We first provide an overview of the ground-bounce in CDAs, followed by the investigation of its effects on CDAs.

5.2.1 Overview of Ground-Bounce

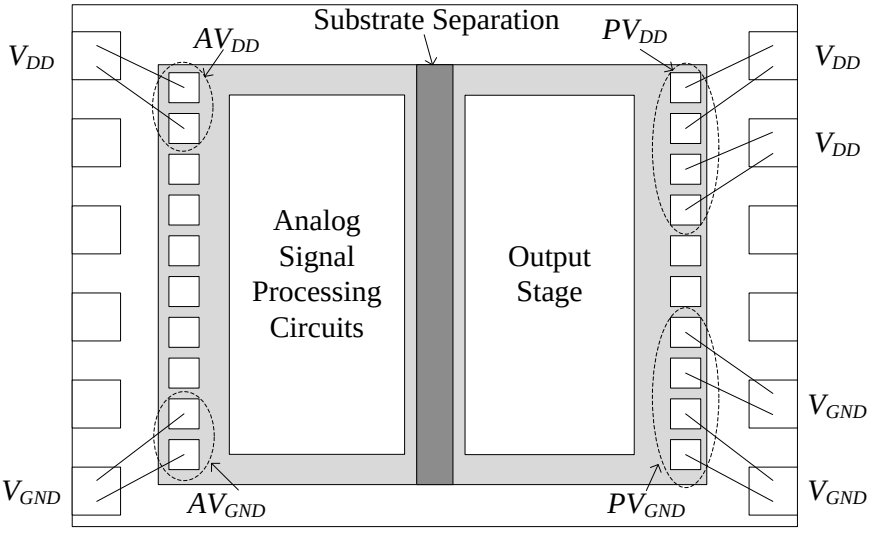
Figure 5-2 (a) and (b) respectively depict the schematic of a typical PWM Bridged-Tied-Load (BTL) CDA, and its floor plan and bonding diagram (where V_{DD} and V_{GND} are respectively the supply and ground on the PCB). For ease of nomenclature, the nodes of the top differential half and bottom half are given subscript *p* and *n* respectively. For example, the input, integrator output, PWM output and CDA output in the top half are $V_{in\text{-}p}$, $V_{int\text{-}p}$, $V_{PWM\text{-}p}$ and $V_{out\text{-}p}$ respectively. To reduce the effect of ground-bounce, the following well-accepted design methods are normally adopted. The analog signal processing circuits therein (including the integrator, carrier generator and PWM modulator) and the output stage are powered separately, by analog V_{DD} (AV_{DD}) and analog ground (AV_{GND}), and power V_{DD} (PV_{DD}) and power ground (PV_{GND}) respectively. Further, they are placed in two separate regions with a substrate isolation block placed in between (to reduce the substrate coupling) and sometimes, an in-situ decoupling capacitor(s) is

placed between PV_{DD} and PV_{GND} and/or AV_{DD} and AV_{GND}. Multiple power pins and/or multiple bonding wires may be used to reduce the bonding wire inductance (hence reducing the ground-bounce).

These methods are empirical where in general, the number of power pads (and pins) and/or bonding wires is as many as tolerated, the substrate isolation is as wide as tolerated, and the decoupling capacitors as large as tolerated – 'tolerated' herein is largely design/specification dependent and often cost constrained. Put simply, as the methods are largely empirical, they are not necessarily optimized.



(a)



(b)

Figure 5-2 (a) Schematic of a PWM CDA and (b) its floor plan and bonding wires

The ground-bounce persists in both the output stage and the analog signal processing circuits, undermining both the reliability and linearity of the CDA. Specifically, due to the switching operation of the output stage and the inductance of the bonding wires, ground-bounce is generated on PV_{DD} and PV_{GND}. The ground-bounce is coupled to AV_{DD} and AV_{GND} of the analog signal processing circuits from PV_{DD} and PV_{GND} through the substrate and Electrostatic Discharge (ESD) protection circuits. On the other hand, the analog signal processing circuits *generate* little ground-bounce as they largely operate in linear mode (vis-à-vis switching in the output stage) and their bias current (and power dissipation) is nearly constant. Nevertheless they are susceptible to the voltage disturbances caused by the ground-bounce. It is imperative to minimize its effects on CDAs – hence the imperativeness for the investigation of the mechanisms thereto.

5.2.2 Effects of the ground-bounce on CDAs

The two major effects of the ground-bounce on CDAs, the degradation of the reliability and the degradation of the linearity, will now be described in turn.

5.2.2.1 Degradation of the reliability

The ground-bounce on PV_{DD} and PV_{GND} is large – it will be shown later in Sections 5.3 and 5.4 that the ground bounce can easily be >30% of the supply voltage (e.g. >1V for mobile applications whose nominal supply is 3.7V). This is because of the switching of large output transistors in the output stage (typically, very wide transistor width in mm to obtain a low on-impedance [4]) and the ensuing switching of large output current (several hundred mA to several A, depending on the output drive). Consequently, the maximum V_{DD} is higher than the nominal V_{DD}, and if it exceeds the safe-operating range of the transistors, the reliability is degraded and device failure might occur.

In practical designs, it is hence imperative that the maximum spike of the ground-bounce is limited to within the safe range, where no transistor is unduly over-stressed. To this end, the pertinent design parameters and a practical design methodology will be delineated later in Sections 5.3 and 5.4.

5.2.2.2 Reduced linearity

The ground-bounce may result in linearity deterioration because of jitter and erroneous PWM pulses. These will now be described in turn.

(a) Jitter

It is well-established that jitter noise degrades the linearity of CDAs, including THD [92]. To illustrate the mechanisms of increased jitter noise due to ground-bounce, consider the schematic design of a typical carrier generator and the waveforms of its signals in Figure 5-3. The triangular-wave carrier is generated by alternately charging and discharging a capacitor, C_c, and switched according to the voltage difference between the carrier and predetermined voltage reference, V_R. Ideally, with zero ground-bounce, V_R is a constant voltage (of either upper or lower threshold voltage) and there is no jitter noise. However, with ground-bounce, V_R is disturbed, thereby introducing uncertainty on the switching timing, hence jitter noise, as illustrated in Figure 5-3. The larger the ground-bounce on AV_{GND}, the larger the carrier jitter noise is. In short, the ground-bounce may lead to increased carrier jitter noise.

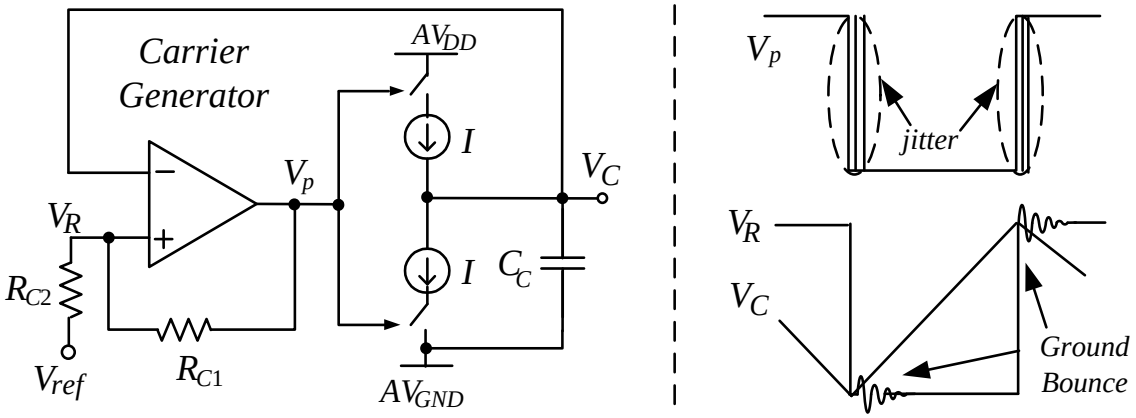


Figure 5-3 Schematic of a carrier generator and its waveforms

(*b*) *Erroneous PWM pulses*

In addition to jitter, the ground-bounce may also degrade the linearity of the CDA by introducing errors into PWM pulses, such as false switching or error in the pulse width. This is because the 'disturbances' (due to ground bounce) at the integrator outputs ($V_{int\text{-p}}$ and $V_{int\text{-n}}$) and at the carrier output (V_C) are different. To illustrate the mechanisms of erroneous PWM pulses, consider a practical case in Figs. 5-4 (a) and (b) which respectively depicts the critical ground-bounce coupling paths (drawn as dashed lines) from the various ground-bounce 'sources' ($V_{out\text{-}p}$, AV_{GND} and AV_{DD}) to the integrator output ($V_{int\text{-}p}$) and the carrier (V_C). For sake of simplicity, only the upper differential branch of the op-amp, *Op*, is depicted in Fig. 5-4 (a). $M_{n\text{-}p}$ and $M_{p\text{-}p}$ are the output stage transistors of the op-amp, *Op*.

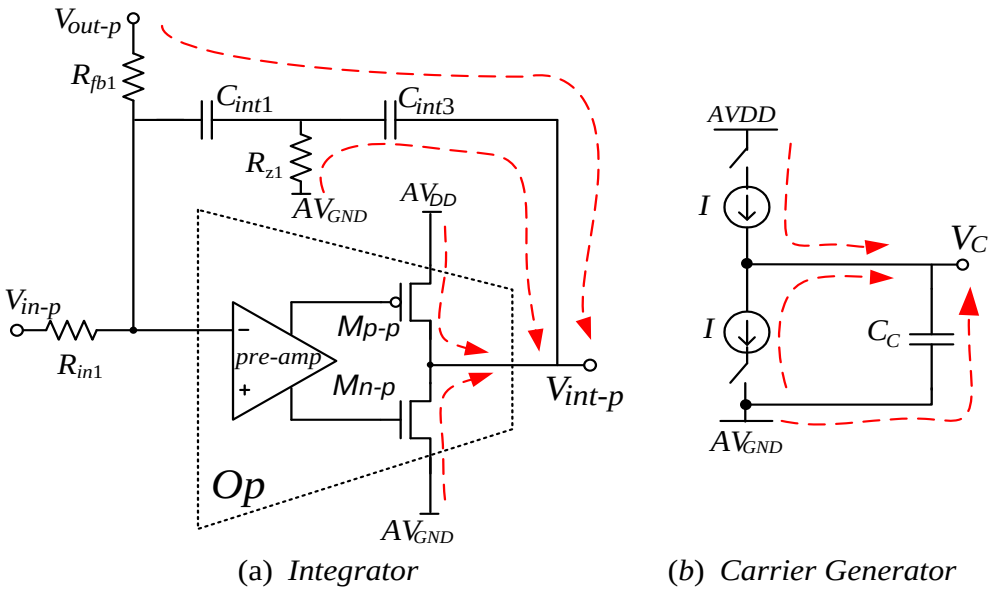


Figure 5-4 Ground-bounce coupling: (a) Integrator, and (b) Carrier Generator

As depicted in Figures 5-4 (a) and (b), there are four coupling paths in the integrator and three coupling paths in the carrier generator. The ensuing noise at $V_{int\text{-}p}$ is different from the noise at V_C. Specifically, the noise at $V_{int\text{-}p}$ is due to ground-bounce on PV_{DD} and PV_{GND} ($V_{out\text{-}p}$ is connected to PV_{DD} and PV_{GND} through output power transistors; see Fig. 2(a)), and on AV_{GND} and AV_{GND}, and is coupled through R_{fb1}, C_{int1}, C_{int3}, R_{z1} and $M_{p\text{-}p}$ and $M_{n\text{-}p}$. On the other hand, the noise at V_C is mainly due to ground-bounce on AV_{DD} and AV_{GND}, and is coupled through two current mirrors (current source, I) and C_C. This difference between the noise at $V_{int\text{-}p}$ and at V_C is interesting and arguably somewhat counter-intuitive because the ground-bounce is typically assumed to be common noise. Conversely, because of this difference and depending on the degree of difference (magnitude and phase), false switching(s) might inadvertently occur. For instance, a scenario of false switching in a practical CDA is depicted in Figure 5-5, where the

ground-bounce noise disturbs V_C markedly while the disturbance to $V_{int\text{-}p}$ is lesser. The consequential difference causes false switching.

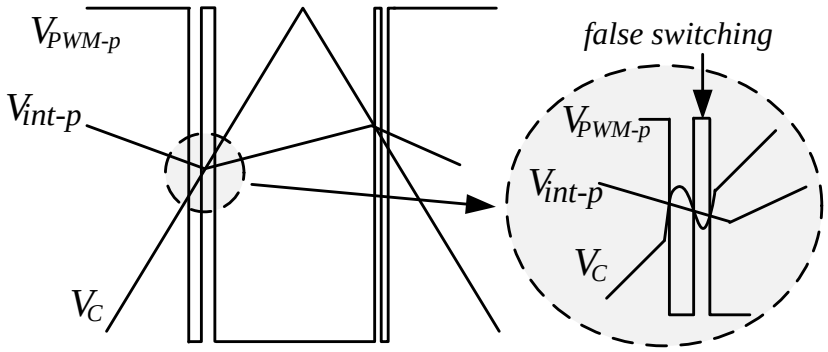


Figure 5-5 A false switching in a PWM signal

Given the false switching, one approach would be to use a comparator with a wide hysteresis (whose difference between the upper and lower thresholds is larger than the noise) and long(er) response time to desensitize the comparator to the noise across its inputs. However, in PWM CDAs, a comparator is used as the PWM modulator, which typically features small-to-moderate hysteresis (a few mVs) and relatively short response-time (a few nanoseconds) because a large hysteresis and/or long response time reduces the output dynamic range of the CDA and increases the overall delay. Furthermore, the ground-bounce spikes can be as high as a few hundred mVs and hence, a hysteresis of this range is practically unrealistic.

Put differently, the comparator is impervious to the ground-bounce noise only if the magnitude of the noise is small (lesser than the hysteresis of the comparator) and

transiently fast-changing (high-frequency). This will be further elaborated upon in Sections 5.3 and 5.4.

5.3 Mechanisms of Ground-Bounce

Given the imperativeness of ground-bounce, it will now be analytically investigated and this serves as a preamble to a proposed practical technique to minimize the effects of ground-bounce on CDAs. The investigation involves first, the identification of various ground-bounce mechanisms and later, the derivation of analytical expressions of the ground-bounce at PV_{DD}, PV_{GND}, AV_{DD} and AV_{GND}. These expressions are particularly insightful as the pertinent design parameters to reduce ground bounce will be identified.

To investigate ground-bounce, the CDA can be modeled as depicted in Figure 5-6. The various elements in this model are as follows: L_{p1} and L_{p2} are the respective inductance of the bonding wires to PV_{GND} and PV_{DD}, and L_{a1} and L_{a2} the respective inductance to AV_{GND} and AV_{DD}. V_{DD} and V_{GND} are the supply rails on the PCB and are assumed to be noise-free, as they are on PCB where large and multiple decoupling capacitors are typically used; in real-life, this is reasonable assumption because the noise at V_{DD} and V_{GND} are much smaller than at PV_{DD}, PV_{GND}, AV_{DD} and AV_{GND}. C_A and C_P are the respective decoupling capacitor for the analog signal processing circuits and the output stage, and R_A and R_P their respective series (parasitic) resistor. C_I and R_I are the respective equivalent capacitor and resistor (due to substrate coupling and due to the parasitic capacitance of the ESD protection circuits) between AV_{GND} and PV_{GND}.

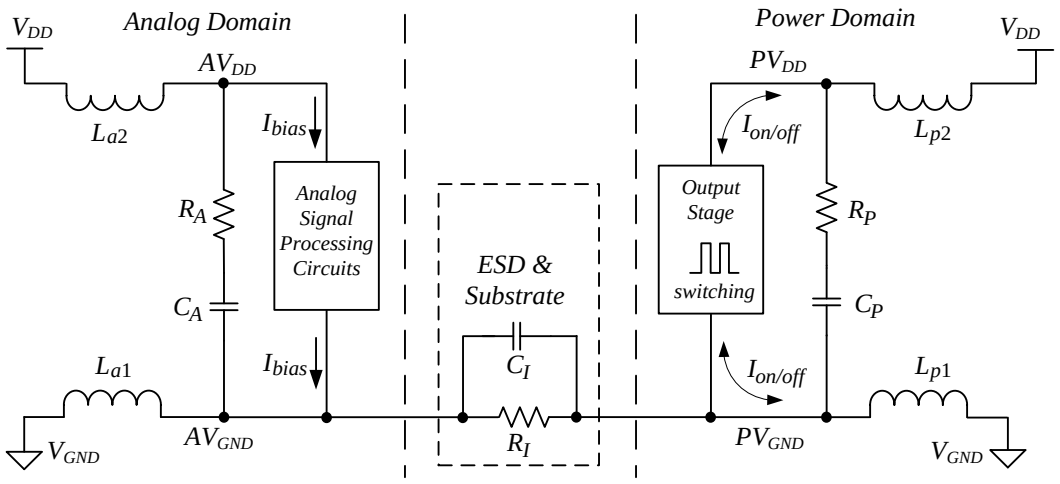


Figure 5-6 Supply rails connections in a typical CDA

Practically, the power drawn from the supply rails is dominated by the output stage (the analog signal processing circuits draw little power by comparison) and hence the dominant noise source is at PV_{GND} and PV_{DD}. The coupling between PV_{DD} and AV_{DD} is negligible compared to that between PV_{GND} and AV_{GND}. This is because there is no direct connection between PV_{DD} and AV_{DD} in the substrate, and often no ESD protection circuits between PV_{DD} and AV_{DD}. Consequently, the ground bounce on AV_{DD} and AV_{GND} is primarily due to the ground bounce on PV_{GND} instead of PV_{DD}. It is hence apparent that to reduce the ground bounce on AV_{DD} and AV_{GND}, it is imperative that ground bounce on PV_{GND} is low. The ground-bounce at PV_{DD} and PV_{GND}, and at AV_{DD} and AV_{GND} will now be investigated in turn.

5.3.1 Ground-bounce on PV_{DD} and PV_{GND}

The investigation herein includes the identification of various ground-bounce mechanisms and the derivation of the analytical expression of ground-bounce on PV_{DD} and PV_{GND}.

5.3.1.1 Mechanisms of Ground-bounce

To investigate the ground-bounce on PV_{DD} and PV_{GND}, the waveforms and current flow in a CDA output stage are first analyzed. Consider a practical CDA BTL output stage depicted in Figure 5-7 (a), where transistors M_{p1} and M_{n1} and transistors M_{p2} and M_{n2} are the output inverters of the opposing ends of the BTL output. The load placed in between these opposing ends of the BTL output is modeled by load resistance R_L and inductance L_L [4, 28]. The switching sequence for a practical BTL output stage, including the dead-time to eliminate short-circuit current, is well-established [79]. The waveforms of a complete switching sequence for $I_{out}>0$ is depicted in Figure 5-7 (b).

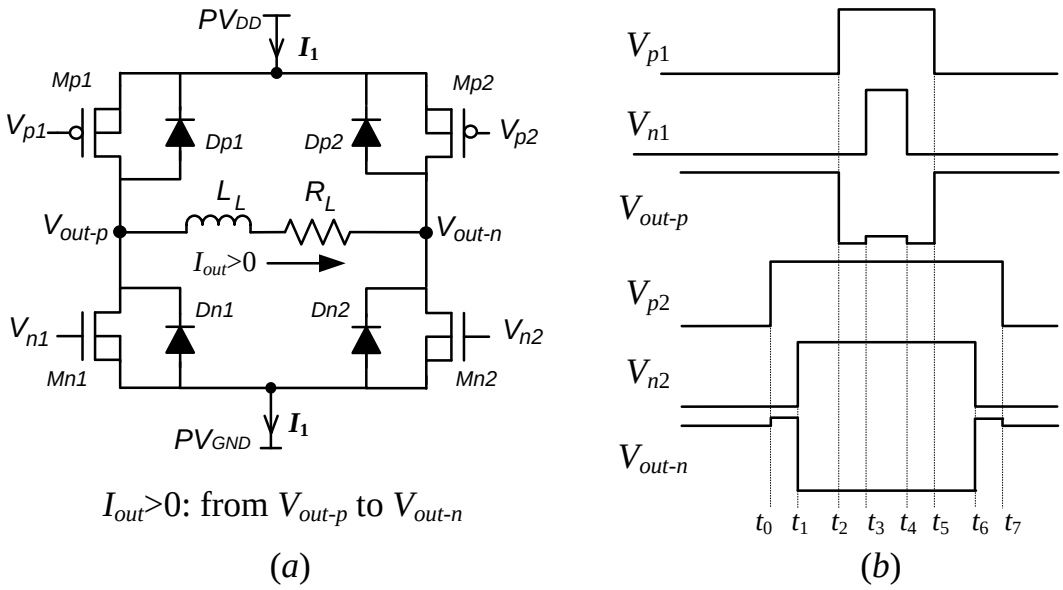


Figure 5-7 BTL output stage (a) Schematic, and (b) For I_{out}>0, the waveforms at V_{p1}, V_{n1}, $V_{out\text{-}p}$, V_{p2}, V_{n2} and $V_{out\text{-}n}$

Figure 5-8 depicts the switching sequence and the current flow path for I_{out}>0 at different switching instances; the current flow for I_{out}<0 can be similarly analysed. For sake of clarity, the circuit elements that have current flow are drawn in black while the remaining are in grey.

From Figures 5-7 and 5-8, we can show that the ground-bounce on PV_{DD} and PV_{GND} is primarily due to Mechanisms I and II, which are now described in turn.

Mechanism I: Change of current flow in PV_{DD} and PV_{GND}

When the output voltage, $V_{out\text{-}p}$ or $V_{out\text{-}n}$, transitions from PV_{DD} to PV_{GND} (or vice versa), the current flow in the supply rails changes. For instance, it can be seen from Figures 5-8 (b) and (c) that at t_1, the current in PV_{DD} (and PV_{GND}) changes from no current

to sourcing (and sinking) current. This change of current flow at PV_{DD} and PV_{GND} consequently leads to the ground-bounce thereat.

Mechanism II: Charge redistribution of parasitic capacitors

When transistors in the output stage are switched on and off, the voltages across their parasitic capacitors change, and charges on the parasitic capacitors redistribute accordingly. This charge redistribution subsequently leads to a change in the current flow in the power supply rails, and hence the ground-bounce. For instance, Figure 5-9 depicts the parasitic capacitors, C_{gsp}, C_{gdp} and C_{dsp} of output transistors M_{P2}, and C_{gsn}, C_{gdn} and C_{dsn} of M_{N2} of one branch of the BTL output stage, and their voltage (in square parentheses) during $t_0<t<t_1$ and during $t_1<t<t_2$, where R_{Don} is the on-impedance of the driver circuits of the output transistors. It is apparent from Figure 5-9 that at t_1, the voltage across capacitors C_{gdp}, C_{dsp}, C_{gdn} and C_{dsn} changes. The current change at other switching instances can be similarly analysed.

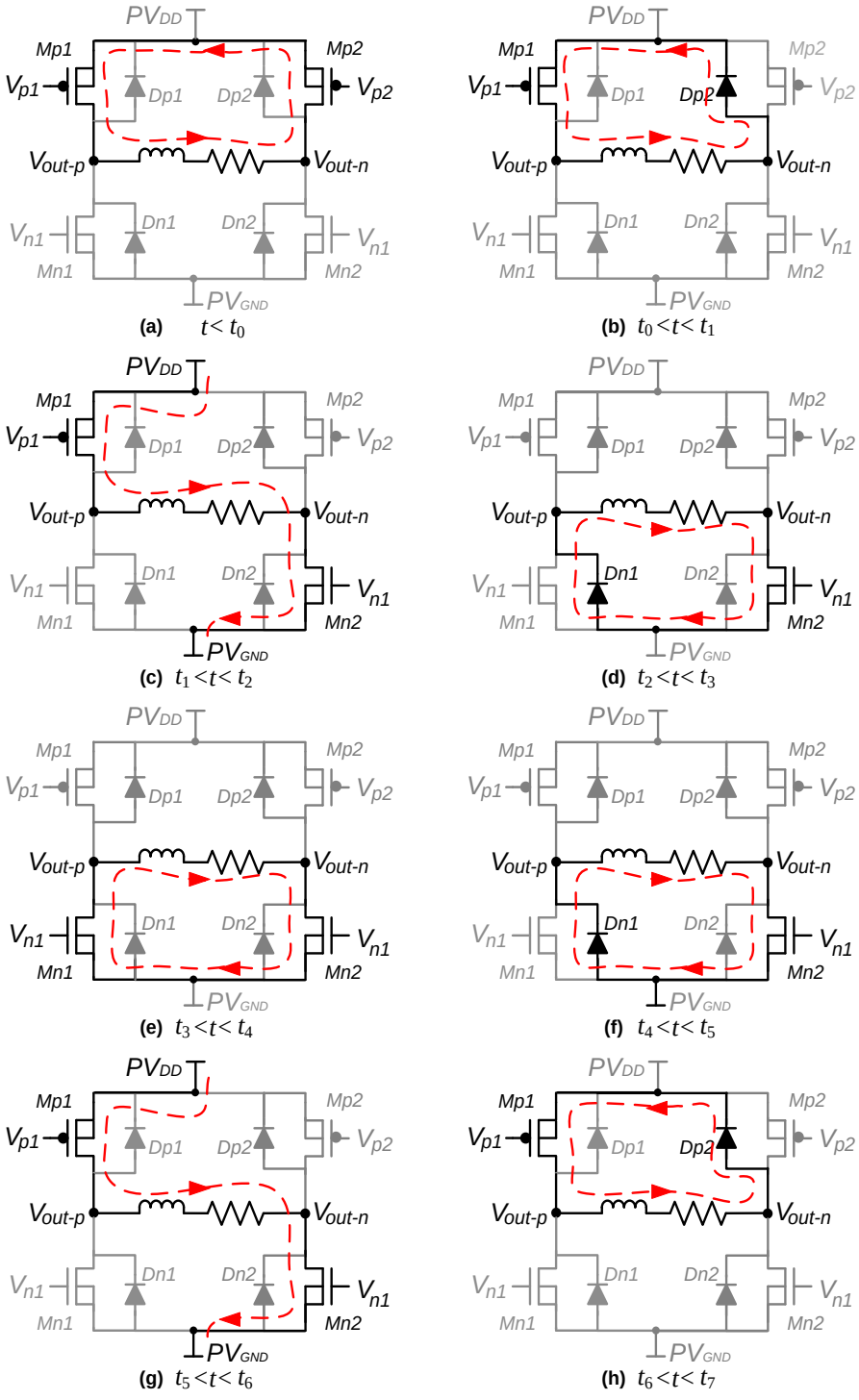


Figure 5-8 Current flows in the BTL output stage

for I_{out}>0 at different switching instances

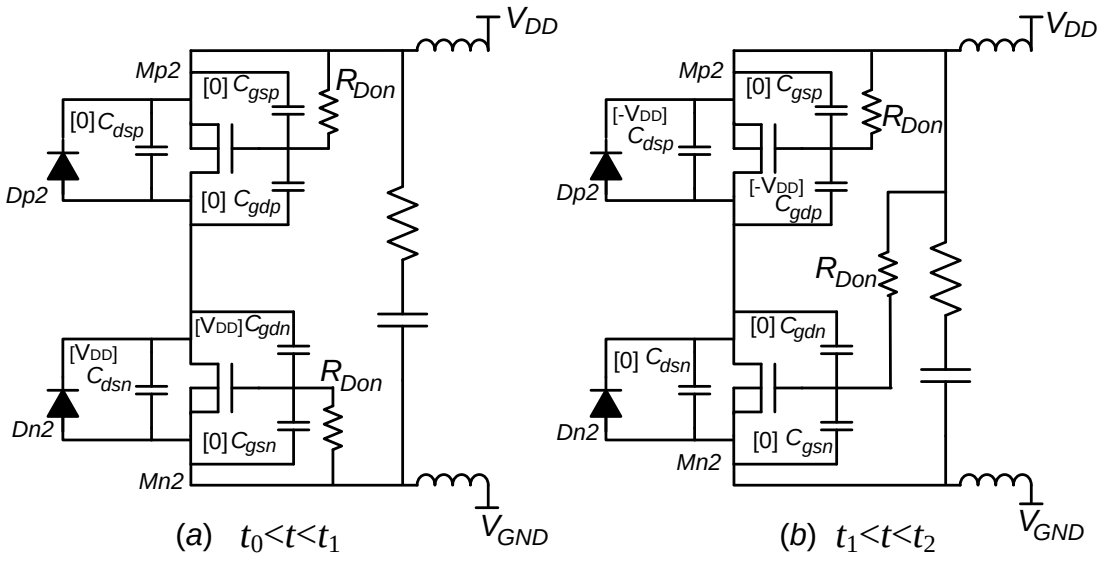


Figure 5-9 Schematic of the output transistors and the voltages (in square parenthesis) of their associated parasitic capacitors for (a) $t_0<t<t_1$ and (b) $t_1<t<t_2$

Table 5-1 tabulates the current change (when $I_{out} > 0$) due to the two mechanisms, where '↑', '↓' and '–' respectively represent increase, decrease and no change in current flow. It can be seen that for $I_{out}>0$, at t_1 and t_5, the changes of current flow due to the Mechanisms I and II are in the same direction, resulting in a change (of current flow) of larger magnitude than that due to Mechanism I or II alone. On the other hand, at t_2 and t_6, the change of current flows due to mechanisms I and II are in opposing directions, resulting in a smaller current flow change than that due to Mechanism I or II alone. There is no change of current flows at other time instances.

Table 5-1 Change of current flow in PV_{DD} and PV_{GND} due to Mechanisms I and II

Time / Mechanism	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7
I	–	↑	↓	–	–	↑	↓	–
II	–	↑	↑	–	–	↑	↑	–

In short, it is apparent that that the worst case ground-bounce for $I_{out}>0$ on PV_{GND} and PV_{DD} occurs at t_1 and at t_5; the same for $I_{out}<0$ can be similarly analysed. We will now analytically derive expressions of the worst case ground-bounce on PV_{DD} and PV_{GND} at t_1 (the ground-bounce at t_5 is the same) for $I_{out}>0$.

5.3.1.2 Analytical Derivation of Ground-Bounce

Figure 5-10 depicts the model of the output stage immediately after t_1, i.e. $t \geq t_1^+$ (Figure 5-9), where C_g and R_g are respectively the parasitic capacitance (comprising C_{gdp}, C_{dsp}, C_{gdn} and C_{dsn}) at the output node and its effective series resistor. As transistor M_{n2} is on, the output V_{outn} is shorted to PV_{GND}. The on-impedance of M_{n2} is negligible in this analysis as it is significantly smaller than R_g.

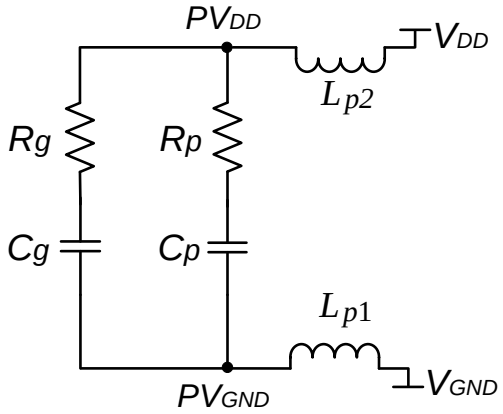


Figure 5-10 Analytical model of the output stage for $t \geq t_1^+$

As depicted in Figure 5-10, the ensuing equivalent network is an *LRC* tank. It has been shown [35] that the ground-bounce is similar to a damped sinusoidal wave and its

analytical expression can be defined by three parameters: the maximum voltage (V_{max}), frequency (f_{GB}) and damping factor (p).

From our derivations in the Appendix herein, V_{max} can be derived as eqn. (5.1a):

$$V_{max} = V_{IC} + V_{CR} \tag{5.1a}$$

$$V_{IC} = \left(I_{out} - \frac{V_{CR} T_{rise}}{L_{p1} + L_{p2}} \right) \sqrt{\frac{L_{p1} + L_{p2}}{C_p + C_g}} \tag{5.1b}$$

$$V_{CR} = \frac{C_g V_{DD}}{C_p + C_g + \frac{T_{rise}^{\ 2}}{2\left(L_{p1} + L_{p2}\right)}} \tag{5.1c}$$

where V_{IC} and V_{CR} are respectively due to ground-bounce Mechanisms I and II. T_{rise} is the rising time for V_{n2} to increase from V_{THN} to (V_{DD}-|V_{THP}|), where V_{THN} and V_{THP} are the threshold voltages of *n*-type and *p*-type transistors respectively, and V_{max} is the maximum voltage swing across the decoupling capacitor, C_p. The respective maximum voltage swing for PV_{GND} and PV_{DD}, V_{max1} and V_{max2}, can be hence expressed as:

$$V_{max1} = V_{max} \frac{L_{p1}}{L_{p1} + L_{p2}} \tag{5.1d}$$

$$V_{max2} = V_{max} \frac{L_{p2}}{L_{p1} + L_{p2}} \tag{5.1e}$$

The ground-bounce frequency, f_{GB}, and the damping factor, p, of the *LRC* network in Figure 5-10 can be derived as:

$$f_{GB} = \frac{1}{2\pi} \sqrt{\frac{-b + \sqrt{b^2 + 4a}}{2a}} \tag{5.2a}$$

where

$$a = C_p\left(L_{p1} + L_{p2}\right)\left({R_g}^2{C_g}^2 + {R_p}^2{C_p}^2\right) - {R_g}^2{C_g}^2{R_p}^2{C_p}^2 \tag{5.2b}$$

$$b = \left(L_{p1} + L_{p2}\right)\left(C_g + C_p\right) - {R_p}^2{C_p}^2 - {R_g}^2{C_g}^2 \tag{5.2c}$$

$$p = -\frac{1}{2R_{eq}C_{eq}} \tag{5.3a}$$

where

$$R_{eq} = \left[R_p \times \left(1 + {Q_1}^2\right)\right]//\left[R_{on} \times \left(1 + {Q_2}^2\right)\right] \tag{5.3b}$$

$$C_{eq} = C_p \times \frac{{Q_1}^2}{1 + {Q_1}^2}//C_g \times \frac{{Q_1}^2}{1 + {Q_1}^2} \tag{5.3c}$$

$$Q_1 = \frac{1}{2\pi f_{GB}C_pR_p} \tag{5.3d}$$

$$Q_2 = \frac{1}{2\pi f_{GB}C_gR_{on}} \tag{5.3e}$$

From the aforesaid derivations, PV_{GND} (with ground-bounce) can finally be derived as eqn. (5.4a):

$$PV_{GND}(t) = \begin{cases} \dfrac{V_{CR}}{T_{rise}}\left(\dfrac{L_{p1}}{L_{p1} + L_{p2}}\right)t & , t < T_{rise} \\ V_{max1}e^{p(t - T_{rise})}\cos\left[2\pi f_0 t - \cos^{-1}\left(\dfrac{V_{CR}}{V_{max}}\right)\right], & t \geq T_{rise} \end{cases} \tag{5.4a}$$

Similarly, the ground-bounce at PV_{DD} can be derived:

$$PV_{DD}(t) = \begin{cases} \dfrac{V_{CR}}{T_{rise}}\left(\dfrac{L_{p2}}{L_{p1} + L_{p2}}\right)t & , t < T_{rise} \\ V_{max2}e^{p(t - T_{rise})}\cos\left[2\pi f_0 t - \cos^{-1}\left(\dfrac{V_{CR}}{V_{max}}\right)\right], & t \geq T_{rise} \end{cases} \tag{5.4b}$$

Intuitively and as delineated previously in Section 5.2, to reduce the adverse effect of ground-bounce, it is desirable that V_{max} be low, and both f_{GB} and p high. Our derived eqns. (5.1a)-(5.4b) provide much more insights – from these equations, we can show that important circuit parameters affecting ground-bounce (V_{max}, f_{GB} and p) include C_p, C_g, T_{rise}, and L_p. The effects of these parameters on the ground-bounce in CDAs will now be delineated in turn.

i) C_p

From eqns. (5.1a)-(5.1c), it can be seen that the larger the C_p, the smaller the V_{max}. This is congruous with the general understanding within the design community that a larger decoupling capacitor reduces the ground-bounce.

In this sense, a larger C_p is preferred, whenever there is available silicon space or a large IC can be tolerated. However, from eqns. (5.2a)-(5.2c), it becomes apparent that increasing C_p inadvertently reduces f_{GB}, hence potentially reducing the linearity of the CDA. To the best of our knowledge, this is not reported or largely unrecognized within the CDA design community – although this is somewhat counter-intuitive, it can be easily explained. Specifically, as delineated earlier in Section 5.2, analog circuits are more susceptible to ground-bounce with lower frequency and this will be verified later in Section 5.5.

In practical designs, we recommend an adequate C_p capacitance be used to ensure the maximum ground-bounce spike (as can be predicted using eqn. (5.1a)) is within the safe range. However, the employment of a C_p larger than adequate should be refrained – in short, the usual practice of designing C_p to be as large as possible is

not always beneficial (i.e. it may conversely exacerbate the effect of ground-bounce); see Figures 5-13 and 5-14 later.

ii) C_g

From eqns. (5.2a)-(5.2c), it can be seen that the larger the C_g, the lower the f_{GB}. The effect of C_g on V_{max}, on the other hand, is not as simple – a larger C_g may result in a higher or lower V_{max}, depending on other parameters (e.g. L_p, C_p).

From a practical design perspective, C_g is largely determined by the size of the output transistor, which is in turn designed to the targeted load and/or efficiency. Put simply, C_g is 'pre-determined' by the output transistors design and can be thereafter used for ascertaining other parameters.

iii) T_{rise}

From eqns. (5.1a)-(5.1c), it can be seen that the larger the T_{rise}, the smaller the V_{max}. This is intuitive because a larger T_{rise} results in slower switching, and therefore smaller ground-bounce.

Although it is tempting to design for a large T_{rise}, other pertinent design aspects should be considered. Specifically, T_{rise} is directly determined by the tapering ratio of the driver design – the ratio of the size the driver to its corresponding output transistor. This ratio affects not only the efficiency of the output stage but also the linearity of the CDA. A large T_{rise} would require an even larger dead-time to avoid short-circuit current, and the longer dead-time in turn increases the distortion of the CDA. Further, a large T_{rise} results in non-ideal switching (slow ramping) at the BTL outputs, deteriorating the linearity [71].

Based on our experience, for a good compromise we recommend a tapering ratio in the range of 15 to 30, and T_{rise} can thereafter be ascertained by simple simulations.

iv) L_p (L_{p1} and L_{p2})

From eqns. (5.1a)-(5.2c), it can be seen that a larger L_p undesirably leads to a larger V_{max} and a higher f_{GB}. Hence it is imperative to reduce L_p.

In practical designs, L_p is determined by the package type and the number of pads/pins used. If an advanced package solution, such as wafer-level-packaging, is available, L_p can be very low – in the range of tens of pico H. However, if a typical wire-bonding package is used, L_p can easily be a few nano H. To reduce L_p, multiple parallel bonding-wires may be used to reduce the effective L_p. Nevertheless, there is a point of diminishing return to the effect of reduced L_p from an increased number of bonding wires.

5.3.2 Ground-bounce on AV_{DD} and AV_{GND}

As delineated earlier, the ground-bounce on AV_{DD} and AV_{GND} is primarily from the coupling (via substrate and ESD) between AV_{GND} and PV_{GND}. On the basis of Figure 5-6, we model this in Figure 5-11 to derive the ground-bounce at AV_{GND} and AV_{DD}, where R_{ASP} represents the equivalent resistance of the analog circuits, and $R_{ASP} \approx V_{DD}/I_{Bias}$ (where I_{Bias} is the total current consumed by the analog circuits). As I_{Bias} is small (usually <5mA), R_{ASP} is significantly higher than the impedance of C_a and its parasitic resistance R_a at f_{GB}.

Hence, the effect of R_{ASP} on ground-bounce is negligible, and therefore neglected in the following analysis.

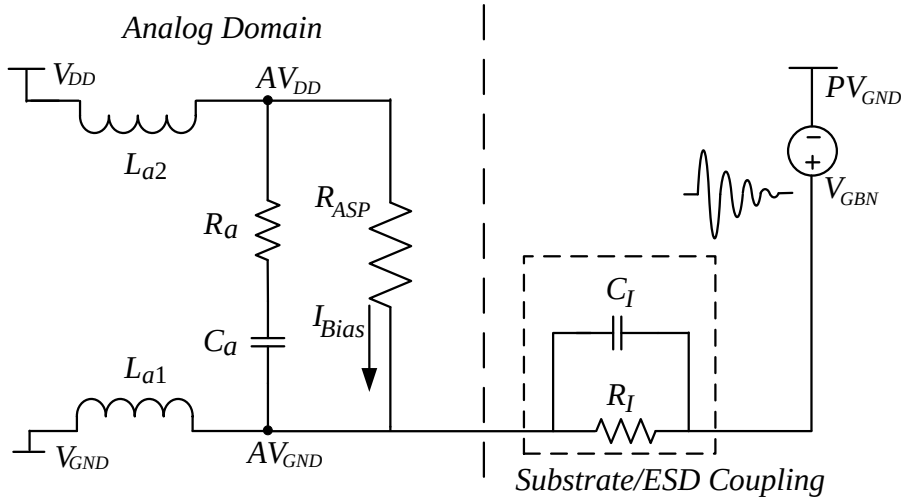


Figure 5-11 Ground-bounce coupling to Analog domain

Based on Figure 5-11, the ground-bounce noise at AV_{GND}, $V_{GB\text{-}AGND}$, due to ground-bounce noise at PV_{GND}, V_{GBN}, can be approximated:

$$V_{GB-AGND} = V_{GBN} \times \frac{Z_a}{Z_a + Z_c} \tag{5.5}$$

where Z_c is the impedance of the substrate/ESD coupling network (C_I//R_I) and Z_a the impedance of the power network (comprising L_{a1}, L_{a2}, C_a and R_a) in the analog domain. It can be seen from eqn. (5.5) that, to reduce the ground-bounce at AV_{GND}, Z_a should be decreased and/or Z_c increased.

In practical designs, there is little design freedom for Z_c. This is because substrate isolation solely depends on the process and the unoccupied area (typically minimum for cost considerations) between analog and power domain. The ESD network, on the other hand, is typically determined by ESD protection requirements. Conversely, Z_a can be

designed to be optimal and this will now be derived – for a given Z_c, the smaller the Z_a, the smaller the ground-bounce at AV_{GND}.

From Figure 5-11, it can be seen that Z_a is:

$$Z_a = j\omega L_{a1} // \left(j\omega L_{a2} + R_a + \frac{1}{j\omega C_a}\right) = \frac{j\omega L_{a1}\left[j\left(\omega L_{a2} - \frac{1}{\omega C_a}\right) + R_a\right]}{j\left[\omega(L_{a1} + L_{a2}) - \frac{1}{\omega C_a}\right] + R_a} \tag{5.6}$$

where $\omega = 2\pi f_{GB}$.

From eqns. (5.5) and (5.6), it can be easily inferred that:

(i) In the best case, Z_a is minimum, and the ground-bounce correspondingly minimized if $C_a = C_{a,opt}$, where

$$C_{a,opt} = \frac{1}{(2\pi f_{GB})^2 L_{a2}} \tag{5.7a}$$

(ii) In the worst case, Z_a is maximum, and the ground-bounce correspondingly maximized if $C_a = C_{a,worse}$, where

$$C_{a,worst} = \frac{1}{(2\pi f_{GB})^2 (L_{a1} + L_{a2})} \tag{5.7b}$$

Put simply, to minimize ground-bounce on AV_{GND}, C_a should be designed to $C_a = C_{a,opt}$. There are several interesting observations herein that may be counter-intuitive:

(a) If $C_a < C_{a,worst}$, increasing C_a inadvertently increases the ground-bounce on AV_{GND};

(b) If $C_{a,worst} < C_a < C_{a,opt}$, increasing C_a leads to a reduced ground-bounce; and

(c) If $C_a > C_{a,opt}$, further increasing C_a will not have marked effect on ground-bounce.

An example to delineate (a)-(c) is given in Section 5.5. In short, C_a, as expected, has a marked effect on ground-bounce AV_{GND} to a point, and thereafter increasing C_a is of diminishing return.

5.4 Ground-Bounce-Aware Design Methodology

We have delineated the effects and mechanisms of ground-bounce on CDAs, and analytically investigated the ground-bounce. Based on said analyses, we will now propose a ground-bounce-aware design methodology to minimize said effects.

We propose that the analog domain and power domain power networks be co-designed in the following manner.

Step 1: Determine the size of the output transistors of the output stage, based on the power-efficiency and power requirements of the CDA;

Step 2: Extract the parasitics of the output stage;

Step 3: Choose the tapering ratio, T_a, for the output stage drivers, noting that a large T_a reduces the ground-bounce, but at the expense of increased output stage non-linearity. A good compromise is $15<T_a<30$.

Step 4: Determine L_p, based on the package type and the number of pads and pins available for power connections.

Step 5: Determine C_p using eqn. (5.1a), such that V_{max} is limited to ensure safe operation of the output transistors. We recommend not increasing C_p beyond said determined value, for the reasons delineated earlier in Section III.

Step 6: Determine f_{GB} using eqn. (5.2a).

Step 7: Determine C_a, based on f_{GB} and using eqn. (5.7a). The ground-bounce is now at its theoretical minimum for the analog circuits.

This proposed methodology provides a design flow to minimize the effects of the ground-bounce in a CDA. The reliability of the CDA is guaranteed (as V_{max} is limited) and the ground-bounce is at its theoretical minimum for the analog circuits. An example for a practical CDA design will now be illustrated – this example will also be used in Section 5.5; see Figures 5-15 and 5-16.

Consider the design of a 1W CDA whose specifications are tabulated in Table 5-2.

Table 5-2 Specifications of a practical 1W CDA

Specification	Value
Power	1W
V_{DD}	3.6V
Load	4Ω
Power-efficiency	>90%

Abiding by the proposed methodology, the steps are as follows:

Step1: From the1W output power and power-efficiency of >90%, the width of the output transistors are respectively 1.2mm and 3mm for NMOS and PMOS. The minimum length is 280nm for I/O transistors.

Step 2: Parasitic capacitors of the output transistors are extracted; see Table 5-2.

Step 3: A tapering ratio of 20 is used; the ensuing T_{rise} is ~200ps based on simulations.

Step 4: Based on a 5mmx5mm QFN package, and five and three bonding-wires are for PV_{GND} and PV_{DD} respectively, L_{P1}=1nH, and L_{P2}=1.5nH are obtained from EM simulations.

Step 5: From eqn. (5.1a), C_p=120pF, such that the maximum ground-bounce, V_{max}, is less than 30% of V_{DD}.

Step 6: From eqn. (5.2a), f_{GB} is ~260MHz.

Step 7: From eqn. (5.7a), the optimal C_a=~150pF, with L_{a1}= L_{a2}=2.5nH.

We will show later in Figure 5-16 that the ensuing CDA features a THD that is very close to the ideal zero ground-bounce case.

5.5 Results and Verification

In this section, the derived expressions of the ground-bounce in eqns. (5.1a)-(5.7b) are verified against HSPICE simulations for a CDA based on a commercial 65nm process (the I/O transistors in this process have minimum length of 280nm). Further, we show that the proposed design methodology in Section 5.4 substantially improves the performance of a PWM CDA, specifically the THD. Table 5-3 tabulates the parameters used in the derived analytical expressions for a 1W practical CDA.

Table 5-3 Parameters of a practical 1W CDA (also see Table 5-2)

Parameter	Value	Comments
T_{rise}	200ps*	Post-layout simulations
C_g	30pF	Post-layout simulations
R_g	2.5Ω	Post-layout simulations
R_p	0.5Ω	Post-layout simulations
C_I	2pF	Post-layout simulations
R_I	10Ω	Estimated, based on substrate resistance
I_{out}	360mA	At modulation index M=0.8

* the tapering ratio, T_a=20

Ground-bounce in the power domain

To depict the transient ground-bounce waveforms at the PV_{GND} in the power domain, Figure 5-12 depicts the analytical prediction from eqn. (5.4a) and that obtained from HSPICE simulations of a practical CDA output stage design. In this design, C_p is 120pF, and L_{p1}=1nH and L_{p2}=1.5nH. The analytically predicted waveform shows a good agreement with HSPICE simulations, thereby validating derived eqn. (5.4a).

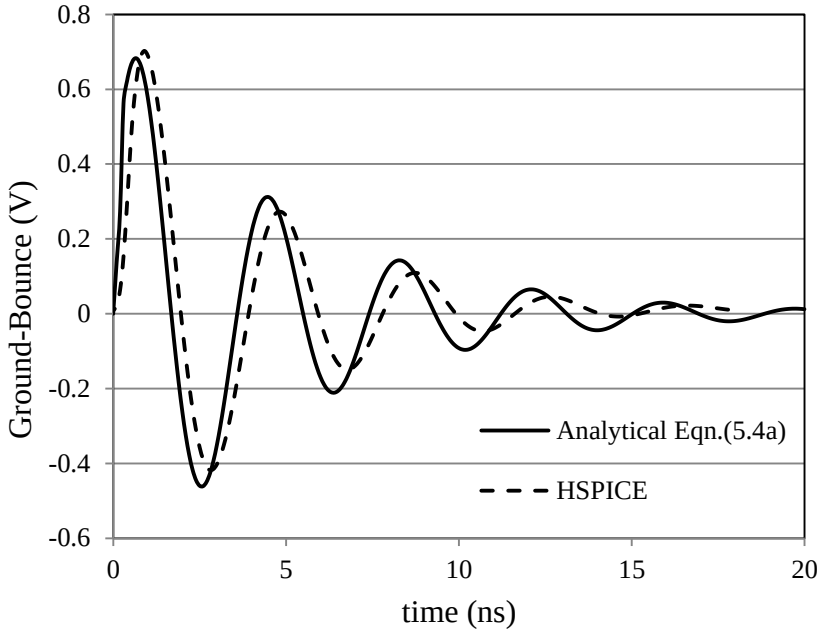


Figure 5-12 Ground-bounce waveforms at PV_{GND}

To depict the maximum voltage of the ground-bounce at PV_{GND} in the power domain with respect to decoupling capacitor C_P, Figure 5-13 depicts the analytical predictions from eqn. (5.1a) and HSPICE simulations for two cases, L_P=0.4nH and L_P-=1.2nH. The analytical predictions for both examples agree well with HSPICE simulations, thereby validating derived eqn. (5.1a).

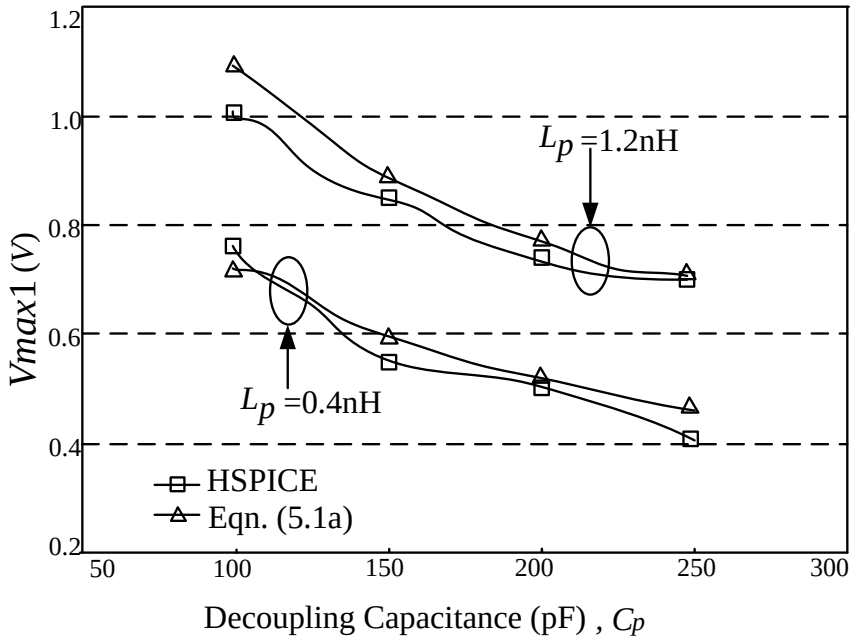


Figure 5-13 Maximum voltage of ground-bounce at PV_{GND}

It can be seen from Figure 5-13 that, as expected, V_{max1} increases with increasing L_P inductance, and decreases with the increasing C_P capacitance. These results corroborate our earlier analysis that the smaller parasitic inductance and/or the larger decoupling capacitor, C_p, the lesser is the maximum voltage, V_{max1}, of the ground-bounce. Nevertheless, it should be noted that the relationship between V_{max} and L_P (and/or C_P) is not linear – doubling L_P (or C_P) does not double (or half) the V_{max1}. For the reasons delineated earlier, the size of C_P should be carefully considered.

To depict the frequency, f_{GB}, of the ground-bounce at PV_{GND} for different L_P and C_P, Figure 5-14 depict the analytical predictions in eqn. (5.2a) and HSPICE simulations of f_{GB}. The analytical predictions again agree well with HSPICE simulations, thereby validating eqn. (5.2a).

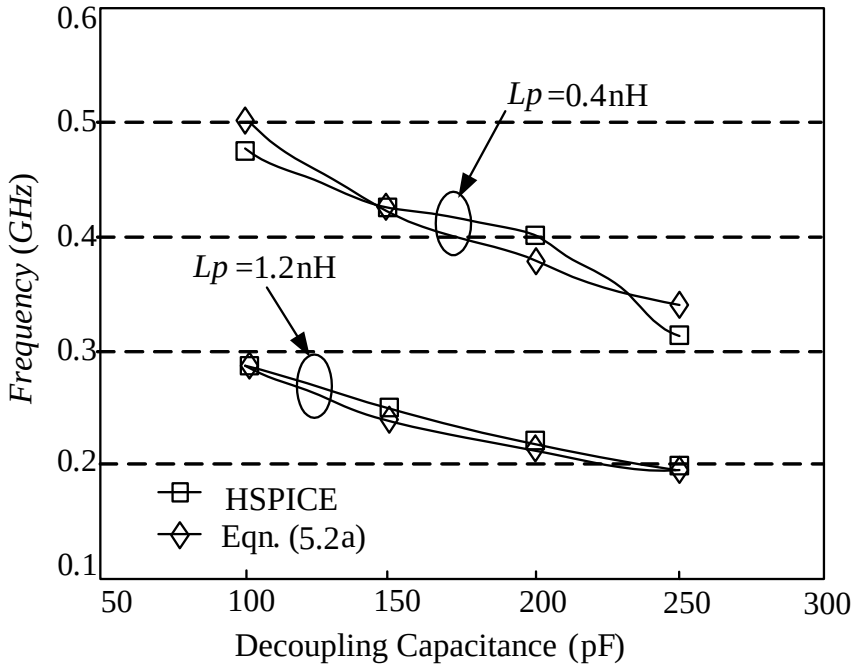


Figure 5-14 f_{GB} of ground-bounce at PV_{GND}

It can be seen from Figure 5-14 that the larger the L_P (or C_P) is, the lower is f_{GB}. It is as expected because a larger inductance (or capacitance) in a *LC* tank results in a lower resonant frequency. In the perspective of CDA designs, a large decoupling capacitor can potentially exacerbate the ground-bounce effect on analog circuits, because the ground-bounce noise is "slower" and, as delineated before, more likely to negatively affect the comparators.

Ground-bounce in analog domain

Consider the same practical CDA design where for the output stage, C_P=120pF, L_{P1}=1nH, L_{P2}=1.5nH and the ensuing f_{GB}=~260MHz, and for analog circuits, L_{a1}=L_{a2}=2.5nH.

To depict the effect of C_a by means of derived eqns. (7a) and (7b), consider three cases – Case 1: optimal C_a=150pF, Case 2: worst-case C_a=70pF, and Case 3: mid-case (but smaller capacitance than worst case) C_a=10pF. Figure 5-15 depicts the ground bounce with these different C_a cases.

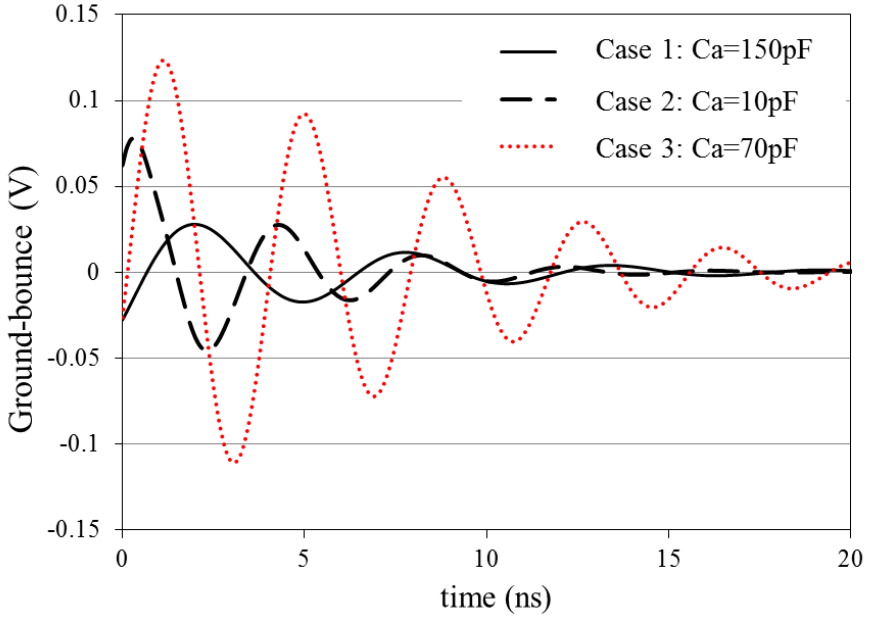


Figure 5-15 Ground-bounce at AV_{GND} with different C_a

As expected, Case 1, optimal C_a, yields the lowest ground-bounce; the Case 2, worst-case C_a, leads to the largest ground-bounce and worst THD. As delineated earlier in Section 5.3, the mid-case C_a, despite it being a *smaller* capacitance than the worst-case, yields the mid ground-bounce and mid THD – better than the worst-case. This is perhaps somewhat unexpected, because intuitively a larger decoupling capacitor provides a more stable ground, i.e. smaller ground-bounce. Put succinctly, in CDA designs, simply increasing the decoupling capacitor is not recommended – instead, the designer could judiciously choose the size of the decoupling capacitor(s), which is largely dependent on

other design parameters such as the (parasitic) inductance of the V_{DD} and V_{GND} connections, decoupling capacitors used in the power domain, etc.

Ground-bounce effects on THD of a PWM CDA

Following section *B* above, the effect of different C_a capacitances to THDs (due to ground-bounce) of a closed-loop 2nd-order integrator PWM CDA is depicted in Figure 5-16. The input signal frequency is 1 kHz and the output power is 300mW on a 4Ω load. All the circuit conditions and parameters are the same, save for the seven different C_a capacitances. For completeness, the case with zero ground-bounce is also plotted, where the THD is ~0.015%; this THD is due to mechanisms elsewhere within the practical CDAs [4, 33]. The ensuing THDs depict the imperativeness of reducing ground-bounce.

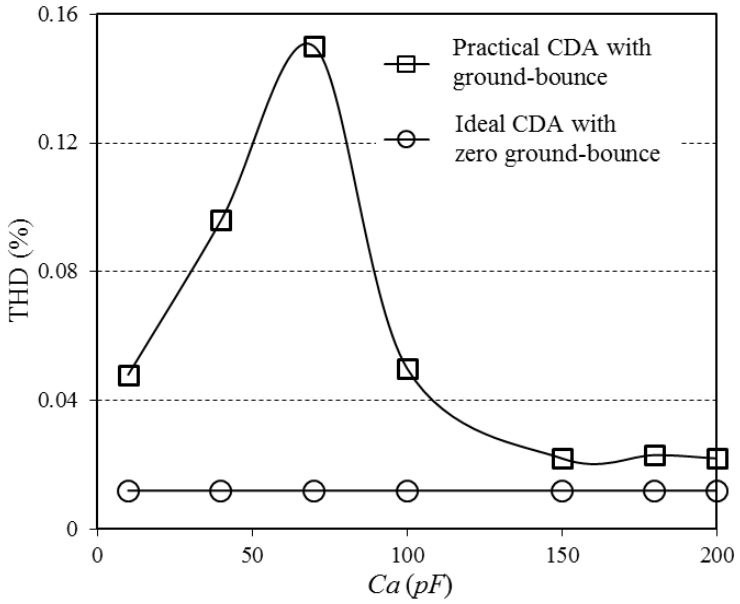


Figure 5-16 THD of a closed-loop PWM CDA (Figure 5-2 (a)) with different C_a capacitances

It can be seen from Figure 5-16 (and Figure 5-15) that, with all other parameters unchanged, the selection of C_a has a marked effect on ground-bounce and the ensuing THDs, where the THD can be reduced by ~400% (between best-case C_a=150pF and worst-case C_a=70pF), a significant ~12dB reduction. This observation corroborates our analysis that ground-bounce significantly affects the THD of CDAs. Furthermore, the comparison between the seven different cases reaffirms our assertion that an increased decoupling capacitor does not guarantee improvement in THDs; in fact, it may have an adverse effect.

In summary, the proposed methodology in Section 5.4 is useful as a ground-bounce-aware design methodology for ascertaining values of C_a and C_p for an optimized design in terms of minimizing ground-bounce.

5.6 Conclusions

We have investigated the ground-bounce noise problem from a fundamental basis, with emphasis towards CDAs, and have ascertained their ensuing effects in CDAs, particularly reliability and linearity (THD). This investigation is particularly useful because the mechanisms of ground-bounce was derived, providing useful insights to CDA designers. On the basis of said investigation, we have proposed a systematic ground-bounce design methodology to optimize (minimize) the ground-bounce. The efficacy of the proposed design methodology has been demonstrated for a practical design where the

CDA embodying said methodology featured ~400% THD improvement over a non-optimized design.

Chapter 6 Conclusions and Recommendations

In this chapter, conclusions will be drawn for the work reported in this Ph.D. program, and recommendations for future work delineated.

6.1 Conclusions

The broad objective of this Ph.D. program pertained to the analysis and design of CDAs, specifically the Bang-bang CDAs and the PWM CDAs for ultra-power-critical devices and high-quality multimedia devices respectively in the *next-generation* applications thereof. The conclusions of research work drawn for these CDAs, and for CDAs in general, will now be delineated.

Chapter 1 delineated the motivations of this Ph.D. research program and the specific objectives of the aforesaid broad objective.

In Chapter 2, CDAs have been comprehensively reviewed, including the different modulation schemes, the output stage design and the load filter (and filterless CDAs) design. Subsequently, an in-depth review of the design and/or analysis of PWM and Bang-bang CDAs was provided. This in-depth review in part focused on the most recent

developments of PWM and Bang-bang CDAs, and offered insights into the limitations of current designs. The review also highlighted aspects of CDA designs that remain incomplete in literature.

In Chapter 3, the mechanisms of and the circuit parameters affecting the IMD of Bang-bang CDAs have been investigated and the analytical expressions of the IMD derived. It has been shown that the even-order IMD, previously unknown/unreported, could be dominant at nominal operating conditions vis-à-vis the commonly-known odd-order IMD. On the basis of said analytical expressions, to obtain good IMD, it is imperative to design Bang-bang CDAs with low on-impedance, low hysteresis, relatively high switching frequency and with small offsets. In addition, the trade-offs between IMD and other imperative specifications of Bang-bang CDAs including power-efficiency and PSRR were also delineated.

In Chapter 4, a novel PWM CDA design has been proposed. The proposed design circumvented the undesirable and inevitable trade-offs (between imperative specifications) in conventional PWM CDA designs, and simultaneously achieved low distortion, high noise-immunity, high power-efficiency and low EMI. The proposed design embodied two innovations – an input-modulated carrier generator and a (probably first-ever) phase-error-free PWM modulator. These two innovations, individually and collectively, permitted the adoption of very-high loop-gain, hence increasing the PSRR, yet without exacerbating the distortions arising from the intermodulation between residual switching components and the carrier.

The prototype CDA IC was measured to verify the efficacy of the proposed design. The prototype CDA simultaneously achieved very-low THD+N of 0.0027% and very-high PSRR of 101 dB while delivering over 500 mW to an 8 Ω load. Its power-efficiency was a high 94%, and its switching frequency was a low 320 kHz and varying, hence reduced EMI. On the basis of both reported and proposed Figures-of-Merit, the proposed CDA was shown to be superior to reported state-of-the-art designs.

In Chapter 5, the ground-bounce in CDAs has been investigated from a fundamental basis. On the basis of the investigation, the mechanisms of and the circuit parameters affecting the ground-bounce have been ascertained and the associated analytical expressions derived. The effects of ground-bounce on CDAs, particularly reliability and linearity (THD), were also identified. This investigation is particularly valuable because it provided useful insights into the ground-bounce in CDAs and, on the basis of said analysis, a systematic ground-bounce-aware design methodology was proposed to optimize (minimize) the ground-bounce. The efficacy of the proposed design methodology has been demonstrated for a practical design where the CDA optimized with said methodology featured ~4x THD improvement over the same CDA without said optimization.

Overall, this Ph.D. program has made significant contributions towards the analysis and design of *next-generation* Bang-bang CDAs and PWM CDAs for ultra-power-critical devices and high-quality multimedia devices.

6.2 Recommendations for Future Work

On the basis of the literature review and the research work in this research program, the following research work is recommended:

(i) Investigation into the design of filterless Bang-bang CDAs without incurring excessive power overheads over conventional Bang-bang CDAs

The currently available and reported Bang-bang CDAs are either single-ended or AD modulated, hence still requiring either a DC blocking capacitor or a lowpass filter. It was discussed in Chapter 2 that the filterless configuration is highly desirable as it facilitates a smaller PCB area and reduces the cost of components. Further, it was shown in Chapter 3 that the Bang-bang CDAs can feature comparable performance to PWM CDAs. Hence, there is potential for Bang-bang CDAs to be widely adopted as their PWM counterparts, particularly for power-critical applications, provided its filterless configuration (i.e. BD modulation) can be designed and realized.

(ii) Further to (i), it would be interesting to improve the performance of filterless Bang-bang CDAs to the level achieved by high-performance PWM CDAs. At this juncture, high-performance PWM CDAs remain superior to Bang-bang CDAs in terms of linearity and noise-immunity.

(iii) Investigation into the noise and SNR of PWM CDAs

It was discussed in Chapter 2 and in Chapter 4 that analytical investigations into the various specifications of PWM CDAs are largely complete. Interestingly, despite both the noise and SNR being commonly-quoted specifications for CDAs, it appears that the noise performance of PWM CDAs remains uninvestigated. Specifically, the (integrated output) noise and the SNR of PWM CDAs remain uninvestigated and its mechanisms largely unreported.

In view of this, it would be interesting to analytically investigate the mechanisms of and the circuit parameters affecting the noise and SNR of PWM CDAs and, on the basis of said investigation, to provide insights into the optimization of PWM CDAs in terms of the noise and SNR.

(iv) Investigation into the design of low-power high-performance PWM CDAs

It was shown in Chapter 2 and in Chapter 4 that currently available PWM CDAs are appropriate for general-purpose mobile applications and their quiescent current dissipation is typically in the range of a few mA. Although said quiescent current (power) is not excessive in the context of smart devices such as smartphones or tablets, it is nevertheless inappropriate for wearable devices whose operating time is expected to be much longer than that of smart devices.

In view of the applications for wearable devices, it is highly desirable to design a low-power/ultra-low-power (in terms of quiescent power) PWM CDAs whose audio performance is comparable to that of general-purpose PWM CDAs. It is

therefore imperative to design novel architectures and circuit blocks that can operate with minimum power dissipation.

Appendix

The maximum voltage spike, V_{max}, can be derived as:

$$V_{max} = V_{CR} + V_{IC} \tag{A1}$$

where V_{CR} is the contribution of charge redistribution, and V_{IC} the contribution of inductor charging (change of current flow).

For the sake of analysis, we first assume the current of L_p cannot change instantaneously within T_{rise}:

$$C_g(V_{DD} - V_{CR}) = C_p V_{CR} \tag{A2}$$

Practically, the inductor L_p contributes part of the charge. Assuming the inductor current, I_{ind}, is linearly varying and, at t=0, I_{ind}=0 and at t=T_{rise}, I_{ind}=ΔI.

We denote the charge contribution from inductor as Q_{ind}:

$$Q_{ind} = \frac{\Delta I}{2} T_{rise} \tag{A3}$$

$$\frac{dI}{dt}\left(L_{p1} + L_{p2}\right) = V_{CR} \leftrightarrow \Delta I = \frac{V_{CR}}{L_{p1} + L_{p2}} T_{rise} \tag{A4}$$

Substitute eqn. (A4) into eqn. (A5), we have

$$Q_{ind} = \frac{V_{CR}}{2\left(L_{p1} + L_{p2}\right)} {T_{rise}}^2 \tag{A5}$$

Taking Q_{ind} into consideration, we can rewrite eqn. (A5) as:

$$C_g(V_{DD} - V_{CR}) = C_p V_{CR} + \frac{V_{CR}}{2(L_{p1} + L_{p2})} {T_{rise}}^2 \tag{A6}$$

$$V_{CR} = \frac{C_g V_{DD}}{C_p + C_g + \frac{{T_{rise}}^2}{2(L_{p1} + L_{p2})}} \tag{A7}$$

At $t=T_{rise}$, I_{ind} has not reached its steady state, I_{out}. Hence the current of the inductor will increase till it reaches I_{out}.

$$\frac{1}{2}(I_{out} - \Delta I)^2 (L_{p1} + L_{p2}) = \frac{1}{2}[{V_{IC}}^2](C_p + C_g) \tag{A8}$$

$$V_{IC} = \sqrt{\frac{L_{p1} + L_{p2}}{C_p + C_g}}(I_{out} - \Delta I) \tag{A9}$$

Hence, substitute eqn. (A8) and eqn. (A9) into eqn. (A10):

$$V_{max} = \sqrt{\frac{2L_p}{C_p + C_g}}(I_{out} - \Delta I) + \frac{C_g V_{DD}}{C_p + C_g + \frac{{T_{rise}}^2}{2(L_{p1} + L_{p2})}} \tag{A10}$$

Author’s Publications

Patent Publications

[1] J. S. Chang, T. Ge, and L. Guo
"Ultra-High-Fidelity -cum- Ultra-Noise-Immunity Audio Class D Amplifier"
US Provisional Patent 61/889,794, 2013

[2] J. S. Chang, T. Ge, and L. Guo
"A Ground-Bounce-Insensitive Deadtime Circuit And High-Gain Loop Filter Design"
US Provisional Patent 61/974,198, 2014

[3] J. S. Chang, T. Ge, and L. Guo
"A Ground-Bounce-Aware Design Methodology"
US Provisional Patent 62/004,499, 2014

Journal Publications

[4] L. Guo, T. Ge, and J. S. Chang
"Intermodulation Distortions of Bang-bang Control Class D Amplifiers"
IEEE Transactions on Power Electronics, vol. 28, pp. 6604 - 6614, 2014.

[5] L. Guo, T. Ge, and J. S. Chang, "A 101 dB PSRR, 0.0027% THD+N and 94% Power-Efficiency Filterless Class D Amplifier," *IEEE Journal of Solid-State Circuits,* vol. 49, pp. 2608 - 2617, 2014.

[6] L. Guo, T. Ge, and J. S. Chang
"Fundamental Investigation into Ground-Bounce and Optimization thereto"
Submitted to *IEEE Transactions on Power Electronics,* 2014.

Conference Publications

[7] L. Guo, T. Ge, Y. Kang, H. He, and J. S. Chang
"Analysis and Design of PWM-in-PWM-Out Class D Amplifiers"
Midwest Symposium on Circuits and Systems, 2014, Accepted.

[8] L. Guo, T. Ge, and J. S. Chang
"Effect of carrier topologies on PSRR and PS-IMD of open-loop Class D amplifiers for hearing aids"
Circuits and Systems for Medical and Environmental Applications Workshop (CASME), 2010 2nd, 2010, pp. 1-4.

[9] L. Guo, T. Ge, and J. S. Chang
"A micropower comparator for high power-efficiency hearing aid class D amplifiers"
IEEE International Symposium on Circuits and Systems, 2010, pp. 1248-1251.

[10] H. He, T. Ge, L. Guo, Y. Kang, and J. S. Chang
"An Investigation into the Effect of Carrier Generators on Power Supply Noise in PWM Class D Amplifiers"
Midwest Symposium on Circuits and Systems, 2014, Accepted.

Bibliography

[1] B. Metzler, *Audio Measurement Handbook.*: Beaverton, OR: Audio Precision, 1993.

[2] B. Duncan, *High Performance Audio Power Amplifiers for music performance and reproduction*: Oxford, UK: Newnes-An imprint of Butterworth-Heinemann Ltd, 1996.

[3] J. S. Chang, T. Meng-Tong, C. Zhihong, and T. Yit-Chow, "Analysis and design of power efficient class D amplifier output stages," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications,* vol. 47, pp. 897-902, 2000.

[4] Y. Choi, W. Tak, Y. Yoon, J. Roh, S. Kwon, and J. Koh, "A 0.018% THD+N, 88-dB PSRR PWM Class-D Amplifier for Direct Battery Hookup," *IEEE Journal of Solid-State Circuits,* vol. 47, pp. 454-463, 2012.

[5] M. Berkhout and L. Dooper, "Class-D Audio Amplifiers in Mobile Applications," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 57, pp. 992-1002, 2010.

[6] T. Ge and J. S. Chang, "Bang-Bang Control Class-D Amplifiers: Power-Supply Noise," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 55, pp. 723-727, 2008.

[7] T. Ge and J. S. Chang, "Modeling and Technique to Improve PSRR and PS-IMD in Analog PWM Class-D Amplifiers," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 55, pp. 512-516, 2008.

[8] Gray P.R., Hurst P.U., Lewis S.H., and M. R.G., *Analysis and Design of Analog Integrated Circuits,* 4th ed.: John Wiley & Sons, Inc, 2001.

[9] T. Ge, "Analog Class D Amplifiers: Non-Linearities and Power-Efficiency," Ph.D. Dissertation, Nanyang Technological University, 2009.

[10] M. T. Tan, J. S. Chang, H. C. Chua, and B. H. Gwee, "An investigation into the parameters affecting total harmonic distortion in low-voltage low-power Class-D amplifiers," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications,* vol. 50, pp. 1304-1315, Oct 2003.

[11] J. S. Chang, B. H. Gwee, Y. S. Lon, and M. T. Tan, "A Novel Low-Power Low-Voltage Class D Amplifier with Feedback for Improving THD, Power Efficiency and Gain Linearity " *IEEE International Symposium on Circuits and Systems,* pp. 6-9, May 2001.

[12] J. S. Chang, M. T. Tan, Z. Cheng, and Y.-C. Tong, "Analysis and design of power efficient class D amplifier output stages," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications,* vol. 47, pp. 897-902, 2000.

[13] C. M. Wu, L. Wing-Hong, and H. Shu-Hung Chung, "Analytical technique for calculating the output harmonics of an H-bridge inverter with dead time," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications,* vol. 46, pp. 617-627, 1999.

[14] "TPA2000D1 - 2W Filterless Mono Class-D Audio Power Amplifier," Texas Instruments,2004.

[15] "TPA2010D1 - 2.5W Mono Filter-free Class-D Audio Power Amplifier," Texas Instruments. 2006.

[16] "SLUS910B - 1.1A, Single-Input, Single Cell Li-Ion Battery Charger With 50mA LDO and 2.3A Production Test Support," Texas Instruments, 2009.

[17] "MAX98304 - Mono 3.2W Class D Amplifier," Maxim Integrated,2010.

[18] "SSM2315 - Filterless, High Efficiency, Mono 3 W Class-D Audio Amplifier," Analog Devices, 2008.

[19] J. Lu and R. Gharpurey, "Design and Analysis of a Self-Oscillating Class D Audio Amplifier Employing a Hysteretic Comparator," *IEEE Journal of Solid-State Circuits,* vol. 46, pp. 2336-2349, 2011.

[20] M. A. Teplechuk, T. Gribben, and C. Amadi, "True Filterless Class-D Audio Amplifier," *IEEE Journal of Solid-State Circuits,* vol. 46, pp. 2784-2793, 2011.

[21] Y. Mei-Ling, L. Wan-Rone, H. Hsiang-Po, and L. Yu-Jei, "An Electromagnetic Interference (EMI) Reduced High-Efficiency Switching Power Amplifier," *IEEE Transactions on Power Electronics,* vol. 25, pp. 710-718, 2010.

[22] M. Xin, C. Zao, Z. Ze-kun, and Z. Bo, "An Advanced Spread Spectrum Architecture Using Pseudorandom Modulation to Improve EMI in Class D Amplifier," *IEEE Transactions on Power Electronics,* vol. 26, pp. 638-646, 2011.

[23] F. Guanziroli, R. Bassoli, C. Crippa, D. Devecchi, and G. Nicollini, "A 1 W 104 dB SNR Filter-Less Fully-Digital Open-Loop Class D Audio Amplifier With EMI Reduction," *IEEE Journal of Solid-State Circuits,* vol. 47, pp. 686-698, 2012.

[24] P. Balmelli, J. M. Khoury, E. Viegas, P. Santos, V. Pereira, J. Alderson, *et al.*, "A Low-EMI 3-W Audio Class-D Amplifier Compatible With AM/FM Radio," *IEEE Journal of Solid-State Circuits,* vol. 48, pp. 1771-1782, 2013.

[25] "LX1792 - Low Voltage, Low Power, AudioMite Class-D Audio Amplifier," Microsemi2001.

[26] A. Nagari, "Tutorial review: audio amplifiers in mobile platforms," *Analog Integrated Circuits and Signal Processing,* vol. 72, pp. 511-520, 2012.

[27] T. Ge and J. S. Chang, "Bang-Bang Control Class D Amplifiers: Total Harmonic Distortion and Supply Noise," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 56, pp. 2353-2361, 2009.

[28] W. Shu and J. S. Chang, "IMD of Closed-Loop Filterless Class D Amplifiers," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 57, pp. 518-527, 2010.

[29] V. Adrian, J. S. Chang, and G. Bah-Hwee, "A Low-Voltage Micropower Digital Class-D Amplifier Modulator for Hearing Aids," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 56, pp. 337-349, 2009.

[30] M. C. W. Hoyerby and M. A. E. Andersen, "Carrier Distortion in Hysteretic Self-Oscillating Class-D Audio Power Amplifiers: Analysis and Optimization," *IEEE Transactions on Power Electronics,* vol. 24, pp. 714-729, 2009.

[31] J. Yu, M. T. Tan, S. M. Cox, and W.-L. Goh, "Time-Domain Analysis of Intermodulation Distortion of Closed-Loop Class-D Amplifiers," *IEEE Transactions on Power Electronics,* vol. 27, pp. 2453-2461, 2012.

[32] L. Chun Kit, T. Meng Tong, S. M. Cox, and Y. Kiat Seng, "Class-D Amplifier Power Stage With PWM Feedback Loop," *IEEE Transactions on Power Electronics,* vol. 28, pp. 3870-3881, 2013.

[33] W. Shu and J. S. Chang, "THD of Closed-Loop Analog PWM Class-D Amplifiers," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 55, pp. 1769-1777, 2008.

[34] A. Kabbani and A. J. Al-Khalili, "Estimation of ground bounce effects on CMOS circuits," *IEEE Transactions on Components and Packaging Technologies,* vol. 22, pp. 316-325, 1999.

[35] T. Gabara, "Estimation of Ground Bounce in CMOS Circuits using a Solution to a Damped RLC Network," in *Proceedings of the European Solid-State Circuits Conference,* 1996, pp. 328-331.

[36] P. Heydari and M. Pedram, "Ground bounce in digital VLSI circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 11, pp. 180-193, 2003.

[37] F. Jiwei and T. Harrison, "Substrate switching noise analysis and layout/circuit considerations in monolithic power converters," in *Energy Conversion Congress and Exposition*, 2012, pp. 2610-2615.

[38] J. S. Chang, T. Ge, and L. Guo, "Ultra-High-Fidelity -cum- Ultra-Noise-Immunity Audio Class D Amplifier," US Provisional Patent 61/889,794, 2013.

[39] J. S. Chang, T. Ge, and L. Guo, "A Ground-Bounce-Aware Design Methodology," US Provisional Patent 62/004,499, 2014.

[40] J. S. Chang, T. Ge, and L. Guo, "A Ground-Bounce-Insensitive Deadtime Circuit And High-Gain Loop Filter Design," US Provisional Patent 61/974,198, 2014.

[41] L. Guo, T. Ge, and J. S. Chang, "Intermodulation Distortion of Bang-bang Control Class D Amplifiers," *IEEE Transactions on Power Electronics*, vol. 29, pp. 6604 - 6614, 2014.

[42] L. Guo, T. Ge, and J. S. Chang, "A 101 dB PSRR, 0.0027% THD+N and 94% Power-Efficiency Filterless Class D Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 49, pp. 2608 - 2617, 2014.

[43] L. Guo, T. Ge, and J. S. Chang, "Fundamental Investigation into Ground-Bounce and Optimization thereto," *IEEE Transactions on Power Electronics*, 2014, Submitted.

[44] L. Guo, T. Ge, and J. S. Chang, "A micropower comparator for high power-efficiency hearing aid class D amplifiers," in *IEEE International Symposium on Circuits and Systems*, 2010, pp. 1248-1251.

[45] L. Guo, T. Ge, and J. S. Chang, "Effect of carrier topologies on PSRR and PS-IMD of open-loop Class D amplifiers for hearing aids," in *Circuits and Systems for Medical and Environmental Applications Workshop (CASME), 2010 2nd*, 2010, pp. 1-4.

[46] L. Guo, T. Ge, Y. Kang, H. He, and J. S. Chang, "Analysis and Design of PWM-in-PWM-Out Class D Amplifiers," in *Midwest Symposium on Circuits and Systems*, 2014, Accepted.

[47] H. He, T. Ge, L. Guo, Y. Kang, and J. S. Chang, "An Investigation into the Effect of Carrier Generators on Power Supply Noise in PWM Class D Amplifiers," in *Midwest Symposium on Circuits and Systems*, 2014, Accepted.

[48] G. Bah-Hwee, J. S. Chang, and V. Adrian, "A micropower low-distortion digital class-D amplifier based on an algorithmic pulsewidth modulator," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, pp. 2007-2022, 2005.

[49] W. Minsheng, J. Xicheng, S. Jungwoo, and T. L. Brooks, "A 120 dB Dynamic Range 400 mW Class-D Speaker Driver With Fourth-Order PWM Modulator," *IEEE Journal of Solid-State Circuits,* vol. 45, pp. 1427-1435, 2010.

[50] H. S. Black, "Modulation Theory," ed Princeton, NJ: Van Nostrand, 1953, pp. 263-281.

[51] R. Adams, E. Gaalaas, B. Y. Liu, R. Morajkar, N. Nishimura, and K. Sweetland, "Integrated Stereo Sigma-Delta Class D Amplifier," in *Audio Engineering Society Convention*, 2005.

[52] E. Gaalaas, B. Y. Liu, and N. Nishimura, "Integrated stereo Delta-Sigma class D amplifier," *ISSCC Dig. Tech. Papers,* pp. 120-122, Feb 2005.

[53] M. A. Rojas-Gonzalez and E. Sanchez-Sinencio, "Low-Power High-Efficiency Class D Audio Power Amplifiers," *IEEE Journal of Solid-State Circuits,* vol. 44, pp. 3272-3284, 2009.

[54] J. Torres, A. Colli-Menchi, G. Rojas, x, M. A. lez, and E. Sanchez-Sinencio, "A 470uW clock-free current-controlled class D amplifier with 0.02% THD and 82dB PSRR," in *Proceedings of the European Solid-State Circuits Conference*, 2010, pp. 326-329.

[55] J. Torres, A. Colli-Menchi, M. A. Rojas-Gonzalez, and E. Sanchez-Sinencio, "A Low-Power High-PSRR Clock-Free Current-Controlled Class-D Audio Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 46, pp. 1553-1561, 2011.

[56] B. H. Candy and S. M. Cox, "Improved Analogue Class-D Amplifier with Carrier Symmetry Modulation," *Audio Engineering Society Convention*, Oct 2004.

[57] I. Deslauriers, N. Avdiu, and B. T. Ooi, "Naturally sampled triangle carrier PWM bandwidth limit and output spectrum," *IEEE Transactions on Power Electronics,* vol. 20, pp. 100-106, 2005.

[58] I. D. Mosely, P. H. Mellor, and C. M. Bingham, "Effect of dead time on harmonic distortion in class-D audio power amplifiers," *Electronics Letters,* vol. 35, pp. 950-952, 1999.

[59] S. M. Cox, Y. Jun, G. Wang Ling, and T. Meng Tong, "Intrinsic Distortion of a Fully Differential BD-Modulated Class-D Amplifier With Analog Feedback," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 60, pp. 63-73, 2013.

[60] B. Krabbenborg and M. Berkhout, "Closed-Loop Class-D Amplifier With Nonlinear Loop Integrators," *IEEE Journal of Solid-State Circuits,* vol. 45, pp. 1389-1398, 2010.

[61] W. Shu and J. S. Chang, "Power Supply Noise in Analog Audio Class D Amplifiers," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 56, 2009.

[62] K. Kyoungsik, R. Jeongjin, C. Youngkil, R. Hyungdong, N. Hyunsuk, and L. Songjun, "Class-D Audio Amplifier Using 1-Bit Fourth-Order Delta-Sigma Modulation," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 55, pp. 728-732, 2008.

[63] R. Engel, "Analog-to-digital conversion via duty-cycle modulation," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing,* vol. 44, pp. 907-914, 1997.

[64] Y. Wenfeng, S. Wei, and J. S. Chang, "A low THD analog Class D Amplifier based on self-oscillating modulation with complete feedback network," in *IEEE International Symposium on Circuits and Systems*, 2009, pp. 2729-2732.

[65] R. Cellier, A. Nagari, H. Souha, G. Pillonnet, and N. Abouchi, "A synchronized self oscillating Class-D amplifier for mobile application," in *Proceedings of the European Solid-State Circuits Conference*, 2012, pp. 422-425.

[66] N. Shao Siang, L. Kuei-Liang, C. Ke-Horng, and C. Yu-Wen, "A 94% efficiency near-constant frequency self-oscillating class-D audio amplifier with voltage control resistor," in *IEEE International Symposium on Circuits and Systems*, 2013, pp. 602-605.

[67] M. Berkhout, "Integrated overcurrent protection system for class-D audio power amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 2237-2245, 2005.

[68] C. M. Wu, W. Lau, and H. S. Chung, "Analytical Technique for Calculating the Output Harmonics of an H-Bridge Inverter with Dead Time," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications,* vol. 46, pp. 617-627, May 1999.

[69] A. Nagari, E. Allier, F. Amiard, V. Binet, and C. Fraisse, "An 8Ω 2.5W 1%-THD 104dB(A)-dynamic-range Class-D audio amplifier with an ultra-low EMI system and current sensing for speaker protection," in *ISSCC Dig. Tech. Papers*, 2012, pp. 92-94.

[70] H. Ma, R. van der Zee, and B. Nauta, "Design and Analysis of a High-Efficiency High-Voltage Class-D Power Output Stage," *IEEE Journal of Solid-State Circuits*, vol. PP, pp. 1-11, 2014.

[71] F. Koeslag, H. D. Mouton, and J. Beukes, "Analytical Modeling of the Effect of Nonlinear Switching Transition Curves on Harmonic Distortion in Class D Audio Amplifiers," *IEEE Transactions on Power Electronics,* vol. 28, pp. 380-389, 2013.

[72] L. Jia-Ming, C. Shih-Hsiung, and K. Tai-Haur, "A 100 W 5.1-Channel Digital Class-D Audio Amplifier With Single-Chip Design," *IEEE Journal of Solid-State Circuits*, vol. 47, pp. 1344-1354, 2012.

[73] P. Morrow, E. Gaalaas, O. McCarthy, A. Devices, and I. Limerick, "A 20-W stereo class-D audio output power stage in 0.6 μm BCDMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 1948-1958, Nov 2004.

[74] S. Balkir, M. Hoffman, and D. White, "CMOS Self-Oscillating Class D Amplifier with Output Optimization," *Audio Engineering Society Convention*, 2006.

[75] P. Moens and G. Van Den Bosch, "Characterization of Total Safe Operating Area of Lateral DMOS Transistors," *IEEE Transactions on Device and Materials Reliability*, vol. 6, pp. 349-357, Sept 2006.

[76] T. Instruments. Reducing and Eliminating the Class-D Output Filter [Online]. Available: http://focus.ti.com/general/docs/lit/getliterature.tsp?baseLiteratureNumber=sloa023.pdf

[77] J. R. Howatt, "Switching Amplifier," U.S. Patent 5,077,539, 1991.

[78] X. Jiang, J. Song, M. Wang, J. Chen, and S. K. Arunachalam, "Integrated Pop-Click Noise Suppression, EMI Reduction, and Short-Circuit Detection for Class-D Audio Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 48, pp. 1099-1108, 2013.

[79] "Layout Guidelines for TPA300x Series Parts," Taxes Instrument, 2003.

[80] "Application Note 3973 - Maxim's Active-Emissions-Limiting Circuitry Demysified," Maxim Integrated2006.

[81] B. Hofer, "Measuring Distortion in Switching Ampliefiers," in *27th International Conference: Efficient Audio Power Amplification*, 2005.

[82] G. Pillonnet, N. Abouchi, R. Cellier, and A. Nagari, "A 0.01%THD, 70dB PSRR Single Ended Class D using variable hysteresis control for headphone amplifiers," *IEEE International Symposium on Circuits and Systems*, 2009.

[83] P. G. Drennan and C. C. McAndrew, "Understanding MOSFET mismatch for analog design," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 450-456, 2003.

[84] "2011 Technology Working Group Reports," International Technology Roadmap for Semiconductors, 2011.

[85] "Guidelines for Measuring Audio Power Amplifier Performance," Texas Instrument Application note, 2001.

[86] A. Bandyopadhyay, M. Determan, K. Sejun, and N. Khiem, "A 120dB-SNR 100dB-THD+N 21.5mW/channel multibit CT sigma-delta DAC," in *ISSCC Dig. Tech. Papers*, 2011, pp. 482-483.

[87] "AD1852 - Stereo, 24-Bit, 192 kHz, Multibit, Sigma-Delta DAC," Analog Devices, 2009.

[88] "SLOA068 – Guidelines for Measuring Audio Power Amplifier Performance," Texas Instruments, 2001.

[89] S. Kwon, I. Kim, S. Yi, S. Kang, S. Lee, T. Hwang, *et al.*, "A 0.028% THD+N, 91% power-efficiency, 3-level PWM Class-D amplifier with a true differential front-end," in *ISSCC Dig. Tech. Papers*, 2012, pp. 96-98.

[90] J. Hailong and V. Kursun, "Ground-Bouncing-Noise-Aware Combinational MTCMOS Circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, pp. 2053-2065, 2010.

[91] M. Felder and J. Ganger, "Analysis of ground-bounce induced substrate noise coupling in a low resistive bulk epitaxial process: design strategies to minimize noise effects on a mixed-signal chip," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, pp. 1427-1436, 1999.

[92] B. Kelleci, E. Sanchez-Sinencio, and A. I. Karsilayan, "THD+Noise Estimation in Class-D Amplifiers," in *IEEE International Symposium on Circuits and Systems*, 2007, pp. 465-468.