A 5-bit 1.25GS/s 4.7mW Delay-Based Pipelined ADC in 65nm CMOS

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***Abstract*- This paper presents a delay based pipeline (DBP) analog to digital converter (ADC) suitable for high speed and low power applications. Active sample and hold and residue amplifier used in conventional pipeline ADCs are replaced by an analog delay line. The analog delay line is implemented by time-interleaved sampling of the signal in each stage of the ADC. A novel multi-phase clock generator is introduced to generate ADC timing signals. A 5-bit, 1.25 GS/s DBP ADC is designed in 65nm CMOS process. Post-layout simulations confirm that the proposed ADC achieves a peak SNDR of 30.5dB while consuming 4.7mW from a single 1.2V power supply.**

I. INTRODUCTION

High speed, low power, medium resolution, analog-to-digital converters (ADC) are widely used in high data-rate serial links and data communication applications such as ultra wide band (UWB) and 60GHz RF systems. In such applications, ADCs with sampling rate of Giga samples per second and low power consumption are usually required [1].

Flash-type ADCs have been widely used for such applications because of their high speed conversion characteristics [2]. In a flash ADC the sampling frequency is mainly limited by the delay of the comparator which can be very small in modern CMOS processes. However, in flash ADCs, the number of comparators, and hence power consumption, area and input capacitance exponentially increase with resolution, which limits the performance of such ADCs.

To address the challenge, sub-ranging flash and pipelined ADCs have been used [3, 4]. In sub-ranging ADCs, the number of comparators is reduced by performing the conversion time in two comparison cycles. In pipeline ADCs, the operation of flash converters is broken into even more steps. In sub-ranging ADCs, coarse flash ADC resolves the most significant bit(s) and a digital to analog converter (DAC) converts the coarse digital code into its analog equivalent. The DAC output is subtracted from the input signal and the residue signal is amplified to full scale by an operational amplifier. The residue signal is then converted in the second flash ADC. When the data is sent to the second stage, another sampled data is fed to the first stage introducing latency. In pipeline ADCs this process can be repeated several times to reach the required resolution. Although sub-ranging greatly reduces the number of comparators compared with flash converters, high precision inter-stage processing is required. However, the residue amplifier usually requires high gain and bandwidth to provide an amplified residue signal for the following flash converter. In high speed applications where sampling rates of GS/s are required, the design of operational amplifier becomes very challenging and the power consumption of opamp can increase drastically.

In this work a new pipelined ADC that does not require any operational amplifier is introduced. As a result, low power consumption is achieved during high speed operation. This paper is organized as follows. The new pipelined ADC architecture is introduced in section II. Section III describes circuit implementation of main building blocks of the ADC. Post-layout simulation results for the proposed 5-bit 1.25GS/s ADC in 65nm CMOS process is presented in section IV. Section V concludes the paper.

II. THE DELAY-BASED PIPELINE (DBP) ADC ARCHITECTURE

As pointed out in previous section, conventional pipelined ADCs suffer in high speed operation regime because of the limitations imposed by the operational amplifier. A different way to perform the sub-ranging is to resolve MSBs in a coarse flash quantizer, find the input signal range by a DAC, delay the analog signal and then quantize the delayed analog signal in smaller ranges in the following stages. At the same time new analog data can be fed to the ADC. Delaying the analog signal can be implemented by time-interleaved sampling of the analog signal at the input of each pipeline stage, holding the data for the required delay time, and transferring it to the next stage afterwards. The sub-ranging and analog delay can be repeated until the required resolution is achieved.

Fig.1 shows 5-bit single-ended implementation of the proposed delay based pipeline (DBP) ADC and its timing diagram. The ADC consists of 2-bit flash quantizers in both first and second stages and 1-bit flash quantizer in the last stage. Three different sampling paths are used at the input of each comparator driven by six-phase non-overlapping clocks. 2-bit and 4-bit DACs are used for converting the digital signal back to analog after the first and second stage quantizers, and for performing the sub-ranging operation. Each DAC consists of thermometer to one hot-code encoder and multiplexer(s). A resistor string is shared among the three stages that generates the required reference voltages. In Fig.1, it is assumed that the comparators are clocked with the falling edge and all flip-flops are positive edge triggered. Notice that the active sample and hold circuit used in conventional pipeline ADCs as analog shift register is replaced by analog delays as shown in Fig.1.

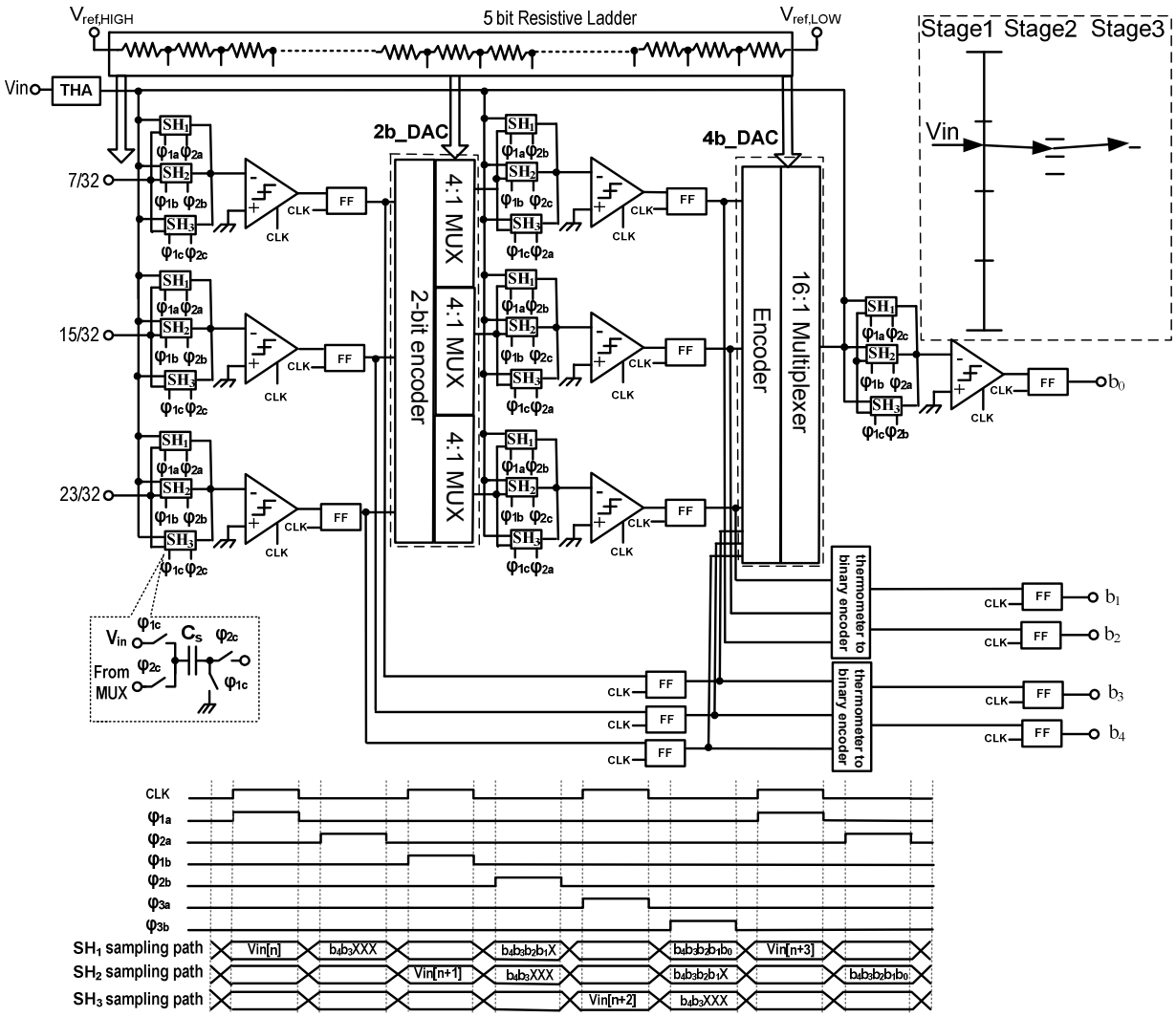

Fig.1 The proposed delay based pipeline analog-to-digital converter and its timing

The ADC operation can be described as follows. The input signals are sampled on three different paths, SH_1, SH_2, and SH_3 in an interleaved fashion. Input signal, $V_{in}[n]$, is sampled on SH_1 path during φ_{1a}. In φ_{2a}, the first-stage flash quantizer determines the first two MSBs corresponding to $V_{in}[n]$. The thermometer output code of the first-stage flash quantizer is then delayed in a flip-flop. The delayed thermometer code is converted into one hot-code in the 2-bit DAC in φ_{1b}. This DAC determines the input signal range with 2-bit accuracy, and breaks that range into 4 equal sub-ranges. Using three multiplexers, three reference voltages from the resistor string are passed to the second-stage 2-b flash quantizer. During φ_{1b}, the new input signal, $V_{in}[n+1]$ is sampled in SH_2 sampling path. In φ_{2b}, the second-stage flash quantizer resolves the next 2 bits corresponding to $V_{in}[n]$. The thermometer outputs of the first and the second stage quantizers are delayed by another clock cycle and then applied to the 4-bit DAC. This DAC decides which reference level to be compared with the $V_{in}[n]$ in the last stage comparator during φ_{1c}. During the same time new input signal $V_{in}[n+2]$ is sampled on the SH_3 sampling path. Finally, in φ_{2c}, the third-stage comparator decides the LSB corresponding to $V_{in}[n]$. At this time new data can be sampled on SH_1 sampling path. Same sampling and conversion process is performed in the SH_2 and SH_3 sampling paths on $V_{in}[n+1]$ and $V_{in}[n+2]$.

The fully differential ADC was implemented in 65nm CMOS process. The details of the design are discussed in the following section, by illustrating the important circuit blocks of the proposed ADC.

III. CITCUIT IMPLEMENTATION

A. Dynamic comparator and offset cancellation

Seven dynamic comparators are used in the proposed 5-bit pipelined ADC. As such, comparators are the main sources of power dissipation in this ADC. Hence, a comparator topology without static power consumption is preferred. Fig.2 shows the schematic of the comparator along with its offset cancellation. The comparator is in precharge mode when clock is high. The regenerative latch operates when the clock signal goes low. Since no static pre-amplifier is used, dynamic offset cancellation technique is adapted. A 5-bit binary weighted

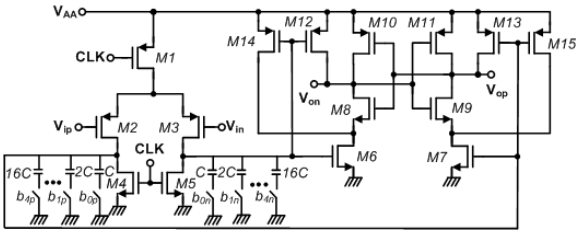

Fig.2 Dynamic comparator and offset cancelaation

capacitive array is used for the offset cancellation in each comparator. The comparator inputs are connected to common mode voltage during the precharge phase to clear the memory effect of the pipelined ADC.

B. Timing generation

A very low power moving-spot frequency divider is proposed to generate the required timing waveforms from the input clock phase. This circuit can generate the required divided sampling phases synchronously [5]. It does not require gating multiple divided clock waveforms to generate the each clock phase. Thus, the technique can provide very accurate, low-phase noise sampling phases for each of the individual sample and hold paths with very low power consumption.

The operation of this moving-spot circuit is as follows. A single high pulse is inserted into a loop of six dynamic self-clearing unit elements during power-on-reset. This is achieved through devices M_{10} -M_{19}. Reset signal clears all the unit elements at the power-up. Following the arrival of the input clock, the reset signal is released allowing PMOS devices M_{15} and M_{16} to pull up the input of the first unit element to high. With the rising clock edge this signal is passed to the output, Q. The output reaching high clears back its own input, D. At the rising edge of the opposite phase clock, CLKB, the high pulse is now passed to the second unit element output. While this happens, the pulse insertion circuit is deactivated assuring only single pulse propagation. This single half-clock width pulse circulates around the loop thereon with the two clock phases feeding the unit elements in an alternate fashion. The unit element schematic including the devices M_1-M_9 is as well shown in the same figure. In all of the unit elements, a very weak pull-down device M_6 is biased through signal R_1, which keeps the output of the preceding stage immune to the

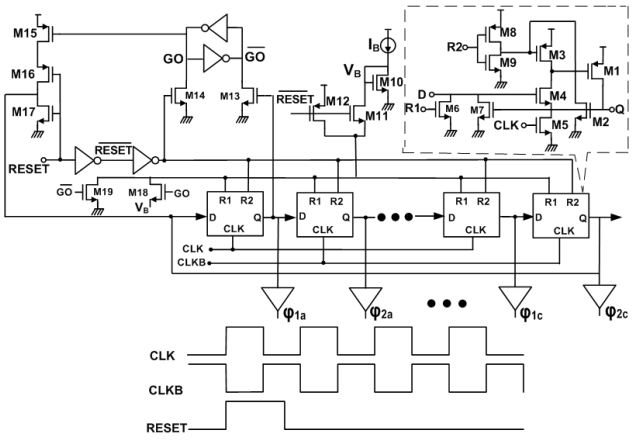

Fig.3 six phase clock generator

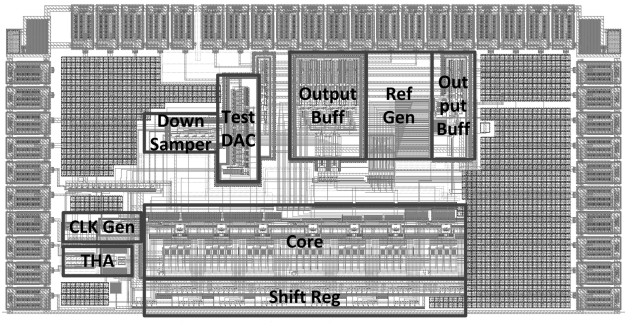

Fig.4 ADC layout in 65nm CMOS

coupling and leakage. During power-on-reset all the elements are reset using both R_1 and R_2 reset signals. The unique advantage of this type of frequency divider timing circuit is that only two of the unit elements experiences transition per clock cycle, hence reducing the power consumption significantly.

C. Track and hold (THA)

Because of the distributed sampling nature in proposed pipelined ADC, a global track and hold circuit is required. Active track and hold circuits usually use a high speed source follower. In high speed operation, the active track and hold circuits require a very wide bandwidth to be able to track the input signal which is challenging to design. Moreover, the source follower introduces non-linearity to the ADC and limits the input dynamic range especially in low voltage processes. Hence, a passive track and hold circuit is used in this design.

An on-chip reference generator is used to bias the resistor string.

IV. POST-LAYOT SIMULATION RESULTS

The proposed DBP ADC was implemented in 65nm low power CMOS process (GF 1P8M). Fig.4 shows the layout with ADC core area of 0.9×0.5 mm^2. Guard ring and deep N-

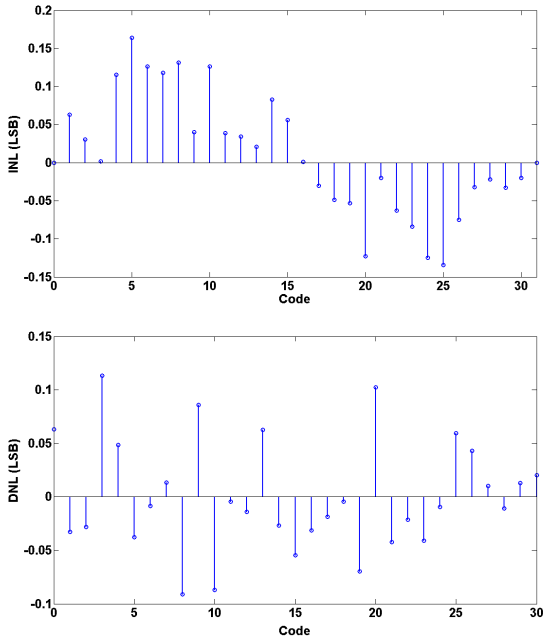

Fig.5. Simulated INL and DNL of ADC

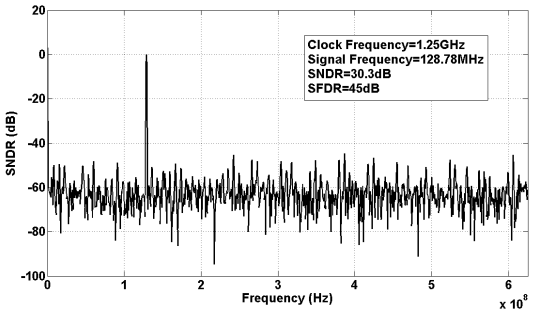

Fig.6. ADC output spectrum for a 127.78 MHz since input

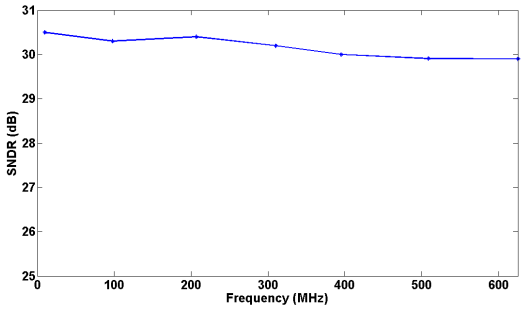

Fig.7. SNDR vs frequency

Well are used to surround the clock generator and output buffer to isolate the switching noise coming from the substrate. Thick oxide capacitors are added to reduce the ripples on the power lines.

Post layout simulation results show that the proposed ADC can achieve a peak SNDR of 30.5dB at 1.25GS/s sampling rate. Fig.5 shows the simulated differential non-linearity (DNL) and integral non-linearity (INL) of the proposed ADC. The simulated DNL and INL are 0.11 LSB and 0.16LSB, respectively. Fig.6 shows the ADC output 2048 point FFT spectrum for a differential 1Vpp sine-wave input at 128.78MHz indicating an SNDR of 30.3dB. Fig.7 shows the SNDR of the proposed ADC for different input frequencies.

The ADC consumes the total power of 4.7mW from a single 1.2V power supply. A dynamic power of 3.9mW is dissipated in comparators, clock generator and clock buffers. Static power is 0.8mW consumed in the on chip reference generator. In the proposed architecture, with a defined Figure-of Merit FoM=POWER/($2^{ENOB}\cdot f_S$), the value obtained is 135fJ/conv-step. Table I summarizes the ADC performance shows the comparison with other state-of-the-art high-speed, low power ADCs.

V. Conclusion

A new high speed and low power pipelined sub-ranging ADC was introduced in this paper. In the proposed pipeline ADC architecture the requirement for a residue amplifier is removed by time-interleaved sampling of the signal at each comparator inputs, which results in higher speed and lower power consumption compared to conventional sub-ranging ADCs. A new accurate, low phase noise, and low power clock

Table I. Performance summary and comparison

Parameter	[2]	[6]	[7]	[8]	[9]	This work
Architecture	Flash	Asynch. Binary Search	Asynch SAR	Asynch Binary Search	Asynch SAR	Subranging Pipeline
Technology (nm)	90	65	65	60	40	65
Supply (V)	1.2/0.9	1.0	1.2	1.2	1	1.2
Resolution	7	5	6	5	6	5
SNDR (dB)	40.29	26.9	30.25	30.7	30.5	30.5
ENOB (bits)	6.4	4.4	5	4.8	4.8	4.8
Sampling Rate (GHz)	1.5	0.7	1	0.5	1.25	1.25
Power (mW)	220	1.97	6.27	1.63	6.08	4.7
FoM (fJ/conv.)	1578	116	210	117	178	135

generator was as well introduced providing the required timing for the ADC. The 5-bit 1.25GS/s prototype was designed and sent for fabrication in 65nm low power CMOS process (GF 1P8M). The post-layout simulation results confirm that the ADC achieves a peak SNDR of 30.5dB. The ADC consumes 4.7 mW in ADC core, clock generator and on chip reference generator from a single 1.2V power supply. This yields to a figure of merit of 135fJ/conversion-step. The ADC achieves simpler timing and higher operating speed compared to the preceding ADC reported in [10].

Acknowledgments

The authors gratefully acknowledge the support from the IC Design Centre of Excellence, Nanyang Technological University. The authors would like to thank Xiwei Huang, and Yong Hao Zhang for their contribution in layout work.

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