

**DEVELOPMENT OF INTERFACE FOR GRID
INTEGRATION OF ENERGY STORAGE
SYSTEMS IN THE BUILT ENVIRONMENT**

HU XIAOLEI

School of Electrical and Electronic Engineering

**A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy
2015**

Acknowledgements

I would like to express my deep gratitude and very great appreciation to my supervisor Associate Professor KingJet Tseng and my co-supervisor Madhavi Srinivasan for their patient and invaluable guidance, support, enthusiastic encouragement and useful critiques of this research work.

I would also like to extend my thanks to the technicians of power electronics research laboratory, Madam Chin Khim Lee-Loh, Mr. Tiong Seng Teo, and Madam Jie Juuan Goh, for their help in offering me the resources in running the project.

My gratitude is also extended to all my friends of power division, especially for Dr. Xiong Liu, Dr. Shao Zhang, Dr. Shuaixun Chen, Dr. Mingqiang Wang and Mr. Chi Jin, I appreciate those insightful discussions with them that inspired me new research ideas. I would like to express my thanks to Yitao Liu, Mengqi Zhang, Shan Yin and Tao Wang for their help and support.

I wish to take this opportunity to express my thanks to my parents. Finally, I would give my special appreciation to my wife, Yijing Chen, for her persistent encouragement, understanding and support over the past three years.

This research is funded by the Republic of Singapore's National Research Foundation through a grant to the Berkeley Education Alliance for Research in Singapore (BEARS) for the Singapore-Berkeley Building Efficiency and Sustainability in the Tropics (SinBerBEST) Program. BEARS has been established by the University of California, Berkeley as a center for intellectual excellence in research and education in Singapore.

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Summary

Power distribution grid in the built environment in future will increasingly have to accommodate a growing number of energy storage systems (ESSs) incorporating with renewable energy sources (RESs). Integrating ESS into buildings can improve energy efficiency and sustainability. ESS also provides a usable power source during fault of the main AC power grid. Batteries and ultra-capacitors are considered as excellent candidates for energy storage devices (ESDs) used for ESS. Batteries have good energy density and ultra-capacitors have good power density. However development of control strategy and electrical interface for integrating ESS into AC power grid in the built environment is still in need of further investigations.

Single battery or ultra-capacitor cell has only a low terminal voltage while the AC power grid has a much higher voltage. Thus, battery or ultra-capacitor cells are connected in series to gain sufficient voltage for grid integration. However, due to varying chemical and electrical characteristics, series-connected cells have unbalancing issue after several charging/discharging cycles. An auxiliary circuit known as battery cell equalizer (BCE) is used for balancing series-connected battery or ultra-capacitor cells. For applications of ESS in the built environment or electrical vehicles, fast-equalizing is desired. A current-fed BCE is proposed in this thesis for fast-equalizing application.

Using power electronics converters (PECs) with high voltage transfer ratio is an alternative solution. It can interface ESS with low terminal voltage to AC power grid to avoid the cell balancing issue. Dual active bridge (DAB) converter cascaded by VSI has been proposed by researchers for ESS to grid application. DAB has the features of simple hardware structure for bidirectional power flow capability and zero voltage switching (ZVS). The system can be optimized when the voltage transfer ratio of the input ESS DC voltage to DC-link voltage is a constant. However, conventional control methods such as traditional phase shift (TPS) and dual phase shift (DPS), have high circulating current and reactive power. A novel hybrid control method of phase shift and PWM is proposed and introduced in this thesis to eliminate the circulating current for DAB. Comparisons of the proposed control method against TPS and DPS are presented as well. Some ESDs have wide varying terminal voltage, such as ultra-capacitors, and bring challenges to the design of using DAB+VSI. DC-link voltage may be quite high when the input to output voltage

transfer ratio is a constant. Furthermore, bulky DC-link capacitors are required for DAB. A novel DC/AC converter based on current-fed topology and current source inverter (CSI) is proposed in this thesis. The proposed circuit has a boost function. Therefore, it is compatible with ESDs having wide terminal voltage variation. Furthermore, DC-link capacitors of DAB+VSI and grid-side current sensors can be eliminated, and system complexity and cost can be thus reduced. Circuit operation and modulation of the proposed converter is explained in this thesis.

Modularized design of ESS has high flexibility and reliability. One common application of ESS used in buildings and industry is in the uninterruptible power supply (UPS). DC bus overvoltage is observed in the investigation of paralleled modularized UPS. This instability issue is also shared by application of renewable power generation. This thesis studied the cause of this DC bus overvoltage. It was found that circulating current at switching frequency caused active power exchange and thus caused the DC bus overvoltage issue. A novel switching frequency shift method is proposed to suppress the DC bus overvoltage.

Using only either batteries or ultra-capacitors in ESS cannot guarantee an optimal system performance, since batteries have limited power rating while ultra-capacitors have low energy density. Hybrid system of batteries and ultra-capacitors has a good system performance of both energy and power density. However, conventional control method using low pass filter (LPF) or PI controller does not optimally regulate battery current and charging/discharging cycles. Model predictive control (MPC), which is ideal for setting constraint and for optimizing, is introduced and designed in this thesis to minimize current stress and charging/discharging cycles of batteries to extend the battery life and to provide a better system performance.

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List of Abbreviations

APF	Active Power Filter
BCE	Battery Cell Equalizer
CAN	Controller-Area-Network
CHB	Cascaded H-bridge
CSB	Current Source Bridge
CSC	Current Source Converter
CSI	Current Source Inverter
DAB	Dual Active Bridge
DER	Distributed Energy Resource
DFIG	Double-fed Induction Generator
DPS	Dual Phase Shift
DSC	Digital Signal Controller
EPS	Extended Phase Shift
ESD	Energy Storage Device
ESS	Energy Storage System
HF	High Frequency
HFACL	High Frequency Ac Link
HFDC	High Frequency Dc Link
HPSP	Hybrid of Phase Shift and PWM
HVS	High Voltage Side
LPF	Low Pass Filter
LVRT	Low-Voltage-Ride-Through
LVS	Low Voltage Side
MPC	Model Predictive Control
MPPT	Maximum Power Point Tracking
MSVS	Modified Space Vector Sequence
MUPS	Modularized Uninterruptible Power Supply
NPC	Neutral Point Clamp

PFC	Power Factor Correction
PI	Proportional Integral
PLL	Phase Lock Loop
PMSG	Permanent Magnetic Synchronous Generator
PV	Photovoltaic
PWM	Pulse Width Modulation
QP	Quadratic Programming
rms	root mean square
SCR	Silicon-Controlled-Rectifier
SOC	State-of-Charge
SPWM	Sinusoidal Pulse Width Modulation
SVM	Space Vector Modulation
SVPWM	Space Vector Pulse Width Modulation
TPS	Traditional Phase Shift
UPS	Uninterruptible Power Supply
V2G	Vehicle-to-Grid
VSB	Voltage Source Bridge
VSI	Voltage Source Inverter
VSR	Voltage Source Rectifier
ZVS	Zero Voltage Switching

Chapter 1 Introduction

1.1 Background and Motivation

Energy storage systems (ESSs) are increasingly used in power distribution applications such as uninterruptible power supply (UPS), wind/photovoltaic power generation and vehicle-to-grid (V2G) applications [1-7]. There are many reasons for using ESS in the built environment. One reason is to facilitate incorporation of building-integrated renewable energy sources (RESs) [8-10]. With the concerns on pollution, greenhouse gases emission, depletion and increasing cost of traditional fossil fuel, the contribution from renewable energy such as wind and solar power to the total energy consumption in the world will increase. Photovoltaic (PV) panels and small scale wind turbines can be installed on residential and commercial buildings. However, the output power of RESs is not stable but is intermittent. Stand-alone systems require ESS for the purpose of maximum power point tracking (MPPT). When load consumes less power than that can be generated by RES, ESS can store the excess energy; when load consumes more power, ESS can be discharged and supply energy to the load. Even for grid-tied system, RES with ESS can provide the main AC power grid a more constant power and improved stability. Furthermore, grid-tied ESS can shave peak load during periods of high electricity tariffs.

UPS systems consisting of ESS have been widely used in buildings and industry [11-14]. Using UPS is an effective way to protect essential load, such as computer, server and medical equipment, and ESS is a vital part. Fig. 1-1 shows a system configuration of ESS incorporating with UPS. The system has two AC buses and one DC bus. Main AC power grid is connected to a DC-link by an AC/DC rectifier with unity power factor and a cascaded DC/AC inverter connects the DC-link to the load. ESS is connected to the DC-link. Load has high quality power supply even when the voltage of the main AC power grid is highly distorted since it is isolated from the grid. During grid faults, ESS can be discharged to supply energy to the load.

Fig. 1-2 shows a UPS system with multiple modules connected in parallel; this modularized design can improve system reliability and flexibility. Malfunctioned

modules can be bypassed without shutting down the entire system. Furthermore, system power rating can be easily increased or decreased by adding or removing modules.

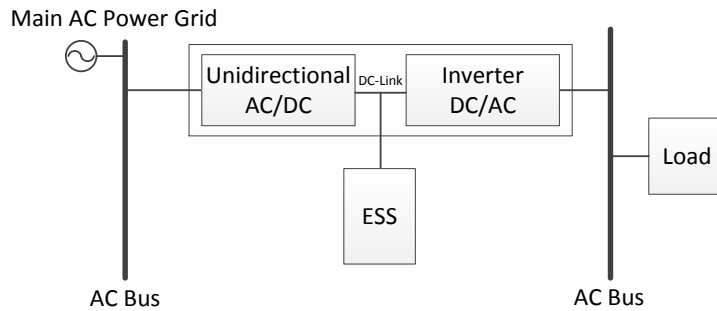


Fig. 1-1 ESS integrated in UPS System

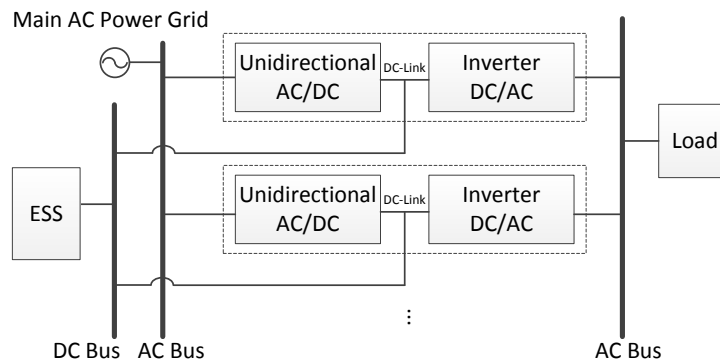


Fig. 1-2 ESS used in modularized UPS system with common DC bus.

Fig. 1-3 shows the integration of ESS to buildings with RESs. ESS may be connected to a common DC bus that is shared by RESs, such as photovoltaic (PV) panels and/or wind turbines. An AC bus connects the main AC power grid, load and some other RESs. ESS may be connected to this AC bus as well depending on system configuration. Bidirectional DC/AC converters connect the DC and AC bus. The power flow between these two buses is controlled by power electronics converters (PECs). This system can also work in island mode without the main AC power grid.

There are many types of energy storage devices (ESDs), such as batteries, ultra-capacitors and flywheels, which are potential candidates for ESS [15]. Ultra-capacitors have high power density and batteries have high energy density [16]. However, a single battery or ultra-capacitor cell has only low DC terminal voltage. Thus, they cannot be connected to the main AC power grid directly. Battery/ultra-capacitor cells are connected in series to obtain sufficient voltage for integration with high voltage AC or DC bus in buildings. The

series-connected battery/ultra-capacitor cells have an unbalancing issue after several charging/discharging cycles because of their varying chemical and electrical characteristics. Some cells may have higher state-of-charge (SOC) than others. Since those cells cannot tolerate over-charging or -discharging, this unbalancing issue reduces overall system utilization. E.g., charging process must be stopped when any cell has been fully-charged, while other cells may not be fully-charged. Therefore, an auxiliary circuit for balancing ESD cells must be developed for ESS. For applications of built environment and V2G, fast-equalizing is desired since large capacity batteries are used. How to develop a BCE for fast-equalizing is still a challenge.

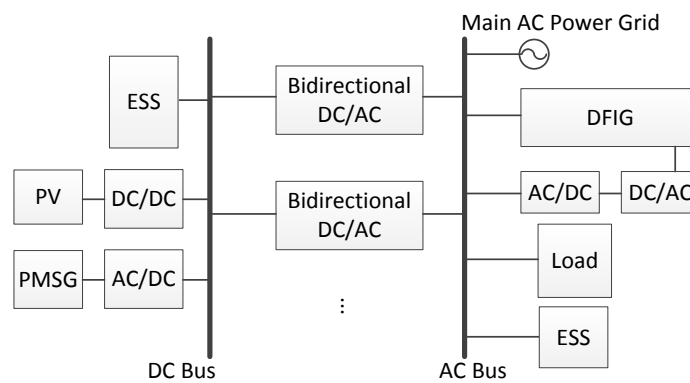


Fig. 1-3 ESS integrated to bulidings with RESs

ESS consisting of parallel-connected ESD cells can avoid the unbalancing issue. PECs employing a high frequency (HF) transformer is used for linking such ESS to the AC grid. Dual active bridge (DAB) cascaded by voltage source inverter (VSI) reported in [17-22] can be a candidate for this application. DAB has bidirectional power flow capability and works under soft-switching. However, it has high reactive power and circulating current when conventional control method is applied. Thus, advanced control method is required to eliminate reactive power and circulating current to improve system performance. Furthermore, DAB can only be optimized when the voltage transfer ratio of low voltage side to high voltage side is constant, otherwise the output power rating will drop. Batteries and ultra-capacitors have wide terminal voltage. When DAB works optimally, the DC bus voltage must be regulated according to the terminal voltage of ESS and it may be much higher than its normal value. Thus, DAB is not an optimum solution for ESDs having wide terminal voltage range. Novel topology should be considered and developed for ESS having wide terminal voltage fluctuation.

Modularized design shown in Fig. 1-2 has great advantages, such as higher flexibility and easier maintenance. However, there are still some challenges to connect multiple inverters in parallel to a common AC bus. DC bus overvoltage of modules is observed when investigating modularized inverters connected in parallel. This instability issue should be studied and solved for applying modularized design to ESS.

Batteries have high energy density but low power density while ultra-capacitors have high power density but low energy density. Hybrid system of batteries and ultra-capacitors provides good energy and power densities. Developing control algorithm for hybrid system of battery and ultra-capacitor becomes an emerging topic since batteries has limited charging/discharging cycles.

1.2 Major Contributions of this Thesis

- *Designed a battery cell equalizer with high power rating and continuous output current for fast-equalizing application.* A current-fed topology is proposed. Compared to conventional topologies, the proposed topology has simple control method and high output current. Furthermore, it requires only one inductor; numbers of passive components are thus significantly reduced. Equalizing speed of different types of BCE are compared to show that the proposed BCE is suitable for fast-equalizing.
- *Proposed a novel hybrid control method of phase shift and PWM for DAB to eliminate reactive power.* Compared to conventional control methods, the proposed hybrid control method eliminates reactive power of DAB and reduces the size of the auxiliary inductor employed by DAB.
- *Designed an isolated bidirectional DC/AC converter with high boost ratio for ESDs having wide terminal voltage swing for grid-tied application.* A novel topology is proposed for interfacing ESDs having wide terminal voltage variation to the main AC power grid. Furthermore, bulky DC bus capacitors and grid side current sensors can be eliminated. Thus, system cost and complexity can be reduced.
- *Investigated the instability issue of multi-paralleled inverters under no-load condition and proposed a novel switching frequency shift method to solve the instability issue:* The instability issue of multi-paralleled inverters is investigated under no-load condition. DC bus overvoltage is observed and the cause is studied.

A novel method based on switching frequency shift is proposed to mitigate the DC bus overvoltage issue.

- *Designed a hybrid system of batteries and ultra-capacitors using model predictive control (MPC):* Batteries have high energy density but cannot be charged or discharged by high current, while ultra-capacitors have high power density but low energy density. The proposed hybrid system of battery and ultra-capacitor has good energy density and can be charged or discharged by high current and therefore has an excellent system performance. Model predictive control (MPC) reduces the current stress and charging/discharging cycles of batteries. This can improve system performance and extend batteries life time.

1.3 Organization of this Thesis

This thesis is divided into eight chapters to explain the theoretical findings for grid integration of ESS in the built environment. A brief description of each chapter is provided here to give an overview of this thesis before going into the details of each individual chapter.

Chapter 1 introduces the background and motivation of this project. Main contributions are summarized and the organization of this thesis is also elaborated to give an overview of each individual chapter. Literature Review is given in Chapter 2. Different kinds of ESDs are introduced and the current development of grid integration of ESS is given.

Chapter 3 proposes a novel topology for fast-equalizing application of series-connected ESD cells. Circuit operation of the proposed topology is presented. Comparisons to other topologies are made to show that the proposed circuit has good performance. Simulation in Matlab/Simulink is conducted and a laboratory hardware prototype is built to verify the proposed topology. This BCE can also be used for ultra-capacitors.

Chapter 4 introduces a power electronics interface consisting of DAB cascaded by VSI for integrating ESS to the main AC power grid in the built environment. High circulating current of DAB reduces system efficiency and limits output power when conventional control methods are employed. A novel hybrid control method of phase shift and PWM is proposed to eliminate the circulating current. Simulation results obtained using Matlab/PLECS libraries are presented to verify the proposed hybrid control method. Chapter 5 proposes a novel circuit for grid integration of ESS with wide terminal voltage

variation. Circuit operation is explained and modulation method is provided. Results of simulation and hardware experiment are given to validate the proposed topology.

Chapter 6 reveals the fact that circulating current at switching frequency of paralleled inverters causes exchange of active power and thus DC bus overvoltage is observed. Theoretical analysis of the DC bus overvoltage using double Fourier transform is presented. Maximum DC bus voltage calculation is introduced. Simulation conducted in Matlab/Simulink verified the theoretical analysis and the maximum DC bus voltage calculation. A novel method based on shifting switching frequency is proposed and explained. Hardware experiments have been conducted to show the effectiveness of the proposed solution.

Chapter 7 introduces a battery/ultra-capacitor hybrid system. MPC is introduced for the proposed hybrid system as it is good at setting constraint and for optimizing. Simulation results in Matlab/Simulink verified the effectiveness of the proposed hybrid system and its control strategy.

The last chapter concludes this thesis and gives recommendations for future research.

Chapter 2 Energy Storage Technology and Its Challenge for Grid Integration

Energy storage systems are widely used in the world. Pumped hydro energy storage (PHES) and compressed air energy storage (CAES) have been used by electric power system for load balancing and frequency regulation for decades. Battery usage in consumer electronics is increasing rapidly in this decade. Hybrid and pure electrical vehicles are becoming more popular. Fig. 2-1 shows the possible usage of ESS in an electric power system [23].

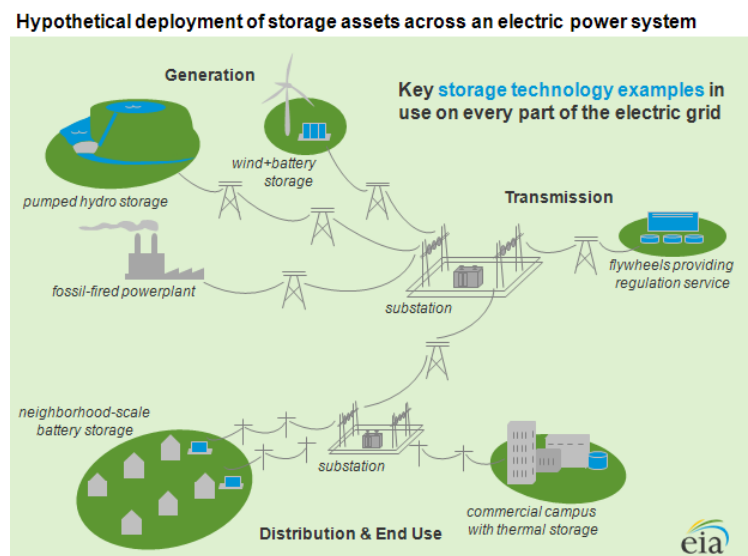


Fig. 2-1 Hypothetical deployment of storage assests across an electric power system[23]

Golden Valley Electric Association (GVEA) initiates a project of building a battery energy storage system (BESS) to improve the reliability of service to its customers. The BESS consists of 13,760 liquid electrolyte-filled Nickel-Cadmium (Ni-Cad) cells and power electronics converters to invert the DC voltage of battery cells to AC voltage[24]. It can provide 27 megawatts of power for 15 minutes in the event of a generation or transmission related outage instantly. The development of this system results in a reduction of 60 percent in power supply type outages.

Electricity consumed by buildings has been increasing in the past 50 years. Residential and commercial electricity consumption in U.S. is about 71.2% of all electricity consumption by 2013 [25]. Fig. 2-2 shows the plot of percentage of electricity consumption by buildings in U.S. over years from 1949 to 2013. It can be concluded from

the figure that electricity energy consumption by buildings plays an important role in modern electric power system.

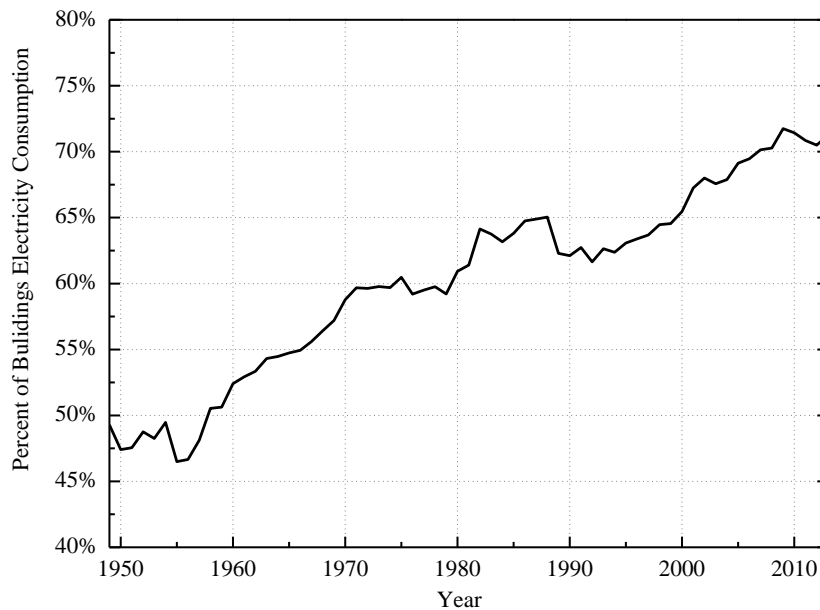


Fig. 2-2 Percentage of buildings electricity consumption over years (1949-2013)

Another trend is that more renewable energy sources (RESs) are going to be integrated into modern electric power system, particularly solar and wind power. According to the study and forecast by U.S. energy information administration (EIA) [26], total renewable generating capacity may grow by 52% from 2012 to 2040 by forecast. Non-hydropower renewable capacity, particularly wind and solar, nearly doubles and accounts for almost all of the growth in renewable capacity as shown in Fig. 2-3. Solar power leads the growth in renewable capacity, increasing from less than 8 GW in 2012 to more than 48 GW in 2040. Wind capacity increases from less than 60 GW in 2012 to 87 GW in 2040, the second-largest amount of new renewable capacity. Wind tops the non-hydropower renewable capacity and will surpass the hydropower share in 2036 by this projection. Even though this study and forecast highly depends on fuel prices and policies, it can be still concluded that more RESs, particularly solar and wind will be integrated in electric generation system. Therefore, microgrid integrating with RES is gaining researchers' interests recently.

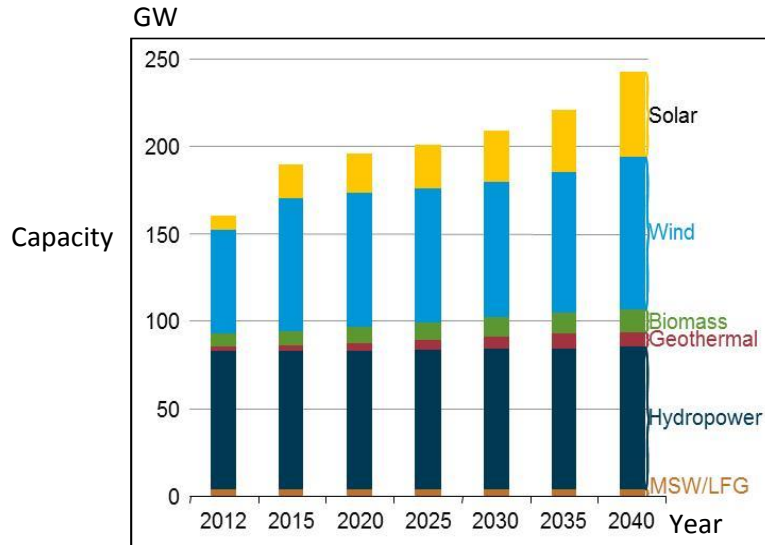


Fig. 2-3 Renewable electricity generation capacity by energy source [26]

The term of microgrid refers to a small scale electricity distribution system, which contains loads and distributed energy resources, (such as distributed generators, storage devices, or controllable loads). A microgrid can connect and disconnect from the grid to enable it to operate in both grid-connected or island mode [27].

Fig. 2-4 shows an illustration of microgrid for residential building [28]. RES such as PV panels and/or wind turbine is installed, and batteries are integrated to provide energy storage.

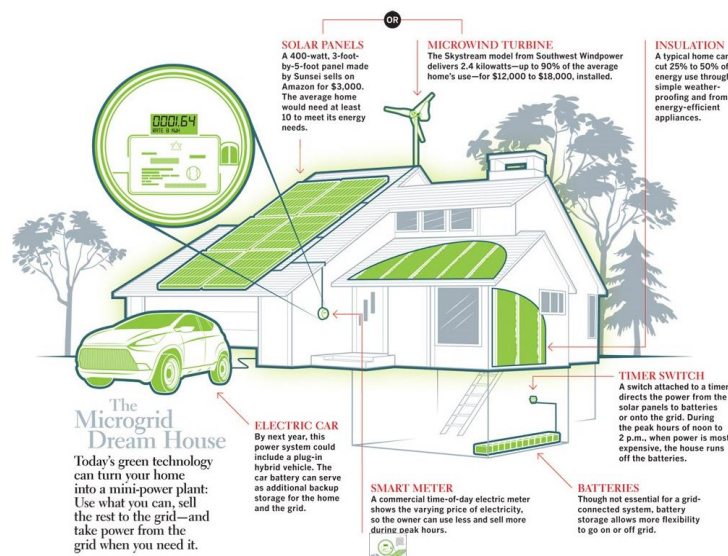


Fig. 2-4 Renewable electricity generation capacity by energy source [28]

Introducing microgrid into the current electric power system will bring a lot of benefits to the costumers. Efficiency, reliability and sustainability are the three major benefits.

- **Efficiency**

6 percent of the electricity is lost in transmission and distribution in average from 1990 to 2012 (eia estimates [29]). In a microgrid infrastructure, electricity is generated and consumed on-site, which means electricity requirement from distant power plant can be reduced and thus transmission and distribution loss can be significantly reduced.
- **Reliability**

Microgrid can operate in grid-connected mode or islanded-mode and it provides highly reliable services to customers. During fault of the main AC power grid, microgrid can still operate by micro-turbine generators, energy storage and other available energy sources. Microgrid also provides electric power supply with high level of security. This distributed on-site power generation can mitigate the chance of losing energy supply under acts of terrorism, natural disasters or other risks.
- **Sustainability**

RESs, such as solar and wind power, integrated in microgrid promise a fossil-fuel free and zero greenhouse gas emission future. Energy storage technology overcomes the energy intermittent issue of RES. With energy storage, solar or wind power generation may operate in MPPT mode to achieve maximum energy utilization. Energy is stored to ESD when RESs generate more power than that can be consumed by load, like in good sunshine or windy weather, and energy can also be released from ESDs and supply to the load when RESs cannot produce enough energy.

RESs and their integration to microgrid as vital part for the technology of deploying microgrid however are still under investigation and development. The next section will introduce and review the current technology of ESDs. Then, the issues of integrating ESDs to microgrid in built environment will be introduced.

2.1 Energy Storage Technology

Various electric energy storage devices are available in the market nowadays. They have different characteristics and may be used for different applications [30]. Fig. 2-5 shows the capacity and discharge time of various energy storage technologies. Selection of energy storage devices for microgrid application of built environment is a trade-off. The considerations are power rating, power and energy density, lifetime and maintenance. Current ESD technologies are introduced and comparisons are made for the application of microgrid for built environment.

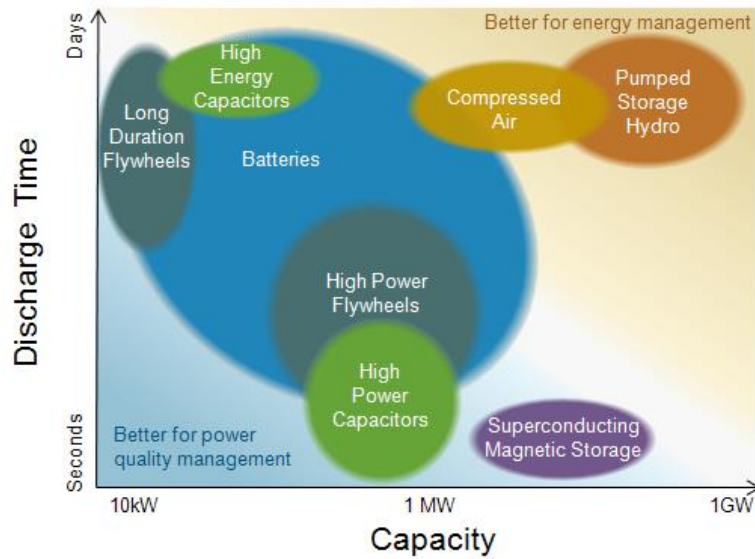


Fig. 2-5 Electric energy storage technologies in terms of capacity and discharge time [30]

2.1.1 Pumped Hydro Energy Storage

Pumped hydro energy storage (PHES) has long history of usage in electric power system, and the first usage can be traced back to 1890s'. PHES system use off-peak power to pump water uphill to an elevated reservoir and release water downhill and through hydroelectric turbine to produce electricity during peak hours. The capacity of PHES can be very large and power rating can be very high, up to several thousands of megawatts. It can provide energy management and load leveling services. Fig. 2-6 shows an illustration of a PHES system [31]. The main disadvantages of PHES system is that hydroelectric power highly depends on geography and has controversy about negative impact on environment. Furthermore, it has high cost.

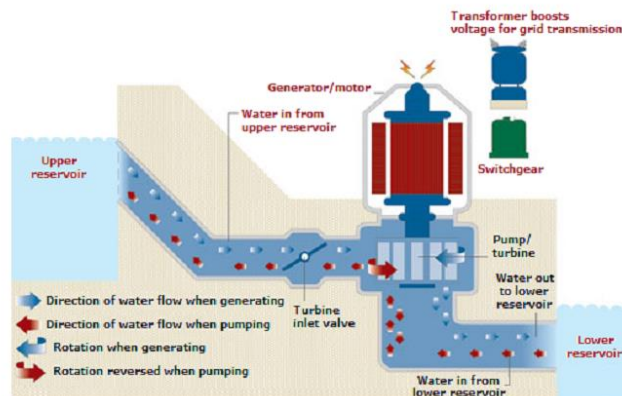


Fig. 2-6 illustration of a PHES system [31]

2.1.2 Compressed Air Energy Storage

Similar to PHES using elevated water, compress air energy storage (CAES) system stores energy by compressing air in suitable structures. Large CAES system often uses geologic structures underground. When off-peak power is available, CAES system compresses air and stores energy. The stored high-pressure air is then used for producing power during peak demand hours[32]. Fig. 2-7 shows an illustration of a CAES system. Similar to PHES system, CAES system has disadvantages of high geographic dependence and high investment cost.

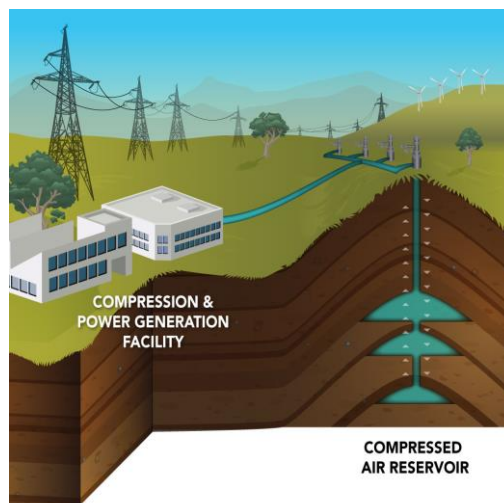


Fig. 2-7 Illustration of a CAES system [31]

2.1.3 Electrochemical Batteries

A battery stores potential energy through the chemical reactions of its electrochemical components. Charging a battery causes reactions in the compounds which then stores the energy in a chemical form. Upon demand, reverse chemical reactions cause electricity to flow out of the battery. Battery energy storage systems (BESS) are widely used in the world and have various scales. Small BESS are commonly used in consumer electronics, such as cell phone, electric tools and notebooks. Large scale system, which can be up to several megawatts, can also be found in power grid. XcelEnergy[®] has built a one megawatts (MW) wind energy BESS in Luverne, Minnesota, using sodium sulfur (NaS) battery technology [33]. There is a wide range of battery technologies available today: lead–acid, nickel–cadmium, nickel–metal hydride, nickel–iron, zinc–air, iron–air, sodium–sulfur, lithium–ion and lithium–polymer. The energy efficiency of battery

modules is in the range of 60-80% depending on how often they are cycled and the electrochemical types used [34],[35]. Fig. 2-8 shows energy density versus power density for various battery technologies, it can be observed that batteries may be optimized to high power density or high energy density but difficult for both [36].

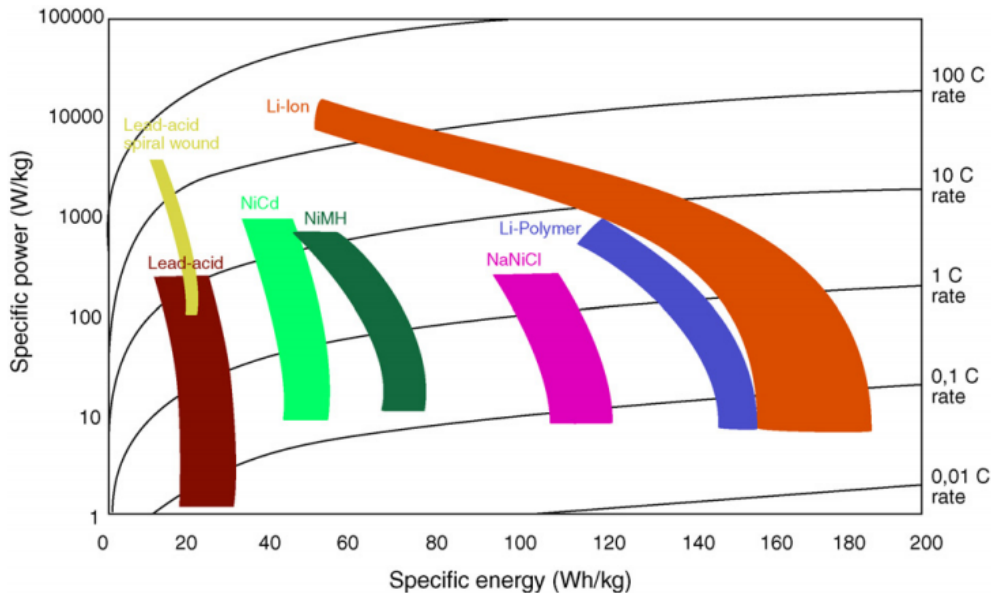


Fig. 2-8 Comparison of various battery technologies regarding their power and energy

Another disadvantage of BESS is that, batteries have limited charging/discharging cycles and are not suitable for applications requiring frequent charging/ discharging.

2.1.4 Ultra-Capacitors

Ultra-capacitors, also known as “double-layer capacitors” or super-capacitors, polarize an electrolytic solution to store energy electrostatically. In an ultra-capacitor, there is a dielectric separator used to prevent the charge from moving between the two electrodes. Unlike batteries having high energy density, ultra-capacitors are more considered as power source. Commercial available ultra-capacitors have lower energy density of less than 5 Wh/kg but higher power density of over 10,000 W/kg [37].

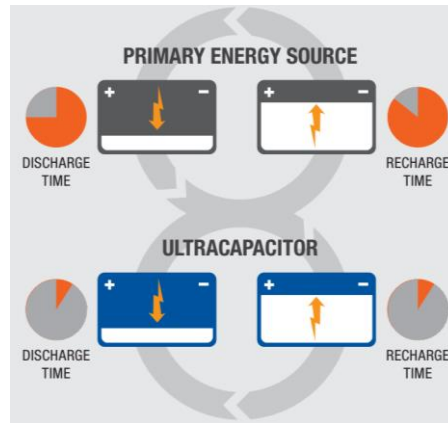


Fig. 2-9 Illustration of how ultra-capacitors work comparing to other primary energy source[36]

Fig. 2-9 shows an Illustration of how ultra-capacitors work comparing to other primary energy source, e.g. batteries or fuel cells. Ultra-capacitors can deliver high power during peak demands, then quickly store energy and capture excess power that is otherwise lost. They efficiently complement a primary source. Furthermore, they can be charged /discharged over hundreds of thousands of times.

2.1.5 Flywheel

Flywheel energy storage systems (FESSs) store kinetic energy in a rotating mass. The energy capacity of an FESS depends on the form and rotational speed of the flywheel. When being charged, flywheel is accelerated by a motor, which is typically driven by a power electronics converter, to store the kinetic energy in its rotational motion. Flywheel keeps rotating and the kinetic energy is maintained in standby mode. When being discharged, energy stored in flywheel is released to load through a generator and a power electronics converter. Normally, motor, generator and power electronics converter are combined in modern FESS design. Fig. 2-10 shows a FESS for UPS application [38]. An AC/DC converter connects a FESS to the DC bus of a UPS. UPS uses the power electronics converter to control the energy flow of the FESS.

FESS has advantages of high power density, low maintenance cost, large charging/discharging cycles and even comparable energy density to battery. It is an attractive energy solution for future demand, especially for applications requiring frequent charge and discharge with high power. However, the cost of flywheel is still relatively high [39-41].

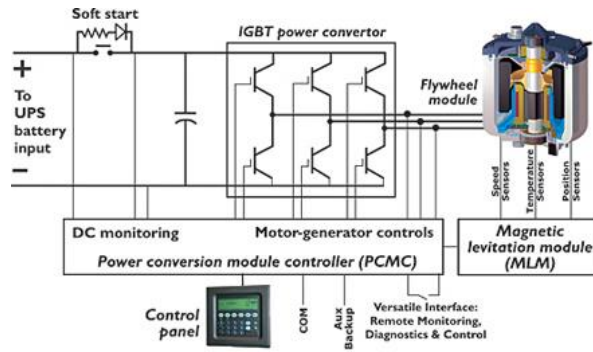


Fig. 2-10 FESS used in UPS application for buildings [37]

2.1.6 Fuel cells

Fuel cells are hydrogen-based ESDs, which are receiving increasing attention recently [42-54]. U.S. Department of Energy (DOE) treats fuel cells as “an important enabling technology for the nation’s energy portfolio and have the potential to revolutionize the way of powering the nation [55]”. Fuel cells are energy-efficient, clean, and fuel-flexible. A fuel cell uses the chemical energy of hydrogen to produce electricity cleanly and efficiently with water and heat as byproducts. A single fuel cell consists of an electrolyte and two catalyst-coated electrodes. Fuel cells are classified by the type of electrolyte employed. Polymer electrolyte membrane (PEM), direct methanol, alkaline, phosphoric acid, molten carbonate and solid oxide are the main types [56]. Fig. 2-11 shows a demonstration of PEM fuel cell.

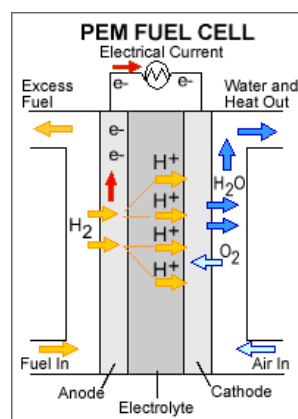


Fig. 2-11 Example of a Polymer Electrolyte Membrane (PEM) fuel cell [55]

A single fuel cell stack has a power rating of several hundred watts to several hundred kilowatts. The power rating of a fuel cell system can be up to one megawatt or even

higher. The disadvantages of fuel cell are that they have very slow dynamics and the issue of hydrogen fuel generation.

2.1.7 Comparisons and Conclusions

There are a lot of parameters that need to be considered for selecting right ESDs in real applications [40],[41],[57]. However, this thesis does not focus on ESD and there are various applications having various requirements, which results a challenge for a single type of ESD fitting for all applications. Furthermore, the technology of ESD keeps developing, thus disadvantages and advantages of different types of ESDs will also be changing in future. Therefore, this chapter is not trying to give a comprehensive comparison of all specific types of ESDs. It is more aimed to give a general guidance on what kind of ESD is more suitable for applications of microgrid in the built environment.

Table 2-1 Key features of different storage technologies [39].

	Power Rating	Discharge Duration	Response Time	Lifetime / cycles
PHES	100-4000 MW	4-12 h	sec-min	30-60 yrs
CAES	50-300 MW	6-20 h	sec-min	30 yrs
Flywheel (low speed)	250kW – 2 MW	3 – 120 s	<20 ms	20 yrs
Flywheel (high speed)	<20 MW	<1 h	<20 ms	20 yrs
Ultra-capacitor	<100 kW	<1 m	<5 ms	5-10 yrs
Lead-acid Battery	<50 MW	1m – 8h	<5 ms	<2,000 cycles
Li-ion battery	<1 MW	1h	< 5ms	<3,000 cycles
NaS Battery	< 90 MW	<8 h	n/a	<3,000 cycles
Fuel Cell	<250 kW	depending on fuel	sec-min	10-20 yrs

In summary, PHES and CAES are geographic dependent and usually have large power rating thus they are more suitable for large scale power grid application, which requires large amount of energy. Battery, ultra-capacitor, flywheel and fuel cell have various power rating and flexible scale configuration, they have power rating from less than 1kW to hundreds of kW, thus are more suitable for microgrid in built environment. It can be observed from Table 2-1 and Fig. 2-5 that ultra-capacitor has high power density, large

charging/discharging cycles, and fast dynamics and thus is perfect for applications requiring fast charging/discharging. Battery can be optimized for high power density or high energy density but not for both. Thus, battery/ultra-capacitor hybrid system with both high energy and power density becomes attractive. Flywheel is similar to battery, and has long lifetime and more charging/discharging cycles. This technology is ideal for applications requiring frequent charging/discharging. Flywheel shows a promising future however is still expensive. Fuel cell can provide clean energy with only heat and water as byproducts. But it has an issue of energy regenerating, which means the energy flow is only unidirectional. Regenerative fuel cell (RFC) can also be found. NASA built a RFC in Glenn research center[58], however existing state-of-the-art RFC systems require two separate stacks and significant auxiliary support hardware. This structure results in high cost, thus it is not practical for buildings. Energy storage systems in built environment usually need bidirectional energy flow. Therefore, fuel cell is an ideal primary or backup energy source but not for energy storage applications of buildings. Based on the review of key features of different energy storage technologies, batteries and ultra-capacitors are considered to be qualified candidates for applications in built environment.

2.2 Challenges for Grid Integration of Energy Storage System

Among reviewed energy storage technologies, batteries and ultra-capacitors are considered to be candidates for ESS in buildings. However, they have different electrical interface re the current main AC power grid used in buildings. The terminal voltage of a single lithium-ion battery is 3.6-3.7 V and a single ultra-capacitor cell has even lower voltage of 2.5V, while the main AC power grid system is about 220V/110V, 50/60Hz. Therefore, power electronics converters are required to interface those ESD cells with low DC voltage to the main AC power grid with high AC voltage. This section will introduce issues of integrating ESDs to main AC power grid for microgrid in the built environment.

2.2.1 Unbalancing Issue of Series-Connected Cells

Single battery or ultra-capacitor cell has only low terminal voltage while AC grid or DC grid in buildings have much higher voltage. Thus, battery and ultra-capacitor cells are stacked in series to provide sufficient voltage for grid integration. Due to varying chemical and electrical characteristics, there will be unbalancing issue for those series-

connected ESDs (battery or ultra-capacitor cells) after several charging/discharging cycles. This unbalancing issue will reduce maximum energy utilization or even damage the ESDs, since advanced ESDs cannot tolerate over-charging or discharging. When any cell of the series-connected ESDs is fully-charged or discharged, the stack must be disconnected from the main power grid to prevent damaging of the ESD cells.

A Battery cell equalizer (BCE) is an auxiliary electric circuit that is connected to a battery or ultra-capacitor stack to balance the state-of-charge (SOC) of series-connected ESD cells [59-76]. Fig. 2-12 shows the diagram of a BCE. BCEs can be categorized as dissipative and non-dissipative. Dissipative BCE uses shunt-resistors to remove excess energy from battery cells with higher SOC while non-dissipative BCE uses switching capacitors or power electronics converters to exchange energy between cells [77]. Dissipative BCE suffers from heat dissipation and low efficiency. Non-dissipative BCE with power electronics converters is more efficient and flexible.

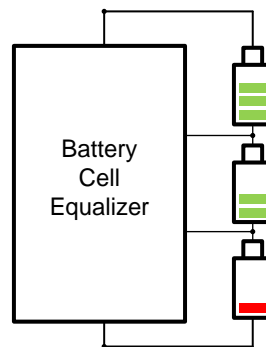


Fig. 2-12 Battery cell equalizer for series connected ESD cells.

BCEs using power electronics converters based on power flow can be classified into three types: charge, discharge and charge-discharge. Charge type BCE charges battery cells having lower SOC [63-67]. Discharge type BCE moves excess energy from battery cells having higher SOC and feeds the energy back to ESS to improve overall system efficiency [78] [79]. Charge-discharge type BCE moves energy between two adjacent cells [68-72],[80]. Fast-equalizing is essential for ESS consisting of batteries with large energy amount, e.g. electrical vehicles and ESS in buildings [81-83]. However, the duration of battery cell equalizing mainly depends on power rating of BCE [62]. Due to the fact that BCEs based on flyback or other topologies that have discontinuous output current are difficult to achieve high power rating, conventional BCEs have long equalizing time. Thus, new technology should be developed for fast-equalizing.

2.2.2 Bidirectional Power Electronics Converter for Interfacing Low Voltage Energy Storage System to AC Grid in Buildings

ESD cells can be connected in parallel to avoid cell balancing issue. Power electronics converters are used for interfacing that ESS with low terminal voltage to main AC power grid. Normally, a high frequency (HF) transformer is employed and provides galvanic isolation. Fig. 2-13 illustrates the system diagram of interfacing ESS with low terminal voltage to AC grid [84],[85]. The ESS is connected to a high voltage DC bus through a bidirectional DC/DC converter, which employs a HF transformer. A cascaded VSI assures bidirectional energy conversion between the main AC grid and the DC-link [86].

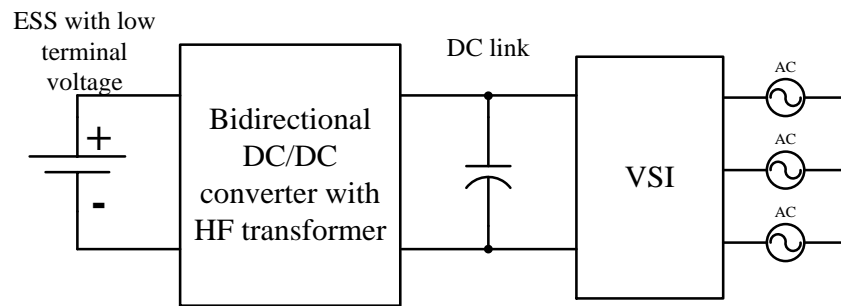


Fig. 2-13 Interfacing ESS to grid by a bidirectional DC/DC converter cascaded by a VSI

Dual active bridge (DAB) converter shown in Fig. 2-14 is reported as the DC/DC converter in this application [17-22]. It has bidirectional power flow with minimum switches.

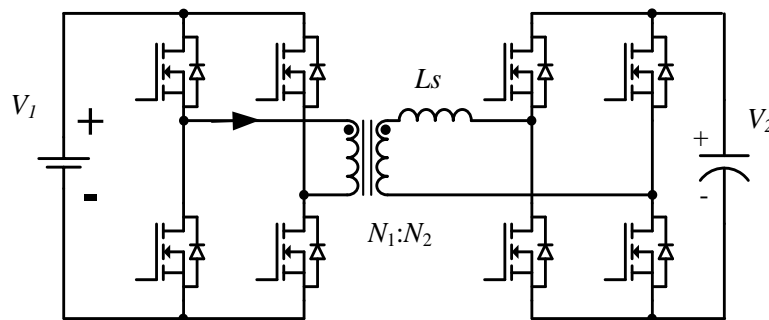


Fig. 2-14 Schematic of dual active bridge (DAB) converter

Topology of two-stage converters with adjustable DC bus is reported in [87]. It has extended zero voltage switching (ZVS) range and a comparable efficiency against DAB. However more switches and passive components are required. Alternatives using high frequency AC link (HFACL) converters without DC capacitors are also reported in [88-

91]. However, bidirectional switches are required for bidirectional power flow, and the modulation scheme is complex.

Traditional phase shift (TPS) control reported in [92] has been widely adopted for controlling DAB. Power flow between low voltage side (LVS), i.e. ESS, and high voltage side (HVS), i.e. DC-link, are controlled by the phase shift of the two full bridges. Soft switching characteristics of DAB have been studied in [20]. Power loss model is studied and discussed in [17]. However, TPS control causes high circulating current and reactive power, which increases system loss and reduces output power capability. Extended phase shift (EPS) control [21] and dual phase shift (DPS) control [19],[93-96] are proposed to reduce the undesired circulating current. Those control methods can reduce reactive power and even eliminate it in certain circumstance. However, circulating current still exists in most cases. In [22], PWM control is introduced, however this method is very complex. How to eliminate circulating current is still remained to be solved.

DAB has good performance when the terminal voltage of ESS only varies in a narrow range. DC-link voltage can be regulated according to the LVS voltage and the voltage transfer ratio can be kept as a constant to let DAB operate optimally [85],[86]. However, when ESS have wide terminal voltage (such as system consisting of ultra-capacitors), the DC-link voltage has to be regulated widely to keep the voltage ratio as a constant. Otherwise there will be high circulating current and the output power rating will be reduced. E.g., when the voltage of ESS may change from 50% to 100%, HVS voltage will be regulated from 50% to 100% and the maximum DC bus voltage will be doubled comparing to normal DC bus voltage. Furthermore, DAB requires bulky DC capacitors to smooth the bus voltage due to high current ripple. Novel bidirectional DC/AC converter is needed to be considered for ESS with wide terminal voltage swing.

2.2.3 Instability Issue of Modularized Energy Storage System

Modularized design can improve system reliability and flexibility, particularly for energy storage applications. Overall energy and power capacity can be easily expanded by adding more modules. One challenge of modularized design for energy storage application is to connect multiple inverters in parallel. Uninterruptable power supply (UPS) is a typical usage of integrating ESS in buildings to protect essential loads [97],[98]. Fig. 2-15 shows the diagram of an on-line UPS system. [11-14].

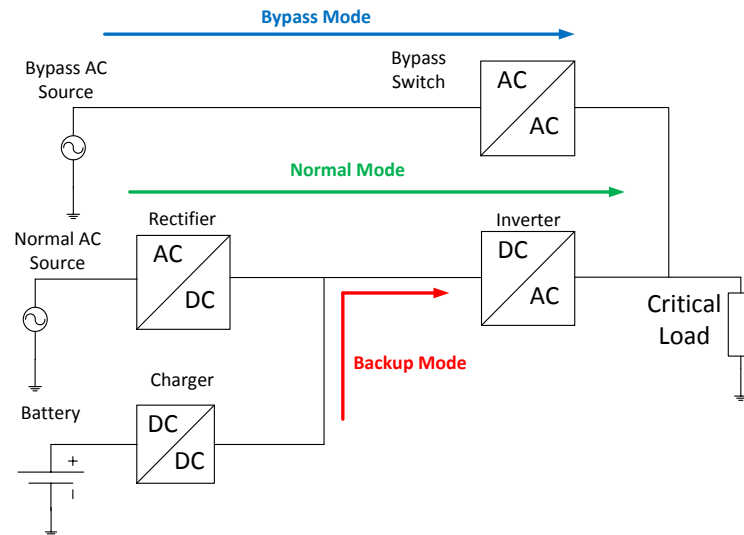


Fig. 2-15 Diagram of an on-line uninterruptible power supply (UPS) system

Output voltage of a practical inverter contains two groups of frequency components. (1) Fundamental component of AC power, which is normally 50/ 60Hz, and its harmonics. (2) Fundamental component of carrier wave and its harmonics. The fundamental frequency of the carrier wave is related to the scheme of PWM generation. Many control schemes have been proposed to balance the output current or power of paralleled inverters. These control schemes can be categorized into two main groups [14]. (1) Active power sharing. This method uses communication circuits to exchange information, such as output power and voltage of each inverter [99-107]. (2) Droop control [108-113]. This method is used for multiple synchronous generators to share current in AC power system and is extended for controlling paralleled inverters [114]. Impacts of the carrier wave components on parallel converters have been investigated by researchers in recent years. In [115], an active-power-filter (APF) based on parallel-interleaved inverters has been proposed. Paralleled inverters are connected to a common DC bus, and the interleaving structure can help to reduce current ripple and the size of the inductors. A modified discontinuous PWM scheme is reported in [116] for paralleled three-phase voltage-source multi-level inverters and an interleaved three-phase AC/DC converter with PFC is proposed in [117] to mitigate voltage stress and current harmonics. An optimized carrier wave interleaving angle (phase difference between two carrier waves) is employed in [118] to minimize grid-side current ripple. However, instability issue of paralleled inverters caused by the phase shift and frequency difference of carrier waves has not been studied. DC bus

overvoltage is observed for paralleled inverters. The causes of the DC bus overvoltage should be investigated, particularly for the impact of carrier wave components.

2.2.4 Power Dispatch for Battery/Ultra-capacitor Hybrid System

As aforementioned, batteries are good energy sources. However they have limited charging/discharging cycles and limited output current. Ultra-capacitors are good power sources, and have many more charging/discharging cycles. Thus, incorporating these two sources will achieve good system performance. In a battery/ultra-capacitor hybrid system, batteries provide system energy and ultra-capacitors provide the transient power. How to dispatch power between batteries and ultra-capacitors optimally is still an issue. Novel control methods are proposed to reduce battery current stress and charging/discharging cycles to extend battery lifetime [119-121]. Frequent charging/discharging batteries by high current can be avoided. However, how to meet the energy demand under fluctuating loads is still in need of further investigations. Low pass filter (LPF) is a popular solution to dispatch power among batteries and ultra-capacitors. However, batteries may still be charged and discharged frequently. Novel control method is still needed to be investigated.

2.3 Conclusions

Electrochemical battery, ultra-capacitor, flywheel and fuel cell are considered as competitive for ESS applications in built environment among various energy storage technologies. Batteries have high energy density and ultra-capacitors have high output current. Hybrid system consisting of both batteries and ultra-capacitors has good system performance. Flywheels have compromising energy and power density, thus can be alternatives to batteries and ultra-capacitors. Fuel-cells have good energy density but have very slow dynamics and the output power is usually unidirectional. They are more used as back-up energy source. Considering the bidirectional power flow requirement and cost, battery and ultra-capacitors are qualified candidates for ESS in built environment.

Battery cell equalizers are essential for batteries and ultra-capacitors that are connected in series to solve the unbalancing issues. Various cell equalizers are proposed by researchers. Recently, cell equalizers for high power application that requires fast-equalizing attract researchers' interests. BCE for fast-equalizing is still a challenge. DAB is considered as a promising power electronics solution for bidirectional DC/DC application and can link

low voltage ESS to high voltage DC bus. However, novel control strategy is still under investigation to reduce circulating current. Furthermore, DAB is not an optimum solution for ESDs with wide terminal voltage variation, such as ultra-capacitors or lead-acid batteries. Thus, how to integrate ESS with wide terminal voltage to AC power grid in a more efficient way is still unsolved. Modularized design has many advantages for ESS application. However, DC bus overvoltage is observed for paralleled inverters and this DC bus overvoltage will cause instability issue. The cause of the DC bus overvoltage is needed for investigation. Hybrid system of batteries and ultra-capacitors has high energy density and high output current. How to dispatch power demand among batteries and ultra-capacitors to reduce battery charging/discharging cycles optimally is still a challenge.

Chapter 3 Developing Fast Battery Cell Equalizers

This chapter is organized with introducing the background of BCE firstly. The proposed BCE is then presented and circuit operation is explained in Section 3.1. Comparison to other topologies is also given in this section. Section 3.2 shows the simulations results of the proposed BCE. Section 3.3 describes an automatically switched maximum current/voltage control method for equalizing battery cells. Section 3.4 compares the cell-equalizing speed of different types of BCEs. Laboratory hardware setup and experimental results are presented in Section 3.5. Section 3.6 concludes this chapter.

A single battery or ultra-capacitor cell only has low terminal voltage of less than 5V while the main AC power grid in built environment has high voltage of 110V or 220V. Thus, battery and ultra-capacitor cells are connected in series to provide sufficient voltage. Fig. 3-1 shows an example of grid integration of ESS with series-connected ESDs. Series-connected battery or ultra-capacitor cells are connected to a DC bus by a DC/DC converter and a voltage source inverter (VSI) is used as an interface to the main AC power grid.

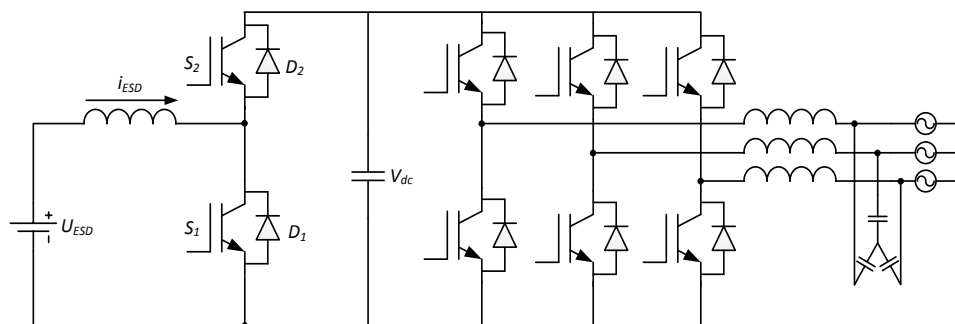


Fig. 3-1 Tie ESDs to main AC power grid through DC/DC converter cascaded by voltage source inverter

Due to varying chemical and electrical characteristics, there will be unbalancing issue for those series-connected ESD cells after several charging/discharging cycles. This unbalancing issue will reduce maximum energy utilization since advanced ESDs cannot tolerate over-charging or -discharging. Battery cell equalizer (BCE) can be incorporated in ESS to balance the state-of-charge (SOC) of series-connected battery or ultra-capacitor cells. As shown in Fig. 3-2, BCEs can be categorized into dissipative and non-dissipative regarding equalizing method.

Dissipative method uses shunt-resistors to remove excess energy from battery cells with higher SOC. Fig. 3-3 shows an example of dissipative BCE. Each battery cell is paralleled by a resistor, and a mosfet is used for connecting or disconnecting the resistor to that cell. During charging process, when a battery cell is fully-charged, the corresponding mosfet will be turned-on to dissipate excess energy. This method is simple and can be implemented easily. However excess energy is dissipated as heat, so this method suffers in terms of low efficiency and heat dissipation.

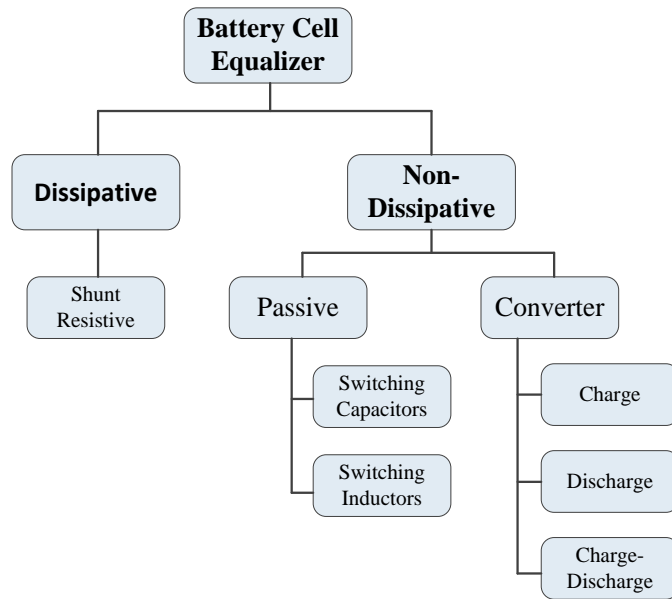


Fig. 3-2 Category of battery cell equalizer.

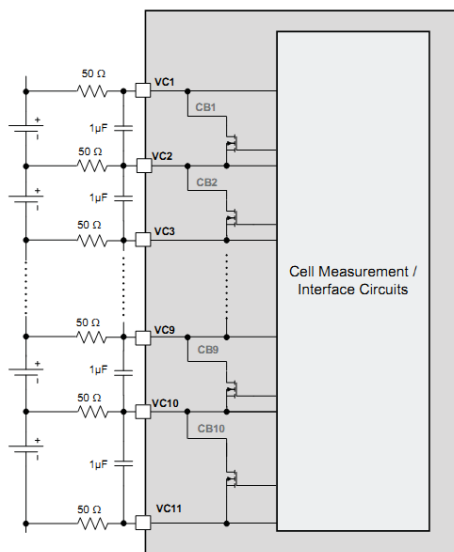


Fig. 3-3 Illustration of dissipative BCE.

Non-dissipative method uses switching capacitors or power electronics converters to exchange energy and balance the battery cells [77]. Switching capacitors is simple but required long equalizing time. Fig. 3-4 shows the topology of BCE using switching capacitors.

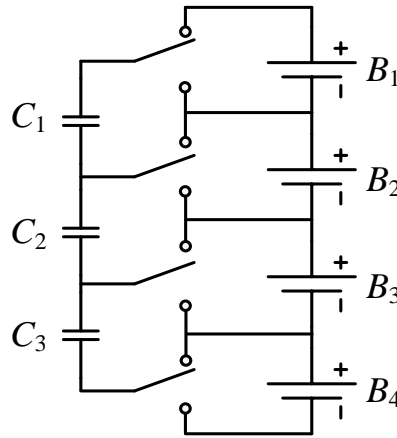


Fig. 3-4 Battery cell equalizer using switching capacitors.

Using power electronics converters is more efficient and flexible. This kind of BCEs can be classified into three types of charge, discharge and charge-discharge in terms of power flow. Charge type BCE charges battery cells with lower SOC [63-67]. Discharge type BCE moves excess energy from battery cells with higher SOC and feeds the energy back to ESS to improve overall system efficiency [78] [79]. Charge-discharge type BCE moves energy between two adjacent cells [68-72],[80].

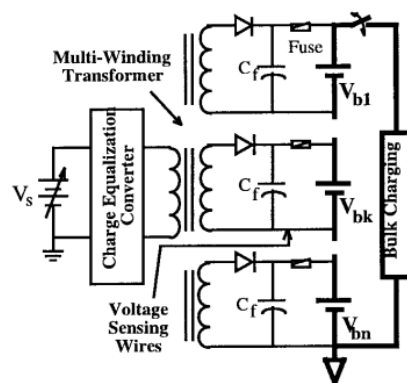


Fig. 3-5 Charge type BCE using multi-winding transformer.

Charge type BCE charges battery cells that are not fully-charged. In [67], a charge type BCE based on a multiple secondary windings transformer is proposed and shown in Fig.

3-5. A power electronics converter transfers energy from a voltage source to the secondary side of a multi-winding transformer to charge battery cells.

The secondary windings of the multi-winding transformer have the same number of turns and thus the battery cells that are connected to the secondary windings have the same charging voltage. In ideal condition, battery cells with lower voltage will be charged while battery cells with higher voltage will not be charged until all cells have the same voltage.

Fig. 3-6 shows a two stages BCE based on flyback converter [79]. In the first stage, each battery cell is connected to a flyback converter. Excess energy in battery cells with higher SOC is removed by the flyback converters in the first stage, and the energy is transferred to the flyback converter in the second stage. The second stage converter recycles the energy by charging the battery pack. However this method uses many converters and are costly and bulky.

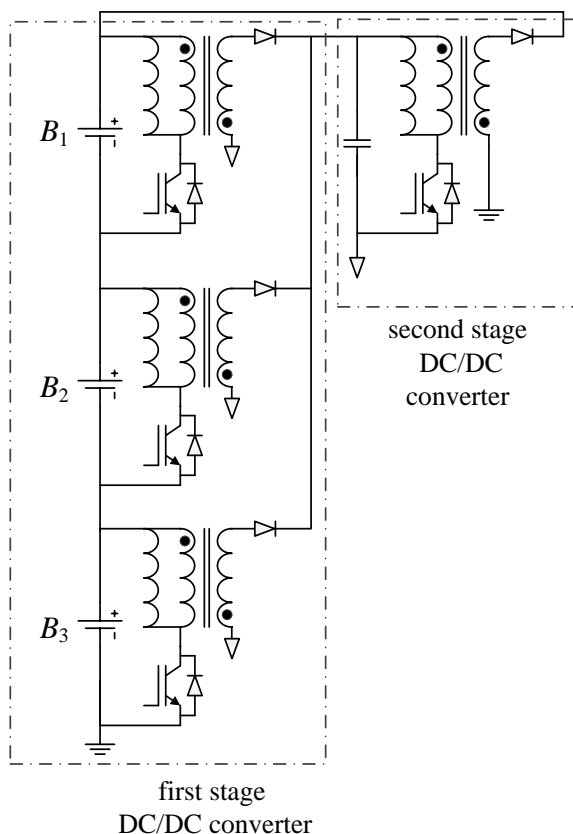


Fig. 3-6 Discharge type BCE using two stages flyback converters.

Charge-discharge type BCE is reported in [68-72],[78],[80]. The idea is to use a bidirectional DC/DC converter to transfer energy between two adjacent battery cells. Fig. 3-7 shows a BCE using bidirectional buck-boost converter [78].

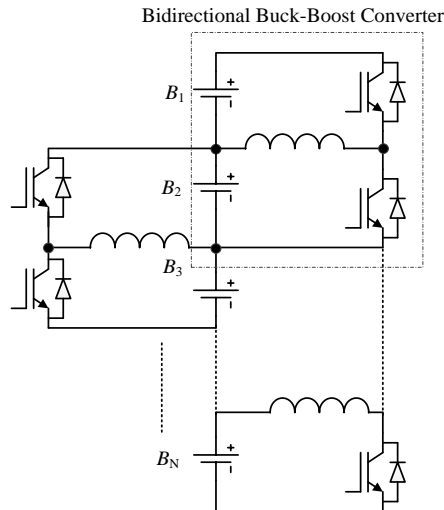


Fig. 3-7 Discharge-discharge type BCE using bidirectional buck-boost converter.

Fast equalizing is essential for applications consisting of large number of battery cells, e.g. electrical vehicles and ESS in built environment [81-83]. However, the cell-equalizing speed mainly depends on power rating or output current capability of BCE [62]. Due to discontinuous output current, conventional BCEs are difficult to achieve high power rating and thus have low cell-equalizing speed.

In this chapter, a novel BCE with continuous current is proposed for fast-equaling. As shown in Fig. 3-8, the proposed BCE works with the charger of battery pack. After the unbalance of battery cells is beyond certain threshold, the proposed BCE is activated. The charger is the input voltage source for the proposed BCE. Since the proposed BCE has continuous output current and high power rating, equalizing process could be shortened. Furthermore, the equalizing process is essentially a part of the charging process.

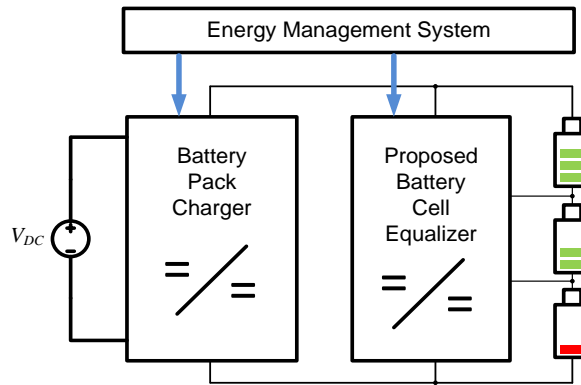


Fig. 3-8 Proposed current-fed full-bridge BCE with battery pack charger.

3.1 Proposed Current-Fed Full-Bridge Battery Cell Equalizer

Fig. 3-10 shows a charge type BCE using voltage-fed full-bridge topology with continuous output current, which can be considered as the candidate for fast-equalizing application. Phase shift control can be used for controlling switches of the full-bridge [28] and generates a square wave AC voltage, which is applied at primary side of a high frequency (HF) transformer consisting of a single primary winding and multi-secondary windings. This HF transformer is used as an interface to link the charger and secondary side battery cells. After rectified by diodes and filtering, the AC voltage that generated by the DC voltage source charges each battery cell at the secondary side with continuous current. However this topology requires many secondary windings and an individual inductor for each battery cell. This will make the BCE bulky and costly.

In this chapter, a novel current-fed topology is proposed. Compared to the voltage-fed topology, it requires only half secondary windings and no secondary side inductor. Fig. 3-9 shows the proposed current-fed BCE. Unlike voltage-fed topology delivering a voltage, the proposed current-fed topology injects a current to charge the secondary side battery cells. All the individual inductors connected to the secondary side battery cells in voltage-fed topology are replaced by a single inductor L_s at the primary side for the proposed topology. System volume and cost can be reduced significantly. Fig. 3-9 shows that the current-fed BCE for 8 battery cells only has one inductor at the primary side while 8 inductors are required for voltage-fed topology.

The HF transformer used for the proposed current-fed BCE only has one primary side winding, and all secondary side windings have the same number of turns. The number of

the secondary side windings equals to the number of battery cells. Full-wave voltage doubler is adopted at the secondary side. Compared to other topology, e.g. half wave rectifier shown in Fig. 3-10 or full wave rectifier, voltage doubler has a continuous output current with minimum components. Table 3-1 summaries the comparison of required number of secondary side windings and diodes for different topologies connecting N battery cells.

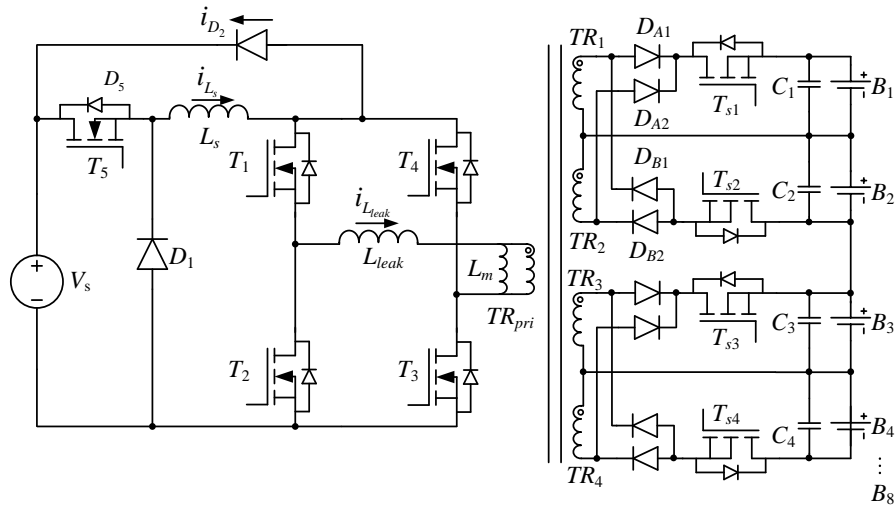


Fig. 3-9 Proposed current-fed full-bridge BCE

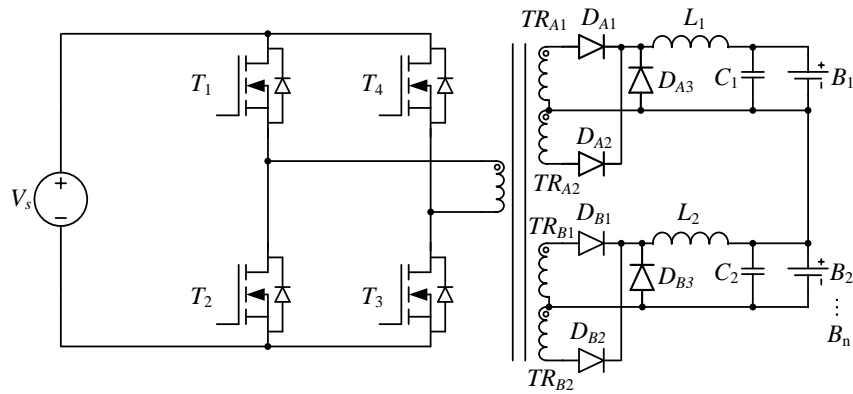


Fig. 3-10 Voltage-fed full-bridge BCE

Table 3-1 Comparison of required number of secondary side windings and diodes for N battery cells for voltage doubler, half-wave rectifier and full-wave rectifier.

	Secondary side windings	Secondary side diodes
Voltage doubler	N	$2N$
Half-wave rectifier	$2N$	$3N$
Full-wave rectifier	N	$4N$

The proposed BCE has a step-down function. D_1 is a free-wheeling diode, which provides a current path when T_5 is off. T_1 - T_4 of the H-bridge are used for generating a square AC current and transferring the primary side current to the secondary side to charge battery cells with lower SOC. Diagonal switch pair of the H-bridge, e.g., T_1 and T_3 , has the same driving signal. Switches in the same leg, e.g., T_1 and T_2 , have complementary driving signals. All switches of the H-bridge have a duty cycle of 0.5. During the current commutation of the primary side, T_1 - T_4 may have a high voltage spike due to the existence of transformer leakage inductance and mosfets junction capacitance. Thus, D_2 is used for clamping possible spike of the drain-source voltages of T_1 - T_4 . Furthermore, neither shoot-through state nor dead-beat is required for the switches belonging to the same leg of the H-bridge, because that D_2 provides a current path for inductor current during commutation. Thus driving signal generation for T_1 - T_4 can be very simple.

Battery cell equalizing current can be regulated by the inductor current, which can be controlled by the duty cycle of T_5 . By properly controlling T_5 and letting the primary inductor work in continuous current mode (CCM), battery cells can be charged by maximum current and equalizing time can be thus shortened. However only one charging current or voltage can be tightly regulated. An automatically switched maximum charging current/voltage method is proposed to regulate charging current/voltage during equalizing. This method will be introduced in section 3.3.

Mosfets connecting battery cells at secondary side, e.g. (T_{s1} - T_{s4}) shown in Fig. 3-9, have function of disconnecting battery cells that has been charged to the target SOC and do not work in high frequency switching mode. Those mosfets can be ignored in some design, since battery cell with lower SOC will catch up with those battery cells with higher SOC. In the work described this chapter, those mosfets are used for precise control and better demonstration of equalizing process.

3.2 Simulation Results

The proposed circuit is verified by simulation results using MATLAB/SIMULINK and PLECS power electronics libraries. For simplicity, two battery cells are connected at the secondary side to verify the proposed circuit. Table 3-2 summaries system parameters used in the simulation. T_5 has a doubled switching frequency compared to that of the switches of the H-bridge. Since the proposed BCE has a step-down function, the turns-ratio of the transformer must be lower than V_{DC}/V_B . The battery cell reference current is the constant charging current.

Table 3-2 System parameters for simulation

Symbol	Description	Value
L_s	Inductance of inductor L_s	1 mH
$C_{1,2,3,4}$	Capacitance of output capacitor	470 μ F
V_{DC}	Voltage of the dc Source	100 V
f_s	Switching Frequency of T_5	25 kHz
f_b	Switching Frequency of T_1 to T_4	50 kHz
$N_p : N_s$	Transformer turns ratio	10 : 1
L_{leak}	Leakage inductance	20 μ H
V_{Bi}	Open circuit voltage of battery cell	8 V
i_{1ref}	Battery cell reference current	5 A

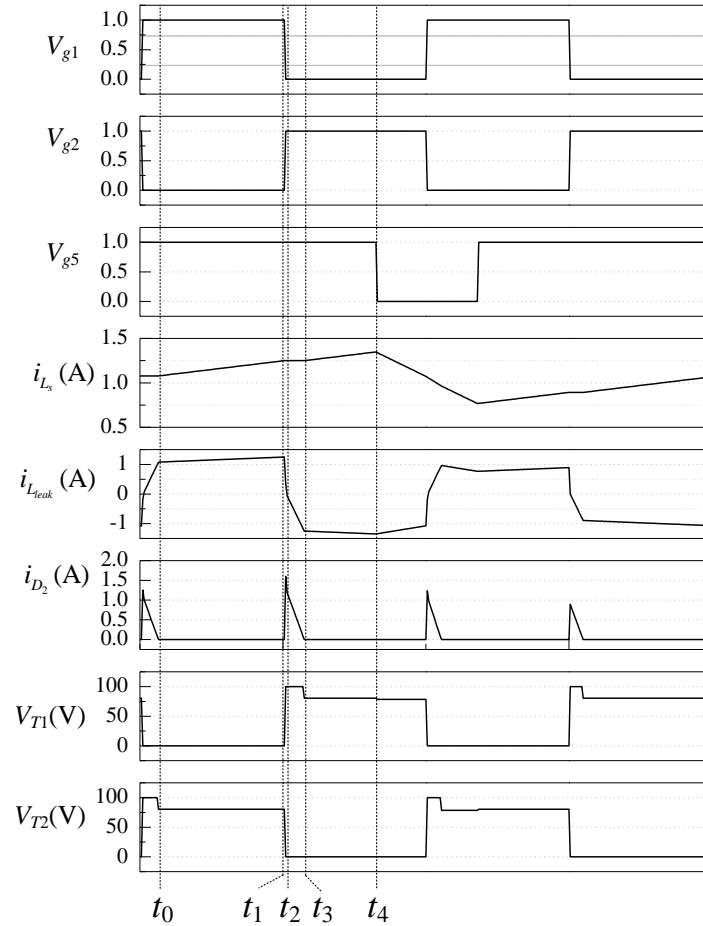


Fig. 3-11 Driving signals and key waveforms of the proposed current-fed BCE

Fig. 3-11 shows driving signals and key waveforms of the simulation. The proposed BCE has three main operation modes during current commutation and will be introduced in the following.

Mode 1 (t_0 - t_1): Fig. 3-12 (a) shows the equivalent circuit for this mode. T_5 is turned on, V_s charges L_s , and thus inductor current i_{L_s} increases. Secondary winding TR_1 charges B_1 through D_{A1} and TR_2 charges B_2 through D_{B2} , since T_1 and T_3 are turned on. Energy is transferred from the DC voltage source to the battery cells.

Mode 2 (t_1 - t_2): Fig. 3-12 (b) shows that when T_1 and T_3 are turned off, D_2 provides a free-wheeling path for inductor current during current commutation. The voltage applied at the primary winding is clamped to V_s . Thus, voltage stress across T_1 and T_3 is V_s . Before T_2 and T_4 are turned on, their anti-paralleled body diodes conduct. Thus, when T_2 and T_4 are turned on, their drain-source voltage is zero and they are turned on under zero voltage

switching (ZVS). In this mode, the transformer leakage inductor is discharged by V_s and battery cells; the energy stored in it is transferred to battery cells and fed back to the voltage source. When the circuit works in steady state, the current of D_2 can be calculated by:

$$i_{D_2}(t) = 2 \cdot \overline{i_{L_s}} - V_s \cdot (1 + D) \cdot t / L_{leak}, \quad (3.1)$$

where $\overline{i_{L_s}}$ is the average inductor current, D is the duty cycle of T_5 .

Mode 3 (t_2 - t_3): After t_2 , the direction of the transformer leakage inductor current reserves. As shown in Fig. 3-12 (c), TR_1 charges B_2 through D_{B2} and TR_2 charges B_1 through D_{A2} , while D_{A1} and D_{B2} stop conducting. D_2 still conducts, the transformer leakage inductor is charged by the difference of V_s and the reflected secondary winding voltage at the primary side. In the end of this mode, the current of D_2 decreases to zero and stop conducting at t_3 . Transformer leakage inductor current equals to $\overline{i_{L_s}}$. When the circuit works in steady state, the current of D_2 can be calculated by:

$$i_{D_2}(t) = \overline{i_{L_s}} - V_s \cdot (1 - D) \cdot t / L_{leak} \quad (3.2)$$

After t_3 , circuit operation is similar to that of mode 1. DC voltage source charges the inductor and battery cells through T_2 and T_4 until t_4 . At t_4 , T_5 is turned off and after that battery cells are charged by the energy stored in L_s . Thus, $\overline{i_{L_s}}$ decreases. Following current commutation process is similar to that of t_1 - t_3 except that D_1 conducts current while T_5 is off. $\overline{i_{D_2}}$ can be calculated by (3.1) and (3.2). As shown in Fig. 3-11, voltage stress of the H-bridge is clamped to V_s by D_2 during the current commutation within a switching period.

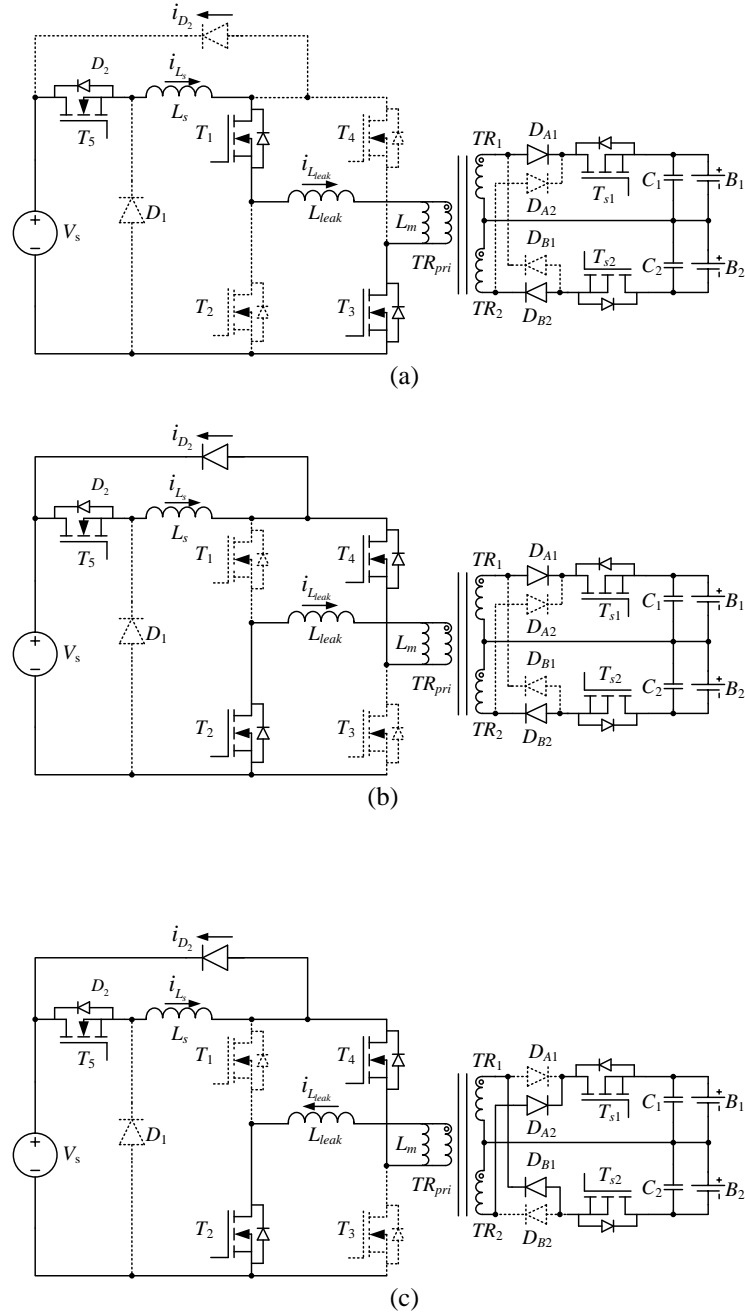


Fig. 3-12 Equivalent circuit of the proposed BCE during current commutation (a) mode 1 (b) mode 2, and (c) mode 3.

As shown in Fig. 3-11, D_2 has maximum current at t_2 and can be calculated by:

$$i_{D_2} = \begin{cases} 2 \cdot \left(\overline{i_{L_s}} + (1-D) \cdot V_s \cdot T_s / 4L_s \right) & D \geq 0.5 \\ 2 \cdot \left(\overline{i_{L_s}} + D \cdot V_s \cdot T_s / 4L_s \right) & D < 0.5 \end{cases}, \quad (3.3)$$

where, T_s is the switching period of T_5 . When $D = 0.5$, the maximum current of D_2 can be calculated by:

$$i_{D_2\max} = 2 \cdot \overline{i_{L_s}} + V_s \cdot T_s / 2L_s \quad (3.4)$$

The ripple of inductor current is negligible when the average current is high and inductance is large enough. In steady state, rms current of D_2 can be calculated by considering (3.1) and (3.2), and can be expressed as:

$$I_{D_2} = \sqrt{\frac{4 \cdot \overline{i_{L_s}^3} \cdot L_{\text{leak}}}{3 \cdot T_s \cdot V_s} \cdot \left(\frac{7}{1+D} + \frac{1}{1-D} \right)}. \quad (3.5)$$

Thurs, D_2 can be selected based on (3.4) and (3.5).

Table 3-3 summaries the comparison of the proposed current-fed BCE and reported cell equalizers regarding number of components and equalizing current. Ramp converter is reported in [64]. Current diverter and two stages flyback converter are used in [78] and [79] respectively. Buck-boost, Ćuk and switching inductor are reported in [63] [70] and [122]. The proposed current-fed BCE has continuous equalizing current and uses less inductors and capacitors. Furthermore, only one switch is required to be controlled; in contrast every switch of BCE using buck-boost converters must be controlled. So the proposed topology has less control complexity.

Table 3-3 Comparison of the proposed current-fed and reported equalizers

Topology	Switches	Diodes	Inductors	Capacitors	Transformer [Primary + Secondary]	Equalizing Current
Charge						
Ramp Converter	2	N	1	2	$1[1+N]$	Discontinuous
Discharge						
Current Diverter	N	N	0	0	$1[1+1]$	Discontinuous
Two stages Flyback	$N+1$	$N+1$	0	1	$N+1[1+1]$	Discontinuous
Buck Boost	$2(N-1)$	0	$N-1$	0	0	Discontinuous
Ćuk	$2(N-1)$	0	$2(N-1)$	$N-1$	0	Continuous
Switching Inductor	N	0	$N-1$	0	0	Discontinuous
Proposed Current-fed BCE	5	$2N+1$	1	N	$1[1+N]$	Continuous

3.3 Control of Battery Cell Equalizing

3.3.1 Equalizing Algorithm

Constant current and voltage charging are two common steps for charging battery cells. In constant current charging, battery cell is charged by a constant current and the charging voltage is maintained under a limitation. In this step, large amount of energy is charged into battery cell. Charging voltage approaches and eventually reaches the limitation. After that, constant voltage charging begins. Charging current decreases to zero in the end and charging voltage remains unchanged.

For the purpose of fast-equalizing, battery cells are designated to be charged at maximum possible current that is for constant current charging. However, multiple battery cells are connected at the secondary side of the proposed BCE, only one control degree of freedom is provided by the duty cycle of T_5 . Thus only one charging current can be tightly regulated and other charging current is automatically decided by the electrical characteristics of the circuitry and battery cells. Maximum charging current among all cells must track the rated charging current, otherwise over-current charging may damage battery cells or even cause ignition. An automatically switched maximum charging current (ASMC²) selection method is proposed for fast-equalizing and preventing battery cells from over-current charging. Fig. 3-13 shows the flow chart of the proposed equalizing algorithm and the proposed control method.

When equalizing process starts, SOC of all battery cells are retrieved by a measurement sub-module. Maximum SOC (SOC_{max}) among all battery cells can be decided and will be used as target SOC for other battery cells. The goal of cell equalizing is to charge all battery cells to the same SOC of SOC_{max} eventually. Since no charging is required for the battery cell having the maximum SOC of SOC_{max} , the corresponding mosfet T_{si} , which connects the battery cell to the BCE, is turned off. During equalizing, charging current of each battery cell having SOC not equal to SOC_{max} is sampled, and the battery cell having maximum charging current can be decided. As aforementioned, the maximum charging current must track the rated charging current. The controller searches the battery cell that has the maximum charging current within every switching period and controls the charging current of the corresponding battery cell to the rated value. The battery cell charging current that is required to be regulated tightly is selected and controlled

automatically. This method ensures that all charging currents are under limitation and at least one cell is charged by maximum charging current. Initially, charging current of the battery cell with the lowest SOC can be selected to be controlled.

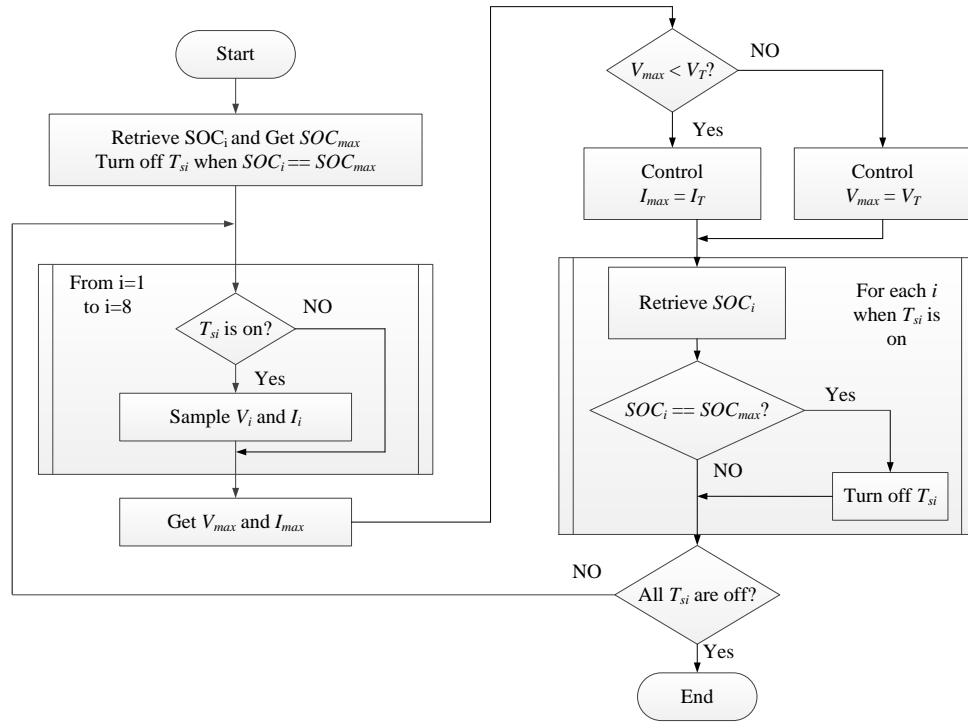


Fig. 3-13 Flow chart of the proposed cell equalizing algorithm with automatically switched maximum charging current.

In some circumstance, battery cells have to be equalized when they have higher SOC and they must be charged in constant voltage mode. Though this case is better to be avoided due to the requirement of fast-equalizing, it is still possible. In this case, charging voltage of each cell is monitored and the maximum charging voltage among all battery cells is controlled under the limit. This process is similar to the ASMC² method.

3.3.2 Control Loop Design

Various battery cell models are discussed in recent years[123]-[124]. Some of them are accurate in terms of describing battery cells in certain operation but are complex. However, this chapter more focuses on battery cell equalizing and the purpose of the control loop is to regulate charging current or voltage. Thus a simple model, which is shown in Fig. 3-14 and consists of a voltage source and a series connected resistor R_s , is sufficient for designing control loop of the proposed BCE.

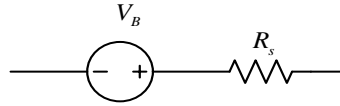


Fig. 3-14 Equivalent circuit of a battery cell for control loop design.

Assuming the charging current of battery cell i is the maximum current among all battery cells and is selected to be controlled, the system model can be expressed by:

$$\begin{cases} L_s \cdot \frac{di_{L_s}}{dt} = d \cdot V_s - (i_i \cdot R_{si} + V_{B_i}) \\ i_{L_s} = \left(i_i + \sum_{j=1, j \neq i}^N i_j \right) \cdot \frac{N_s}{N_p} \end{cases}, \quad (3.6)$$

where V_{B_i} is the open-circuit voltage, i_i is charging current and R_{si} is the series resistance of the i_{th} battery cell that has the maximum charging current. i_j is battery charging current of other battery cells.

Fig. 3-15 shows the close-loop current control diagram, and a two loop strategy is adopted.

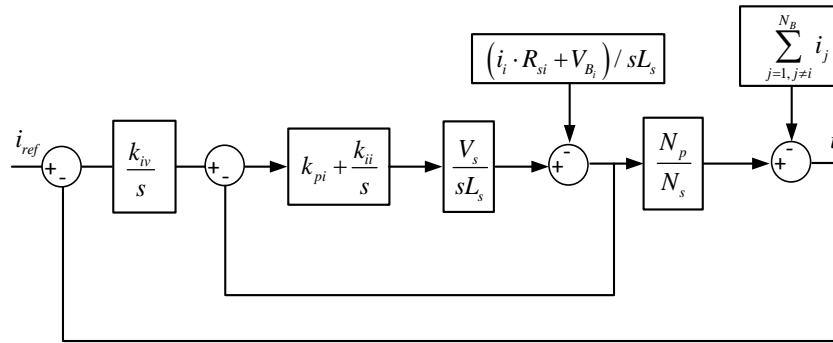


Fig. 3-15 Close-loop current control diagram of the proposed BCE

An outer loop uses an integrator and generates current reference for the inner loop. The inner loop regulates the primary side inductor current by generating duty cycle for T_5 . When battery cell charging voltage must be controlled, a voltage control loop is needed. Diagram of voltage control loop is shown in Fig. 3-16.

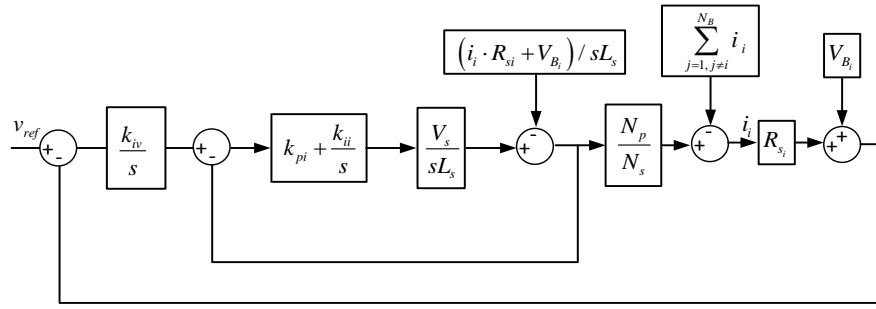


Fig. 3-16 Close-loop voltage control diagram of the proposed BCE

3.4 Comparison of Equalizing Speed for Different Type Battery Cell Equalizers

The speed of cell equalizing process can be evaluated by the power rating for same type BCE. High output power of BCE will shorten equalizing process. For the same power rating, different types of BCEs have varying performance and the cell equalizing speed highly depends on the initial SOC of battery cells, which are random for different battery strings. In this section, cell equalizing time is evaluated and compared for different types of BCEs. In order to simplify the analysis and speed up the simulation, BCEs are modeled as ideal current source and power loss is ignored. Fig. 3-17 shows an example of a Charge/Discharge (C/D)-type BCE using bidirectional buck-boost converters for N battery cells.

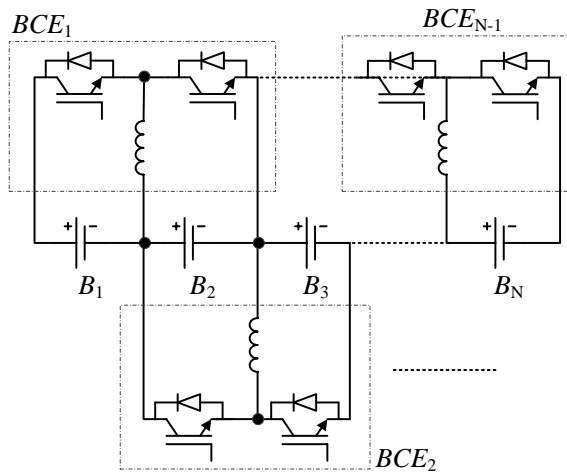


Fig. 3-17 Charge/Discharge type BCE based on bidirectional buck-boost converter.

Simplified model is shown in Fig. 3-18.

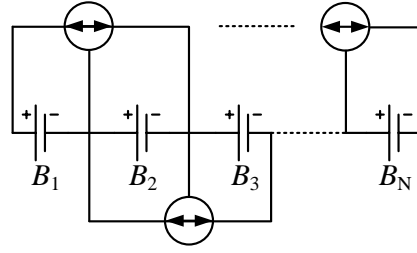


Fig. 3-18 Simplified model of Charge/Discharge (C/D) type BCE.

Each buck-boost converter in a C/D-type BCE tries to balance two adjacent battery cells connected to it. As all battery cells have similar terminal voltage, equalizing time T_{Eq} of this type of BCE connecting to two cells can be calculated by:

$$\int_0^{T_{Eq}} V_1(t) I(t) dt = |SOC_1 - (SOC_1 + SOC_2) / 2| \cdot Q_B \quad (3.7)$$

where Q_B is the battery cell capacity, SOC_1 and SOC_2 are the state-of-charge of battery cell 1 and 2 respectively, $V_1(t)$ is the voltage of cell 1 and $I(t)$ is the output current of one single converter. During equalizing process, battery cell voltage is a constant and the converter is controlled to have output maximum current. Thus $I(t)$ is also a constant and (3.7) can be simplified to:

$$T_{Eq} = \frac{|SOC_1 - (SOC_1 + SOC_2) / 2| \cdot Q_B}{VI} \quad (3.8)$$

When the battery string has 3 cells, SOC_{max} , SOC_{min} , and SOC_{avg} are defined as the maximum, minimum and average SOC of the battery cells in the string and

$$SOC_{min} \leq SOC_{mid} \leq SOC_{max} \quad (3.9)$$

is valid. T_{Eq} can be calculated by:

$$T_{Eq} = \frac{|SOC_{max} - SOC_{avg}| \cdot Q_B}{VI}, \quad (3.10)$$

When $SOC_2 = SOC_{mid} < SOC_{avg}$ or $SOC_2 = SOC_{min}$.

When $SOC_2 = SOC_{mid} > SOC_{avg}$ or $SOC_2 = SOC_{max}$, (3.11) can be used for calculating T_{Eq} .

$$T_{Eq} = \frac{|SOC_{min} - SOC_{avg}| \cdot Q_B}{VI} \quad (3.11)$$

It is more complex to derive analytical solution for battery string having more than 3 cells. For battery string having more than 4 cells, simulation can be setup-up to study cell equalizing process.

Charge (C)-type BCE charges every cell of a battery string to the maximum SOC. Its simplified model is shown in Fig. 3-19.

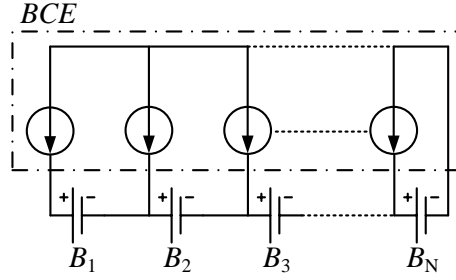


Fig. 3-19 Simplified model of a Charge (C)-type BCE.

The equalizing time for C-type BCE can be calculated by:

$$T_{Eq}(C) = \frac{(SOC_{max} - SOC_{min}) \cdot Q_B}{VI} \quad (3.12)$$

When equalizing process finished, every cell of the battery string has the same SOC of SOC_{max} . Furthermore, the equalizing process of C-type BCE is also part of charging the battery string. C-type BCE charges all battery cells to SOC_{max} and shorten the total charging time. Define T_t as total equalizing time that is the duration from initial to when all battery cells are charged to SOC_{max} . For C-type BCE:

$$T_t(C) = T_{Eq}(C). \quad (3.13)$$

While, for C/D-type BCE $T_t(C/D)$ is:

$$T_t(C/D) = T_{Eq}(C/D) + \frac{(SOC_{max} - SOC_{avg}) Q_B}{VI}. \quad (3.14)$$

Discharge (D)-type BCE discharges all battery cells to the same SOC of SOC_{min} , thus equalizing time $T_{Eq}(D)$ is equal to that of C-type BCE and can be expressed by (3.12). However, the total equalizing time is twice that of the C-type BCE. Thus, it is not suitable for fast-equalizing application.

A battery string contains 8 cells is used for evaluating the equalizing speed of C/D-type and C-type BCEs. Each cell in the string has a capacity of 2 A h. The initial SOC for the 8 cells are generated randomly and $SOC_{\max} - SOC_{\min}$ is limited to be less than 10%. The battery string is then used for evaluating $T_t (C)$ and $T_t (C/D)$. After 10000 times' simulation, the frequency chart of the total equalizing time of $T_t (C)$ and $T_t (C/D)$ are shown in Fig. 3-20. Each group of two bars shows how many times of the equalizing time fall in the range of two adjacent ticks. In each group, the first bar indicates $T_t (C)$ and the second bar is $T_t (C/D)$. It can be observed that the majority of $T_t (C)$ falls in between 250s and 350s, which means charge type BCE takes 250s to 350s to equalize the battery string. However, C/D-type BCE takes 250s to 500s.

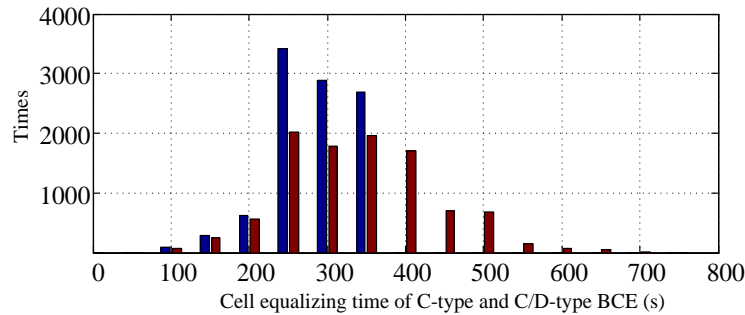


Fig. 3-20 Frequency chart of total battery cell equalizing time for both of C-type and C/D-type BCE

Fig. 3-21 shows the cumulative summation of how many times of the cell equalizing time falls in the same range in the simulation. It shows that nearly 80% of equalizing time of C-type BCE is less than 300s and all of that is less than 400s. However, nearly 20% of equalizing time of C/D-type BCE is more than 400s. Furthermore, the expectation of $T_t (C)$ is 304.2s while the expectation of $T_t (C/D)$ is 362.2s. Maximum value of $T_t (C)$ is 360s while it is 797s $T_t (C/D)$.

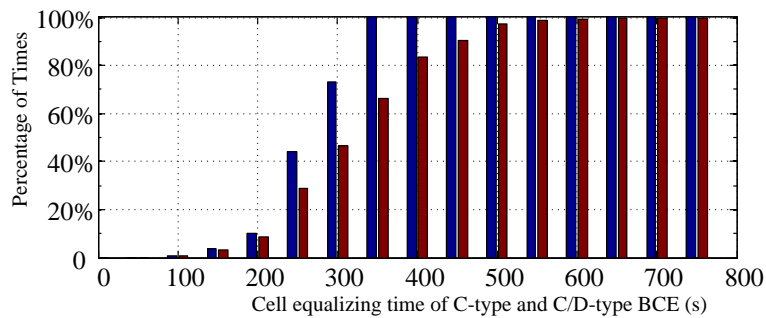


Fig. 3-21 Percentage of cumulative summation of frequency chart of total battery cell equalizing time for both of charge type and charge / discharge type BCE

It can be concluded that C-type BCE requires less time than C/D-type BCE in average and C-type BCE can be twice faster than C/D-type BCE in some cases. Thus, C-type is more superior for fast-equalizing application.

3.5 Hardware Implementation and Experiment Results

Fig. 3-22 shows a 200 W laboratory prototype of the proposed BCE. The controller is implemented by the DSP of TMSF28335 from Texas Instruments. Four battery modules, each contains 2 independent cells and totally 8 battery cells, are connected in series to the proposed BCE. Since this chapter more focuses on cell equalizing, SOC calculation is not implemented in the controller. The battery module used in this experiment has a function of measuring SOC, and the results are available for retrieving by SMBus protocol. A communication board with electrical isolation is developed to interface the controller and battery modules. Circuit parameters are shown in Table 3-4.

Table 3-4 Circuit parameters for hardware experiment

Symbol	Description	Value
L_s	Inductance of L_s	0.5 mH
$N_p : N_s$	Transformer turns ratio	5 : 1
L_{leak}	Leakage inductance at primary	10 μ H
V_{Bmax}	Maximum battery cell charging	17 V
i_{ref}	Rated battery charging current	2 A
BC	Battery capacity	6.2 A H

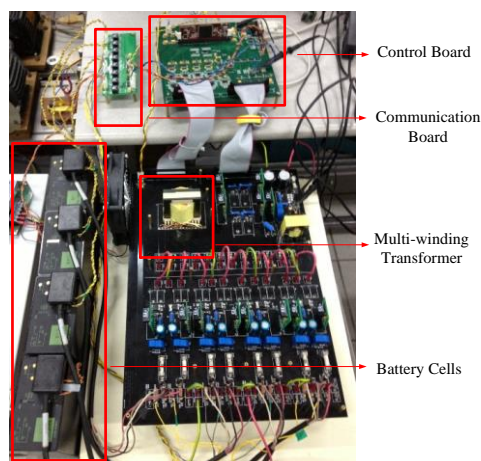


Fig. 3-22 laboratory prototype of the proposed current-fed BCE.

The battery modules has the function of calculating SOC and since the focus of this chapter is not for SOC calculation, the SOC calculated by the battery modules are used and retrieved by the microprocessor controller every 30 seconds in this experimental setup.

Fig. 3-23 shows drain-source voltage (V_{T1} , V_{T2}) of a switching leg. It can be observed that V_{T1} , V_{T2} are clamped to the DC source voltage during current commutation through the diode D_2 and no high voltage-spike is observed.

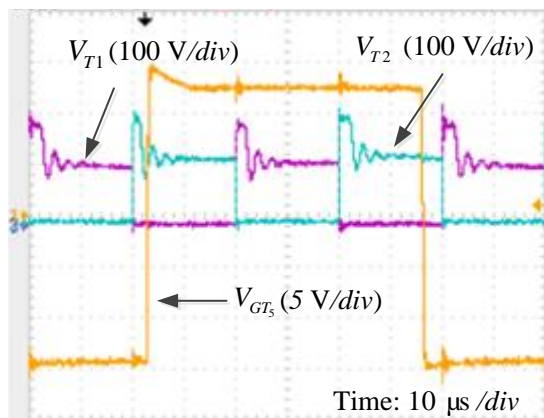


Fig. 3-23 Drain-source voltage V_{DS1} and V_{DS2} of T_1 and T_2 , and the driving signal of T_5 .

Fig. 3-24 shows charging current I_B and voltage V_B of the battery cell that has the maximum charging current. According to the data sheet provided by the battery module manufacturer, the recommended constant charging current for each battery cell is 2 A. Since each battery cell is under constant current charging, the charging current tracks the rated value and charging voltage is less than 17 V.

It is to be noticed that the battery cell that has maximum charging current varies with time and the current that requires to be controlled is automatically switched by the controller to ensure that charging current of each battery cell is under its rated value.

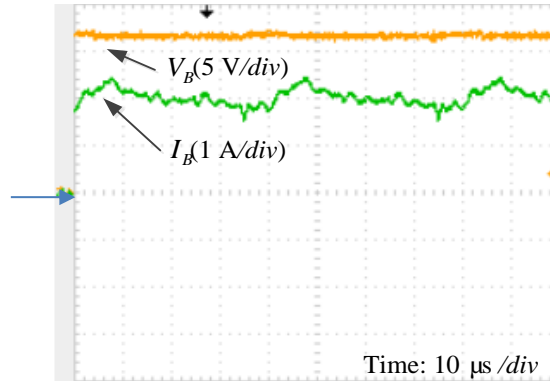


Fig. 3-24 Charging current I_B and voltage V_B of the battery cell that has the maximum charging current.

Fig. 3-25 and Fig. 3-26 show the SOC and charging current of all battery cells during the entire equalizing process respectively. Initially, the controller retrieves SOC from all battery cells and decides that B_7 and B_8 have highest SOC of 57% among all battery cells is. Thus they are not required to be charged, and T_{s7} and T_{s8} are turned off to disconnect B_7 and B_8 from the BCE. When the BCE starts to operate, B_1 and B_2 have the lowest SOC of 44%. Normally, battery cells that have lower SOC have higher charging current. Therefore, B_2 has the maximum charging current and its charging current is controlled to be the rated charging current. As shown in Fig. 3-26, charging currents of other battery cells with lower SOC are less than 2 A.

Around 13mins, SOC of B_6 and B_5 reach 57% and then B_6 and B_5 are disconnected by turning off T_{s6} and T_{s5} . Now they have the same SOC as B_7 and B_8 . Around 23 mins, when SOC₂ reaches 57%, B_2 is disconnected. Then B_1 has the maximum charging current. Around 25.5 mins, when SOC₁ is 57%, B_1 is disconnected from the BCE. After that, B_3 and B_4 are charged by the rated charging current. Around 28 mins, SOC₃ and SOC₄ are 57%, and B_3 and B_4 are then disconnected from the BCE. At this moment, all battery cells have the same SOC of 57% and the equalizing process finishes.

During the equalizing process, all the battery cells charging current are lower the rated value. Furthermore, there is always a battery cell being charged by the rated current and charging current of other battery cells are decided by the electrical parameters of the circuitry of the BCE and battery cells. Therefore, this maximum charging current promises maximum power transferred to battery cells and minimizes equalizing time.

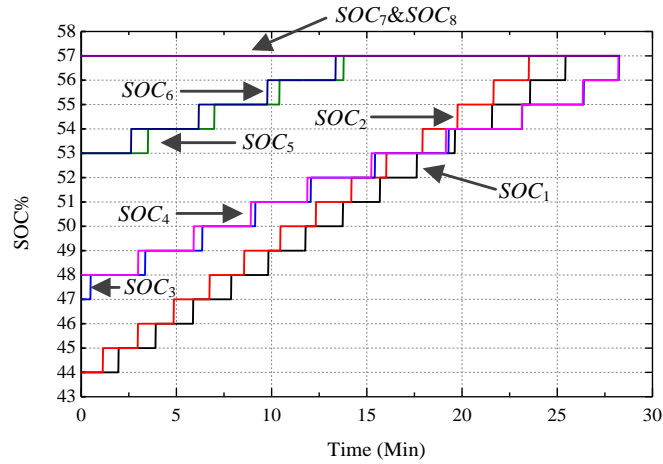


Fig. 3-25 SOC of battery cells during equalizing process

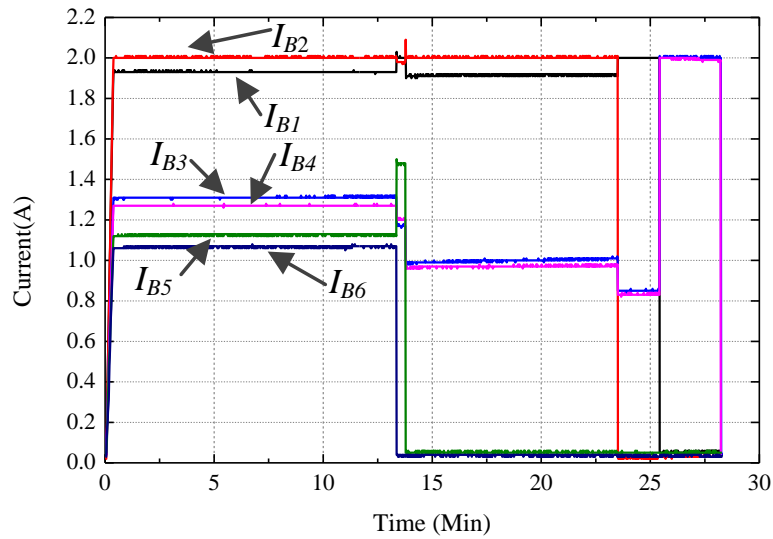


Fig. 3-26 Charging Current of I_{B1} to I_{B6} during equalizing process

3.6 Conclusion

In this chapter, a charge-type battery cell equalizer with continuous charging current based on current-fed full-bridge was proposed for fast-equalizing. Compared to conventional BCE the proposed circuitry can shorten equalizing time due to its continuous charging current and higher power rating. Furthermore the proposed BCE only requires one inductor at the primary side, and the voltage doubler at secondary side requires minimum number of transformer windings and diodes. Battery cell charging current/voltage are controlled by the duty cycle of one switch. Neither dead-time nor shoot-through state is required. Thus, the modulation method and control strategy is easy for implementation. This can reduce system cost and complexity.

Simulation is conducted in MATLAB/SIMULINK and using PLECS libraries. The results proved the correctness and effectiveness of the proposed circuit. A control algorithm based on automatically switched maximum current/voltage is proposed. It not only ensures that all battery cells are being charged safely but also improves hardware utilization and minimizes equalizing time by using a maximum possible battery cell charging current. A 200-W laboratory prototype of 8 battery cells in series was built to verify the proposed topology and control strategy. Experiment results have shown that the proposed cell equalizer has good performance.

Chapter 4 Grid Integration of Energy Storage System by Dual Active Bridge

The challenge for incorporating ESS into AC power grid is that AC power grid has a much higher voltage than the terminal voltage of a single ESD cell. As aforementioned, there are two ways to interface ESDs to AC power grid. One way is to connect ESD cells in series to achieve a sufficient DC voltage. E.g., in a typical V2G application, battery cells are connected in series to form a string and the battery string is tied to main AC power grid by a bidirectional DC/DC converter cascaded by a voltage source inverter (VSI) [125] [126]. In [127], a battery string with series-connected battery cells is connected to the AC power grid by a novel bidirectional DC/AC converter. However, due to varying chemical characteristics and aging effects of ESD cells, maintaining the many series-connected cells in balance is a major issue. In Chapter 3, auxiliary circuits known as battery cell equalizers are proposed to balance series-connected cells, however this will add to system complexity and cost.

The other way is to use power electronics converters with high voltage transfer ratio. In this case, ESD cells of ESS are connected in parallel to avoid cell balancing issue. Converters used for this application usually have a high frequency (HF) transformer to link the ESS with low terminal voltage to AC power grid. Fig. 4-1 shows the solution of bidirectional DC/DC converter cascaded by VSI, which assures bidirectional energy conversion between the AC power grid and the DC-link [85],[86].

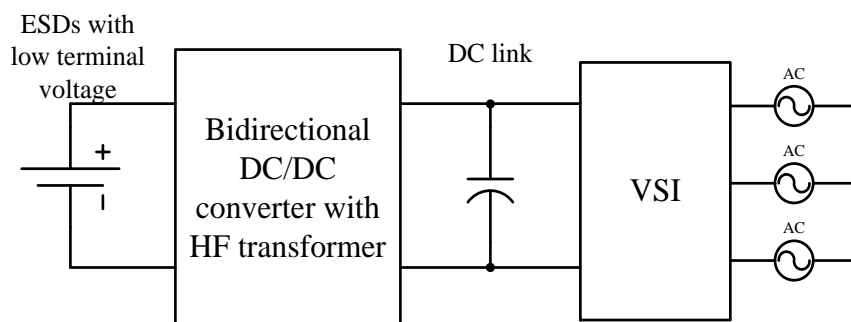


Fig. 4-1 Interfacing ESS to AC power grid by a bidirectional DC/DC converter cascaded VSI

Dual Active Bridge (DAB) converter reported in [17-22] is a popular implementation of the DC/DC converter. Other topologies can also be found, in [87] a two stage converter consisting of a bidirectional DC/DC converter and a resonant converter with galvanic

isolation is reported. This solution has a second DC-link and the voltage of the DC-link can be regulated accordingly to let the resonant converter work optimally at a fixed switching frequency. This topology has extended ZVS operation range and a comparable efficiency with DAB. However, the additional DC-link adds to system complexity and cost. High frequency AC link (HFACL) converters reported in [88-91] can be an alternative. They do not require DC capacitors. However, bidirectional switches are required for bidirectional power flow, and complex modulation scheme is adopted for current commutation. In the following of this chapter, the design of DAB+VSI for integrating ESS to AC power grid will be investigated.

Fig. 4-2 shows the schematic of DAB+VSI [85]. DAB converter consists of two voltage source bridges (VSBs). One is connected to the ESS at low voltage side (LVS) and the other one is connected to a DC bus at high voltage side (HVS). Fig. 4-3 shows the equivalent circuit of a DAB converter, VSB converts DC voltage to AC voltage and two equivalent AC sources are connected by an inductor. Thus phase shift and voltage difference of the two AC voltage sources can control the power flow. It is to be noted that L_s can be the leakage inductance of the HF transformer or a separate auxiliary inductor.

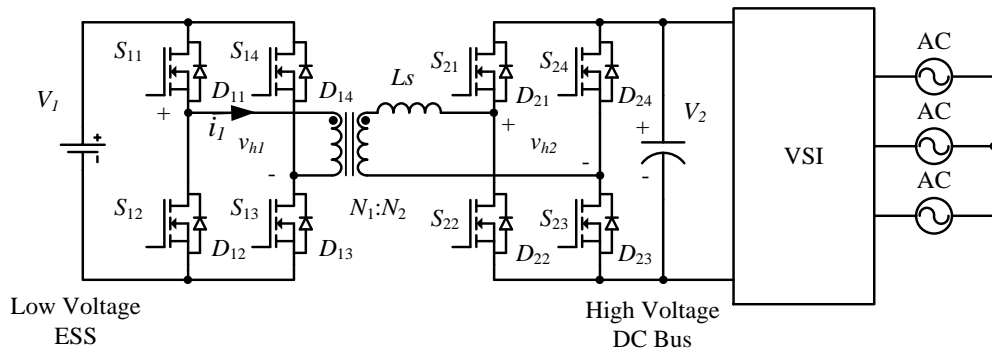


Fig. 4-2 Interfacing ESS to grid by DAB+VSI

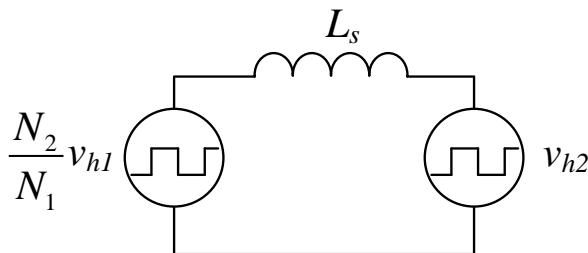


Fig. 4-3 Equivalent circuit of DAB

Traditional phase shift (TPS) control reported in [92] is used for controlling DAB. Fig. 4-4 shows driving signals of TPS control. Any diagonal switch pair of the VSBs of the DAB, e.g. S_{11} and S_{13} , have same driving signals while any switch pair of the same leg, e.g., S_{11} and S_{12} has complementary driving signals. Thus phase shift between two diagonal switch-pairs of the same VSB is π . Power flow between LVS and HVS can be controlled by the phase shift of driving signals of S_{11} and S_{21} . This phase shift can be defined by DT_{hs} , where T_{hs} is a half switching period, T_s is the switching period and f_s is the switching frequency.

Soft switching characteristics of DAB have been studied in [20] for TPS control. Power losses model is studied and discussed in [17]. Although TPS control is easy for implementing and has a simple structure, it causes high circulating current and reactive power. This adds to system loss and reduces output power rating.

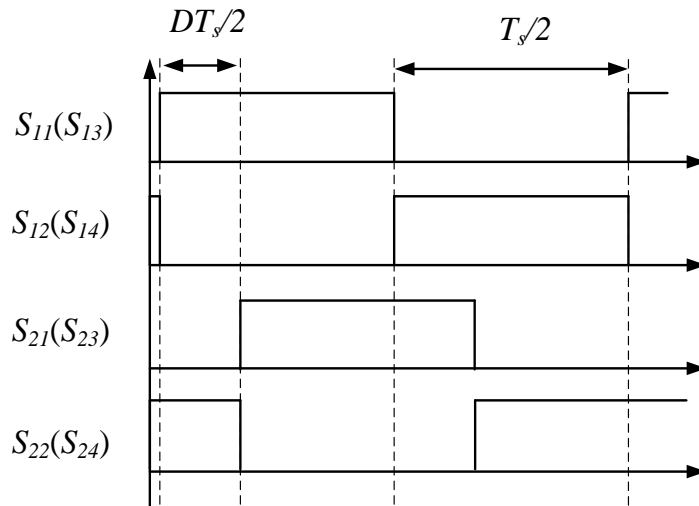


Fig. 4-4 Driving signals of TPS control for DAB

Extended Phase Shift (EPS) [21] control and Dual Phase Shift (DPS) control [19],[93-96] are proposed to reduce undesired reactive power and circulating current inherent in TPS control. Those control methods can reduce reactive power and even eliminate it in some certain circumstance. However, reactive power still exists in most cases. In [22], PWM control is introduced, however this method is complicated and results in difficulty of implementation. In this chapter, a novel control method of hybrid phase shift and PWM (HPSP) is proposed. The proposed control method can eliminate reactive power for DAB and has inherent soft switching characteristics.

4.1 Analysis of Dual Active Bridge under Traditional Phase Shift Control

For simplicity, assuming transformer magnetizing inductance is infinite and the device snubber capacitances are negligible. DAB has a symmetrical structure and the power transfer from LVS to HVS will be analyzed since the reversed power flow transfer is similar. When $N_1:N_2 = 1:n$, active power transferred from LVS to HVS can be calculated by [96],[128]:

$$P = \frac{nV_1V_2D(1-D)}{2f_sL_s} \quad (4.1)$$

When power is transferred from LVS to HVS, D is greater than zero. Thus in the following analysis, only $D>0$ is considered. Fig. 4-5 shows waveforms of voltage and current of LVS and voltage of HVS of the HF within a switching period at steady-state.

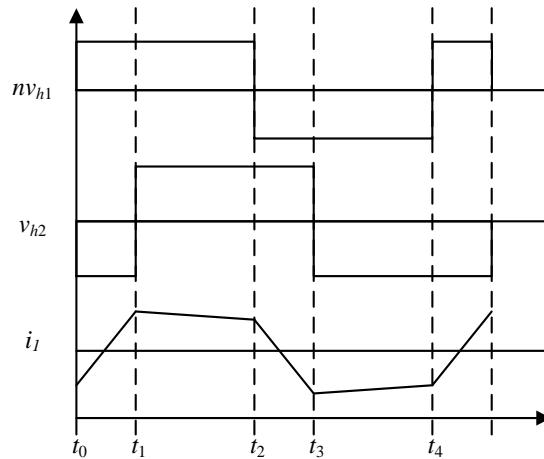


Fig. 4-5 Waveforms of HF transformer of DAB under TPS control

LVS transformer current i_l at t_0 can be calculated by:

$$i_l(t_0) = \frac{n}{4f_sL_s} \cdot [-nV_1 + (1-2D) \cdot V_2] \quad (4.2)$$

i_l at t_1 can be calculated by:

$$i_l(t_1) = \frac{n}{4f_sL_s} \cdot [V_2 - (1-2D) \cdot nV_1] \quad (4.3)$$

Based on (4.2), (4.3) and Fig. 4-5, it can be concluded that the absolute value of the maximum current of i_1 equals to $i_1(t_0)$ or $i_1(t_1)$, which depends on nV_1 and V_2 .

$$\begin{aligned} |i_1(t_0)| &\leq |i_1(t_1)|, \text{ when } nV_1 \leq V_2 \\ |i_1(t_0)| &> |i_1(t_1)|, \text{ when } nV_1 > V_2 \end{aligned} \quad (4.4)$$

In (4.1), when $D = 0.5$ and V_1 and V_2 are constant, the maximum transferrable active power from LVS to HVS can be calculated by:

$$P_{\max} = \frac{nV_1V_2}{8f_sL_s} \quad (4.5)$$

Define the unit power as P_{\max} and current as P_{\max}/V_1 . The output power and current in per-unit system can be expressed by:

$$\begin{aligned} P_{(p.u.)} &= 4D(1-D) \\ i_1(t_0)_{(p.u.)} &= 2 \cdot \left(-\frac{nV_1}{V_2} + (1-2D) \right) \\ i_1(t_1)_{(p.u.)} &= 2 \cdot \left((2D-1)\frac{nV_1}{V_2} + 1 \right) \end{aligned} \quad (4.6)$$

Fig. 4-6 shows per-unit power and LVS current versus D when $nV_1 = V_2$. It can be observed that when D is lower than 0.5, active power transferred from LVS to HVS and the maximum LVS current will increase as phase shift increases. However, when D is higher than 0.5, maximum current still increases but active power P decreases, which means that undesired circulating current increases. Thus, $D > 0.5$ must be avoided. In the following of this chapter, D is always less than 0.5 when TPS control is adopted.

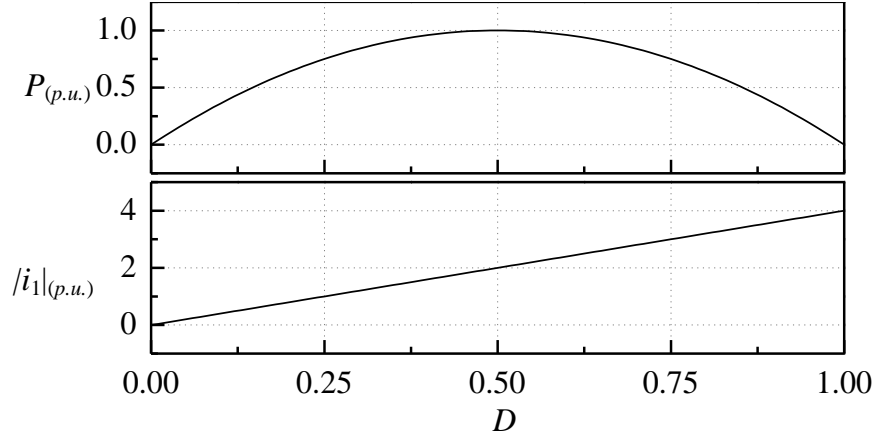


Fig. 4-6 Per-unit power and LVS current versus D

Reactive power of DAB converter can be defined as the portion of the power that is first transferred from the source side to the load side and then transferred back to the source side. This portion of power does not contribute to the total energy transferred from LVS to HVS and causes a high circulating current, which increases system loss and current stress of the switches. Fig. 4-7 shows a demonstration the reactive power over a switching period under TPS control. Fig. 4-7 (a) shows the case under heavy load while Fig. 4-7 (b) shows the case under light load. This definition of reactive power is also applicable for other control methods.

The dark shaded areas in Fig. 4-7 are defined as reactive power, and the definition is given by:

$$Q = \frac{1}{T_{hs}} \cdot nV_1 \cdot \int_{t_2}^{t_3} i_{Ls}(t) dt \quad (4.7)$$

It can be calculated by:

$$Q = \frac{nV_1 \cdot [nV_1 - (1-2D)V_2]^2}{16f_s Ls} \cdot \begin{cases} \frac{1}{nV_1 - V_2}, & i_1(t_0) > 0 \\ 0, & i_1(t_0) = 0 \\ \frac{1}{nV_1 + V_2}, & i_1(t_0) < 0 \end{cases} \quad (4.8)$$

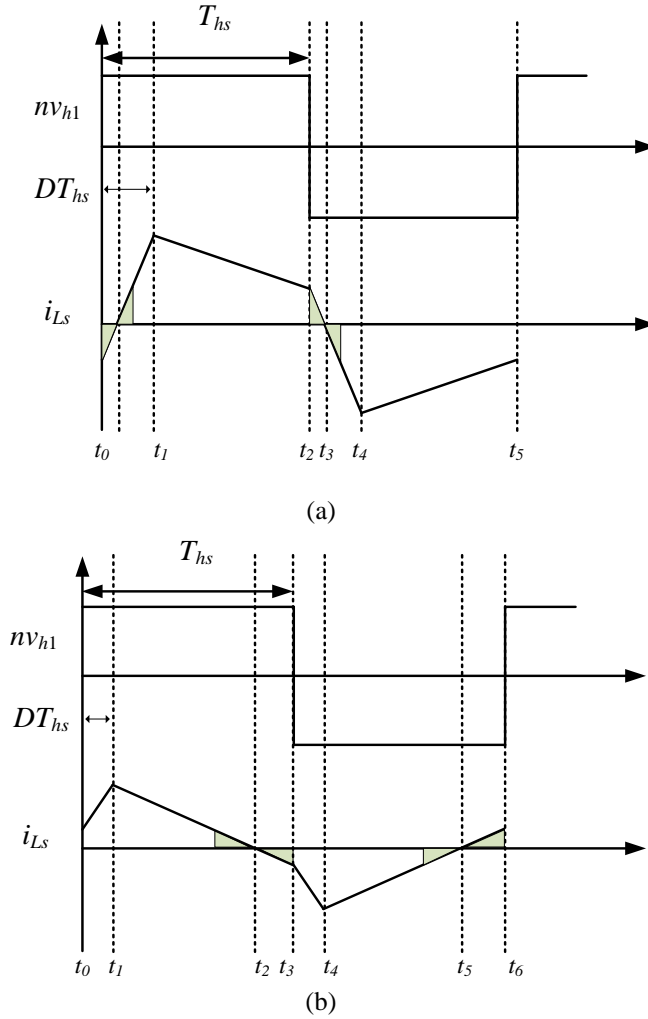


Fig. 4-7 Reactive power of DAB converter under TPS control under (a) heavy load, (b) light load.

When $i_1(t_0) < 0$, current is lagging voltage, thus Q is inductive reactive power. When $i_1(t_0) > 0$, current is leading voltage, thus Q is capacitive reactive power. Furthermore, $i_1(t_0)$ is always lower than zero, when $nV_1 > V_2$ or $nV_1 = V_2$. When $nV_1 < V_2$, $i_1(t_0)$ may be positive, negative or zero. When $i_1(t_0) = 0$, there is no reactive power and:

$$(1-2D) \cdot V_2 = nV_1 \quad (4.9)$$

When V_2 is known, normalized active power is defined by:

$$P_N = \frac{V_2^2}{8f_s L_s} \quad (4.10)$$

Then, active power and reactive power can be normalized to P_N .

$$\frac{P}{P_N} = 4k \cdot D(1-D)$$

$$\frac{Q}{P_N} = \frac{k \cdot [k - (1-2D)]^2}{2} \cdot \begin{cases} \frac{1}{k-1}, & i_1(t_0) > 0 \\ 0, & i_1(t_0) = 0 \\ \frac{1}{k+1}, & i_1(t_0) < 0 \end{cases} \quad (4.11)$$

Fig. 4-8 shows reactive power versus active power under different $k = nV_1/V_2$. It can be observed that when $k < 1$, the per-unit maximum transferrable power is less than 1 and output power capability is reduced. Furthermore, when P is low, which means DAB works under light load condition, reactive power is negative and initial current of i_1 is higher than zero. In this case, LVS switches are not in ZVS and results in additional switching loss. When $k > 0$, reactive power is inductive and LVS switches work in ZVS. When k increases, maximum output power increases meanwhile, reactive power. Higher reactive power means higher rms current when transferring the same amount of active power. Thus reactive power should be minimized when transferring the same active power.

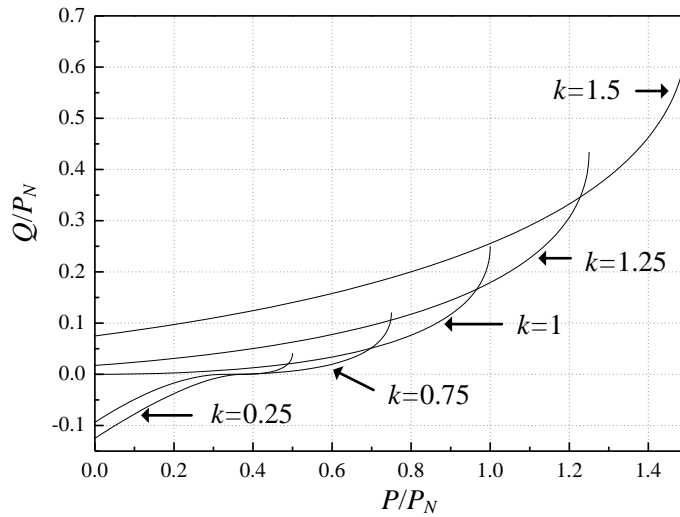


Fig. 4-8 Reactive power Q versus active power P under different voltage transfer ratio.

4.2 Dual Phase Shift Control of Dual Active Bridge

Advanced methods are proposed to reduce the reactive power and improve system output capability. Dual Phase Shift (DPS) control was first reported in [96] and the power transmission characteristics are studied in [19],[21],[129]. Diagonal switches of a bridge

do not have the same driving signals in contrast to that in TPS control. Fig. 4-9 shows the driving signals of DPS control. S_{13} is turned on before S_{11} and the lead time is $D_1T_s/2$. D_2 is the phase shift between different bridges. DPS control essentially adds another control degree of freedom. Voltage applied at HF transformer changes from 2-level in TPS control to 3-level in DPS control. DAB has three possible operation models considering relationship of D_1 , D_2 and $1-D_1$.

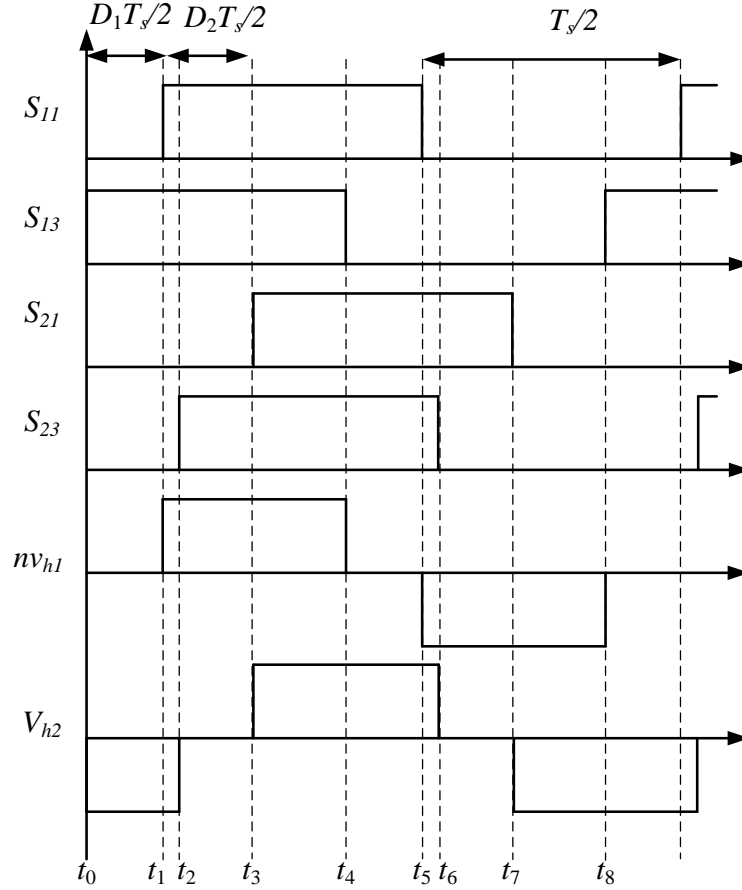


Fig. 4-9 Driving signals and transformer equivalent voltage of DPS control

Fig. 4-10 shows inductor voltage and LVS voltage reflecting to HVS. Phase shift D_1 brings another control degree of freedom, during D_1T_{hs} , nv_{h1} can be zero. When D_2 is fixed and $D_1 < D_2$, there are four possible voltage levels that can be applied to L_s . From t_0 to t_1 , $V_{L_s} = nV_1 + V_2$ since $v_{h2} = V_2$. From t_1 to t_2 , $V_{L_s} = nV_1$. At t_2 , v_{h2} reverses and after that energy is transferred from LVS to HVS. During this period, $V_{L_s} = nV_1 - V_2$. After t_3 , nv_{h1} and LVS current are zero. From t_3 to t_4 , V_{L_s} equals to $-V_2$. At t_0 , i_1 can be calculated by:

$$i_1(t_0) = -\frac{nV_2}{4f_s L_s} [k(1-D_1) + (2D_2 - D_1 - 1)] \quad (4.12)$$

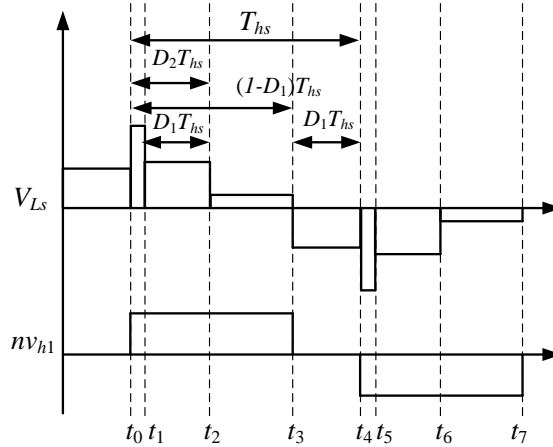


Fig. 4-10 inductor voltage of DPS when $D_1 \leq D_2 \leq (1-D_1)$ and $nV_1 > V_2$

Fig. 4-11 shows the case when $D_2 < D_1$ and $D_2 < (1-D_1)$. In this case, circuit operation is similar to that of the previous case. V_{Ls} also has four possible voltages. The difference is that the period of $V_{Ls} = nV_1 + V_2$ shown in Fig. 4-10 is replaced by $V_{Ls} = 0$ shown in Fig. 4-11. In this case, i_1 at t_0 can be calculated by:

$$i_1(t_0) = -\frac{nV_2}{4f_s Ls} \cdot [k(1-D_1) + (D_1 - 1)] \quad (4.13)$$

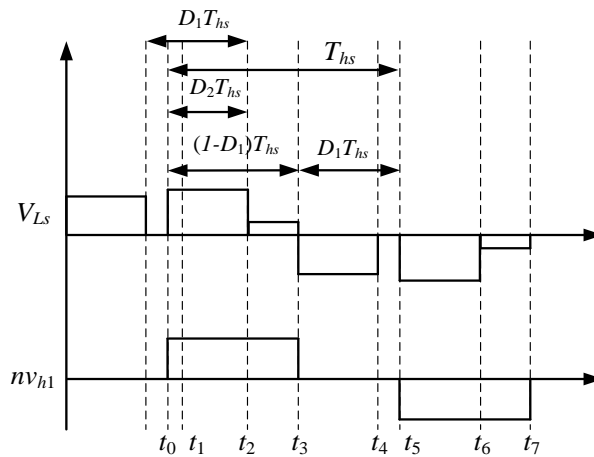


Fig. 4-11 Inductor voltage of DPS when $D_2 < D_1$ and $(1-D_1)$ and $nV_1 > V_2$

Fig. 4-12 shows the last case when $D_2 > (1-D_1)$ and $D_2 < D_1$.

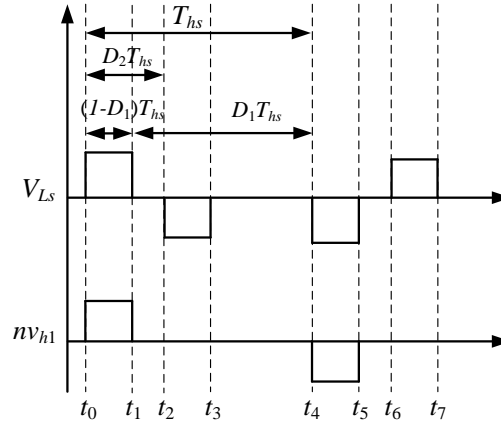


Fig. 4-12 inductor voltage of DPS when $(1-D_1) < D_2 < D_1$ and $nV_1 > V_2$

In this case V_{Ls} only has three possible voltages. Since $(1-D_1) < D_2$, $V_{Ls} = nV_1 - V_2$ shown in Fig. 4-12 is replaced by $V_{Ls} = 0$. When $nV_1 = V_2$, $i_1(t_0)$ equals to zero, which means reactive power is zero. As it is given in [21], active power can be calculated by:

$$\frac{P}{P_N} = \begin{cases} 4D_2(1-D_2) - 2D_1^2 & 0 \leq D_1 \leq D_2 \leq 1 \\ 4D_2 \left(1 - D_1 - \frac{1}{2}D_2 \right) & 0 \leq D_2 \leq D_1 \leq 1 \end{cases} \quad (4.14)$$

When consider the constraint that $0 \leq D_1 + D_2 \leq 1$, the 3D plot of P/P_N versus D_1 and D_2 is plotted in Fig. 4-13. It can be observed that D_1 provides additional control degree of freedom for active power.

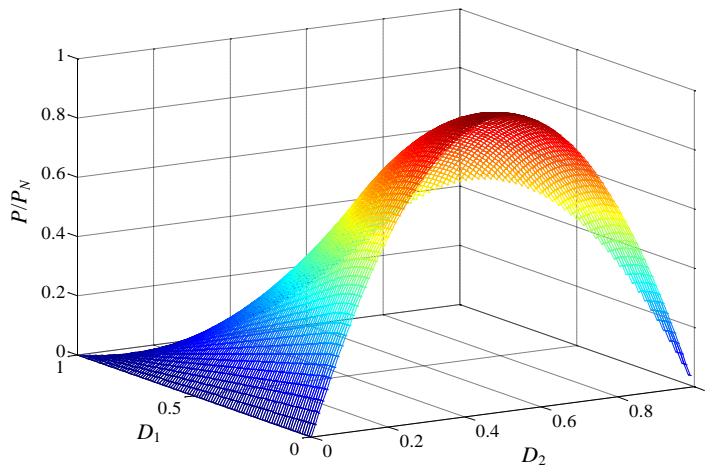


Fig. 4-13 3D plot of normalized transferrable active power versus D_1 and D_2

Fig. 4-14 and Fig. 4-15 show the 2D contour of the 3D plot for D_1 and D_2 respectively. It can be observed that introducing D_1 cannot change maximum power transfer. For any D_2 , the maximum active power can be obtained when $D_1=0$. D_1 just provides more possibilities for transferring the same active power. As mentioned above, reactive power can be reduced or even eliminated when $nV_1=V_2$. However, those literatures only discuss active power transfer characteristics and did not address how to select D_2 and D_1 for a certain active power. As a conclusion, DPS control can reduce reactive power and even eliminate it when $nV_1=V_2$ and DAB has better system performance when $nV_1=V_2$.

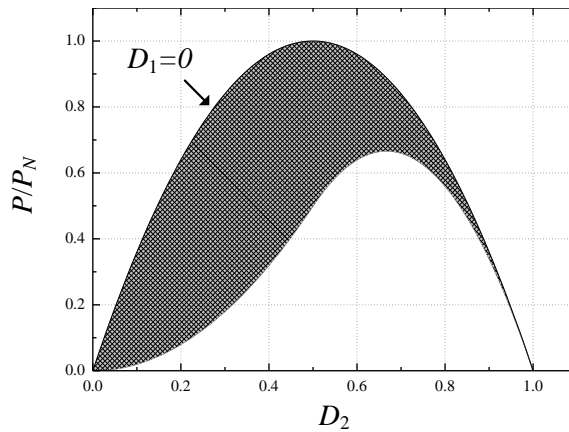


Fig. 4-14 2D contour of the 3D plot of normalized power versus D_2

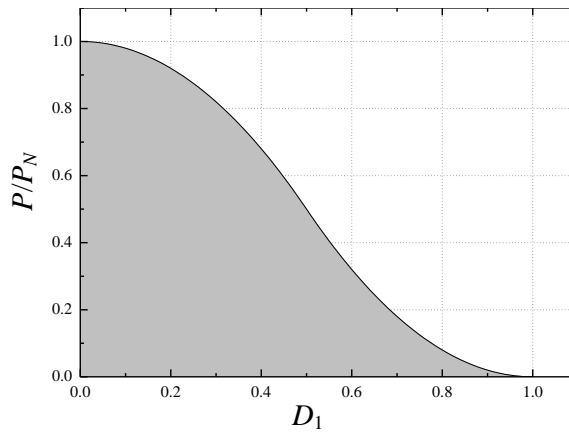


Fig. 4-15 2D contour of the 3D plot of normalized power versus D_1

4.3 Hybrid Phase Shift and PWM Control

In this section, a Hybrid method of Phase Shift and PWM (HPSP) control is proposed to eliminate reactive power for DAB. According to power flow, phase shift control is

applied at source and load side, and PWM control is applied at load side. Fig. 4-16 shows the driving signals and key waveforms for the proposed control method.

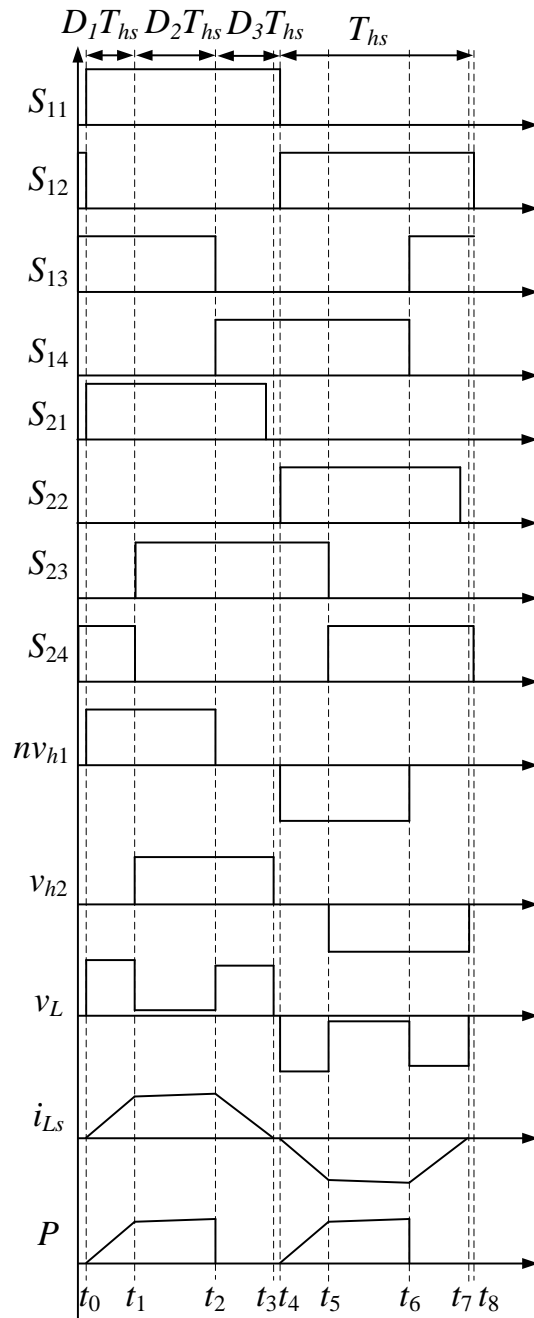


Fig. 4-16 Driving signals and key waveforms of HPSP control.

Switch driving signals of a same leg, e.g., S_{11} and S_{12} , are complementary with a duty ratio of 0.5. The driving signal of S_{14} is leading that of S_{12} by D_3T_{hs} . Contrary to TPS control, there is no phase shift of the source side diagonal switches and the load side diagonal switches. However, there is a phase shift of diagonal switches of the load side,

which is defined as $D_1 T_{hs}$. S_{23} and S_{24} have duty ratio of 0.5 while S_{21} and S_{22} have duty ratio less than 0.5. The circuit has four operating modes.

Mode 1 (t_0-t_1): as shown in Fig. 4-17, S_{11} and S_{21} are turned on at t_0 , L_s is magnetized by $N_2 V_1 / N_1$, and i_{L_s} goes through S_{11} and S_{24} . Energy is transferred from V_1 to L_s , and is stored in it. In this mode, no power is transferred to load. Since i_{L_s} is zero before the corresponding switches are turned on, switches are under ZCS. In this mode, current is established in both sides, and energy is stored in the inductor, which will be transferred to the load side later.

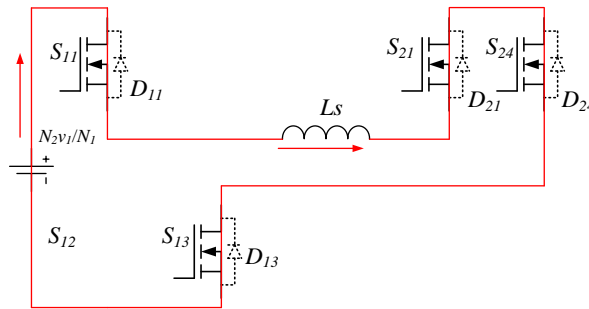


Fig. 4-17 Mode 1 of the circuit operation of DAB under HPSP control.

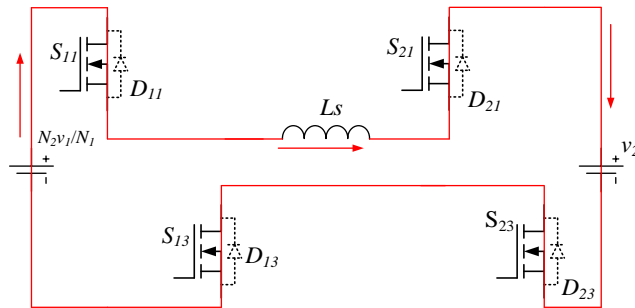


Fig. 4-18 Mode 2 of the circuit operation of DAB under the proposed HPSP control.

Mode 2 (t_1-t_2): Fig. 4-18 shows the circuit operation of mode2. S_{24} is turned off at t_1 . V_2 is connected to the source through L_s , S_{21} and S_{23} . S_{21} and S_{23} work in synchronous rectifying mode to minimize system power loss. Bulky Energy is transferred from LVS to HVS in mode. There are three possible magnetizing statuses for L_s . If $N_2 V_1 / N_1 > V_2$, L_s is magnetized, and i_{L_s} increases. When $N_2 V_1 / N_1 < V_2$, L_s is demagnetized, and i_{L_s} decreases. When $N_2 V_1 / N_1 = V_2$, i_{L_s} is unchanged.

Mode 3 (t_2-t_3): In this mode, S_{13} is turned off and S_{14} is turned on. Energy left in the inductor is transferred to the load instead of being fed back to the source. i_{L_s} is zero at t_3 ,

and S_{21} is turned off before i_{Ls} decreases to zero. When S_{21} is turned off, its body diode conducts, so it is under ZVS. A half cycle of power transferring finishes. Inductor current is reset in this mode.

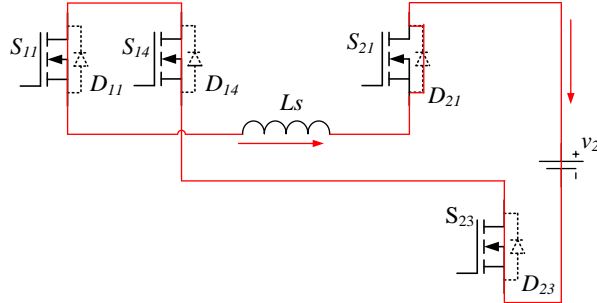


Fig. 4-19 Mode 3 of the circuit operation of DAB under the proposed HPSP control.

The circuit operation for the other half switching period is similar and the equivalent circuit is shown in Fig. 4-20 to Fig. 4-22.

Fig. 4-20 shows mode 4 and this mode is similar to mode 1. In this mode, Ls is charged by the LVS DC source through S_{14} and S_{12} . The current in Ls reverses compared to mode 1.

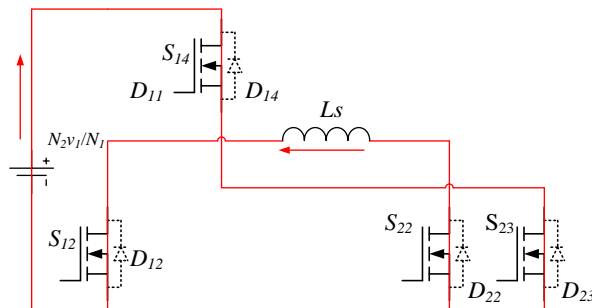


Fig. 4-20 Mode 4 of the circuit operation of DAB under the proposed HPSP control.

Fig. 4-21 shows the circuit operation of mode 5. In this mode bulky energy is transferred from LVS to HVS. This mode is similar to mode 2.

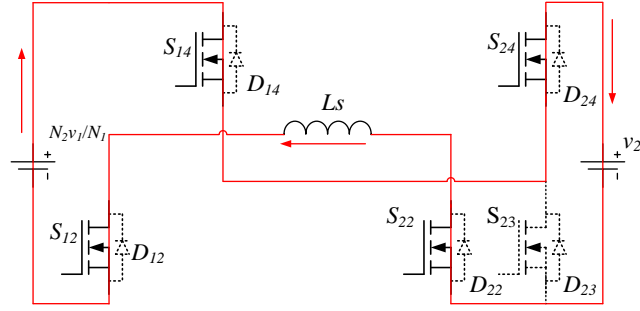


Fig. 4-21 Mode 5 of the circuit operation of DAB under the proposed HPSP control.

Circuit operation of mode 6 is shown in Fig. 4-22. This mode is similar to mode 3 and current of L_s is reset.

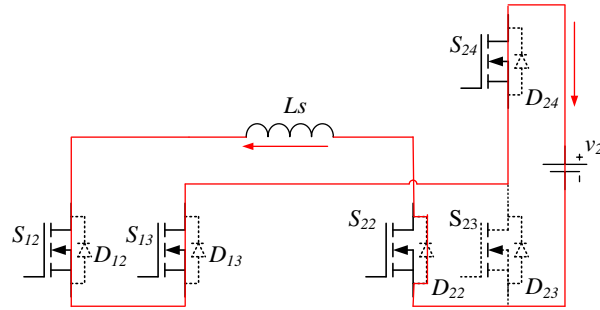


Fig. 4-22 Mode 6 of the circuit operation of DAB under the proposed HPSP control.

4.4 Analysis and Comparisons

In this section, power transfer characteristics of the proposed hybrid control method will be present and compared to TPS and DPS control.

D_1 , D_2 , and D_3 have the constraint given by(4.15). This constraint is applied to the following analysis.

$$D_2 = 1 - (D_1 + D_3). \quad (4.15)$$

The average power within one switching period can be calculated by:

$$P_1 = \frac{n^2 V_1^2}{4 f_s L} \left(D_1^2 + 2 D_1 D_2 + \left(1 - \frac{V_2}{n V_1} \right) \cdot D_2^2 \right) \quad (4.16)$$

In order to eliminate the reactive power, the following constraint will be applied:

$$\left(1 + \frac{N_1 v_1 / N_2}{v_2} \right) \cdot D_1 + \frac{N_1 v_1 / N_2}{v_2} \cdot D_2 \leq 1$$

$$(4.17)$$

By defining:

$$k = \frac{v_2}{N_2 v_1 / N_1}, \quad (4.18)$$

The maximum power transferred under (4.16) can be calculated by:

$$P_{\max} = \frac{N_2 v_1 v_2 / N_1}{4 f_s L \left(k + \frac{1}{k} + 1 \right)}. \quad (4.19)$$

Fig. 4-23 shows the normalized maximum power varies versus k . The maximum power can be calculated by:

$$P_{\max} = \frac{N_2 v_1 v_2 / N_1}{12 f_s L} \Big|_{k=1}. \quad (4.20)$$

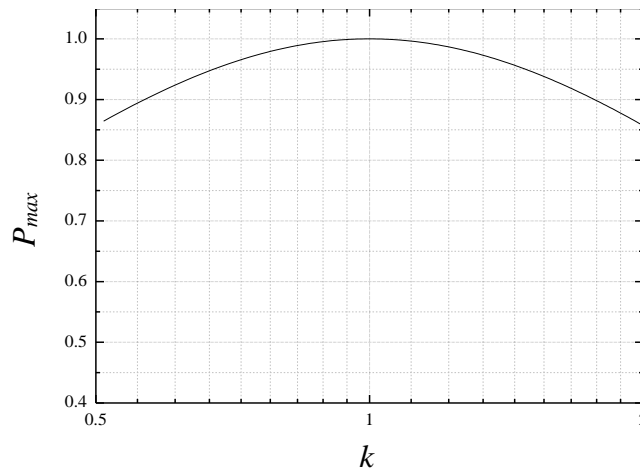


Fig. 4-23 Maximum power varies versus k of proposed HPSP control.

It can be observed that when k deviates from 1, P_{\max} decreases. In applications for buildings where ESDs are interfaced to a fixed DC bus, k can be designed close to unity by appropriately selecting transformer turns ratio $N_1:N_2$. Maximum power of TPS or its extended control method can be calculated by:

$$P'_{\max} = \frac{N_2 v_1 v_2 / N_1}{8 f_s L'}. \quad (4.21)$$

Where, L' is the inductance used in TPS and DPS control. The proposed HPSP method has lower maximum power transfer capability and lower peak current for the same inductance by comparing (4.20) and (4.21). However by choosing:

$$L = 2L'/3 \quad (4.22)$$

when $k=1$, we have $P=P'_{max}$. In this case, HPSP control has the same maximum power transfer capability and the same peak current as the TPS control. Fig. 4-24 shows i'_L and P' , which are the current and instantaneous power for TPS control. It can be observed that i'_L and i_L have the same peak value, but the rms of i_L is smaller than that of i'_L . Dark shaded area of P' is the reactive power for TPS control during maximum power transferring. However P is always positive for HPSP control, and there is no reactive power. HPSP control method both reduces the rms value of current and increases system efficiency.

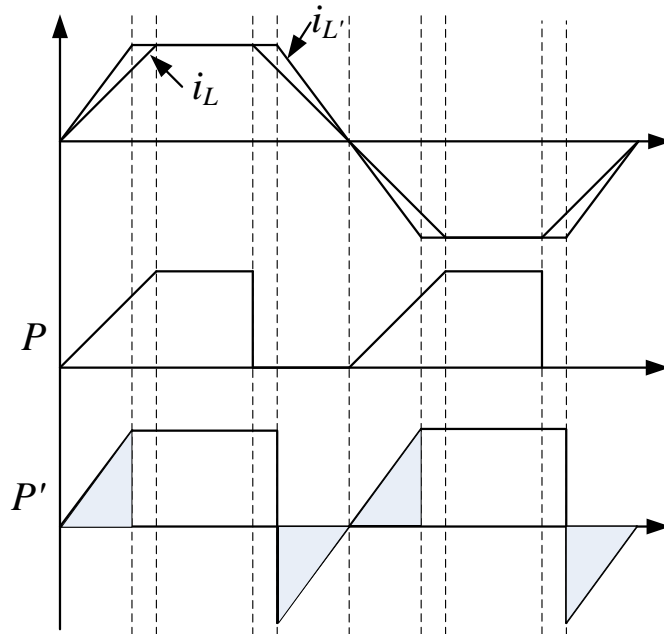


Fig. 4-24 Comparison of current and power for HPSP control and TPS.

By defining:

$$P_N = \frac{N_2 v_1 v_2 / N_1}{8 f_s L'} \quad (4.23)$$

In the case of $L=2L'/3$. The normalized power of the HPSP and TPS control are:

$$\begin{cases} p = 3(D_1^2 + 2D_1D_2) \\ p' = 4D(1-D) \end{cases} \quad (4.24)$$

Fig. 4-25 shows the 3D curve of the normalized power of HPSP and TPS control.

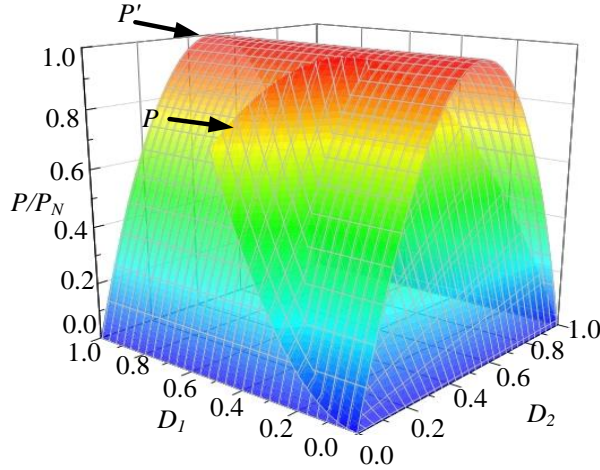


Fig. 4-25 3D curve of the normalized power of the HPSP and TPS control.

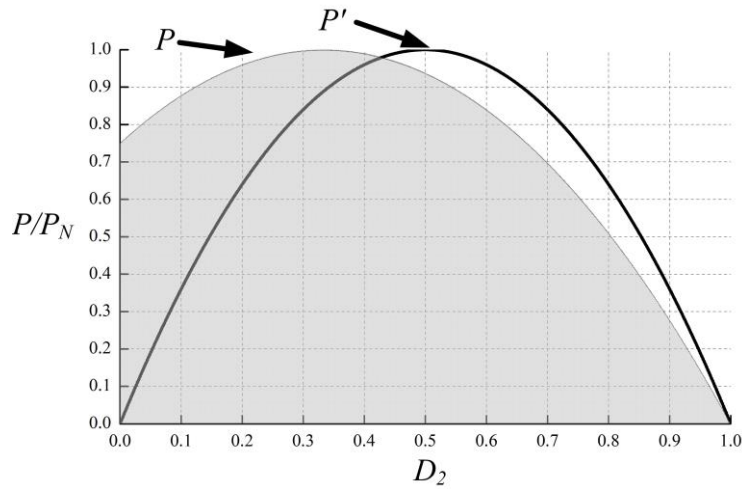


Fig. 4-26 2D curve of the normalized power of the HPSP and TPS control.

When consider the relationship of D_2 and active power, the 3D curve becomes the 2D curve shown in Fig. 4-26. It can be concluded that the proposed HPSP control method has more flexibility than conventional control method.

4.5 Simulation Results

The proposed HSPS control has been verified in MATLAB/SIMULINK. In the simulation, transformer turns ratio $N_1:N_2$ is 1:25, the leakage inductance at the secondary side of the transformer is 60.2 μH , switching frequency f_s is 100 kHz, and V_1 is 15.2 V and V_2 is 380 V. By substituting L_s , f_s , V_1 and V_2 into(4.19), the average maximum transferred power within a switching period is 2 kW. In this case the phase shift duty ratio of D_1 is 1/3 and D_2 is 1/3.

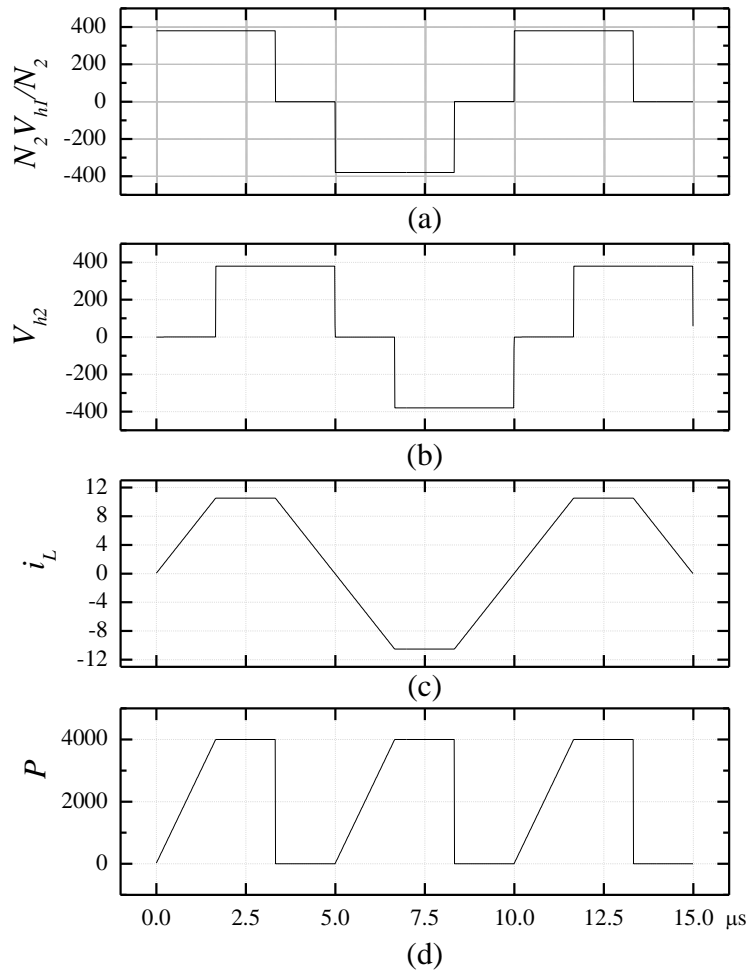


Fig. 4-27 Simulation Results for HPSP control.

As in the analysis of section 4.4, in the first $5/3 \mu\text{s}$, L_s is charged by the source and no power is transferred to the load. Therefore, i_{L_s} increases rapidly. During this stage, L_s is magnetized by the source, and energy is stored in the leakage inductor. After V_{h2} jumped to positive, which is equal to the output voltage, energy begins to be transferred to load. In the second $5/3 \mu\text{s}$, i_{L_s} remains unchanged, because N_2V_1/N_1 is equal to V_2 . In the next $5/3 \mu\text{s}$, i_{L_s} decreases, and L_s is demagnetized by V_2 . i_{L_s} drops to zero eventually. In this

stage, no power is transferred from the source to the load. Load is powered only by the energy stored in the leakage inductance. So, P shown in Fig. 4-27 (d) is zero. This simulation is for heavy load condition. For light load condition, only a small amount of energy is transferred from the source to the load. Therefore, D_1 is small, and i_{L_s} is smaller than then current shown in Fig. 4-27(c) when v_{h2} changes from zero to positive. When i_{L_s} is small enough and the magnetizing stage of L_s finishes, mode 2 shown in Fig. 4-18 and Fig. 4-20 will eventually vanish. This circuit works like a flyback converter, energy is stored in the leakage inductance and then transferred to the load. However, the TPS control requires reactive power, which is first transferred to L_s , and then fed back to the source. This causes high circulating current and extra loss.

4.6 Conclusion

In this chapter a hybrid control method of phase shift and PWM (HPSP) is proposed for DAB converter. Reactive power, which is inherent in TPS control and its extensions, can now be eliminated. By selecting appropriate transformer turns ratio and leakage inductance, HPSP has a smaller rms current with the same maximum power and current as TPS control and its extensions. HPSP also has soft switching feature for the full working range. For conditions of nV_1 is close to V_2 , the proposed HPSP control method has great advantage and is appropriate for interfacing ESS with low terminal voltage to a fixed DC bus in applications for integration of ESS in buildings.

Chapter 5 Grid Integration of Energy Storage System with Wide Terminal Voltage Range

As discussed in the previous chapter, DAB+VSI can be adopted for grid integration of ESS. When the terminal voltage of ESS varies in a small range, DAB+VSI have good system performance. However, when ESSs have wide terminal voltage, such as batteries or ultra-capacitors, it is a challenge to keep the ratio of the DC-link voltage to ESS terminal voltage as a constant. E.g., when ESS terminal voltage varies from 50% to 100% of its maximum value, the DC-link voltage V_{bus} is also required to vary from 50% to 100% of its maximum value. As the DC bus voltage of a VSI must be higher than its output AC line voltage, the maximum DC bus voltage may be twice of the output AC line voltage. For example, assuming AC power grid has a 3-phase configuration and the rated per-phase rms voltage is 220V, the minimum DC bus voltage can be calculated by:

$$V_{bus}(\min)|_{SVPWM} = 220 \cdot \sqrt{3} \cdot \sqrt{2} = 538.8V, \quad (5.1)$$

when space vector pulse width modulation (SVPWM) is adopted. For sinusoidal pulse width modulation (SPWM), DC bus voltage is even higher and can be calculated by:

$$V_{bus}(\min)|_{SPWM} = 2 \cdot 220 \cdot \sqrt{2} = 622.1V \quad (5.2)$$

In the following, SVPWM is considered for maximum DC bus voltage utilization. If the terminal voltage the ESS varies from 50% to 100%, the maximum DC bus voltage can be 1078 V, which results in a great challenge for design. Thus, it is not practical to regulate DC bus voltage in a wide range. Some ESS cells, such as lead-acid batteries and ultra-capacitors have varying terminal voltages and hence DAB+VSI is not optimal for them. Furthermore, DAB+VSI require bulky DC capacitors to smooth DC bus voltage due to high current ripple. In this chapter, a novel bidirectional DC/AC converter is proposed for grid integration of ESS with wide terminal voltage. It adopts a current-fed topology and does not use DC-link capacitors. Simulation and hardware experiments verified the proposed circuit to have good system performance.

5.1 Proposed Topology and Control Strategy

Fig. 5-1 shows the proposed DC/AC converter, which consists of a high frequency DC link (HFDCL) and a current source converter (CSC). The HFDCL consists of a voltage

source bridge (VSB), which connects a HF transformer and ESS, and a current source bridge (CSB), which connects the HF transformer and a DC-link inductor. DC-link capacitors are eliminated in the proposed topology. The HFDCL converts a low DC voltage to a high DC voltage and feeds the DC-link inductor. A cascaded CSC is connected to the three-phase AC grid.

In the following analysis, it is assumed that an ideal and symmetrical three-phase AC voltage is applied at the input of the CSC. By properly controlling the DC-link current, the grid-side AC current can be controlled in an open loop fashion, and no current sensor for grid-side is required [130]. The proposed DC/AC converter has two operation modes regarding the direction of power flow [131]. In discharging mode, energy in the ESS is released to the AC power grid. In charging mode, the ESS is charged by the AC power grid. The equivalent circuit of the HFDCL of proposed converter can be simplified as two voltage sources connecting a DC-link inductor, and is shown in Fig. 5-2.

For the purpose of maximum DC voltage utilization, each diagonal switch pair of the VSB in discharging mode or the CSB in charging mode has the same driving signal with the duty cycle of 0.5. The phase shift of the two switch pairs of the same bridge is π . By neglecting the dead-beat of the VSB in discharging mode and shoot-through of the CSB in charging mode, v_{link1} is proportional to v_{dc} . The only difference is that v_{link1} is positive in discharging mode while it is negative in charging mode. So, in a single operation mode, v_{link1} can be treated as a DC voltage source and can be calculated by:

$$v_{link1} = \begin{cases} (N_2 / N_1) \cdot v_{dc} & | \text{ In discharging mode} \\ -(N_2 / N_1) \cdot v_{dc} & | \text{ In charging mode} \end{cases} \quad (5.3)$$

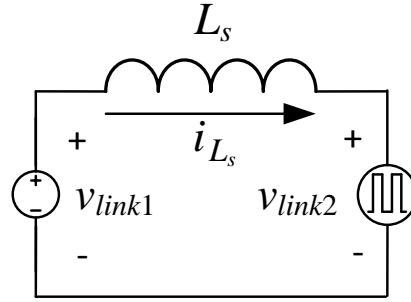


Fig. 5-2 Simplified equivalent circuit of the HFDC link of the proposed DC/AC converter

Space vector modulation (SVM) can be applied to the CSC [132],[133]. Fig. 5-3 and Fig. 5-4 show the equivalent circuit of the proposed converter in discharging mode when a null and an active space vectors are selected respectively. When a null space vector is selected, the secondary side of the HF is short circuited through T_{31} , D_{31} , T_{34} and D_{34} , thus $v_{link2} = 0$. Therefore, L_s is charged by v_{link1} . When an active space vector is selected, v_{link2} equals to the corresponding AC power grid line voltage and L_s is discharged by the AC power grid. When L_s works in continuous conduction mode (CCM), the change of the average DC-link current within a switching period can be calculated by:

$$\Delta i_{L_s} = \frac{T_s}{L_s} \cdot (v_{link1} - v_{link2}) = \frac{T_s}{L_s} \left(\frac{N_2}{N_1} \cdot v_{dc} - \frac{3}{\sqrt{2}} v_{ac} \cdot m \right) \quad (5.4)$$

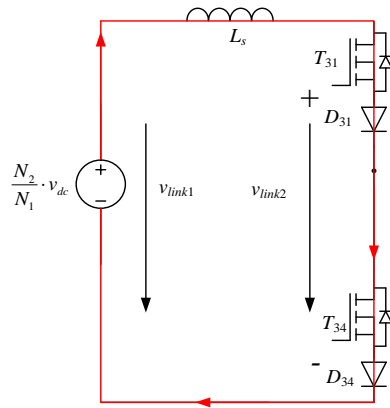


Fig. 5-3 Equivalent circuit of the proposed DC/AC converter in discharging mode when a null space vector is selected.

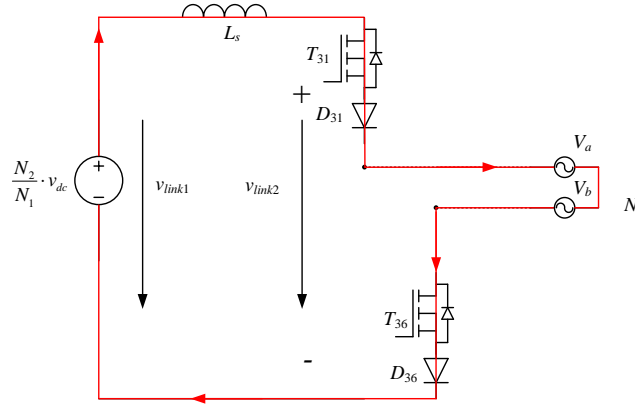


Fig. 5-4 Equivalent circuit of the proposed DC/AC converter in discharging mode when an active space vector is selected.

where m is the modulation index and is defined as the ratio of the amplitude of the reference current space vector and the mean DC-link current, v_{ac} is the per-phase rms-voltage of the AC power grid voltage.

Fig. 5-5 and Fig. 5-6 show the equivalent circuit of the proposed converter in charging mode when a null and an active space vectors are selected respectively. Contrary to the previous operation mode, L_s is discharged by v_{link1} when a null space vector is selected, while L_s is charged by the AC power line voltage when an active space vector is selected. Compared to discharging mode, the polarity of v_{link1} and v_{link2} is reversed while the current direction of the DC-link inductor remains unchanged. (5.4) is still valid in charging mode. Thus, voltage transfer ratio for both of charging and discharging mode can be calculated by (5.5) in steady state when Δi_{L_s} is zero.

$$\frac{v_{ac}}{v_{dc}} = \frac{N_2}{N_1} \cdot \frac{\sqrt{2}}{3} \cdot \frac{1}{m} \quad (5.5)$$

Furthermore, the average DC-link current i_{L_s} is a constant and proportional to the current of ESS i_{dc} . So i_{L_s} can be controlled by regulating the modulation index m and discharging or charging mode can be selected based on the sign of the reference of i_{dc} . Since m in (5.5) is less than 1, it is required that:

$$v_{ac} \geq \frac{N_2}{N_1} \cdot \frac{\sqrt{2}}{3} \cdot v_{dc} \quad (5.6)$$

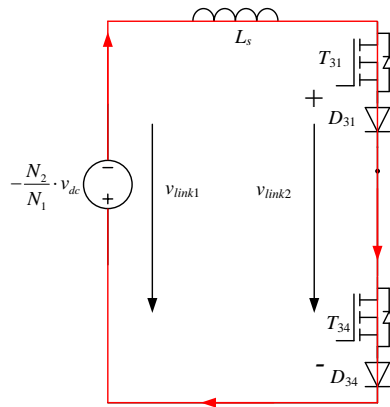
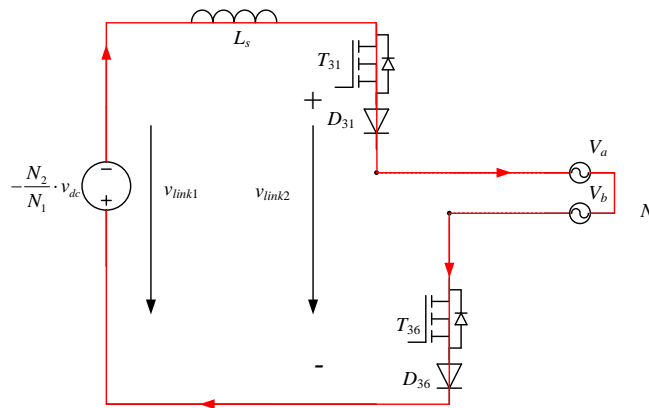


Fig. 5-5 Equivalent circuit of the proposed DC/AC converter in charging mode when a null space vector is selected.



(b)

Fig. 5-6 Equivalent circuit of the proposed DC/AC converter in charging mode when an active space vector is selected.

Therefore, the proposed topology can work even when the terminal voltage of ESS drops dramatically. Compared to the design of DAB+VSI, the proposed DC/AC converter is compatible with ESS having wide terminal voltage. In the next section, the design consideration of the proposed converter will be introduced and comparison to DAB+VSI will be present. Modulation in discharging and charging mode will be introduced in Sections 5.3 and 5.4 respectively.

5.2 Design Considerations and Comparisons

Assuming the terminal voltage range of the ESS is between V_{BMin} to V_{BMax} . Define $V_{BMin} = k V_{BMax}$. v_{ac} is the normal per-phase rms AC voltage and it varies in $(1 \pm x\%) v_{ac}$. For the design of DAB+VSI, minimum DC bus voltage can be calculated by:

$$V_{BusMin} = \sqrt{6}V_{ac} \cdot (1 + x\%) \quad (5.7)$$

Turns ratio of the transformer can be calculated by:

$$N_1 : N_2 = V_{BMin} : \sqrt{6}V_{ac} \quad (5.8)$$

When ESS has maximum DC voltage, V_{bus} can be calculated by:

$$V_{busMax} = V_{BMax} \cdot (N_2 : N_1) \quad (5.9)$$

Substitute (5.8) into (5.9) and replace V_{BMax} with $(1/k)V_{BMin}$, (5.9) can be expressed by:

$$V_{busMax} = \sqrt{6}V_{ac} (1 + x\%) / k \quad (5.10)$$

When $k=0.5$, the maximum DC bus voltage is twice that of the minimum DC bus voltage and this results in a great challenge for system design. DC bus capacitors and switches of DAB and VSI must be selected to be compatible with the maximum DC bus voltage.

For the proposed converter, there is no physical DC bus. The maximum value of v_{link1} can be calculated by:

$$v_{link1Max} = (3 / \sqrt{2}) \cdot V_{ac} \cdot (1 - x\%) \quad (5.11)$$

Voltage stress of the switches of the CSC is decided by the input AC voltage and the voltage stress of the CSB of the HFDCL is decided by v_{link1} . (5.12) can be obtained from (5.10) and (5.11):

$$\zeta = \frac{V_{link1Max}}{V_{busMax}} = \frac{\sqrt{3}}{2} \cdot \frac{1 - x\%}{1 + x\%} \cdot k \quad (5.12)$$

When $x=30$ which means AC voltage works in the range of $(1 \pm 30\%)$ and $k = 0.5$, $\zeta = 0.23315$. Thus, voltage stress of the proposed converter is much smaller than that of DAB+VSI.

5.3 Modulation of Current Source Converter

SVM is widely used for controlling CSC [8-10],[134],[135]. Six active space vectors as well as three null space vectors are defined and shown in Fig. 5-7. In modulation of indirect matrix converters, current source inverter (CSI) must coordinate with voltage source rectifier (VSR) to avoid volt-second error [73],[136-139]. The same idea should be applied to the proposed converter since volt-second balance is essential for HF transformer to avoid flux saturation. Unlike avoiding usage of null space vectors in the control of indirect matrix converters, they must be utilized to assist current commutation of the HFDCL for the proposed converter. In classical SVM, two adjacent active space vectors and one null space vector synthesis the reference. Various space vector sequences are discussed in [140]. In order to keep volt-second balance, space vector sequence of $I_n \rightarrow I_{n+1} \rightarrow I_0$ can be considered as a candidate, where I_0 is one of the three null space vectors, i.e. I_7, I_8 or I_9 shown in Fig. 5-7.

Active space vector selection for the proposed converter has a limitation. v_{link2} must be positive in discharging mode while it must be negative in charging mode. The sextants definition of three-phase AC voltage within a fundamental cycle is shown in Fig. 5-8 in (a) three-phase and (b) space-vector respectively.

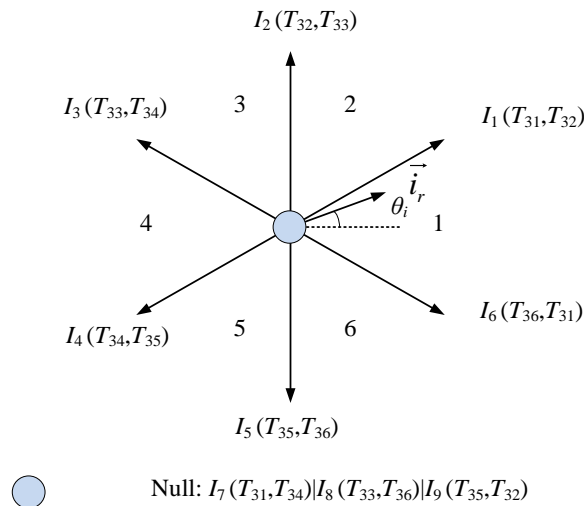


Fig. 5-7 Space vector representations of CSC.

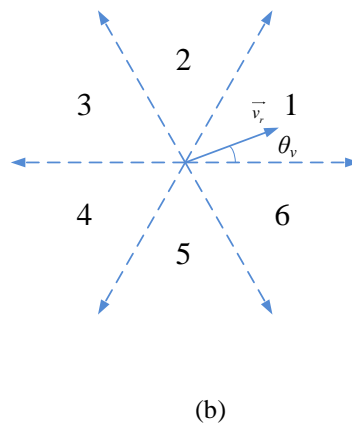
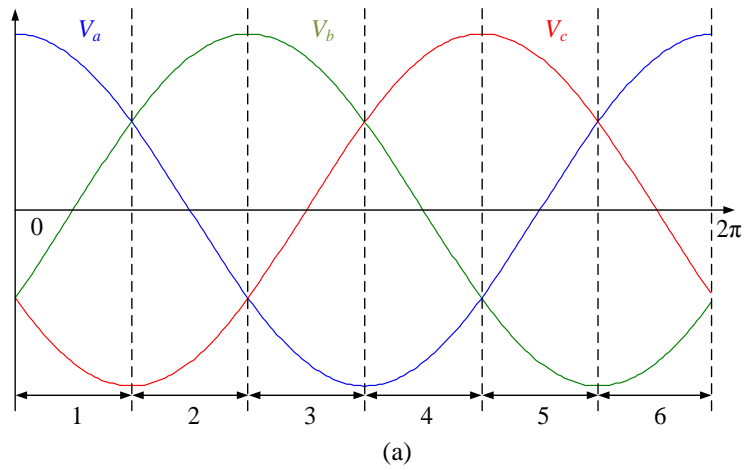


Fig. 5-8 Sextants definition of three-phase AC voltage within a fundamental cycle (a) three-phase (b) space vector.

For discharging mode, when the AC voltage is in sextant 1 shown as Fig. 5-8 (b), v_A is the highest, and v_B is higher than v_C . Therefore, only $v_A - v_B$, $v_A - v_C$, or $v_B - v_C$ can synthesize positive v_{link2} , and the corresponding active space vectors are I_6 , I_1 , and I_2 . So the reference current must lie in sextant 1 or 2 shown as Fig. 5-7. For charging mode, space vector in sextant 4 or 5 is the only possible selection since v_{link2} must be negative. Possible active space vectors for AC voltage lying in sextant 1 are shown in Fig. 5-9 (a) and (b) for discharging and charging mode respectively. Space vectors in bold are possible selections and the shadowed area indicates the AC voltage space vector.

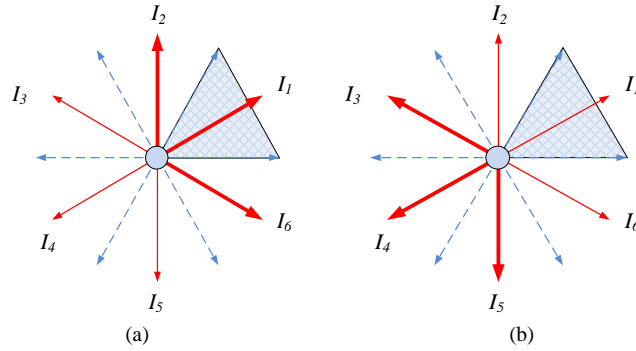


Fig. 5-9 Possible current active space vectors when the AC grid voltage is in sextant 1 (a) charging mode, (b) discharging mode.

Possible selections of active space vectors of AC voltage in different sextants are shown in Table 5-1. It also shows how the AC line voltages form v_{link2} for both charging and discharging mode.

Table 5-1 Possible selections of active space vector for the Ac grid voltage within a fundamental cycle.

Voltage sextant	discharging mode		charging mode	
	possible space vector	v_{link2}	possible space vector	v_{link2}
1	I_6	$v_A - v_B$	I_3	$-(v_A - v_B)$
	I_1	$v_A - v_C$	I_4	$-(v_A - v_C)$
	I_2	$v_B - v_C$	I_5	$-(v_B - v_C)$
2	I_1	$v_A - v_C$	I_4	$-(v_A - v_C)$
	I_2	$v_B - v_C$	I_5	$-(v_B - v_C)$
	I_3	$v_B - v_A$	I_6	$-(v_B - v_A)$
3	I_2	$v_B - v_C$	I_5	$-(v_B - v_C)$
	I_3	$v_B - v_A$	I_6	$-(v_B - v_A)$
	I_4	$v_C - v_A$	I_1	$-(v_C - v_A)$
4	I_3	$v_B - v_A$	I_6	$-(v_B - v_A)$
	I_4	$v_C - v_A$	I_1	$-(v_C - v_A)$
	I_5	$v_C - v_B$	I_2	$-(v_C - v_B)$
5	I_4	$v_C - v_A$	I_1	$-(v_C - v_A)$
	I_5	$v_C - v_B$	I_2	$-(v_C - v_B)$
	I_6	$v_A - v_B$	I_3	$-(v_A - v_B)$
6	I_5	$v_C - v_B$	I_2	$-(v_C - v_B)$
	I_6	$v_A - v_B$	I_3	$-(v_A - v_B)$
	I_1	$v_A - v_C$	I_4	$-(v_A - v_C)$

5.4 Current Commutation of the High Frequency DC Link

In this section, current commutation and modulation of HFDCL is introduced in detail for both of charging and discharging mode.

5.4.1 Current Commutation in Discharging Mode

Driving signals and waveforms for discharging mode within a switching period of the HFDCL are exhibited in Fig. 5-10.

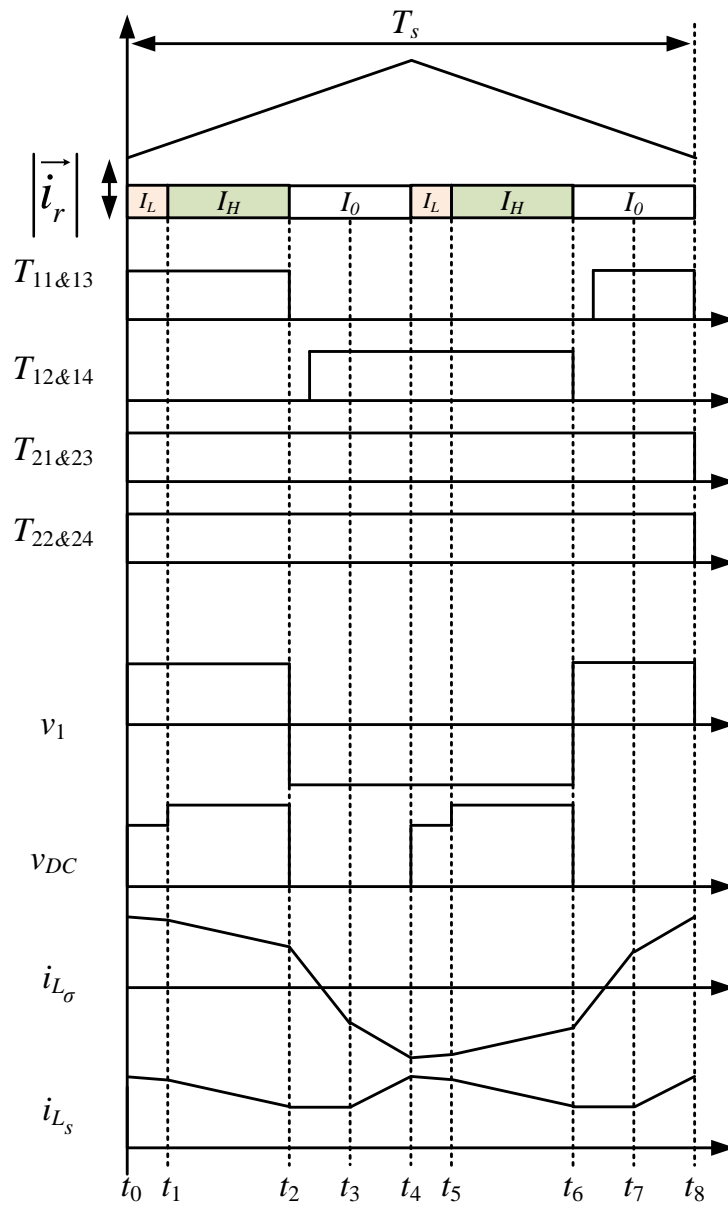


Fig. 5-10 Driving signals and waveforms of the proposed DC/AC converter in discharging mode.

Switching frequency of the CSC is twice that of the HFDCL. For minimizing switching loss, current commutation will perform when L_s has minimum current and a null space vector of the CSC is selected. Based on these two rules, driving signals of the VSB must coordinate with SVM of the CSC. As shown in Fig. 5-10, the diagonal switch pair of T_{11} and T_{13} is turned off at t_2 , when an active space vector transits to a null space vector. After dead-beat, the other diagonal switch pair of T_{12} and T_{14} is turned on. Switches of the CSB are always on to rectify a square AC voltage to synthesis v_{link1} . The duration of the current commutation, i.e. t_2-t_3 or t_6-t_7 shown in Fig. 5-10, does not contribute to magnetize L_s . Time elapsed is mainly decided by the average DC-link current and can be calculated by:

$$\frac{1}{2}T_{CD} = \frac{1}{2}T_s D_{CD} = 2L_s \bar{i}_{L_s} / \left(\frac{N_2}{N_1} v_{dc} \right) \quad (5.13)$$

Assuming the DC-link inductor is large enough, and the current ripple can be neglected. In (5.13), T_{CD} is the total time elapsed in commutation over a switching period (T_s), and D_{CD} is defined as the ratio of T_{CD} and T_s . Therefore m in (5.4) must be in $(0, D_{CD})$ for performing correct current commutation.

5.4.2 Modified Space Vector Sequence for Current Source Converter

To minimize DC-link current and time elapsed in current commutation, space vector sequence of the CSC modulation must be modified. $I_n \rightarrow I_{n+1} \rightarrow I_0$ cannot guarantee a minimal DC-link current during current commutation. The space vector that can form v_{link2} with the highest voltage is shaded for each AC voltage sextant in Table 5-1 among three possible space vectors. The DC-link inductor is demagnetized when it is selected in discharging mode. However, if the other two space vectors are selected, v_{link2} may be lower than v_{link1} . For example, when AC voltage lies in sextant 1, possible active space vectors are I_6 , I_1 and I_2 . When I_1 is selected, v_{link2} equals to v_A-v_C and is always higher than v_{link1} . However, when I_6 or I_2 is selected, v_{link2} equals to v_A-v_B or v_B-v_C , and may be lower than v_{link1} . Fig. 5-11 shows the normalized voltage of v_{link1} , v_A-v_B , and v_B-v_C . Assuming $m = 0.7$ and $\theta_v \in (0, \pi/3)$, when I_2 is selected and v_B-v_C is in the shaded area shown in Fig. 5-11, v_{link1} is higher than v_{link2} , and DC-link inductor is magnetized. Therefore, the DC-link current is not minimal during current commutation.

The sequence of the space vectors of the CSC should be modified from $I_n \rightarrow I_{n+1} \rightarrow I_0$ to $I_L \rightarrow I_H \rightarrow I_0$, where I_H means the space vector that forms a higher voltage at v_{link2} , and I_L

means a space vector that forms a lower voltage at V_{link2} . The selection of I_H can be based on Table 5-1, where shade area marks I_H for each AC voltage sextant. E.g., the sequence should be $I_2 \rightarrow I_1 \rightarrow I_0$ instead of $I_1 \rightarrow I_2 \rightarrow I_0$, which is used in classical SVM. When I_H is selected, DC-link inductor is demagnetized in discharging mode. Minimum DC-link current is at when I_H ends. This MSVS can also guarantee D_{CD} in (5.13) is adequate for current commutation since average DC-link current is higher than its minimum.

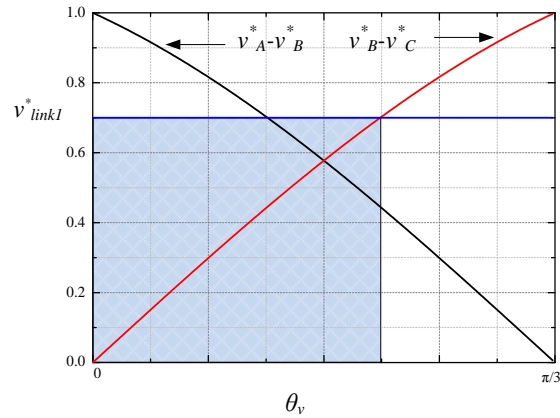


Fig. 5-11 Normalized voltage of v_{link1}^* , $v_{A-v_B}^*$, and $v_{B-v_C}^*$ assuming $m=0.7$ and $0 < \theta_v < \pi/3$.

5.4.3 Current Commutation in Charging Mode

Current commutation in charging mode is similar to that in discharging mode. Fig. 5-12 shows the driving signals and waveforms in charging mode.

VSB works in synchronous rectifying mode to reduce conduction loss. MSVS is also applied in charging mode. The proposed circuit works like a buck converter in charging mode and both of v_{link1} and v_{link2} are negative. I_H and I_L can be selected based on Table 5-1. When I_H is selected, $-v_{link1} < -v_{link2}$, and DC-link inductor is magnetized. However, when I_L is selected, the charging status of the DC-link inductor is uncertain and depends on the relationship of θ_v and θ_i . Therefore, the current commutation should be performed during I_0 and before I_H .

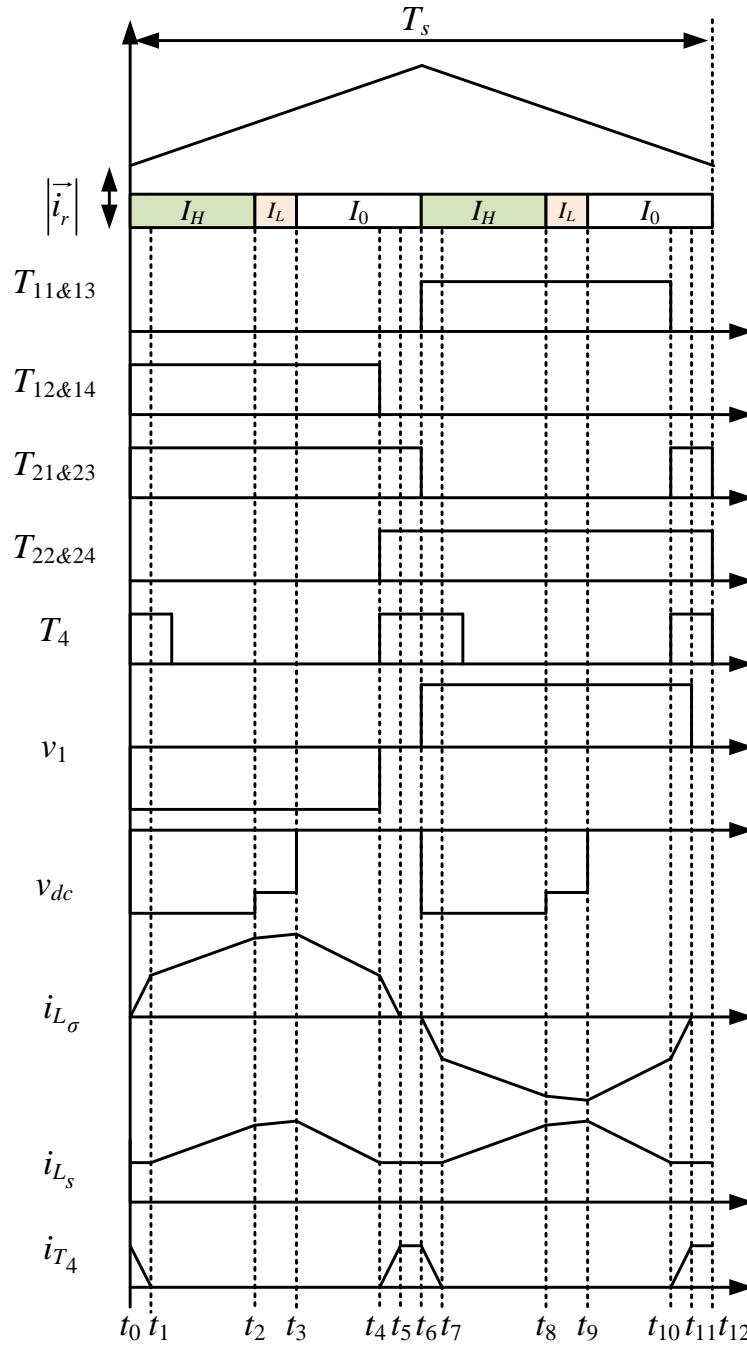


Fig. 5-12 Gate signals and waveforms of the proposed current-fed DC/AC converter in charging mode.

At t_4 , the diagonal switch pair of T_{22} and T_{24} and the auxiliary switch T_4 are turned on, and T_{21} and T_{23} are still on. L_σ is discharged by N_2 , and i_{T_4} increases. After t_5 , $i_{L_\sigma} = 0$. The time elapsed (t_4-t_5 or $t_{10}-t_{11}$) during a null space vector can be defined as T_{CC} and the ratio of T_{CC} over T_s can be defined as D_{CC} . T_{CC} and D_{CC} can be expressed by:

$$\frac{1}{2}T_{CC} = \frac{1}{2}T_s D_{CC} = L_\sigma \overline{i_{L_\sigma}} / \left(\frac{N_2}{N_1} v_{dc} \right) \quad (5.14)$$

Therefore, the maximum value of m in (5.4) must be smaller than D_{CC} to avoid error when performing current commutation. At t_6 , T_{21}, T_{23} and T_4 are turned on, and I_H is selected. L_σ is charged until t_7 when $i_{L_\sigma} = i_{L_s}$, and current commutation finishes. Time elapsed of t_6-t_7 or t_0-t_1 does not contribute to magnetize the DC-link inductor, and can be expressed by:

$$\frac{1}{2}T_{CCL} = \frac{1}{2}T_s D_{CCL} = L_\sigma \overline{I_{L_s}} / \left(v_{lmax} - \frac{N_2}{N_1} v_{dc} \right) \quad (5.15)$$

where T_{CCL} is the time elapsed, D_{CCL} is the ratio of T_{CCL} over T_s , and v_{lmax} is the line voltage that is applied at v_{link2} when I_H is selected.

5.5 Simulation Results

The proposed DC/AC converter and the MSVS modulation method were verified by Matlab/Simulink and PLECS power electronics libraries. The AC grid has a configuration of three-phase 50 Hz/220 V (per-phase rms-voltage), and a DC source is used for simulating ESS. $N_1:N_2 = 1:17$. $f_s = 10$ kHz, $L_s = 4$ mH, and $L_\sigma = 30$ μ H.

5.5.1 Discharging Mode

Fig. 5-13 (a) shows v_{link2} , which is the AC line voltage when active space vector is selected. When a null space vector is selected, v_{link2} is zero. It can be observed that a higher voltage always appears before a zero voltage. Thus, current commutation of the HFDCL performs during the transition of v_{link2} to zero. Fig. 5-13 (b) and (c) shows the current of the leakage inductance and the DC-link inductor respectively. The average DC-link current is controlled to be 10A and the LVS DC current can be calculated by the turns-ratio of the transformer. It can be observed that minimum DC-link current appears at current commutation of HFDCL. Fig. 5-14 shows the waveforms within a fundamental cycle of AC voltage. Fig. 5-14 (a) and Fig. 5-14 (b) show the voltage and current of phase A. i_A is a pulse current, which is the DC-link current modulated by the CSC. The average of the pulse current is shown in Fig. 5-14 (c) and it is sinusoidal. Fig. 5-14 (d) shows the LVS discharging current of the DC source. Fig. 5-14 (e) shows the pulse voltage which is the modulated AC line voltage and is always positive.

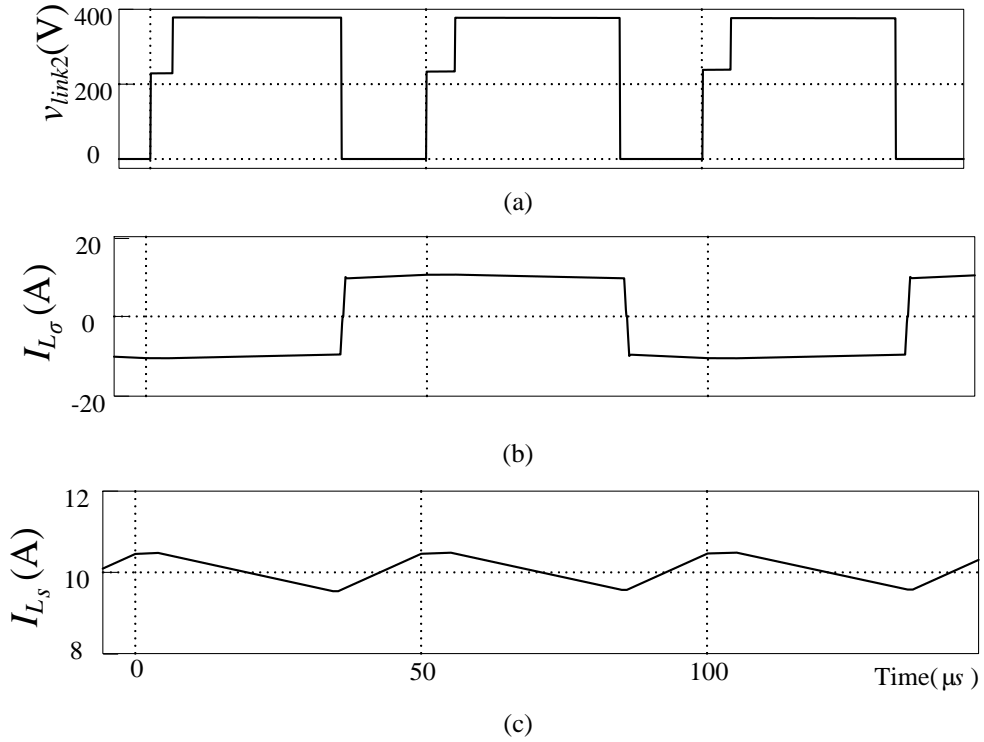


Fig. 5-13 Simulated waveforms in discharging mode of (a) v_{link2} (b) leakage inductance current $i_{L\sigma}$ and (c) DC-link current i_{Ls} .

In discharge mode, the circuit works like a boost converter. After the HFDCL transfers the low DC voltage to a high DC voltage, an inductor is linked this high voltage DC and the AC voltage. The CSC boosts the high DC voltage to the AC voltage.

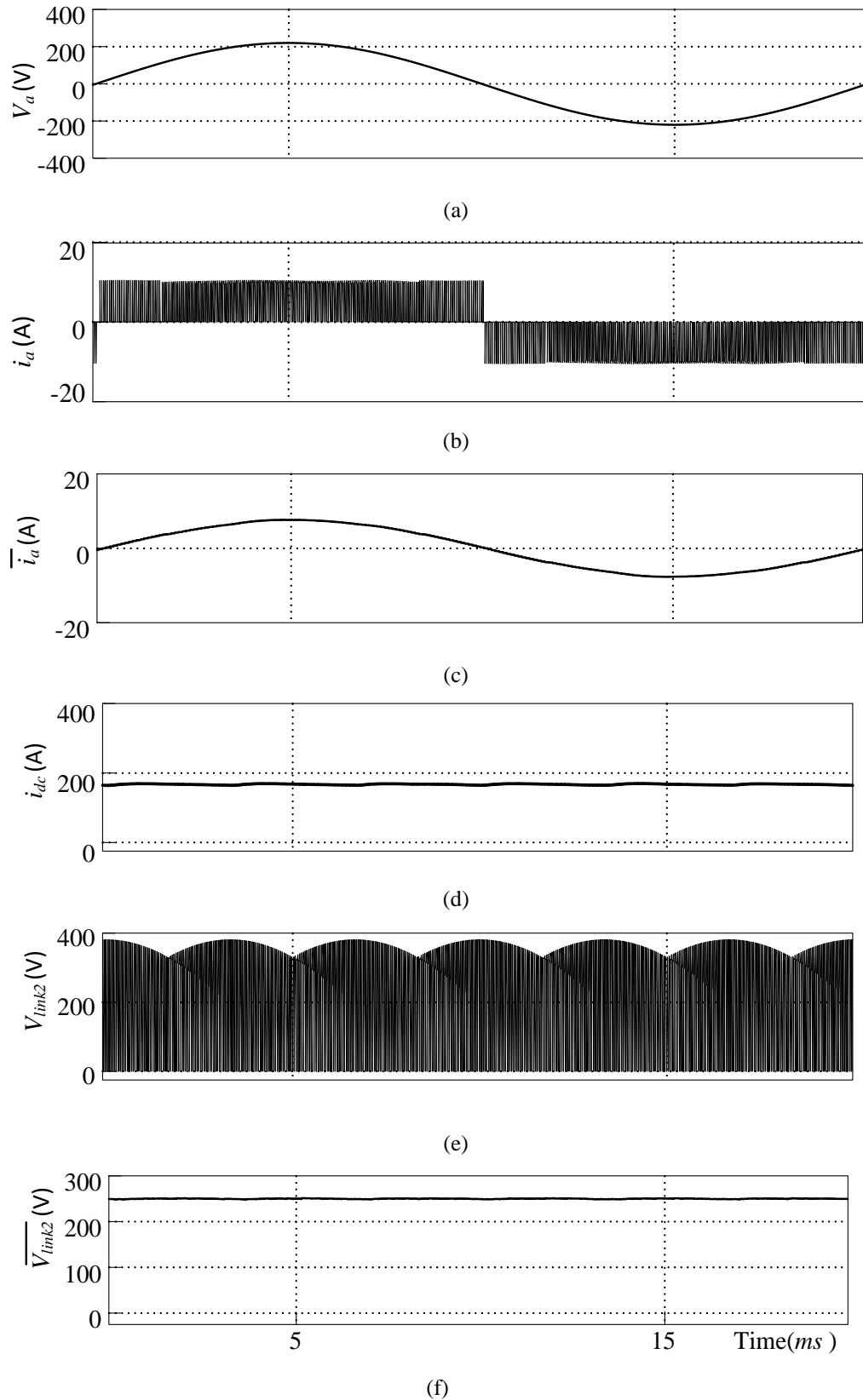


Fig. 5-14 Simulated waveforms in discharging mode of (a) AC grid voltage, (b) pulsed phase current, (c) average phase current, (d) DC current and (e) v_{link2} and (f) average of v_{link2}

Fig. 5-15 shows the simulation results when the LVS DC voltage is 7V. Since the power rating is the same, the virtual average DC current is doubled and is shown in Fig. 5-15 (c). Fig. 5-15 (a) shows the pulse current. Average voltage of V_{link2} is shown in Fig. 5-15 (c) and is halved according to (5.3).

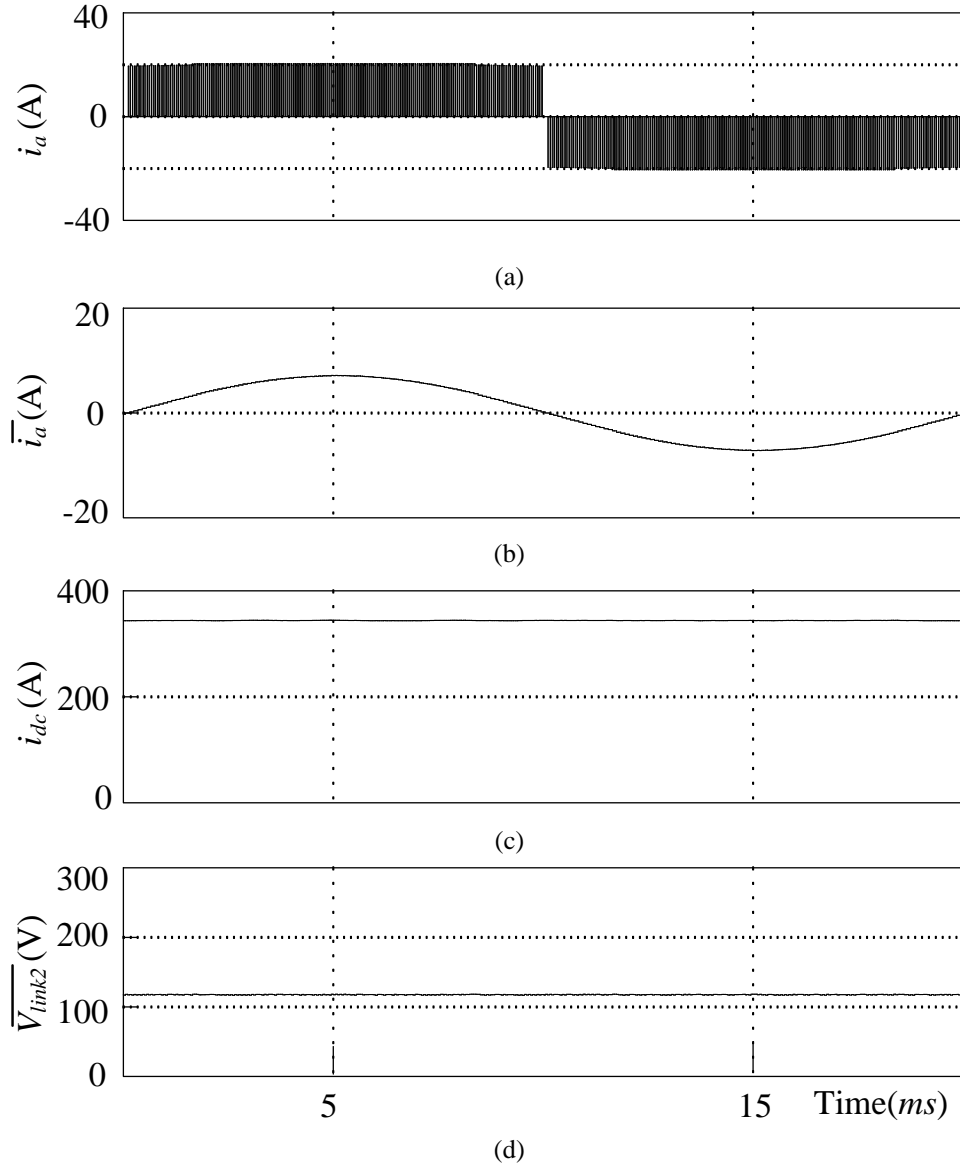


Fig. 5-15 Simulated waveforms in discharging mode of (a) pulsed phase current, (b) average phase current, (c) DC current, and (d) average v_{link2} . When LVS DC voltage is 7V.

5.5.2 Charging Mode

As shown in Fig. 5-16 (a), v_{link2} is negative, and a lower AC grid voltage is applied at v_{link2} after a null space vector is selected. DC-link inductor is magnetized when v_{link2} equals to the lowest negative voltage, and it is demagnetized when $v_{link2} = 0$. Minimum DC-link inductor current appears at the current commutation of HFDCL. Fig. 5-17 shows the

waveforms of the AC grid voltage and current over a fundamental cycle. Fig. 5-17 (a), (b), and (c) show voltage, pulse current and average current of phase A respectively. The phase voltage and current have a phase angle difference of 180° .

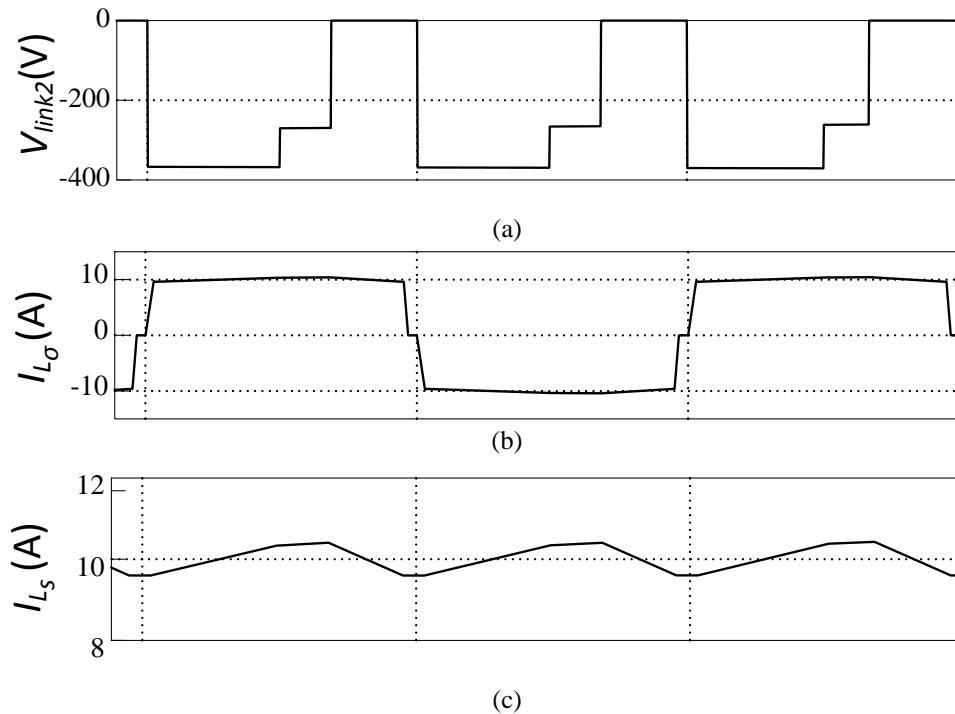


Fig. 5-16 Simulated waveforms in charging mode of (a) V_{link2} (b) leakage inductor current, and (c) DC-link inductor current.

In charge mode, the circuit works like a buck converter. The CSC chops the AC voltage and an inductor links the chopped AC voltage to the high DC voltage. The HFDCL transfers this high DC voltage to low DC voltage and charges the ESDs.

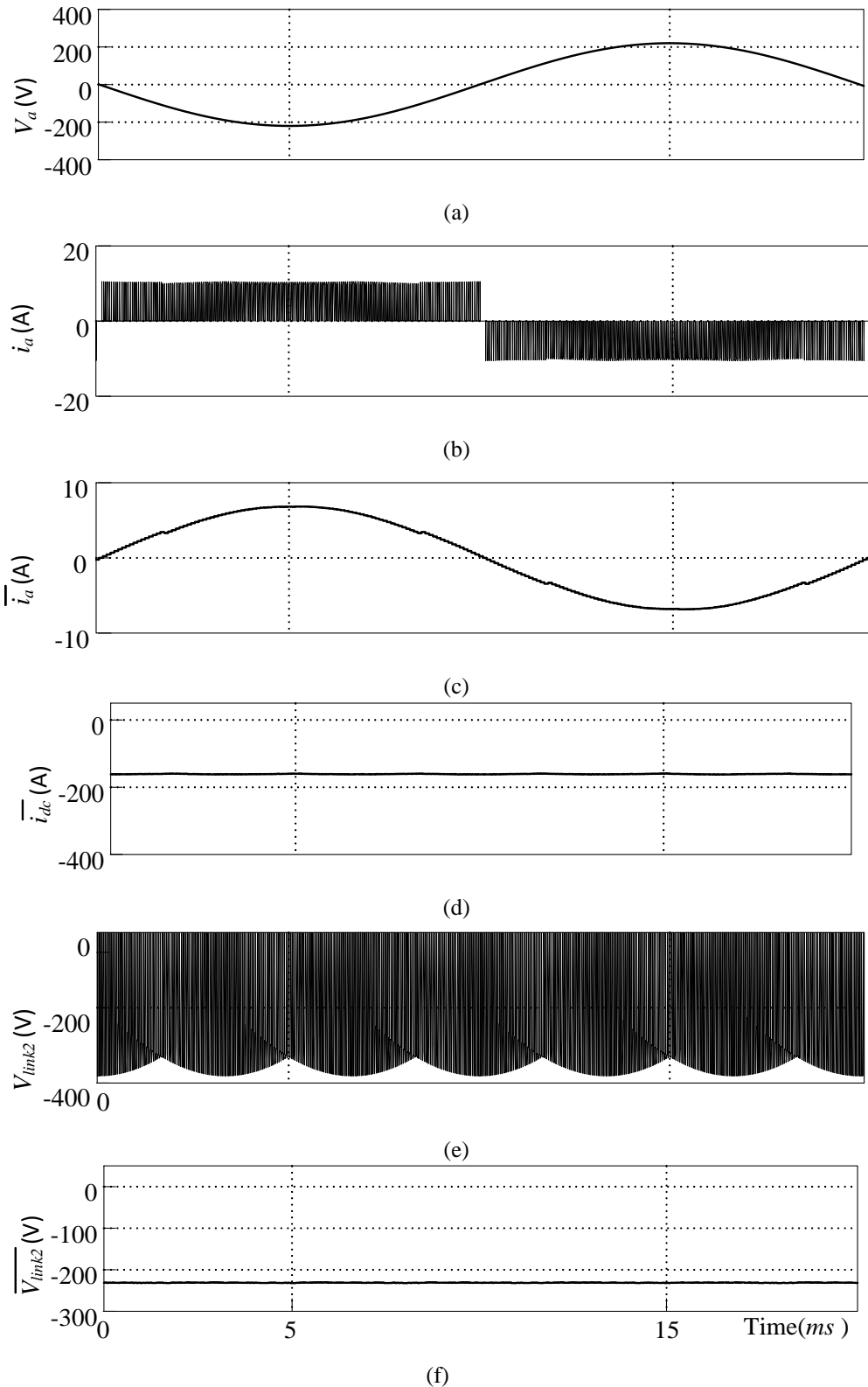


Fig. 5-17 Simulated waveforms in charging mode of (a) phase voltage of AC grid, (b) pulsed phase current, (c) average phase current, (d) DC current and (e) v_{link2} and (f) average of v_{link2} .

Fig. 5-18 shows the simulation results in charging mode when the LVS DC voltage is 7V. Compared to the previous case, pulsed AC current and LVS DC current are doubled. V_{link2} is halved while average AC current is unchanged.

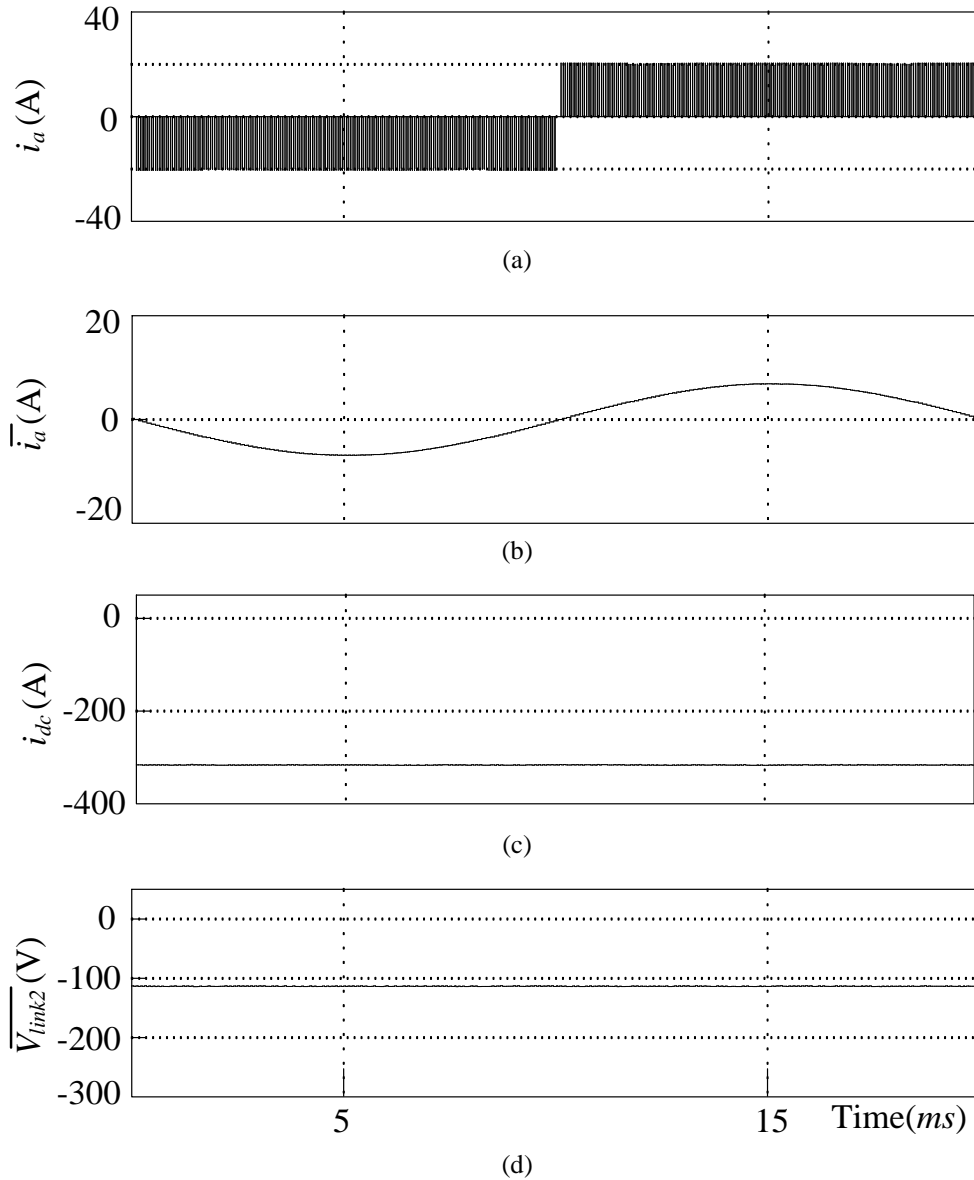


Fig. 5-18 Simulated waveforms in charging mode of (a) pulsed phase current, (b) average phase current, (c) DC current, and (d) average v_{link2} . When LVS DC voltage is 7V.

5.6 Experimental Results

A laboratory prototype that is shown in Fig. 5-19 was built to verify the circuitry and modulation method of the proposed DC/AC converter. AC grid is simulated by a three-phase AC voltage source with 110V/50 Hz output (per-phase rms-voltage), and ESS are simulated by a DC source having a terminal voltage of 10V. In discharging mode,

resistive load is connected to the output of the AC source to avoid power flowing into it. Switching frequency of the HFDCL is 20 kHz. Therefore, the CSC has a switching frequency of 40 kHz. $L_s = 500 \mu\text{H}$, and the transfer ratio $N_1:N_2$ of the HF transformer is 1:17. A three-phase CL ($C=20 \mu\text{F}$ and $L= 200 \mu\text{H}$ per phase) filter is connected between the AC source and the proposed converter. Digital control is implemented by DSP from Texas Instrument. The HFDCL locates at the left side of Fig. 5-19 and CSC locates at the central bottom.

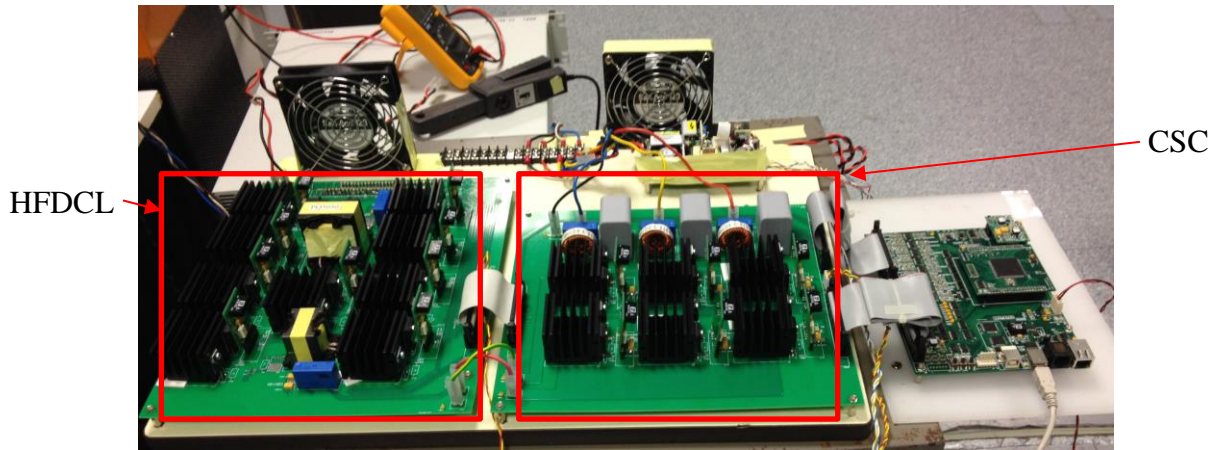


Fig. 5-19 Laboratory prototype of the proposed dc/ac converter

Fig. 5-20 (a) shows the DC-link inductor current i_{L_s} and v_{link2} within switching cycle in discharging mode. Envelop of v_{link2} shown in Fig. 5-20 (b) reflects the line voltage of the AC source over fundamental cycles. Fig. 5-20 (c) exhibits the voltage and current of phase A with current direction defined in Fig. 5-1.

It can be observed that the polarity of v_{link2} is reversed in Fig. 5-21 (a) in charging mode, while the direction of i_{L_s} is unchanged. As it is stated in section 5.3 and verified by simulation results, the current commutation of the HFDCL occurs when a null space vector ends and a lower negative line voltage is applied at v_{link2} . Fig. 5-21 (b) shows the envelope of v_{link2} , which reflects the lowest negative line voltage of the AC source. The voltage and current of phase A of the AC source are shown in Fig. 5-21 (c) with a phase angle difference close to 180°

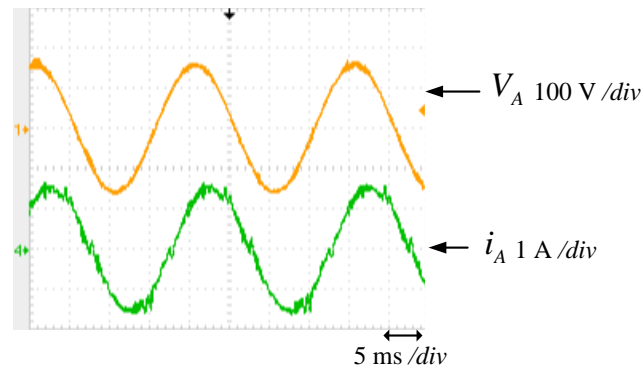
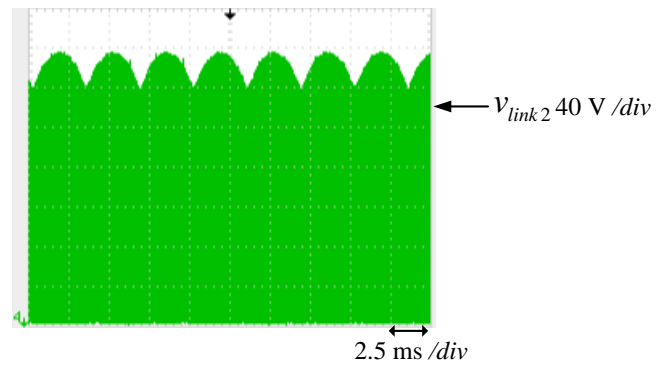
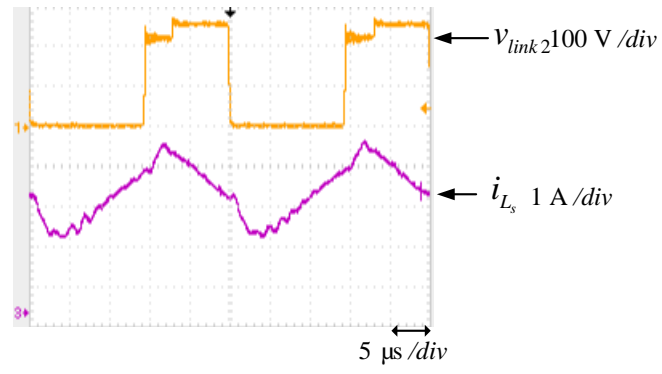
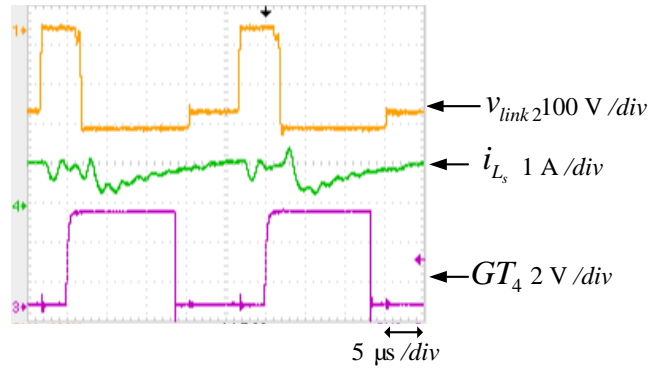
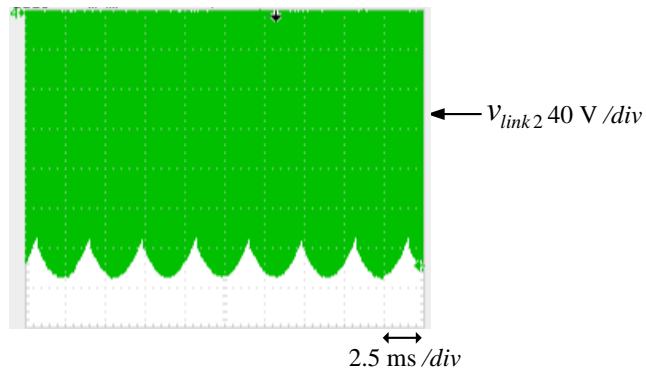


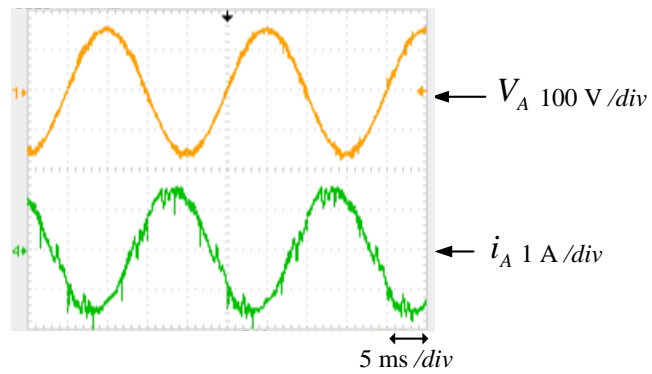
Fig. 5-20 Experimental waveforms for discharging mode of (a) v_{link2} and DC-link inductor current i_{L_s} (b) envelop of v_{link2} (c) AC source phase voltage v_A and current i_A



(a)



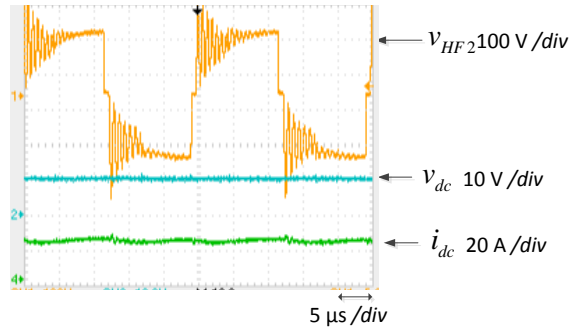
(b)



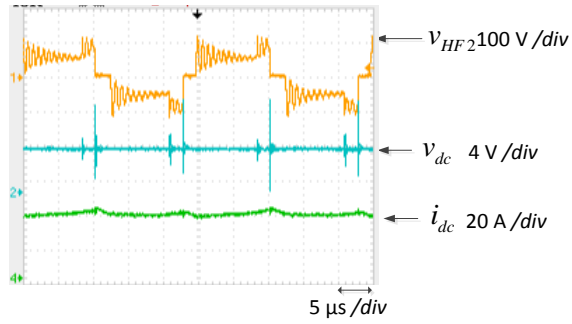
(c)

Fig. 5-21 Experimental waveforms in charging mode (a) v_{link2} and DC-link inductor current i_{L_s} (b) envelop of v_{link2} (c) AC source phase voltage v_A and current i_A

Fig. 5-22 (a) shows the voltage and current of ESS in discharging mode when $v_{dc} = 10$ V and Fig. 5-22 (b) shows that when $v_{dc} = 5$ V. V_{HF2} is the secondary side voltage of the HF. The proposed converter works fine in the two cases.

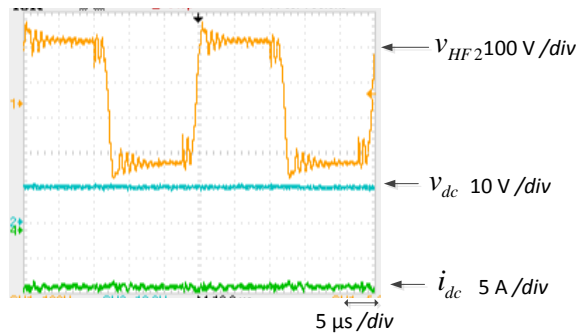


(a)



(b)

Fig. 5-22 Experimental waveforms for discharging mode of voltage and current of ESS (a) $v_{dc} = 10$ V (b) $v_{dc} = 5$ V



(a)

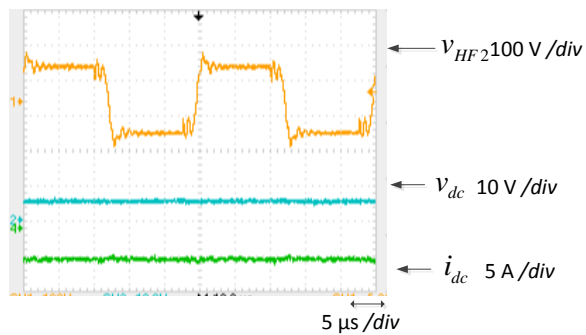


Fig. 5-23 (a) shows the voltage and current in charging mode when $v_{dc} = 10$ V and Fig. 5-23 shows that when $v_{dc} = 5$ V.

5.7 Conclusion

A bidirectional DC/AC converter consisting of HFDCL+CSC for grid-tied ESS application is proposed in this chapter. Compared with other topologies, the proposed converter can avoid using bulky DC capacitors or extra cell equalizer circuitries. Furthermore, no grid-side current sensor is required. The control algorithm for the proposed converter is also easy for implementation. The proposed topology has a high boost ratio and thus can be used for ESS with wide terminal voltage. A novel MSVS is proposed for coordinating the HFDCL and the CSC to keep the volt-second balance for the HF transformer. Results obtained by Simulation and hardware experiment verified the effectiveness of the proposed circuitry and the modulation method.

Chapter 6 Instability Investigation of Multiple Paralleled Modularized Energy Storage System

Modularized design can improve reliability and flexibility for ESS application. One challenge to incorporate ESSs to AC power grid is to integrate multiple parallel inverters. [141] investigated active damping of multiple resonances for parallel inverters used in micro-grid application. [142] discussed the modeling and control of parallel inverters for PV system based on master-slave method. [114] gave a hierarchical control method based on droop control. To allow ESSs to operate without main AC grid in emergency or for the purpose of improving overall system efficiency, paralleled inverters associated with ESSs need to operate in voltage-source mode, such as modularized uninterruptible power supply (MUPS) with high reliability of $N+1$ or $N+X$ redundancy. MUPS system has been widely used to provide reliable power for critical loads in wafer fabrication industries, communication networks, and data centers [11].

Parallel inverters used for various types of distributed energy resources (DER), such as wind turbines and PV panels, all have the same challenge of sharing an equal output power among modules. In this chapter, an MUPS is used as an example to investigate parallel inverters associated with generalized DERs operating in voltage-source mode. Each module of MUPS consists of a rectifier with power factor correction (PFC) and an inverter. Theoretically, the output power can be equally shared if the output voltage and frequency of each inverter of the MUPS are exactly the same, otherwise there will be circulating current among modules. Fig. 6-1 shows an example of the circulating current between two modules with 3-phase/4-wire configuration and a common neutral point. The circulating current will cause exchange of active and reactive power between the two modules. Exchange of reactive power creates additional loss and limits system output capacity while exchange of active power can result in stability problems.

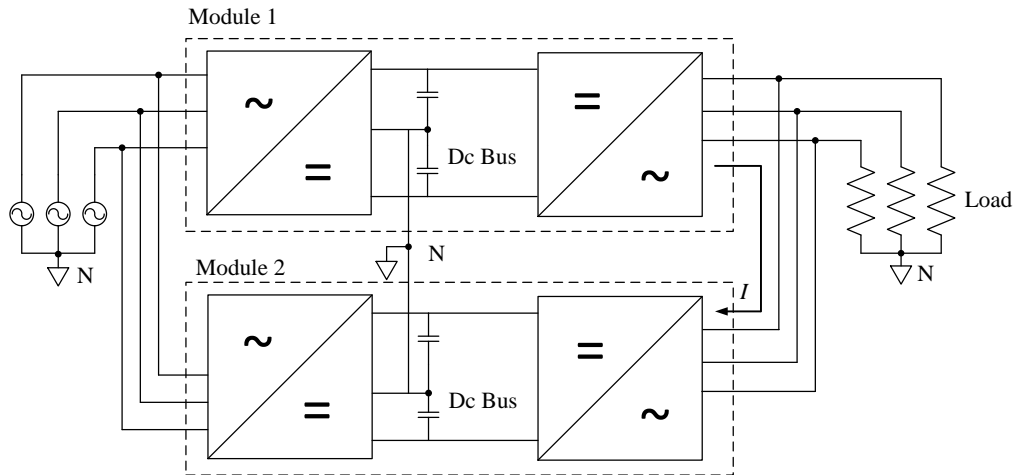


Fig. 6-1 Circulating current between two modules in parallel of a 3-phase/4-wire system

Many control schemes have been proposed to balance the output current or power for parallel inverters. These control schemes can be categorized into two main groups [14]. One group is based on active power sharing, in which communication circuits are used for exchanging information such as output power and voltage of each inverter [99-107], the other group is mainly based on droop control [108-113].

Output voltage of a practical inverter contains two groups of frequency components. One group consists of the fundamental component of AC power, which is normally 50/60Hz, and its harmonics. The other group consists of the fundamental component of carrier wave and its harmonics. The fundamental frequency of the carrier wave is related to the scheme of PWM generation. Impacts of the carrier wave components on parallel converters have been investigated by researchers in recent years. In [115], an active-power-filter (APF) topology based on parallel-interleaved inverters has been proposed. Parallel inverters are connected to a common DC bus, and the interleaving structure reduces current ripple and the size of the inductors. A modified discontinuous PWM scheme is reported in [116] for parallel three-phase voltage-source multi-level inverters, and an interleaved three-phase AC/DC converter with PFC is proposed in [117] to mitigate voltage stress and current harmonics. An optimized carrier wave interleaving angle is used in [118] to minimize grid-current ripple. Interleaving angle, which is the phase difference between carrier waves, also has a significant impact on the stability of parallel inverters. However, due to the distributed nature of MUPS, the phase shift and frequency difference of the carrier waves are difficult to control, which will lead to system instability issues.

In order to improve overall system efficiency, all inverter outputs are directly connected to a common AC bus to minimize cable loss. When the MUPS operates under no-load condition, DC bus overvoltage is observed. This overvoltage usually triggers a DC bus protection, which leads to MUPS malfunction and sometime damages the DC bus capacitors. DC bus protection is also essential for wind power converters during low-voltage-ride-through (LVRT), in which the converters are required to be connected to the main AC grid when a voltage dip occurs. Since there is a mismatch between the generated power and the power delivered to the grid, additional circuit and/or control scheme is required to protect DC bus from being charged to overvoltage. Breaking chopper is used in [143] and [144] to protect the DC bus during LVRT for permanent-magnet synchronous generator (PMSG). This method is easy to implement and may be applied to MUPS systems. However, the breaking chopper only dissipates power as heat and requires additional control circuit. Advanced control strategies are proposed in [145],[146] without the requirement of a breaking chopper. However, these methods are not applicable for MUPS systems.

This chapter investigates the causes of the DC bus overvoltage of multiple-parallel MUPS modules with detailed analysis. This investigation is started with two parallel modules and then extended to multiple modules. A novel method based on carrier wave frequency shifting is proposed to suppress the DC bus overvoltage. The proposed method is illustrated by using an MUPS with two parallel modules as well as that with three modules. The impact of the proposed method on normal operation of the MUPS is also investigated.

6.1 DC Bus Overvoltage under No-load Condition

In high power UPS applications, 3-level inverters are commonly used to provide 3-phase/4-wire configuration due to the requirement of a neutral wire. Fig. 6-2 shows two parallel inverters, each of which adopts a 3-level neutral-point-clamped (NPC) topology, to investigate the DC bus overvoltage issue. System parameters are summarized in Table 6-1. Each inverter has an output LC filter.

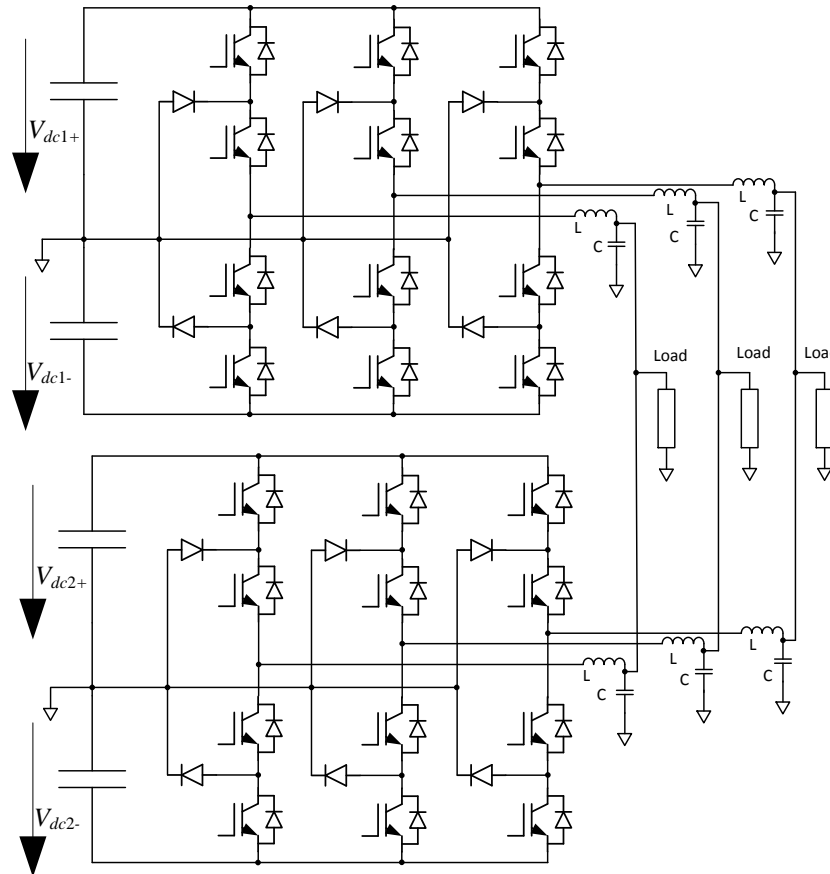


Fig. 6-2 Two 3-level NPC inverters with a common neutral wire connected in parallel.

Table 6-1 System parameters of the paralleled inverters for hardware experiment

Symbol	Description	Value
L	inductance of output filter	320 μH
C	capacitance of output filter	40 μF
f_c	carrier wave frequency	17 kHz
$V_{dc\pm/}$	normal dc bus voltage	± 360 V
C_{dc}	capacitance of single dc bus	8 220 μF

The operation and control scheme of an individual 3-level NPC inverter are fully described in [147-150]. Since the focus of this chapter is specifically on parallel operation, an individual 3-level NPC inverter is assumed to be well controlled by a two-loop strategy, i.e., an inner inductor-current loop and an outer capacitor-voltage loop. Current sharing is based on a master-slave structure. The active and reactive power information of each inverter is transmitted to others within every AC power fundamental cycle. Output

power rating of every single module is 20 kW. The topology of the rectifier with PFC used in this investigation is shown in Fig. 6-3, which only has unidirectional power flow.

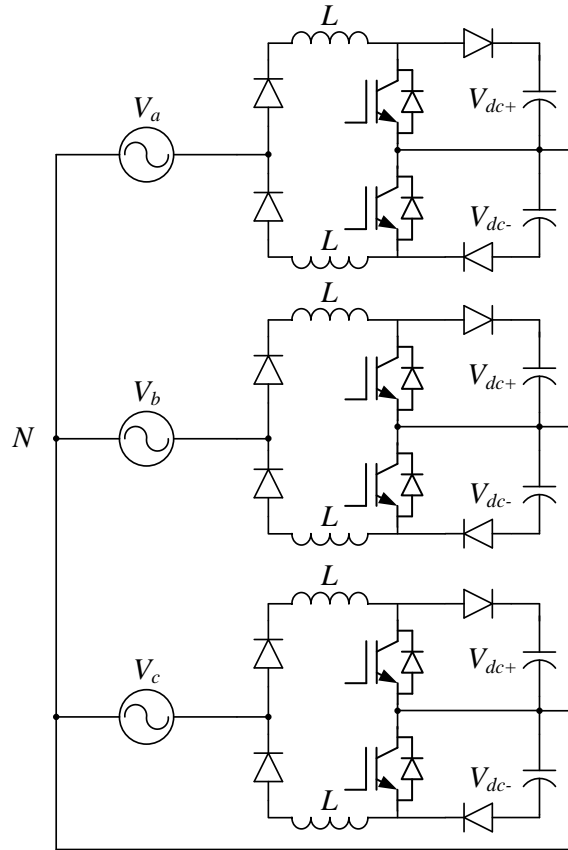


Fig. 6-3 3-phase/3-level rectifier with PFC with unidirectional power flow

The positive and negative DC bus voltages of each module are controlled to be $\pm 360\text{V}$ respectively, and the per-phase output rms-voltage is 220V. An autonomous current sharing method is adopted for the parallel inverters. Information of active and reactive power is transmitted between inverters by a controller-area-network (CAN) bus. The frequency and amplitude of the AC power component of the output voltage of each inverter are regulated based on the maximum value among all the inverters. Details of the power sharing method are described in [105].

The positive DC bus voltage waveforms of the two modules under no-load condition are shown in Fig. 6-4. It can be observed that overvoltage occurs. For most parallel modules, DC bus overvoltage is caused by modules charging each other; and the fact that the rectifier, which is used to generate the DC input to the inverter, only has unidirectional power flow. When load is connected to the output of the MUPS, overvoltage may not be

observed if the active power consumed by the load is higher than the active power transferred between the two modules. However, an MUPS is required to work under no-load condition in some circumstance; so, the DC bus overvoltage of the MUPS under no-load condition should be suppressed. Detailed causes of the DC bus overvoltage will be discussed in the following sections.

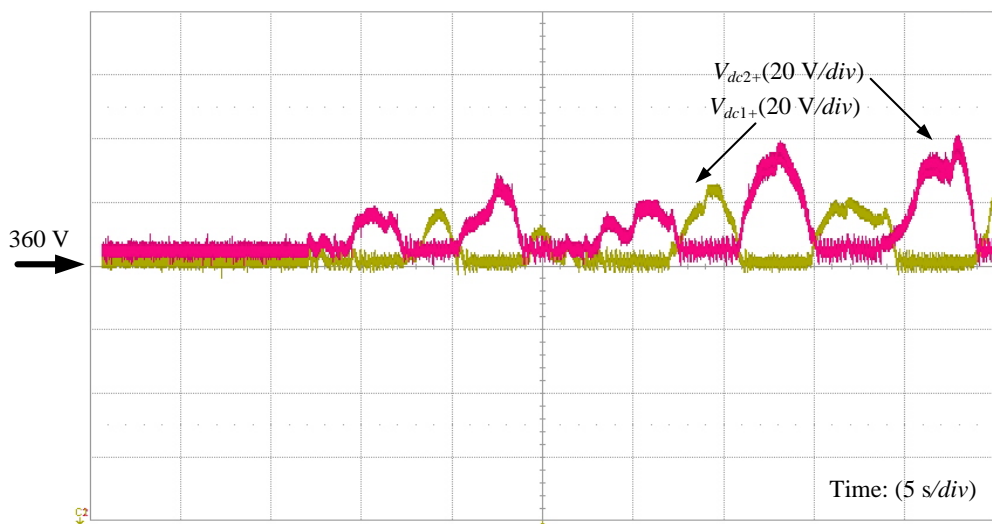


Fig. 6-4 Positive DC bus voltages of two parallel modules under no-load condition.

6.2 Analysis of Active Power Circulation Issue

The analysis of the active power circulation will be presented in this section, for two inverters initially and is subsequently extended for any number of inverters. It is assumed that each individual inverter is intended to be identical and the power sharing method used in [105] is applied. Typically, this is indeed the case of a number of identical MUPS modules or that of a number of identical PV inverters, which are connected in parallel and operate in voltage-source mode. Difference of the AC power frequency components of the output voltages between the two inverters is assumed to be relatively minor. The following analysis is based on the regular-sampled PWM scheme for the 3-level NPC inverter shown in Fig. 6-3 (a). The 3-phase inputs of each module are assumed to be balanced, so per-phase analysis is sufficient for the study.

6.2.1 Two Inverters in Parallel

Fig. 6-5 shows the simplified single-phase circuit diagram of two parallel inverters under no-load condition.

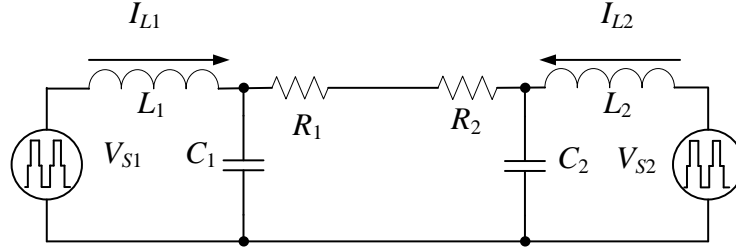


Fig. 6-5 Per-phase simplified equivalent circuit of two parallel inverters under no-load condition.

V_{S1} and V_{S2} represent the output voltages of the switching bridges of inverter 1 and 2 respectively. Each has three possible voltages of $+V_{dc}$, $-V_{dc}$ and 0. L_1 , L_2 and C_1 , C_2 are the inductors and capacitors of the output filters of inverter 1 and 2 respectively. R_1 and R_2 are the resistances of the cable and connectors that connect the two inverters, which are usually very small and can be neglected in this analysis. V_{S1} and V_{S2} can each be decomposed into a series of sinusoidal waves as (6.1) [151].

$$V_{Si} = \sum_{n=1}^{\infty} A_{0n} e^{j(n[\omega_{0i}t + \theta_{0i}])} + \sum_{m=1}^{\infty} A_{m0} e^{j(m[\omega_{ci}t + \theta_{ci}])} + \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ n \neq 0}}^{\infty} A_{mn} e^{j(m[\omega_{0i}t + \theta_{0i}] + n[\omega_{ci}t + \theta_{ci}])} \quad (6.1)$$

where $i = 1, 2$, ω_{ci} and θ_{ci} are the angular frequency and the phase angle of the carrier wave of inverter i respectively, ω_{0i} and θ_{0i} are the angular frequency and the phase angle of the output voltage of inverter i respectively. m is the carrier wave components index variable, and n is the AC power components index variable. A_{mn} is the magnitude of the frequency component at mn^{th} order.

If the two inverters are properly controlled, the AC output voltages will have the same AC power frequency and phase. Therefore, $\theta_{01} = \theta_{02} = \theta_0$ and $\omega_{01} = \omega_{02} = \omega_0$. The two carrier wave frequencies are similar but not exactly the same; therefore, $\omega_{c1} \cong \omega_{c2} \cong \omega_c$. There is also phase difference between the carrier waves ($\Delta\theta_c = \theta_{c1} - \theta_{c2}$), which is shown in Fig. 6-6.

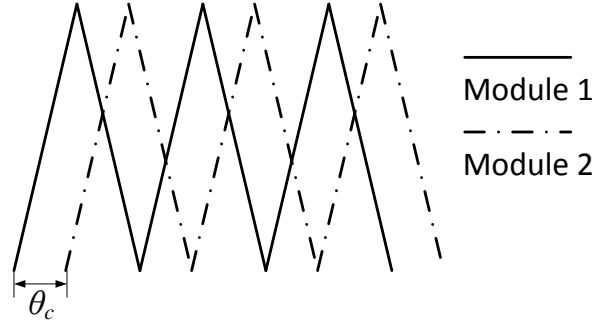


Fig. 6-6 Phase difference of the carrier waves of two parallel inverters.

The inductor current of inverter 1 at the mn^{th} order can be calculated by:

$$I_{L1}(m, n) = \frac{Z_L}{Z_L^2 + Z_C \cdot Z_L} \cdot V_{S1}(m, n) + \frac{Z_C / 2}{Z_L^2 + Z_C \cdot Z_L} \cdot [V_{S1}(m, n) - V_{S2}(m, n)] \quad (6.2)$$

where, Z_L and Z_C are the impedances of the inductor and capacitor of the output LC filter respectively. The output apparent power of inverter 1 can be calculated by:

$$\begin{aligned} S_{V_{S1}}(m, n) &= V_{S1}(m, n) \cdot \overline{I_{L1}(m, n)} \\ &= V_{S1}(m, n) \cdot \overline{(2Z_P \cdot V_{S1}(m, n) - Z_P \cdot V_{S2}(m, n))} \end{aligned} \quad (6.3)$$

$$\text{Where, } Z_P = \frac{Z_L}{Z_L^2 + Z_C \cdot Z_L}.$$

By substituting (6.1) into (6.3), the circulating apparent-power of inverter 1 at angular frequency $\omega_{mn} = m\omega_c + n\omega_0$ can be calculated by:

$$S_{V_{S1}}(m, n) = A_{mn}^2 \cdot \left[\begin{array}{l} -j \cdot \frac{\omega_{mn} L}{-\omega_{mn}^2 L^2 + L/C} \\ + j \cdot \frac{1/2 \omega_{mn} C}{-\omega_{mn}^2 L^2 + L/C} \cdot (1 - \sin(\pi/2 + m\Delta\theta_c)) \\ \underbrace{\hspace{10em}}_{\text{Reactive Power}} \\ + \frac{-1/2 \omega_{mn} C}{-\omega_{mn}^2 L^2 + L/C} \cdot \cos(\pi/2 - m\Delta\theta_c) \\ \underbrace{\hspace{10em}}_{\text{Active Power}} \end{array} \right] \quad (6.4)$$

The reactive power in (6.4) implies a circulating power exchanging between the two modules at the angular frequency of ω_{mn} , and the reactive power has a minimum impact on the voltage of the DC buses feeding the inverters. However, the active power transferred from one module to the other without consumption may cause energy

accumulation, which highly depends on the phase difference between the carrier waves.

The active power delivered from V_{S1} to V_{S2} can be calculated by:

$$P(m, n) = \frac{(\sin m\Delta\theta_c) A_{mn}^2}{2(\omega_{mn}^3 L^2 C - \omega_{mn} L)} \quad (6.5)$$

By defining $x = \omega_c t + \theta_{ci}$, $y = \omega_0 t + \theta_0$, (6.1) can be expressed as (6.6), where $J_n(\cdot)$ is the n^{th} order Bessel function and M is the modulation index.

$$\begin{aligned} V_{Si} = & 2V_{dc} \sum_{n=1}^{\infty} \frac{-\cos(n\pi) \cdot J_n \left(\left([2n-1] \cdot \frac{\omega_0}{\omega_c} \right) \pi M \right)}{\left([2n-1] \cdot \frac{\omega_0}{\omega_c} \right) \pi} \cdot \cos(ny) \\ & + \sum_{m=1}^{\infty} \frac{8V_{dc}}{m\pi^2} \cdot \sum_{k=0}^{\infty} \frac{J_{2k+1} \left([2m-1] \pi M \right)}{2k+1} \cdot \cos([2m-1]x) \\ & + \frac{2V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{\cos(n\pi) / \left(2m + [2n+1] \cdot \frac{\omega_0}{\omega_c} \right)}{J_{|2n+1|} \left(\left(2m + [2n+1] \cdot \frac{\omega_0}{\omega_c} \right) \pi M \right)} \cdot \cos([2m]x + [2n+1]y) \\ & + \frac{8V_{dc}}{\pi^2} \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ n \neq 0}}^{\infty} \frac{1}{\left([2m-1] + 2n \cdot \frac{\omega_0}{\omega_c} \right)} \cdot \sum_{k=0}^{\infty} \frac{J_{2k+1} \left(\left([2m-1] + 2n \cdot \frac{\omega_0}{\omega_c} \right) \pi M \right)}{\left([2k+1] + 2n \right) \cdot \left([2k+1] - 2n \right)} \cdot \cos([2m-1]x + [2n]y) \end{aligned} \quad (6.6)$$

The spectrum of the output voltage in (6.6) under the condition of $M=0.9$ and $f_c / f_0 = 200$ is shown in Fig. 6-7. The spectrum of the corresponding active power $P(m,n)$ defined in (6.5) is shown in Fig. 6-8.

It can be observed from Fig. 6-7 and Fig. 6-8 that the fundamental component of the carrier wave dominates the spectrum. The other harmonic components with relatively small amplitudes can hardly impact the analysis in this chapter. From (6.5), the active power decreases rapidly as the frequency increases. Therefore, high frequency components of the carrier wave can be neglected, and only the fundamental component needs to be considered. The active power of the fundamental component of the carrier wave, i.e., $(m = 1, n = 0)$ in (6.5), is given by:

$$P(1,0) = \frac{A_{10}^2}{2\omega_c L(\omega_c^2 LC - 1)} \cdot \sin \Delta\theta_c \quad (6.7)$$

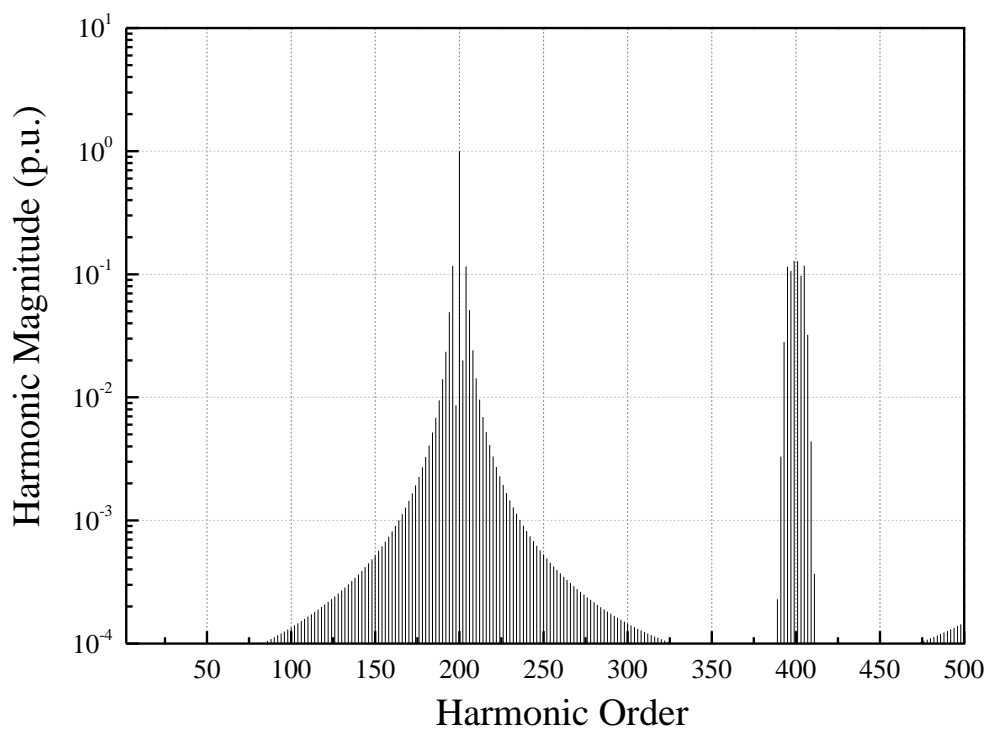


Fig. 6-7 Spectrum of the phase voltage when $M=0.9$ and $f_c/f_0 = 200$.

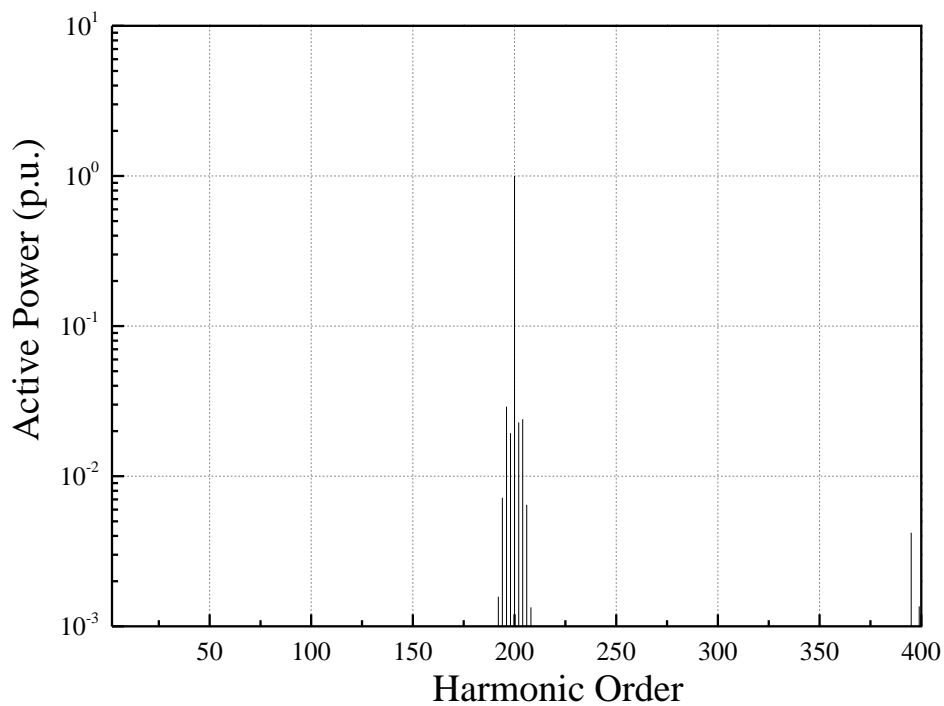


Fig. 6-8 Spectrum of the active power when $M = 0.9$ and $f_c/f_0 = 200$.

Theoretically, the two carrier waves have the same frequency. However, in practice, the carrier wave frequencies cannot be exactly the same even if the two inverters are manufactured to identical specifications. This is because the properties of the crystal oscillators used in the control circuit are different due to batch manufacturing variance. The frequency difference is defined as:

$$\Delta f_c = f_{c1} - f_{c2} \quad (6.8)$$

As a result, the phase difference drifts with time, and it is expressed as:

$$\Delta \theta_c(t) = 2\pi \Delta f_c t = \Delta \omega_c t \quad (6.9)$$

and shown in Fig. 6-9.

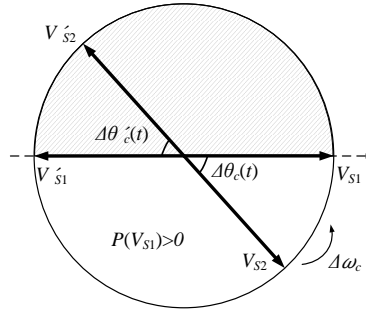


Fig. 6-9 Phase difference between the fundamental components of the carrier waves.

In the lower half of the circle ($0 < \Delta \theta_c(t) < \pi$) shown in Fig. 6-9, the active power delivered from V_{S1} to V_{S2} is always positive, and V_{S1} therefore charges V_{S2} ; as a result, the DC bus voltage of inverter 2 will rise. In the upper half of the circle ($-\pi < \Delta \theta_c(t) < 0$), the active power delivered from V_{S1} to V_{S2} is negative, and V_{S2} therefore charges V_{S1} . Under no-load or light-load condition, energy stored in the DC bus cannot be dissipated. The maximum energy E transferred from one module to the other can be calculated by:

$$E = \int_0^{\frac{\pi}{\Delta \omega_c}} P(1,0) dt = \frac{1}{\Delta \omega_c} \int_0^{\pi} P(1,0) d\Delta \theta_c(t) = \frac{1}{\Delta \omega_c} \cdot \frac{A_{10}^2}{\omega_c L (\omega_c^2 LC - 1)} \quad (6.10)$$

If $\omega_{c1} = \omega_{c2}$ and $\theta_{c1} = \theta_{c2}$, according to (6.7), there is no active power transferred between the two modules; therefore, there is no DC bus overvoltage. If $\theta_{c1} \neq \theta_{c2}$, $\Delta \theta_c$ is fixed and the active power is invariant, which means that the DC bus of one module charges the DC

bus of the other one. If $\omega_{c1} \neq \omega_{c2}$, $\Delta\theta_c$ varies with time and the charging/discharging status of each module can be decided by the sign of $\Delta\theta_c$.

The magnitude of the fundamental component of the carrier wave can be obtained by:

$$A_{10} = \frac{8V_{dc}}{\pi^2} \sum_{k=1}^{\infty} \frac{J_{2k-1}(\pi M)}{2k-1} \quad (6.11)$$

The maximum absolute value of V_{dc+} and V_{dc-} can be calculated by:

$$V_{\max} = \sqrt{V_{dc}^2 + 2 \cdot 3 \cdot E / C_{dc}} \quad (6.12)$$

In conclusion, (6.10) shows that smaller difference of the carrier wave frequency can lead to more energy to be accumulated; therefore, higher DC bus voltage is obtained.

6.2.2 Simulation Results

Simulation in Matlab/Simulink has been conducted to verify (6.12) and explain how energy is accumulated on the DC buses of parallel modules. System parameters for the simulation are the same as those described in Table 6-1.

The per-phase output rms-voltage is 220 V, and M can be calculated by (6.13) when the voltage drop across the switches and output inductors are ignored.

$$M = \sqrt{2} \cdot V_p / V_{dc} \quad (6.13)$$

where V_p is the per-phase output rms-voltage. M varies with load under close-loop control. However, this study mainly focuses on no-load operation, and M does not vary far from the value under open-loop control. Although a close-loop control is adopted in the simulation and hardware experiment, a fixed M of 0.8639 is used for simplicity. When $\Delta f_c = 0.2$ Hz, the calculated maximum DC bus voltage is 377.65 V by using (6.12).

Fig. 6-10 shows the simplified equivalent circuit of the two parallel inverters under no-load condition. This equivalent circuit simplifies the DC bus and VSI as a controllable AC source. Even though the paralleled system is a three-phase system, it can be simplified as a single-phase system. Because the three-phase system has different phase at main AC power frequency component but the system has no phase difference at switching frequency. Thus, per phase analysis is sufficient. Energy transferred for the three-phase system can be obtained after finding the solution for per-phase analysis.

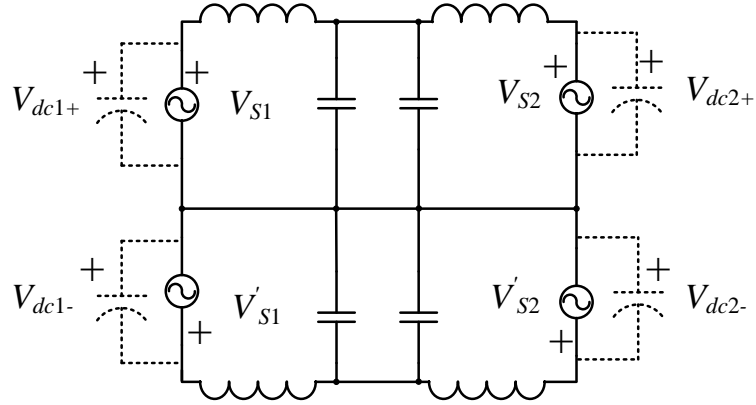


Fig. 6-10 Simplified equivalent circuit of two parallel inverters under no-load condition.

The simulated waveforms of the DC bus voltages of the two paralleled modules are shown in Fig. 6-11. Energy transfer can be explained as follows. For the positive DC bus shown in Fig. 6-11, when $t = 0$ s, the phase difference in radians ($\Delta\theta_c(t)$) is zero, and according to (6.7), $P(1,0) = 0$ W. From $t = 0$ s to $t = 2.5$ s, $\Delta\theta_c(t)$ increases from 0 to π . When $0 < \Delta\theta_c(t) < \pi$, $P(1,0)$ is always positive. $P(1,0)$ increases during $0 \leq \Delta\theta_c(t) < \pi/2$, and reaches the maximum when $\Delta\theta_c(t) = \pi/2$. From $\Delta\theta_c(t) = \pi/2$ to $\Delta\theta_c(t) = \pi$, $P(1,0)$ decreases. When $\Delta\theta_c(t) = \pi$, $P(1,0) = 0$ W. From $t = 2.5$ s to $t = 5$ s, $P(1,0)$ is negative and reaches the minimum at $t = 3.75$ s when $\Delta\theta_c(t) = 3\pi/2$. When $P(1,0)$ is positive, V_{S1} charges V_{S2} , and the positive DC bus of module 1 charges the positive DC bus of module 2. Since energy is transferred from V_{dc+} to V_{dc2+} , V_{dc1+} decreases, and V_{dc2+} increases and reaches the maximum at $t = 2.5$ s. Meanwhile, for negative DC bus, from (6), $V'_{S1} = -V_{S1}$ and $V'_{S2} = -V_{S2}$. As shown in Fig. 9, $\Delta\theta'_c(t) = -\Delta\theta_c(t)$, so V_{dc2-} charges V_{dc1-} , and reaches the maximum at $t = 2.5$ s. V_{dc2+} charges V_{dc1+} and V_{dc1-} charges V_{dc2-} when $\pi \leq \Delta\theta_c(t) < 2\pi$. At $t = 5$ s, $\Delta\theta_c(t) = 2\pi$. V_{dc1+} and V_{dc2-} reach the maximum simultaneously. The same charging/discharging cycle is repeated after $t = 5$ s. As shown in Fig. 6-11, the maximum DC bus voltage is around 380 V which matches the result calculated by (6.12).

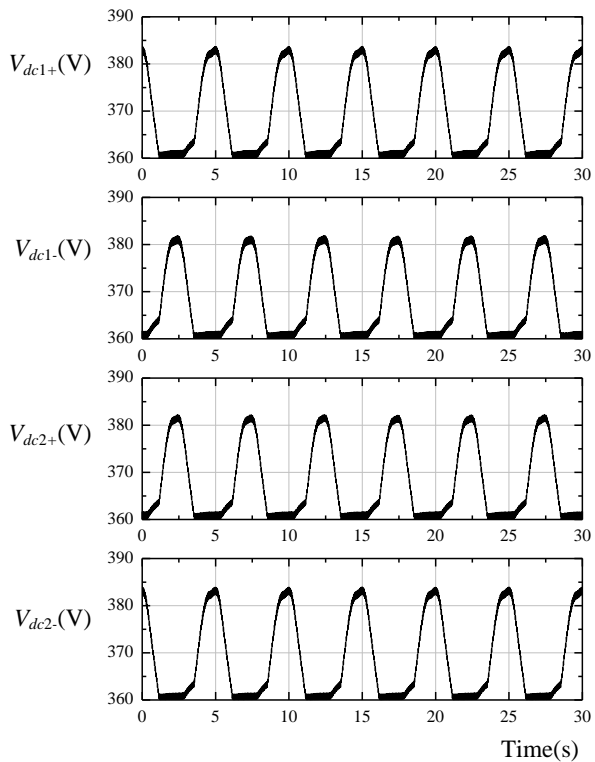


Fig. 6-11 Positive and negative dc bus voltages of two parallel inverters when $\Delta f_c = 0.2$ Hz.

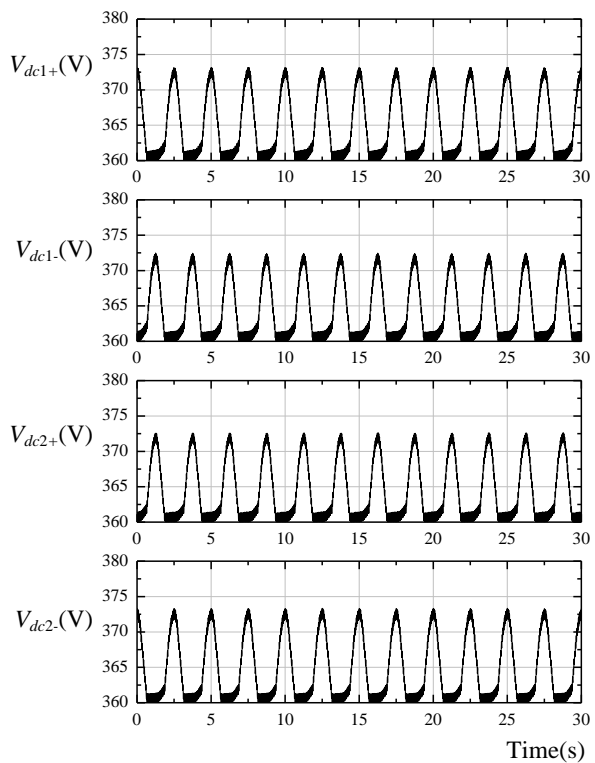


Fig. 6-12 Positive and negative DC bus voltages of two parallel inverters when $\Delta f_c = 0.4$ Hz

The voltages of the four DC buses are shown in Fig. 6-12 when $\Delta f_c = 0.4$ Hz. The energy transferring process is similar to the previous case except that its charging/discharging period is halved. The maximum DC bus voltage calculated by (6.12) is 369 V, which can also be obtained by the simulation results. It can be observed that larger Δf_c generates less DC bus overvoltage.

6.2.3 N Modules in Parallel

The formulations for two inverters in parallel can be easily extended to N number of inverters. Fig. 6-13 shows the equivalent circuit when N modules are in parallel.

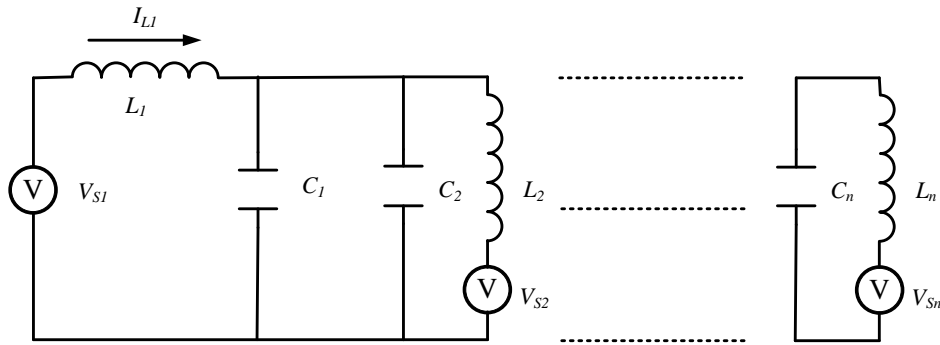


Fig. 6-13 Equivalent circuit of N modules in parallel.

Assuming that inductors and capacitors of the output filters of all inverters are identical, the inductor current of module 1 can be calculated by:

$$I_{L1} = \frac{1}{Z_L + Z_C} \cdot V_{S1} + \frac{Z_C}{N(Z_L + Z_C)Z_L} \sum_{i=2}^N (V_{S1} - V_{Si}) \quad (6.14)$$

Defining $\Delta\theta_{ci} = \theta_{c1} - \theta_{ci}$ as the phase difference between inverter 1 and inverter k , the active power P_N transferred out of V_{S1} can be calculated by:

$$P_N(1,0) = \frac{1}{N} \cdot \sum_{i=2}^N \frac{A_{10}^2}{\omega_c L (\omega_c^2 LC - 1)} \cdot \sin(\Delta\theta_{ci}) \quad (6.15)$$

The maximum active power transferred into inverter 1 can be obtained when all the other $(N-1)$ inverters have the same phase angle but inverter 1 has a different one. Define E_N as the maximum energy transferred into inverter 1 from all the other $(N-1)$ modules, and E_N can be calculated by:

$$E_N = \int_0^{\frac{\pi}{\Delta\omega_c}} P^N(1,0)dt = \frac{2(N-1)}{N} \cdot \frac{1}{\Delta\omega_c} \cdot \frac{A_{10}^2}{\omega_c L(\omega_c^2 LC - 1)} = \frac{2(N-1)}{N} \cdot E_2 \quad (6.16)$$

where E_2 is the energy that can be transferred to module 1 when only two modules are paralleled. When $N \rightarrow \infty$, $\lim_{N \rightarrow \infty} E_N = 2E_2$. This shows, when N inverters are connected in parallel, the maximum energy, which can be transferred into any inverter, is twice that of the case when two inverters are connected in parallel.

6.3 Proposed Solution for Suppressing the DC Bus Overvoltage

From (6.10) and (6.12), the maximum DC bus overvoltage of two parallel inverters is related to the parameters of the output LC filters, the modulation index M and the frequency difference of the carrier waves $\Delta\omega_c$. The maximum energy transferred between the two modules can be reduced by increasing $\omega_c^2 LC$ or $\omega_c L$. However, selection of the carrier wave frequency is limited by practical design, because the resonant frequency of the LC filter is dependent on the carrier wave frequency. $\omega_c^2 LC$ can only be adjusted within a very small range and is regarded more as a constant. Because the inductance of the LC filter is usually inversely proportional to the carrier wave frequency, $\omega_c L$ is constrained to a limited range. Therefore, it is not practical to reduce the DC bus overvoltage by selecting different LC filters or carrier wave frequency. However, since the accumulated energy on the DC bus is inversely proportional to $\Delta\omega_c$, a possible solution would be introduced to control on it, i.e., if $\Delta\omega_c$ can be deliberately controlled to a larger value, the unwanted DC bus overvoltage may be suppressed.

In order to illustrate how the difference of the carrier wave frequencies relates to the maximum dc bus voltage, Fig. 6-14 shows the Phasor diagram of V_{S1} and V_{S2} , the positive dc bus voltage of module 2 (V_{DC}), and the instantaneous active power transferred from module 1 to module 2 (P), for two different cases of $\Delta\omega_c = 4\omega$ and $\Delta\omega_c = \omega$. At t_0 , the phase difference for the two cases of $\Delta\omega_c = 4\omega$ and $\Delta\omega_c = \omega$ are both zero. When $\Delta\omega_c = 4\omega$, from t_0 to t_1 , $\Delta\theta_c(t)$ changes from 0 to π , P changes from zero to the maximum value and then backs to zero. During this period, V_{S1} charges V_{S2} , V_{DC} increases and reaches the maximum value of V_{4max} at t_1 . From t_1 to t_2 , $\Delta\theta_c(t)$ changes from π to 2π and P is negative. During this period V_{S2} charges V_{S1} , V_{DC} decreases from V_{4max} and backs to zero at t_2 . The period from t_0 to t_2 is a complete energy circulating cycle when $\Delta\omega_c = 4\omega$, and the period

from t_2 to t_5 is another energy circulating cycle. From t_0 to t_5 , P is always positive and reaches the maximum value at t_2 when $\Delta\theta_c(t) = \pi$. During this period, V_{S1} charges V_{S2} , V_{DC} increases and reaches the maximum value of V_{1max} at t_5 . According to the analysis above, from t_0 to t_5 , there are two complete energy circulating cycles when $\Delta\omega_c = 4\omega$, while there is only a half energy circulating cycle when $\Delta\omega_c = \omega$.

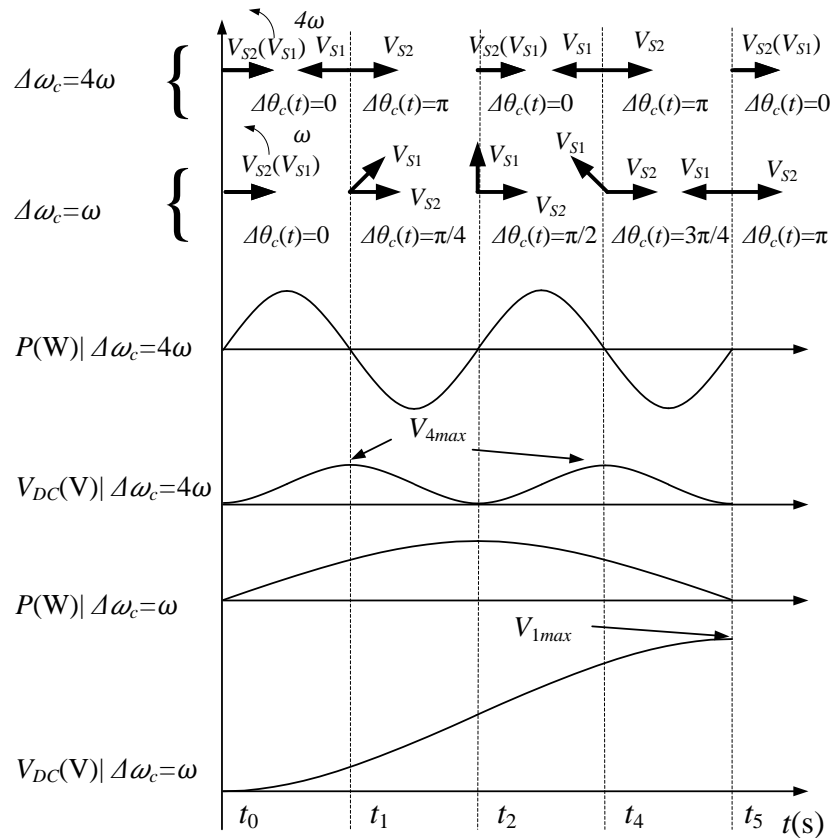


Fig. 6-14 Voltage phasor diagram, and the DC bus voltage which reflects the energy accumulated on the DC bus capacitors under carrier wave angular difference of 4ω and ω .

The energy stored in the DC bus capacitors from t_0 to t_1 (corresponding to the maximum dc bus voltage V_{4max}) is released from t_1 to t_2 for the case of $\Delta\omega_c = 4\omega$; while there is only charging process within $t_0 < t < t_5$ for the case of $\Delta\omega_c = \omega$. During this period, energy is only stored in the dc bus capacitors and cannot be released. Therefore, the corresponding maximum voltage V_{4max} at t_1 is lower than V_{1max} at t_5 . From (6.10) the maximum energy for the case of $\Delta\omega_c = 4\omega$ is one-fourth of that for the case of $\Delta\omega_c = \omega$. It can be concluded that introducing a higher carrier wave frequency difference will reduce the maximum accumulated energy on the dc bus, and therefore, can suppress the dc bus overvoltage.

Considering the previous example, which is shown in Section 6.1, the maximum dc bus voltage can be reduced to 360.38 V when the difference of the carrier wave frequencies is 0.1%. Although 0.1% is not an optimized selection, it is a trade-off between dc bus overvoltage suppressing and the influence on normal operation of the parallel inverters based on engineering experience. When the carrier waves have a frequency difference of 0.1%, the maximum dc bus overvoltage under no-load condition can be suppressed to an acceptable level, and this difference has no side-effect on the inverter normal operation. 360.38 V is very close to the normal dc bus voltage of 360 V, and it can be concluded that the dc bus overvoltage is eliminated.

The carrier wave frequency f_{ci} of module i can be decided by:

$$f_{ci} = \begin{cases} -(i-1) \cdot 0.1\% \cdot f_c / 2 + f_c & |i \text{ is odd} \\ i \cdot 0.1\% \cdot f_c / 2 + f_c & |i \text{ is even} \end{cases} \quad (6.17)$$

Since the maximum energy accumulated on the DC bus for N modules in parallel is at most twice that of the case of two modules by considering the worst case, this method is also effective for a multi-module system.

6.4 Experimental Results

Two modules are used to validate the proposed solution for the DC bus overvoltage issue firstly. The parameters of each module are the same as those given in Table 6-1. The per-phase output rms-voltage is 220 V, the controller of each module is implemented by a TMS320F2407 digital signal controller (DSC) from Texas Instruments. Before shifting the carrier wave frequency, the waveforms of the positive DC bus voltage of the two modules are shown in Fig. 6-4. As mentioned above, when M is 0.8639, the calculated maximum DC bus voltage is 394.5 V, which matches the data shown in Fig. 6-4. This DC bus overvoltage will cause instability issue.

By shifting the carrier wave frequency of module 2 based on (6.17), the DC bus overvoltage is eliminated. Fig. 6-15 shows the positive and negative DC bus voltages of module 1. This can be implemented by changing the corresponding PWM counter of the controller. After shifting the carrier wave frequency of module 2, the carrier wave frequency of module 1 is unchanged, while the carrier wave frequency of module 2 is 17.009 kHz.

When three modules are connected in parallel under no-load condition, the DC bus voltage of module 1 is shown in Fig. 6-16. The maximum DC bus voltage was over 400 V, and the overvoltage protection was eventually triggered to protect the DC bus capacitors.

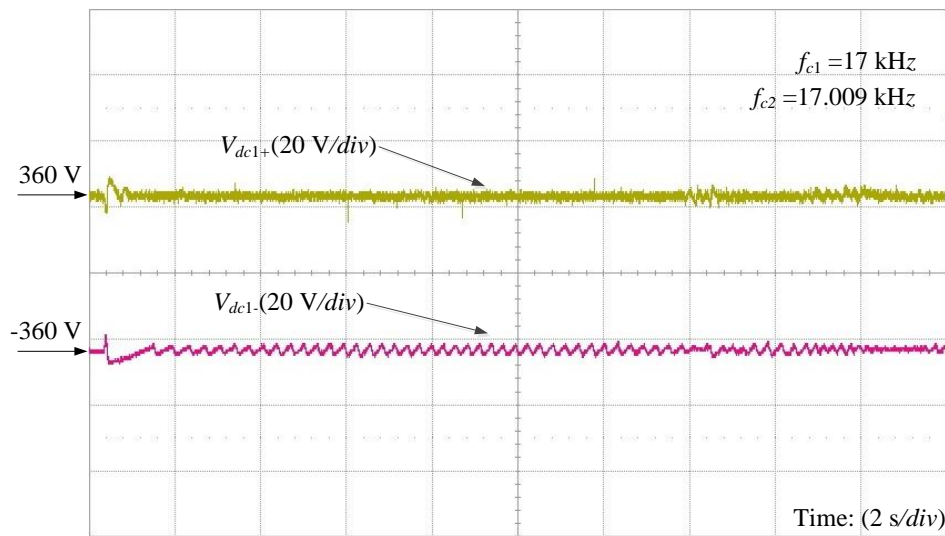


Fig. 6-15 Positive and negative DC bus voltages of module 1 under no-load condition when two modules are connected in parallel.

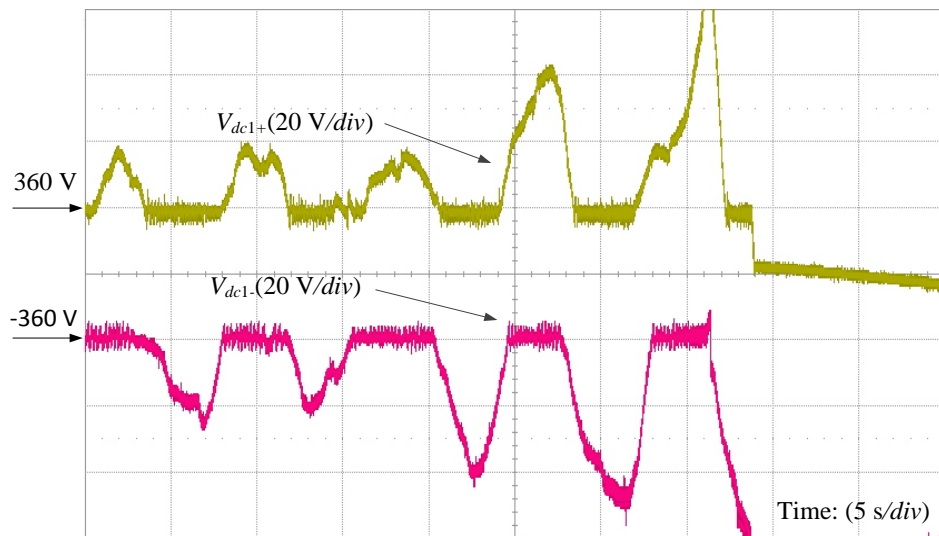


Fig. 6-16 Positive and negative DC bus voltages of module 1 under no-load condition when three modules are connected in parallel.

Frequencies of the carrier waves of module 2 and module 3 are shifted by $\pm 0.1\%$, and they are 17.009 kHz and 16.991 kHz respectively.

Fig. 6-17 shows the positive DC bus voltage of module 1 (V_{dc1+}) and the negative DC bus voltage of module 2 (V_{dc2-}) under no-load condition.

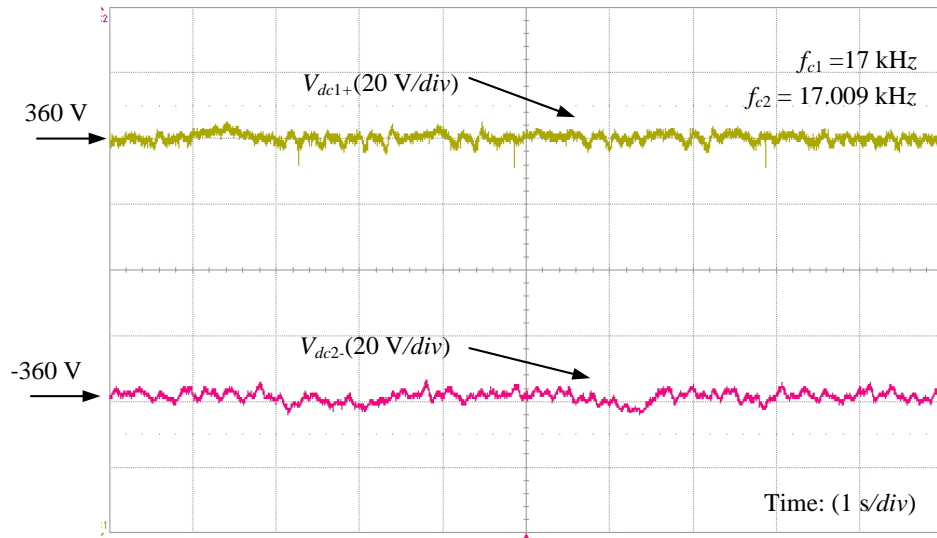


Fig. 6-17 Positive DC bus voltage of module 1 and negative DC bus voltage of module 2 after shifting the corresponding frequency of the carrier waves.

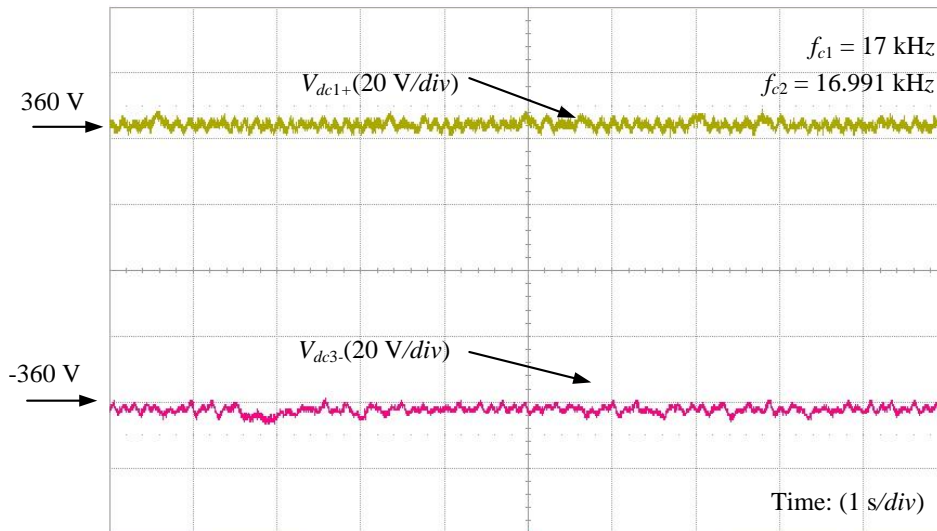


Fig. 6-18 Positive DC bus voltage of module 1 and negative DC bus voltage of module 3 after shifting the corresponding frequency of the carrier waves.

Fig. 6-18 shows the positive DC bus voltage of module 1 (V_{dc1+}) and the negative DC bus voltage of module 3 (V_{dc3-}) under no-load condition after the inverters are activated. It can be observed that DC bus voltages of all three modules are stable compared to that in Fig. 6-16 and there is no overvoltage.

Fig. 6-19 and Fig. 6-20 show the waveforms of two modules in parallel under non-linear load condition. I_{o1a} and V_{o1a} are the inductor current and output voltage of phase A of

module 1 respectively. It can be observed that a small controlled carrier wave frequency difference has negligible effect on the normal operation of the parallel modules.

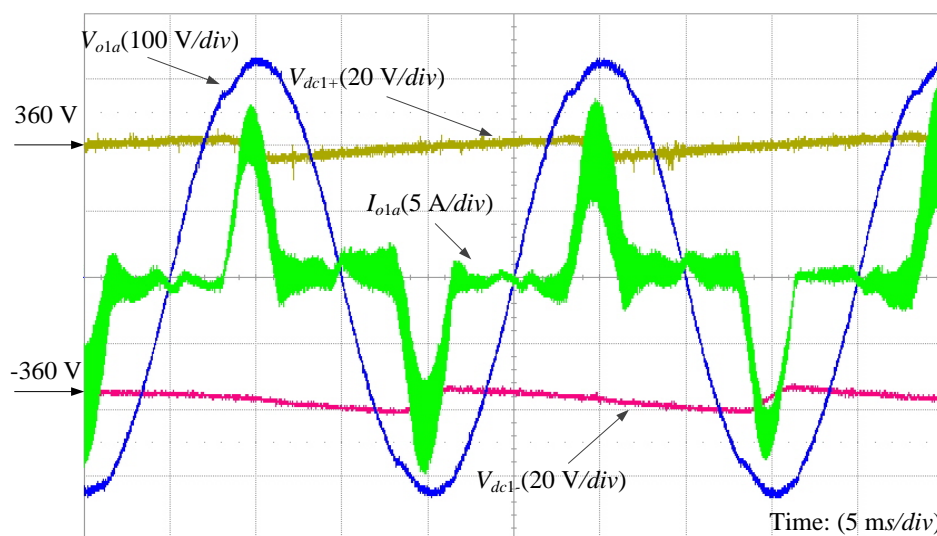


Fig. 6-19 DC bus voltage and inverter output voltage and current under non-linear load before shifting the carrier wave frequency.

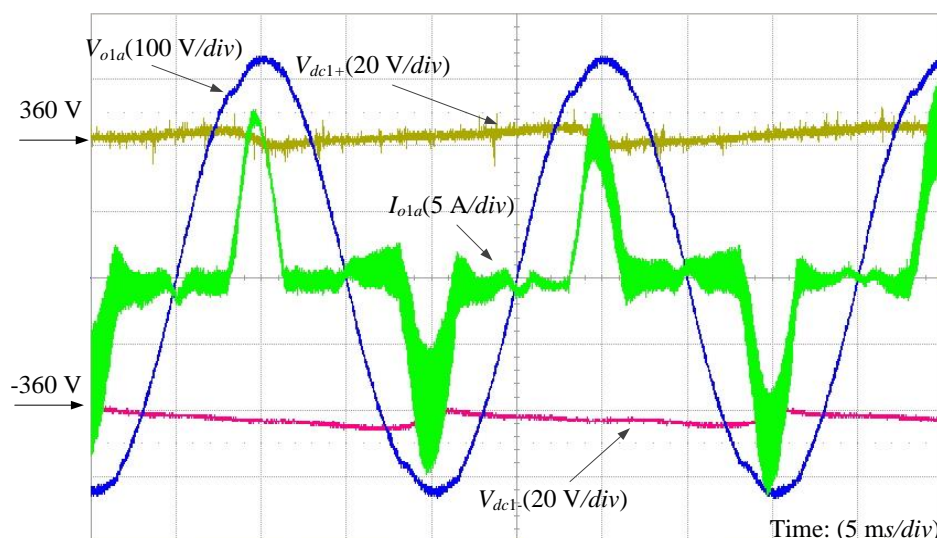


Fig. 6-20 DC bus voltage and inverter output voltage and current under non-linear load after shifting the carrier wave frequency.

6.5 Conclusion

The study in this chapter shows that active power can be circulated among parallel identical inverters and it has a significant impact on the operation of modularized DER converters such as MUPS modules and solar inverters. The energy accumulation in the modules can cause DC bus overvoltage if the DC input stage has only unidirectional

power flow capability. One module can therefore charge others at carrier wave frequency. The charged energy cannot be easily consumed under no-load condition. As a result, DC bus overvoltage is caused with energy accumulating on the DC bus capacitors. Active power at carrier wave frequency and its sideband harmonic components have been analyzed in this chapter. It has been found that the minute difference of the carrier wave frequencies among the supposedly identical inverters in parallel has a significant impact on the amount of energy accumulated on the DC bus capacitors of each module. A DC bus overvoltage suppression method for a two-module system has been proposed and subsequently extended to an N -module system. It has been proven that the maximum energy charged to one module of an N -module system is twice larger than that of a two-module system, when N approaches infinite. Small shift of carrier wave frequency can make the active power cycling faster among the modules and avoid the DC bus overvoltage. Experimental results show that the proposed method can suppress the DC bus overvoltage, and has no negative impact on the normal operation of the MUPS system.

Chapter 7 Hybrid Energy Storage System of Battery/Ultra-capacitor with Model Predictive Control

As it is discussed in Chapter 2, batteries are good energy sources, however they have limited charging / discharging cycles and current. Ultra-capacitors are good power sources, and they have much higher charging / discharging cycles and current. Thus, incorporating these two sources will achieve good system performance.

In a battery/ultra-capacitor hybrid system, batteries supply system energy and ultra-capacitors provide system power. Control strategies are proposed to reduce battery current stress and charging / discharging cycles to extend battery lifetime [119-121]. By adopting those methods, frequent charging/discharging of batteries by high current can be avoided. However, how to meet the energy demand under fluctuating loads is still in need for further investigations. To date, low pass filter (LPF) is popular for filtering transient power demand; and the output of the LPF is used as power reference for the batteries. The power reference of ultra-capacitors can be calculated by subtracting that of the batteries from the total power demand of the ESS. However, this method has a poor performance. Current stress of the batteries can be reduced but the charging/discharging cycles cannot be reduced significantly. Batteries may still be charged or discharged frequently. In this chapter, a hybrid system of batteries and ultra-capacitors will be introduced. It consists of two bidirectional DC/DC converters connecting batteries and ultra-capacitors to a common DC bus respectively. Model predictive control (MPC) is proposed to minimize battery current stress and reduce battery charging / discharging cycles. Simulation results verified the effectiveness of the proposed system.

7.1 Configuration and Control Strategy of the Proposed Battery/Ultra-capacitor Hybrid System

Fig. 7-1 shows the proposed hybrid system of batteries and ultra-capacitors incorporating with RES in built environment. Wind turbines and photovoltaic panels are connected to a common DC bus through AC/DC and DC/DC converters. Batteries and ultra-capacitors are connected to the DC bus by bidirectional DC/DC converters respectively.

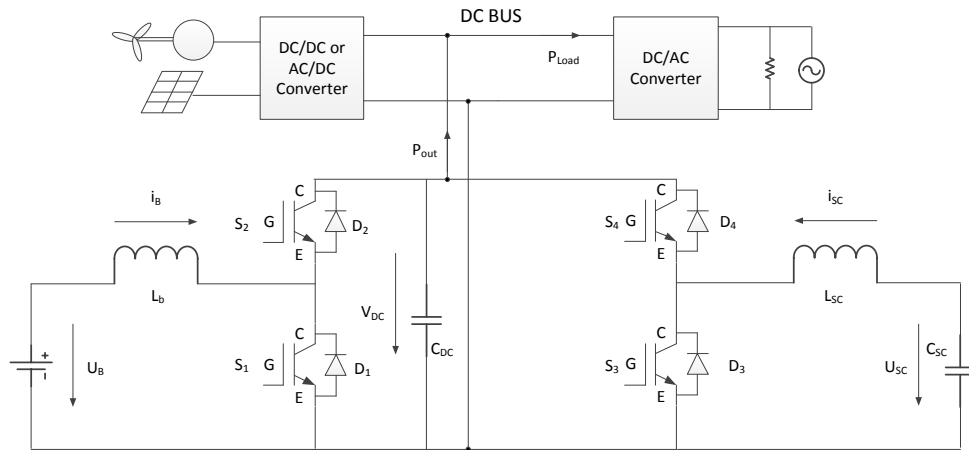


Fig. 7-1 Battery/ultra-capacitor hybrid system in renewable power generation

As shown in Fig. 7-1, when the DC bus charges batteries or ultra-capacitors, S_2 or S_4 works in switching mode and converter works in buck mode. When batteries or ultra-capacitors are discharged, S_1 or S_3 works in switching mode and converter works in boost mode. In this system, power consumed by load is not equal to the power generated by RES when MPPT is desired. In this case, ESS is integrated as an energy buffer, so that it can provide extra power when load requires more power than that can be generated by the RES, or store the excess power that cannot be consumed by the load. Inductor average current i_B and i_{SC} can be controlled and voltage of batteries/ultra-capacitors is a constant in a short duration. Therefore, output power of the battery/ultra-capacitor hybrid system can be controlled and the DC bus voltage can be maintained by regulating the inductor current. As mentioned above, the challenge for designing such a hybrid system is to let batteries have minimized current stress while maintain a constant DC bus voltage. So, load is supplied by rated voltage when the power generated by renewable power source is fluctuating and DC bus voltage remains as a constant.

In this chapter, model predictive control (MPC) shown in Fig. 7-2 is proposed to control the proposed hybrid system. MPC is ideal for setting constraints and optimizing. The proposed MPC can minimize battery current stress and maintain DC bus voltage as constant. System model and controller design of the proposed hybrid system will be introduced. Simulations in Matlab/Simulink verified the effectiveness of the proposed MPC and the battery/ultra-capacitor hybrid system.

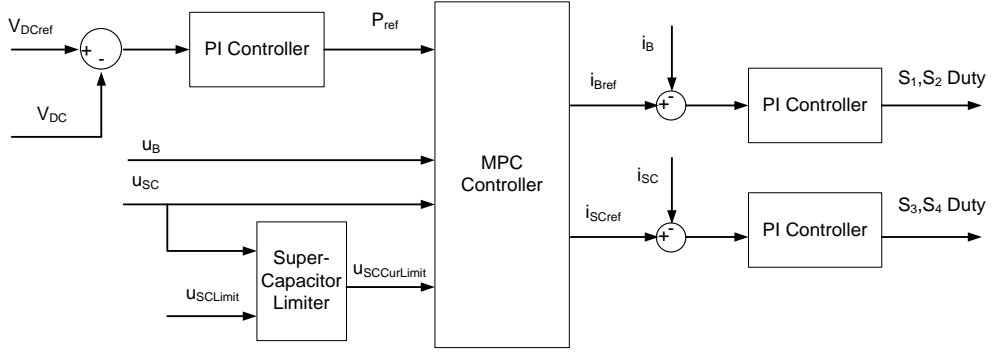


Fig. 7-2 MPC for battery / ultra-capacitor hybrid system

7.2 System Model and Controller Design

Since DC bus voltage only varies in a small range, it can be treated as a constant in dynamic analysis. System model can be expressed as (7.1) and (7.2).

$$C_{dc} \cdot \frac{dv_{dc}}{dt} = \frac{p_{out} - p_{in}}{v_{dc}} \quad (7.1)$$

$$p_{in} = U_B \cdot i_B + U_{SC} \cdot i_{SC} \quad (7.2)$$

Design objective of the MPC is to generate current reference for batteries and ultra-capacitors. Current control loops of batteries and ultra-capacitors are assumed to be well designed. PI controller is adopted for controlling battery/ultra-capacitor current to eliminate the steady-state error for a step reference and the PI controller is much faster than MPC controller. System model can be expressed in discrete state-space as (7.3).

$$\begin{cases} x(k+1) = \begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix} x(k) + \begin{bmatrix} U_B & U_{SC} \\ 0 & -\frac{T_s}{C_{dc}} \end{bmatrix} \cdot u(k) \\ y(k) = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot x(k) \end{cases}, \quad (7.3)$$

where $u(1)$ is the battery current, $u(2)$ is the ultra-capacitor current, $y(1)$ is the input power p_{in} , $y(2)$ is the ultra-capacitor voltage, and T_s is the sampling time of the MPC. System model should be updated at each sampling period since U_B and U_{SC} varies with time. The augmented model with integrator can be expressed:

$$\begin{aligned} \begin{bmatrix} \Delta x_m(k+1) \\ y(k+1) \end{bmatrix} &= A \cdot \begin{bmatrix} \Delta x_m(k) \\ y(k) \end{bmatrix} + B \cdot \Delta u(k) \\ y(k) &= C \cdot \begin{bmatrix} \Delta x_m(k) \\ y(k) \end{bmatrix} \end{aligned}, \quad (7.4)$$

where, matrices of A, B and C are defined in (7.5):

$$A = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \end{bmatrix}, B = \begin{bmatrix} u_b & u_{SC} \\ 0 & -\frac{T_s}{C_{DC}} \\ u_b & u_{SC} \\ 0 & -\frac{T_s}{C_{DC}} \end{bmatrix}, C = \begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \quad (7.5)$$

The solution of (7.4) is given in (7.6):

$$Y = K \cdot x(k_i) + \Phi \cdot \Delta u \quad (7.6)$$

where, K is defined by (7.7).

$$K = \begin{bmatrix} CA \\ CA^2 \\ \vdots \\ CA^{N_p} \end{bmatrix}, \Phi = \begin{bmatrix} CB & 0 & 0 & \dots & 0 \\ CAB & CB & 0 & \dots & 0 \\ \vdots & & & & \\ CA^{N_p-1}B & CA^{N_p-2}B & CA^{N_p-3}B & \dots & CA^{N_p-N_c}B \end{bmatrix}. \quad (7.7)$$

In this application, a PI controller is adopted to control the DC bus voltage. The output of the PI controller is used as the reference for MPC. MPC has two objectives. One is to track the power command of the DC bus. The other one is to minimize perturbation of the battery current. Cost function can be defined as:

$$J = \sum_{i=0}^{N_p-1} \left\{ \begin{aligned} &\left[y(k+i+1|k) - r(k+i+1) \right]^T \cdot Q \cdot \left[y(k+i+1|k) - r(k+i+1) \right] \\ &+ \Delta u(k+i|k)^T \cdot R_{\Delta u} \cdot \Delta u(k+i|k) \end{aligned} \right\} \quad (7.8)$$

where, $r(k)$ is the tracking trajectory.

Weight matrices Q and $R_{\Delta u}$ are given in (7.9).

$$Q = \begin{bmatrix} 0.01 & 0 \\ 0 & 0 \end{bmatrix}, R_{\Delta u} = \begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix} \quad (7.9)$$

$u(1)$ and $u(2)$ are currents of batteries and ultra-capacitors respectively, and $y(1)$ represents the output power. The output power error must be minimized while the voltage of ultra-capacitors may vary. Meanwhile, perturbation of battery current must be minimized, and thus $R_{\Delta u}$ is in the cost function.

MPC is good for setting constraints on manipulated or output variables. Two kinds of constraints are considered in this design. One is to limit the slope of the battery current, which is defined as k_B in A/s (ampere per second). This constraint is defined by (7.10). The other one is to maintain the ultra-capacitor voltage in a range, and this constraint can be expressed by (7.11). MPC problem can be converted to Quadratic Programming (QP) and solved after defining the weight matrix and constraints.

$$\begin{bmatrix} I_{N_C} \\ -I_{N_C} \end{bmatrix} \cdot \Delta U(1) \leq \begin{bmatrix} \varphi \cdot k_b \cdot Ts \\ \varphi \cdot k_b \cdot Ts \end{bmatrix}, \varphi = \underbrace{[1 \ 1 \ \dots \ 1]}_{N_C}^T \quad (7.10)$$

$$\begin{bmatrix} I_{N_P} \\ -I_{N_P} \end{bmatrix} \cdot \Delta Y(2) \leq \begin{bmatrix} \theta \cdot U_{curMax} \\ \theta \cdot U_{curMin} \end{bmatrix}, \theta = \underbrace{[1 \ 1 \ \dots \ 1]}_{N_P}^T \quad (7.11)$$

Voltage indicates state of charge (SOC) of ultra-capacitors. At any time, for any power demand and a particular battery current, energy stored in the ultra-capacitors should support the output power without a steep slope of battery current. These constrains can be expressed by (7.12).

$$\begin{cases} \frac{1}{2} \cdot C_{SC} \cdot U_{curMin}^2 \geq \frac{1}{2} \cdot C_{SC} \cdot U_{Min}^2 + \frac{(P_{Max} - i_B \cdot U_B)^2}{2 \cdot k_B \cdot i_B \cdot U_B} \\ \frac{1}{2} \cdot C_{SC} \cdot U_{curMax}^2 \leq \frac{1}{2} \cdot C_{SC} \cdot U_{Max}^2 - \frac{(P_{Min} - i_B \cdot U_B)^2}{2 \cdot k_B \cdot i_B \cdot U_B} \end{cases}, \quad (7.12)$$

Where U_{CurMax} and U_{CurMin} are the real-time voltage limitation of ultra-capacitors, U_{Max} and U_{Min} are the absolute voltage limitation of ultra-capacitors, P_{Max} and P_{Min} the maximum output power of the hybrid system. In this case, $P_{Min} = -P_{Max}$. To avoid violation, (7.13) must be valid.

$$\frac{1}{2} \cdot C_{SC} \cdot U_{curMax}^2 - \frac{1}{2} \cdot C_{SC} \cdot U_{curMin}^2 \geq 0, \quad (7.13)$$

By combining (7.12) and (7.13), (7.14) can be deduced.

$$\frac{1}{2} \cdot C_{SC} (U_{Max}^2 - U_{Min}^2) \geq \frac{P_{Max}^2 + i_B \cdot U_B^2}{k_B \cdot i_B \cdot U_B} \quad (7.14)$$

The minimum capacitance of the ultra-capacitors can be calculated by (7.14) and the absolute working range can be determined. Initially, the voltage of the ultra-capacitor can be calculated by:

$$U_{init}^2 = \frac{U_{max}^2 - U_{min}^2}{2}, U_{init} = \sqrt{\frac{U_{max}^2 + U_{min}^2}{2}} \quad (7.15)$$

Fig. 7-3 shows the run-time flow-chart of the proposed MPC. Firstly, MPC controller samples the voltage of batteries and ultra-capacitors, and then the linear model can be obtained. State variables are sampled and updated. As mentioned above, constraints of the voltage of ultra-capacitors are updated online. After that, the original problem can be converted to QP problem. (7.10) and (7.11) are used as constraints when solving the QP problem. After that, the control signal can be generated.

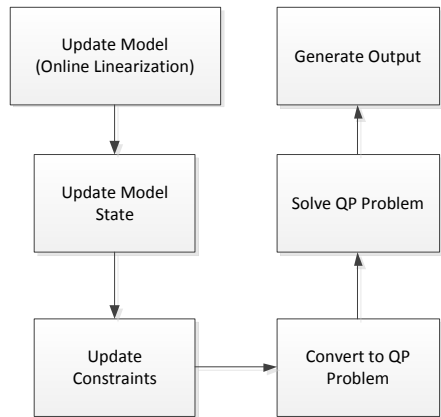


Fig. 7-3 Run-time flow-chart of the proposed MPC controller

7.3 Simulation Results

The proposed system and control method is verified by simulations using MATLAB/SIMULINK. The system configuration is shown in Fig. 7-4. Parameters are summarized in Table 7-1.

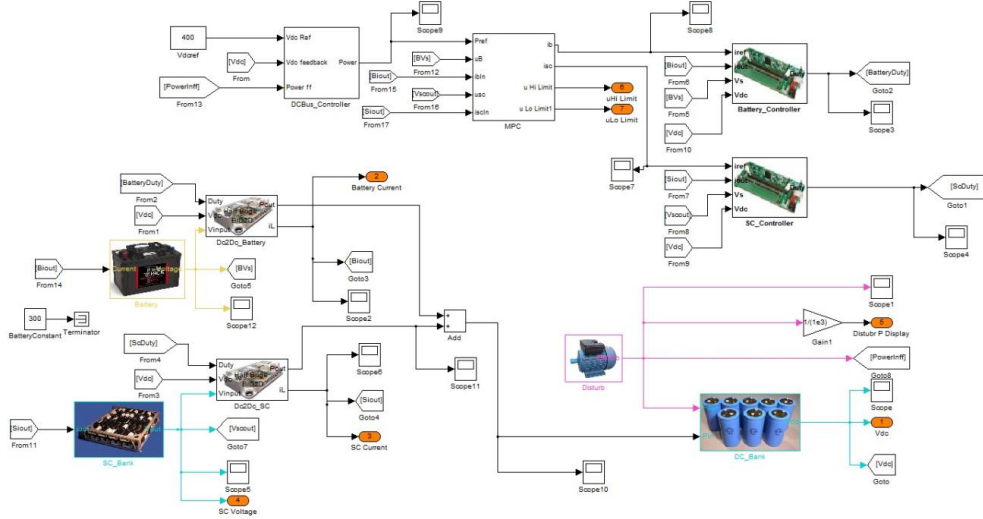


Fig. 7-4 SIMULINK blocks of the proposed battery ultra-capacitor hybrid system

Table 7-1 System parameters for simulation of the proposed hybrid system

Symbol	Description	Value
P_{max}	Maximum output power	100 kW
P_{Min}	Minimum output power	-100 kW
k_B	Maximum battery change rate	100 A/s
C_{dc}	Dc-Link Capacitance	0.47 F
V_{dcref}	Dc-Link reference voltage	400 V
L_B	Inductance of battery converter	10 mH
L_{SC}	Inductance of ultra-capacitor converter	1 mH
f_s	Converter switching frequency	10 kHz
C_{SC}	Capacitance of ultra-Capacitor	29.3 F
U_{SCinit}	Initial voltage of ultra -Capacitor	255 V
U_{SCMax}	Maximum voltage of ultra -Capacitor	300 V
U_{SCMin}	Minimum voltage of Ultra-capacitor	200 V
N_P	Prediction horizon	30
N_C	Control horizon	30

In this simulation setup, the power generated by RES and consumed by load is simplified as one disturbance, which equals to the output of the hybrid system. Fig. 7-5 and Fig. 7-6 show system dynamic response under step disturbance. At $t = 0$ s, system has a disturbance power of 100 kW, and at $t = 10$ s, the disturbance power jumps to -100kW. Fig. 7-5 shows current of battery and ultra-capacitor. Initially, batteries have no output

current, since ultra-capacitors support system output current. When MPC detects that the ultra-capacitors have a low SOC, and cannot support system current output, batteries bank start to work. Fig. 7-6 shows the voltage of the ultra-capacitors.

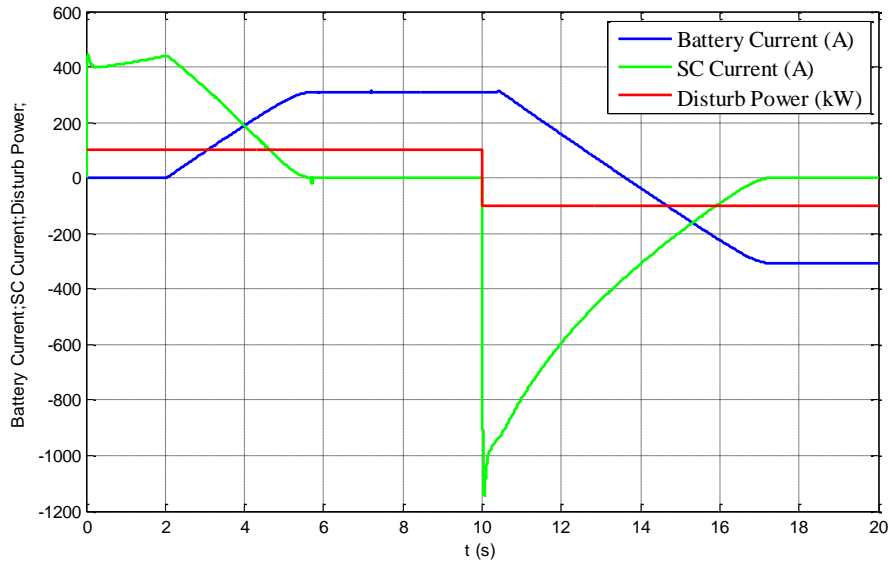


Fig. 7-5 Currents of batteries and ultra-capacitors under step disturbance.

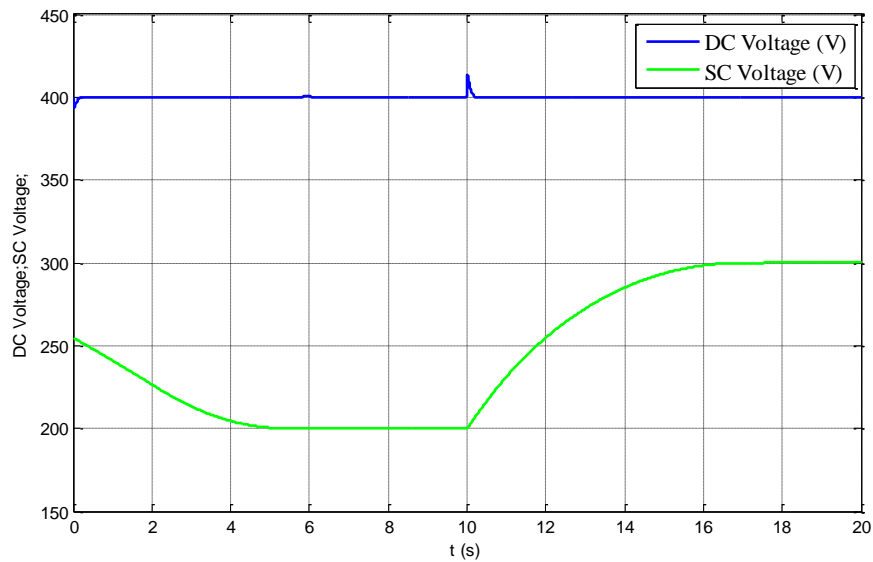


Fig. 7-6 Voltages of ultra-capacitors and DC bus under step disturbance.

At $t = 10$ s, when the output power disturbance changes to negative, the proposed ESS needs to absorb energy and battery current starts to decrease. However, batteries are still being discharged as long as its current is above zero. In this case, ultra-capacitors are

charged by batteries and the DC bus. Fig. 7-5 shows that ultra-capacitors have a high charging current. Fig. 7-6 shows that the voltages of ultra-capacitors increases when the power disturbance is negative. The charging current of ultra-capacitors decreases to zero eventually and its voltage reaches the up-limit. During this process, the DC bus voltage of the system is almost a constant.

Fig. 7-7 shows currents of batteries and ultra-capacitors under pulse disturbance, which has a period of 5 s and magnitude changing from 100 kW to -100kW. It can be observed that battery current has a minimized variation and batteries almost do not response to this pulse disturbance since ultra-capacitors are able to support system power demand. This simulation shows that the proposed MPC can avoid frequently charging/discharging of batteries under pulse disturbance. Because that lifetime of ultra-capacitors is less sensitive to charging and discharging cycles, it helps to extend the life time of batteries of the proposed ESS.

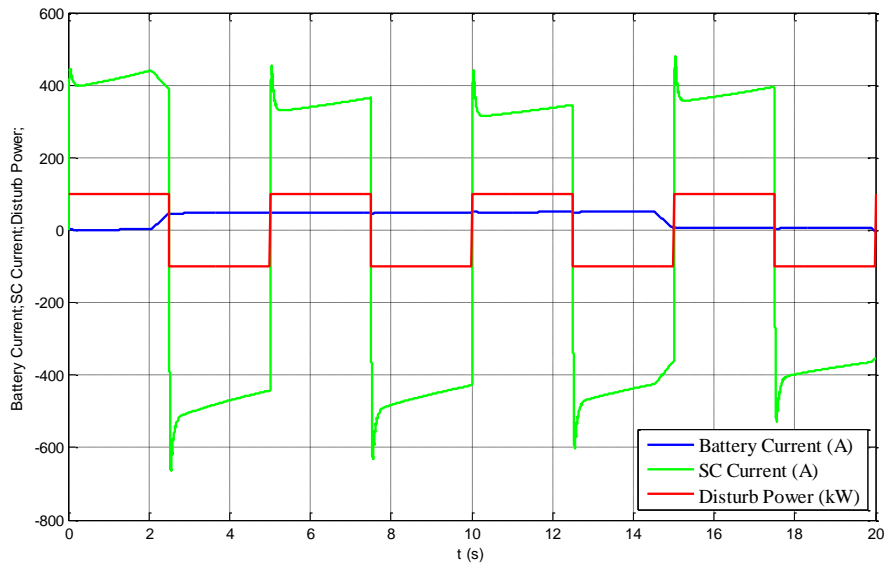


Fig. 7-7 Battery and ultra-capacitor currents under pulse disturbance.

Fig. 7-8 shows the voltages of the ultra-capacitors and the DC bus. It can be observed that the terminal voltage of the ultra-capacitors never exceeds its limitation and the DC bus voltage is almost a constant.

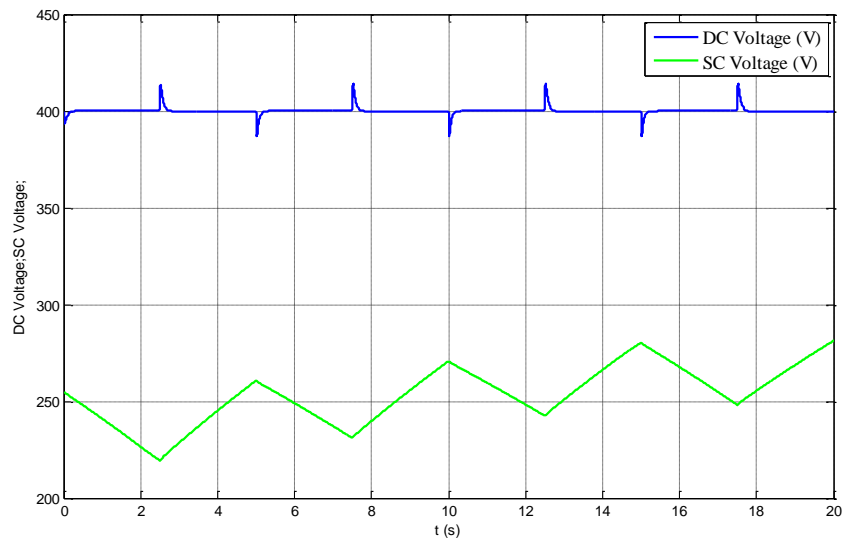


Fig. 7-8 Voltages of ultra-capacitor and DC bus under pulse disturbance.

Fig. 7-9 shows the system performance under random power disturbance, and Fig. 7-10 shows the voltages of ultra-capacitors and the DC bus. It can be observed that even under random disturbance, battery has low stress and minimized charging/discharging cycles. DC-link voltage is a constant.

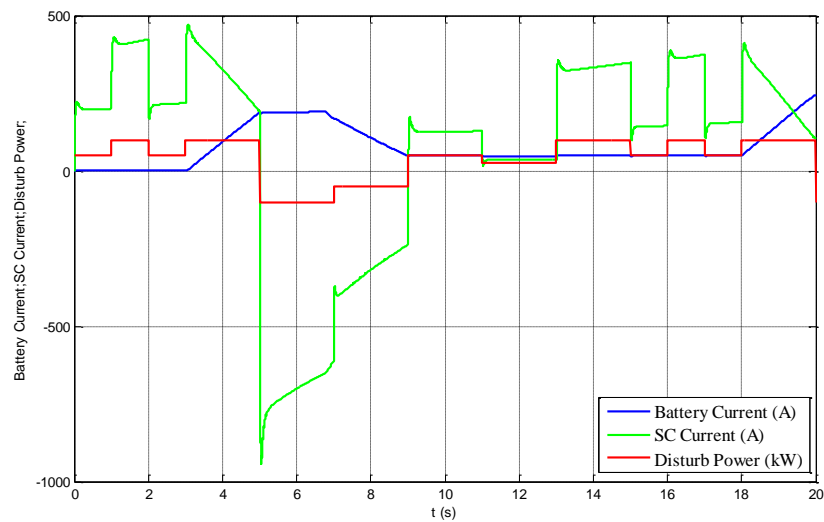


Fig. 7-9 Battery and ultra-capacitor currents under random disturbance.

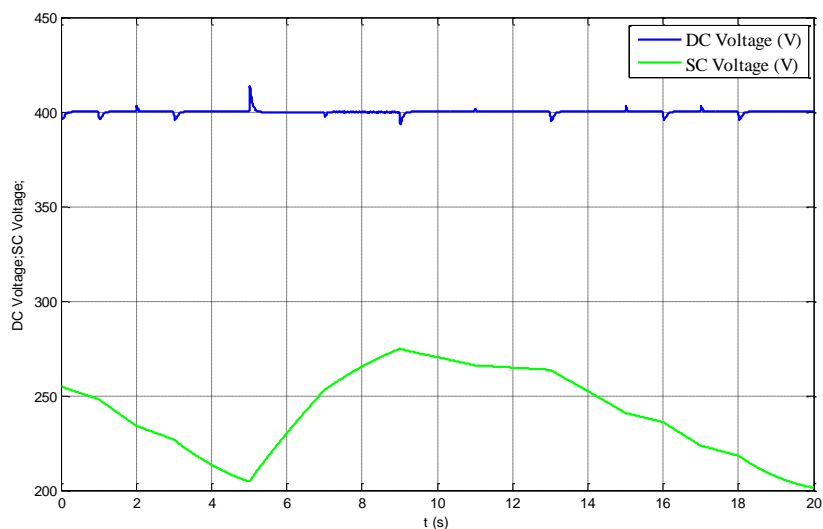


Fig. 7-10 Voltages of ultra-capacitor and DC-link under random disturbance power.

7.4 Conclusion

In this chapter, a hybrid ESS consisting of batteries and ultra-capacitors is introduced. The proposed ESS uses two bidirectional DC/DC converters to connect batteries and ultra-capacitors to a common DC bus. MPC is introduced and designed to generate current reference for batteries and ultra-capacitors respectively. Simulations results in Matlab/Simulink show that the proposed MPC controller can limit the current variation and minimize the current stress of batteries. Thus, the proposed battery/ultra-capacitor hybrid ESS has excellent system performance.

Chapter 8 Conclusions and Recommendations

8.1 Conclusions

This thesis begins with introducing system configuration of energy storage system (ESS) in the built environment. ESS can be connected to the AC power grid of buildings by power electronics converters to protect critical load to overcome energy fluctuation of renewable power generation and to shave peak load in moments of high electricity tariffs. Various energy storage devices are reviewed and comparisons are given for applications in buildings. Battery and ultra-capacitor are superior regarding bidirectional power flow capability and cost. However, single battery or ultra-capacitor cell has only a low terminal voltage. Many ESD cells may be connected in series to provide sufficient terminal voltage, and a cascaded VSI is connected to interface to the AC power grid. However, due to varying chemical and electrical characteristics, there is the unbalancing issue, which may limit ESD cell utilization. Chapter 3 introduced battery cell equalizers to balance series-connected ESD cells and proposed a current-fed charge-type BCE with continuous charging current for fast-equalizing application. Different types of BCE are compared, and charge-type BCE is considered to be better than other types in terms of equalizing speed. Compared to conventional BCEs, the proposed charge-type BCE can shorten equalizing time due to continuous output current and higher power rating. Furthermore, the proposed BCE requires fewer components. System cost and complexity is thus reduced.

Another way to integrate ESS to the main AC power grid in buildings is to use converters with high boost ratio to avoid connecting many ESD cells in series. Dual active bridge (DAB) converter can interface low voltage ESDs to a high voltage DC bus and a cascaded VSI connects the DC bus to the main AC power grid. DAB has features of simple structure and soft switching characteristics, however conventional control method causes high circulating current. In Chapter 4, a hybrid control method of phase shift and PWM (HPSP) is proposed to eliminate circulating current. The proposed control method has smaller auxiliary inductor and lower rms current for the same power rating comparing to TPS and DPS. It also has soft switching feature. A novel bidirectional DC/AC converter is proposed in Chapter 5. Compared to the solution of DAB+VSI, bulky DC capacitors can be avoided and less current sensor is required. The proposed topology is

suitable for ESS with wide terminal voltage variation. Simulation results and hardware experiment verified the effectiveness of the proposed circuitry as well as the modulation and control method.

Modularized design is attractive for ESS. Modularized uninterruptible power supply (MUPS) is commonly used in industry and buildings. The study in Chapter 6 shows that active power can be circulated among paralleled inverters of MUPS. Active power circulating at carrier wave frequency and its sideband harmonic components are analyzed. It has been found that the minute difference of the carrier wave frequencies caused energy accumulation on the DC bus capacitors of MUPS. A DC bus overvoltage suppression method for a two-module system has been proposed and subsequently extended to an N -module system. Small shift of carrier wave frequency can make the active power cycling faster among the modules and the DC bus overvoltage can thus be avoided. Experimental results show that the proposed method can suppress the DC bus overvoltage, and has no negative impact on the normal operation of MUPS systems.

In Chapter 7, a hybrid ESS consisting of batteries and ultra-capacitors was proposed. The hybrid system uses two bidirectional DC/DC converters to connect batteries and ultra-capacitors to a common DC bus respectively. It can be tied to DC power grid directly or AC power grid through inverters. Design of model predictive control (MPC) for controlling the power dispatch of batteries and ultra-capacitors is introduced. Simulations results in Matlab/Simulink show that the proposed MPC controller can limit the current variation and minimize the current stress of batteries. Thus, the proposed hybrid ESS has better system performance.

8.2 Recommendations for Future Research

Materials on topology, modulation and control of power electronics converters and system control strategy of integration of ESS to main AC power grid in built environment are presented in this thesis. This research mainly focuses on developing technologies for interfacing ESS to AC grid in built environment, which is more for low voltage and small scale system. Large scale energy storage systems are more likely to be installed at medium voltage side (1 – 35 kV). There are a lot of challenges to be explored and solved for medium-voltage ESS applications. Furthermore, these technologies developed in this thesis are not limited for the applications discussed in this thesis. They can be applied for

many other applications. This section briefly discusses these challenges and provides insights for future investigation.

Large scale energy storage systems can be integrated with large wind farm or solar plant. The integration of ESS can smooth the fluctuant power generated by wind turbines or PV panels and provide high quality power supply with higher reliability. Furthermore, ESS may provide a solution for the requirement of low-voltage-ride-through for wind power generation. A centralized ESS may be installed at medium-voltage side. It is still a challenge to design power electronics converters for medium voltage application because of the limitation of power devices. The maximum break-down voltage for IGBT modules can be found in the market is 6.5 kV. Thus, multi-level converters can be a candidate for this application. Cascaded H-bridge (CHB) shown in Fig. 8-1 [152],[153] has advantages of simple structure and less components. Modular design can improve system reliability and availability. Any fault module can be bypassed without shutting down the whole system. The hybrid system of battery and ultra-capacitor proposed in Chapter 7 can be integrated with single power cell of CHB to provide better system performance.

Furthermore, multi-level converters can be candidate for low voltage ESS. Each level can be implemented by a single ESD cell or ESD cells in parallel, and then battery-cell-equalizer can be avoided. These converters can be used for DC or AC grid. The challenge of designing multi-level converters is to dispatch power equally among all ESD cells and maintain their SOC in balance.

Solid state transformer (it is also called power electronic transformer) attracts much attention for its application in the distribution system[154]. This technology utilizes power electronics devices and high frequency transformer to replace the conventional 50/60 Hz power transformer in AC-AC conversion application. Since solid state transformer works at high frequency, the transformer volume can be much smaller than conventional 50/60 Hz power transformer. Dual active bridge and the associated control method developed in this thesis could be applied to solid state transformer to improve energy conversion efficiency.

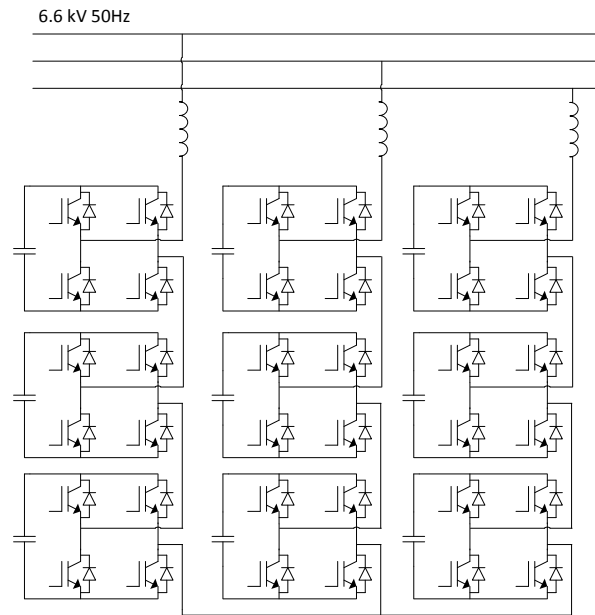


Fig. 8-1 Cascaded H-bridge converter for medium voltage application.

In this thesis, MPC is proposed to control the hybrid system of battery and ultra-capacitor. However, hardware implementation of MPC is still a challenge. MPC requires a large amount of matrix calculation, which consumes a lot of computational resources and is time-consuming. Power electronics converters require real-time control but MPC currently may not be qualified for real-time control. How to simplify MPC algorithm and implement it for real-time control efficiently is still a challenge.

Author's Publications

- [1] Xiaolei Hu and K. J. Tseng. "Integration of Multiple Modularized Distributed Energy Resource Devices into AC Grid of Buildings: Issue of Active Power Circulation", *IEEE Trans. Ind. Electron.*, vol.61, no.11, pp. 6188-6127, 2014.
- [2] Xiaolei Hu, K. J. Tseng, and M. Srinivasan. "Optimization of Battery Energy Storage System with Ultra-capacitor for Renewable Energy Applications." *In Proc. ICPE (ISPE)*, 2011, pp. 1552-1557. *Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on*, 2011, pp. 1552-1557.
- [3] Xiaolei Hu, K. J. Tseng, S. Yin, R. Tjandra, and T. Wang. "Elimination of reactive power in dual active bridge by hybrid of phase shift and PWM control." *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, 2013, pp. 4985-4990.
- [4] Xiaolei Hu, K. J. Tseng, Y. Liu, S. Yin, and M. Zhang. "A high frequency isolated current-fed bidirectional DC/AC converter for grid-tied energy storage system." *in ECCE Asia Downunder (ECCE Asia), 2013 IEEE, 2013*, pp. 291-296.

Bibliography

- [1] M. A. Abusara, J. M. Guerrero, and S. M. Sharkh, "Line-Interactive Ups for Microgrids," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1292-1300, Mar. 2014.
- [2] Q. Jiang, Y. Gong, and H. Wang, "A Battery Energy Storage System Dual-Layer Control Strategy for Mitigating Wind Farm Fluctuations," *IEEE Trans. Power Syst.*, vol. 28, no. 3, pp. 3263-3273, Aug. 2013.
- [3] A. Lahyani, P. Venet, A. Guermazi, and A. Troudi, "Battery/Supercapacitors Combination in Uninterruptible Power Supply (Ups)," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1509-1522, Apr. 2013.
- [4] D. Velasco de la Fuente, C. L. T. Rodriguez, G. Garcera, E. Figueres, and R. O. Gonzalez, "Photovoltaic Power System with Battery Backup with Grid-Connection and Islanded Operation Capabilities," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1571-1581, Apr. 2013.
- [5] J. Tant, F. Geth, D. Six, P. Tant, and J. Driesen, "Multiobjective Battery Storage to Improve Pv Integration in Residential Distribution Grids," *IEEE Trans. Sustainable Energy*, vol. 4, no. 1, pp. 182-191, Jan. 2013.
- [6] M. C. Kisacikoglu, B. Ozpineci, and L. M. Tolbert, "Ev/Phev Bidirectional Charger Assessment for V2g Reactive Power Operation," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5717-5727, Dec. 2013.
- [7] M. Yilmaz and P. T. Krein, "Review of the Impact of Vehicle-to-Grid Technologies on Distribution Systems and Utility Interfaces," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5673-5689, Dec. 2013.
- [8] B. Mary and S. Goran, "Value of Bulk Energy Storage for Managing Wind Power Fluctuations," *IEEE Trans. Energy Convers.*, vol. 22, no. 1, pp. 197-205, Mar. 2007.
- [9] K. Agbossou, M. Kolhe, J. Hamelin, and T. K. Bose, "Performance of a Stand-Alone Renewable Energy System Based on Energy Storage as Hydrogen," *IEEE Trans. Energy Convers.*, vol. 19, no. 3, pp. 633-640, Sep. 2004.
- [10] J. P. Barton and D. G. Infield, "Energy Storage and Its Use with Intermittent Renewable Energy," *IEEE Trans. Energy Convers.*, vol. 19, no. 2, pp. 441-448, Jun. 2004.

- [11] J. M. Gurrero, L. Garc ía de Vicuña, and J. Uceda, "Uninterruptible Power Supply Systems Provide Protection," *IEEE Ind. Electr. Mag.*, vol. 1, no. 1, pp. 28-38, Jan. 2007.
- [12] Y. Chen, D. K.-W. Cheng, and Y.-S. Lee, "A Hot-Swap Solution for Paralleled Power Modules by Using Current-Sharing Interface Circuits," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1564-1571, Nov. 2006.
- [13] T.-F. Wu, H.-M. Hsieh, Y.-E. Wu, and Y.-K. Chen, "Parallel-Inverter System with Failure Isolation and Hot-Swap Features," *IEEE Trans. Ind. Appl.*, vol. 43, no. 5, pp. 1329-1340, Sep./Oct. 2007.
- [14] J. M. Guerrero, L. Hang, and J. Uceda, "Control of Distributed Uninterruptible Power Supply Systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 2845-2859, Aug. 2008.
- [15] P. F. Ribeiro, B. K. Johnson, M. L. Crow, A. Arsoy, and Y. Liu, "Energy Storage Systems for Advanced Power Applications," *Proceedings of the IEEE*, vol. 89, no. 12, pp. 1744-1756, 2001.
- [16] U. Koehler, F. J. Kruger, J. Kuempers, M. Maul, E. Niggemann, and H. H. Schoenfelder, "High Performance Nickel-Metal Hydride and Lithium-Ion Batteries," in *1997 IECEC-97. Proceedings of the 32nd Intersociety Energy Conversion Engineering Conference*, pp. 93-98 vol.1.
- [17] F. Krismer and J. W. Kolar, "Accurate Power Loss Model Derivation of a High-Current Dual Active Bridge Converter for an Automotive Application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 881-891, Mar. 2010.
- [18] F. Krismer and J. W. Kolar, "Closed Form Solution for Minimum Conduction Loss Modulation of Dab Converters," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 174-188, Jan. 2012.
- [19] H. Bai, Z. Nie, and C. C. Mi, "Experimental Comparison of Traditional Phase-Shift, Dual-Phase-Shift, and Model-Based Control of Isolated Bidirectional Dc/Dc Converters," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1444-1449, Jun. 2010.
- [20] G. G. Oggier, G. O. Garcia, and A. R. Oliva, "Modulation Strategy to Operate the Dual Active Bridge Dc-Dc Converter under Soft Switching in the Whole Operating Range," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1228-1236, Apr. 2011.

- [21] B. Zhao, Q. Song, and W. Liu, "Power Characterization of Isolated Bidirectional Dual-Active-Bridge Dc-Dc Converter with Dual-Phase-Shift Control," *IEEE Trans. Power Electron.*, vol. 27, no. 9, pp. 4172-4176, Sep. 2012.
- [22] A. K. Jain and R. Ayyanar, "Pwm Control of Dual Active Bridge: Comprehensive Analysis and Experimental Verification," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1215-1227, Apr. 2011.
- [23] *Electricity Storage: Location, Location, Location ... And Cost*. Available: http://www.eia.gov/todayinenergy/detail.cfm?id=6910#tabs_ElecStorage-5
- [24] *Battery Energy Storage System (Bess)*. Available: <http://www.gvea.com/energy/bess>
- [25] *Electricity End Use, 1949 - 2012*. Available: <http://www.eia.gov/totalenergy/data/browser/xls.cfm?tbl=T07.06>
- [26] *Annual Energy Outlook 2014 with Projections to 2040*. Available: [http://www.eia.gov/forecasts/aeo/pdf/0383\(2014\).pdf](http://www.eia.gov/forecasts/aeo/pdf/0383(2014).pdf)
- [27] *Microgrid Definitions*. Available: <http://building-microgrid.lbl.gov/microgrid-definitions>
- [28] *What Is a Microgrid*. Available: <http://austinspc.com/2011/04/10/what-is-a-microgrid/>
- [29] *Table 10. Supply and Disposition of Electricity, 1990-2012 (Million Kilowatthours)*. Available: <http://www.eia.gov/electricity/state/unitedstates/xls/sept10us.xls>
- [30] *Electricity Storage Technologies Can Be Used for Energy Management and Power Quality*. Available: <http://www.eia.gov/todayinenergy/detail.cfm?id=4310>
- [31] *International Power First Hydro, Uk*. Available: http://www.fhc.co.uk/pumped_storage.htm
- [32] *Compressed Air Energy Storage*. Available: <http://caes.pnnl.gov/>
- [33] *Investing in Renewable Energy*. Available: http://www.xcelenergy.com/staticfiles/xcel/Corporate/Renewable%20Energy%20Grants/Project_Fact_Sheet-SodiumSulfurBattery_RDF.pdf
- [34] R. B. Schainker, "Executive Overview: Energy Storage Options for a Sustainable Energy Future," in *Power Engineering Society General Meeting, 2004. IEEE*, pp. 2309-2314 Vol.2.
- [35] *Electric Storage Association*. Available: <http://www.electricitystorage.org>

- [36] P. Van den Bossche, F. Vergels, J. Van Mierlo, J. Matheys, and W. Van Autenboer, "Subat: An Assessment of Sustainable Battery Technology," *Journal of Power Sources*, vol. 162, no. 2, pp. 913-919, 11/22/ 2006.
- [37] *Maxwell Ultracapacitors*. Available: <http://www.maxwell.com/ultracapacitors/>
- [38] *Powerthru Clean Flywheel Energy Storage*. Available: http://www.powerthru.com/flywheel_detail.html
- [39] F. J. M. Thoolen, "Development of an Advanced High Speed Flywheel Energy Storage System," Ph.D. Thesis, Technische Universiteit Eindhoven, 1993.
- [40] N. T. Duy, "Dual Air-Gap Axial Flux Permanent Magnet Machines for Flywheel Energy Storage Systems," Ph.D. Thesis, Nanyang Technological University, 2012.
- [41] *Energy Storage Association*. Available: <http://energystorage.org/>
- [42] J. P. Torreglosa, P. Garcia, L. M. Fernandez, and F. Jurado, "Predictive Control for the Energy Management of a Fuel-Cell-Battery-Supercapacitor Tramway," *Industrial Informatics, IEEE Transactions on*, vol. 10, no. 1, pp. 276-285, Feb. 2014.
- [43] A. M. O. Haruni, M. Negnevitsky, M. E. Haque, and A. Gargoom, "A Novel Operation and Control Strategy for a Standalone Hybrid Renewable Power System," *IEEE Trans. Sustainable Energy*, vol. 4, no. 2, pp. 402-413, Apr. 2013.
- [44] B. Zahedi and L. E. Norum, "Modeling and Simulation of All-Electric Ships with Low-Voltage Dc Hybrid Power Systems," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4525-4537, Oct. 2013.
- [45] S. K. Nayak and D. N. Gaonkar, "Modeling and Performance Analysis of Hybrid Fuel Cell and Microturbine Based Distributed Generation System, "a Review", " in *Power, Energy and Control (ICPEC), 2013 International Conference on*, pp. 760-766.
- [46] P. Thounthong, A. Luksanasakul, P. Koseeyaporn, and B. Davat, "Intelligent Model-Based Control of a Standalone Photovoltaic/Fuel Cell Power Plant with Supercapacitor Energy Storage," *IEEE Trans. Sustainable Energy*, vol. 4, no. 1, pp. 240-249, 2013.
- [47] R. K. Pachauri and Y. K. Chauhan, "Hybrid Pv/Fc Stand Alone Green Power Generation: A Perspective for Indian Rural Telecommunication Systems," in *Issues and Challenges in Intelligent Computing Techniques (ICICT), 2014 International Conference on*, pp. 802-810.

- [48] A. Benrabeh, F. Khoucha, O. Herizi, M. E. H. Benbouzid, and A. Kheloui, "Fc/Battery Power Management for Electric Vehicle Based Interleaved Dc-Dc Boost Converter Topology," in *2013. 15th European Conference on Power Electronics and Applications (EPE)*, pp. 1-9.
- [49] M. Magno, D. Boyle, D. Brunelli, B. O'Flynn, E. Popovici, and L. Benini, "Extended Wireless Monitoring through Intelligent Hybrid Energy Supply," *IEEE Trans. Ind. Electron.*, vol. 61, no. 4, pp. 1871-1881, Apr. 2014.
- [50] S. Patrabansh, M. Y. El-Sharkh, and M. Alam, "Dynamic Modeling and Simulation of a Dmfc/Uc Based Hybrid Vehicular System," in *Industry Applications Society Annual Meeting, 2013 IEEE*, pp. 1-10.
- [51] L. Valverde, F. Rosa, and C. Bordons, "Design, Planning and Management of a Hydrogen-Based Microgrid," *Industrial Informatics, IEEE Transactions on*, vol. 9, no. 3, pp. 1398-1404, 2013.
- [52] B. S. Sami, B. C. Abderrahmen, and C. Adnane, "Design and Dynamic Modeling of a Fuel Cell/Ultra Capacitor Hybrid Power System," in *Electrical Engineering and Software Applications (ICEESA), 2013 International Conference on*, pp. 1-7.
- [53] S. N. Motapon, L.-A. Dessaint, and K. Al-Haddad, "A Comparative Study of Energy Management Schemes for a Fuel-Cell Hybrid Emergency Power System of More-Electric Aircraft," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1320-1334, Mar. 2014.
- [54] V. Valdivia, A. Barrado, A. Lazaro, M. Sanz, D. Lopez del Moral, and C. Raga, "Black-Box Behavioral Modeling and Identification of Dc-Dc Converters with Input Current Control for Fuel Cell Power Conditioning," *IEEE Trans. Ind. Electron.*, vol. 61, no. 4, pp. 1891-1903, Apr. 2014.
- [55] *U.S Department of Energy*. Available: <http://energy.gov/eere/fuelcells/fuel-cells>
- [56] "Types of Fuel Cells, Department of Energy,."
- [57] A. I. H. Ibrahim, and J. Perron, "Energy Storage Systems-Characteristics and Comparisons," *Renewable and Sustainable Energy Reviews*, vol. 12, no. 5, pp. 1121-1250, 2008.
- [58] *Regenerative Fuel Cells for Energy Storage*. Available: https://www1.eere.energy.gov/hydrogenandfuelcells/pdfs/rev_fc_wkshp_mittelsteadt.pdf

- [59] H.-S. Kim, K.-B. Park, S.-H. Park, G.-W. Moon, and M.-J. Youn, "A New Two-Switch Flyback Battery Equalizer with Low Voltage Stress on the Switches," in *2009. IEEE Energy Conversion Congress and Exposition*, pp. 511-516.
- [60] A. G. Xu, S. J. Xie, and X. B. Liu, "Dynamic Voltage Equalization for Series-Connected Ultracapacitors in Ev/Hev Applications," *Trans. Veh. Technol.*, vol. 58, no. 8, pp. 3981-3987, 2009.
- [61] C. H. Kim, M. Y. Kim, and G. W. Moon, "A Modularized Charge Equalizer Using a Battery Monitoring Ic for Series-Connected Li-Ion Battery Strings in Electric Vehicles," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3779-3787, 2013.
- [62] K. Chol-Ho, K. Moon-Young, P. Hong-Sun, and M. Gun-Woo, "A Modularized Two-Stage Charge Equalizer with Cell Selection Switches for Series-Connected Lithium-Ion Battery String in an Hev," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3764-3774, Aug. 2012.
- [63] M. Tang and T. Stuart, "Selective Buck-Boost Equalizer for Series Battery Packs," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 36, no. 1, pp. 201-211, Jan 2000.
- [64] T. Gottwald, Z. Ye, and T. Stuart, "Equalization of Ev and Hev Batteries with a Ramp Converter," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 33, no. 1, pp. 307-312, Jan 1997.
- [65] H.-S. Park, C.-H. Kim, K.-B. Park, G.-W. Moon, and J.-H. Lee, "Design of a Charge Equalizer Based on Battery Modularization," *Trans. Veh. Technol.*, vol. 58, no. 7, pp. 3216-3223, Sep. 2009.
- [66] H. Sakamoto, K. Murata, K. Nishijima, K. Harada, S. Taniguchi, K. Yamasaki, and G. Ariyoshi, "Balanced Charging of Series Connected Battery Cells," in *Telecommunications Energy Conference, 1998. INTELEC. Twentieth International*, pp. 311-315.
- [67] N. H. Kutkut, H. L. N. Wiegman, D. M. Divan, and D. W. Novotny, "Design Considerations for Charge Equalization of an Electric Vehicle Battery System," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 28-35, Jan./Feb. 1999.
- [68] P. Hong-Sun, K. Chong-Eun, K. Chol-Ho, M. Gun-Woo, and L. Joong-Hui, "A Modularized Charge Equalizer for an Hev Lithium-Ion Battery String," *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1464-1476, May. 2009.
- [69] Y.-S. Lee and G.-T. Cheng, "Quasi-Resonant Zero-Current-Switching Bidirectional Converter for Battery Equalization Applications," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1213-1224, Sep. 2006.

- [70] Y.-S. Lee and M.-W. Cheng, "Intelligent Control Battery Equalization for Series Connected Lithium-Ion Battery Strings," *IEEE Trans. Ind. Electron.*, vol. 52, no. 5, pp. 1297-1307, Oct. 2005.
- [71] S. Yarlagadda, T. T. Hartley, and I. Husain, "A Battery Management System Using an Active Charge Equalization Technique Based on a Dc/Dc Converter Topology," presented at the 2011 IEEE Energy Conversion Congress and Exposition (ECCE), 2011.
- [72] M.-Y. Kim, J.-W. Kim, C.-H. Kim, S.-Y. Cho, and G.-W. Moon, "Automatic Charge Equalization Circuit Based on Regulated Voltage Source for Series Connected Lithium-Ion Batteries," in *2011 IEEE 8th International Conference on Power Electronics and ECCE Asia (ICPE & ECCE)*, pp. 2248-2255.
- [73] S. H. Park, K. B. Park, H. S. Kim, G. W. Moon, and M. J. Youn, "Single-Magnetic Cell-to-Cell Charge Equalization Converter with Reduced Number of Transformer Windings," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2900-2911, Jun. 2012.
- [74] H.-S. Park, C.-E. Kim, G.-W. Moon, J.-H. Lee, and J. K. Oh, "Charge Equalization with Series Coupling of Multiple Primary Windings for Hybrid Electric Vehicle Li-Ion Battery System," in *2007 IEEE Power Electronics Specialists Conference*, pp. 266-272.
- [75] Z. Zhang and S. Cuk, "A High Efficiency 1.8 Kw Battery Equalizer," in *1993 Applied Power Electronics Conference and Exposition, Eighth Annual*, pp. 221-227.
- [76] P. A. Cassani and S. S. Williamson, "Feasibility Analysis of a Novel Cell Equalizer Topology for Plug-in Hybrid Electric Vehicle Energy-Storage Systems," *Trans. Veh. Technol.*, vol. 58, no. 8, pp. 3938-3946, 2009.
- [77] C. Pascual and P. T. Krein, "Switched Capacitor System for Automatic Series Battery Equalization," in *1997 Applied Power Electronics Conference and Exposition, Twelfth Annual*, pp. 848-854 vol.2.
- [78] N. H. Kutkut, "A Modular Nondissipative Current Diverter for Ev Battery Charge Equalization," in *1998 Applied Power Electronics Conference and Exposition, Thirteenth Annual*, pp. 686-690 vol.2.
- [79] P. Hong-Sun, K. Chong-Eun, M. Gun-Woo, L. Joong-Hui, and O. Jeon Keun, "Two-Stage Cell Balancing Scheme for Hybrid Electric Vehicle Lithium-Ion Battery Strings," in *2007 IEEE Power Electronics Specialists Conference*, pp. 273-279.

- [80] A. C. Baughman and M. Ferdowsi, "Double-Tiered Switched-Capacitor Battery Charge Equalization Technique," *IEEE Trans. Ind. Electron.*, vol. 55, no. 6, pp. 2277-2285, Jun. 2008.
- [81] T. A. Stuart and Z. Wei, "Fast Equalization for Large Lithium Ion Batteries," *IEEE Aerosp. Electron. Syst. Mag.*, vol. 24, no. 7, pp. 27-31, Jul. 2009.
- [82] Z. Zuzhi, X. Haiping, S. Lei, L. Dongxu, and H. Yuchen, "A Unit Power Factor Dc Fast Charger for Electric Vehicle Charging Station," in *2012 7th International Power Electronics and Motion Control Conference (IPEMC)*, pp. 411-415.
- [83] G. Waltrich, J. L. Duarte, and M. A. M. Hendrix, "Multiport Converter for Fast Charging of Electrical Vehicle Battery," *IEEE Trans. Ind. Appl.*, vol. 48, no. 6, pp. 2129-2139, Jun. 2012.
- [84] N. M. L. Tan, T. Abe, and H. Akagi, "Topology and Application of Bidirectional Isolated Dc-Dc Converters," in *2011 IEEE 8th International Conference on Power Electronics and ECCE Asia (ICPE & ECCE)*, pp. 1039-1046.
- [85] N. M. L. Tan, T. Abe, and H. Akagi, "Design and Performance of a Bidirectional Isolated Dc-Dc Converter for a Battery Energy Storage System," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1237-1248, Mar. 2012.
- [86] S. Inoue and H. Akagi, "A Bidirectional Dc-Dc Converter for an Energy Storage System with Galvanic Isolation," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2299-2306, Nov. 2007.
- [87] J. Park, M. Kwon, and S. Choi, "Design and Control of a Bi-Directional Resonant Dc-Dc Converter for Automotive Engine/Battery Hybrid Power Generators," in *2013 IEEE ECCE Asia Downunder (ECCE Asia)*, pp. 740-746.
- [88] D. Chen and Y. Chen, "Step-up Ac Voltage Regulators with High-Frequency Link," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 390-397, Jan. 2013.
- [89] D. Sha, G. Xu, and X. Liao, "Control Strategy for Input-Series-Output-Series High-Frequency Ac-Link Inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5283-5292, Nov. 2013.
- [90] D. De and V. Ramanarayanan, "A Dc-to-Three-Phase-Ac High-Frequency Link Converter with Compensation for Nonlinear Distortion," *IEEE Trans. Ind. Electron.*, vol. 57, no. 11, pp. 3669-3677, Nov. 2010.
- [91] D. De and V. Ramanarayanan, "Analysis, Design, Modeling, and Implementation of an Active Clamp Hf Link Converter," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 58, no. 6, pp. 1446-1455, Jun. 2011.

- [92] D. Czarkowski and M. K. Kazimierczuk, "Phase-Controlled Series-Parallel Resonant Converter," *IEEE Trans. Power Electron.*, vol. 8, no. 3, pp. 309-319, 1993.
- [93] H. Bai, C. C. Mi, and S. Gargies, "The Short-Time-Scale Transient Processes in High-Voltage and High-Power Isolated Bidirectional Dc/Dc Converters," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2648-2656, 2008.
- [94] H. Bai, Z. Zhao, and C. Mi, "Framework and Research Methodology of Short-Timescale Pulsed Power Phenomena in High-Voltage and High-Power Converters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 3, pp. 805-816, 2009.
- [95] H. Bai and C. Mi, "Correction to 'Eliminate Reactive Power and Increase System Efficiency of Isolated Bidirectional Dual-Active-Bridge Dc-Dc Converters Using Novel Dual-Phase-Shift Control' [Nov 08 2905-2914]," *IEEE Trans. Power Electron.*, vol. 27, no. 9, pp. 4177-4177, 2012.
- [96] H. Bai and C. Mi, "Eliminate Reactive Power and Increase System Efficiency of Isolated Bidirectional Dual-Active-Bridge Dc-Dc Converters Using Novel Dual-Phase-Shift Control," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2905-2914, 2008.
- [97] K. Eung-Ho, K. Jung-Min, P. Jae-Kyu, and K. Bong-Hwan, "Practical Control Implementation of a Three- to Single-Phase Online Ups," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 2933-2942, 2008.
- [98] J. K. Park, J. M. Kwon, E. H. Kim, and B. H. Kwon, "High-Performance Transformerless Online Ups," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 2943-2953, 2008.
- [99] T.-F. Wu, Y.-K. Chen, and Y.-H. Huang, "3c Strategy for Inverters in Parallel Operation Achieving an Equal Current Distribution," *IEEE Trans. Ind. Electron.*, vol. 47, no. 2, pp. 273-281, Apr 2000.
- [100] J.-F. Chen and C.-L. Chu, "Combination Voltage-Controlled and Current-Controlled Pwm Inverters for Ups Parallel Operation," *IEEE Trans. Power Electron.*, vol. 10, no. 5, pp. 547-558, Sep. 1995.
- [101] M. N. Marwali, J.-W. Jung, and A. Keyhani, "Control of Distributed Generation Systems - Part Ii: Load Sharing Control," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1551-1561, 2004.

- [102] X. Sun, Y.-S. Lee, and D. H. Xu, "Modeling, Analysis, and Implementation of Parallel Multi-Inverter Systems with Instantaneous Average-Current-Sharing Scheme," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 844-856, May 2003.
- [103] J. T. Tan, L. Hua, Z. Jun, and Y. J. Ping, "A Novel Load Sharing Control Technique for Paralleled Inverters," in *2003 IEEE 34th Annual Power Electronics Specialist Conference*, pp. 1432-1437.
- [104] J. T. Tan, J. P. Ying, and H. Lin, "Parallel Inverter System Based on Tracking of System Power Reference," U.S. Patent No. 6,850,425, Feb 1 2005.
- [105] J. T. Tan, Y. Li, Y. H. Cheng, J. P. Ying, and C. Tsai, "Parallel Inverters and Controlling Method Thereof " U.S. Patent No. 7 420 826, Sep 2 2008.
- [106] X. Zhang, H. Zhang, X. Ma, and J. M. Guerrero, "Sharing of Active Power Supply and Reactive Power Compensation for Parallel Inverters," in *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, pp. 353-357.
- [107] H. Cai, R. Zhao, and H. Yang, "Study on Ideal Operation Status of Parallel Inverters," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2964-2969, Nov 2008.
- [108] A. Tuladhar, J. Hua, T. Unger, and K. Mauch, "Control of Parallel Inverters in Distributed Ac Power Systems with Consideration of Line Impedance Effect," *IEEE Trans. Ind. Appl.*, vol. 36, no. 1, pp. 131-138, Jan/Feb 2000.
- [109] K. De Brabandere, B. Bolsens, J. Van den Keybus, A. Woyte, J. Driesen, and R. Belmans, "A Voltage and Frequency Droop Control Method for Parallel Inverters," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1107-1115, Jul 2007.
- [110] J. M. Guerrero, L. G. de Vicuna, J. Matas, M. Castilla, and J. Miret, "A Wireless Controller to Enhance Dynamic Performance of Parallel Inverters in Distributed Generation Systems," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1205-1213, Sep 2004.
- [111] J. C. Vasquez, J. M. Guerrero, M. Savaghebi, J. Eloy-Garcia, and R. Teodorescu, "Modeling, Analysis, and Design of Stationary-Reference-Frame Droop-Controlled Parallel Three-Phase Voltage Source Inverters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1271-1280, 2013.
- [112] Q. C. Zhong, "Robust Droop Controller for Accurate Proportional Load Sharing among Inverters Operated in Parallel," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1281-1290, 2013.
- [113] W. Yao, M. Chen, J. Matas, J. M. Guerrero, and Z.-M. Qian, "Design and Analysis of the Droop Control Method for Parallel Inverters Considering the Impact of the

- Complex Impedance on the Power Sharing," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 576-588, 2011.
- [114] J. M. Guerrero, J. C. Vasquez, J. Matas, L. G. de Vicuna, and M. Castilla, "Hierarchical Control of Droop-Controlled Ac and Dc Microgrids-a General Approach toward Standardization," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 158-172, 2011.
- [115] L. Asiminoaei, E. Aeloiza, P. N. Enjeti, and F. Blaabjerg, "Shunt Active-Power-Filter Topology Based on Parallel Interleaved Inverters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1175-1189, 2008.
- [116] J. Ewanchuk and J. Salmon, "Three-Limb Coupled Inductor Operation for Paralleled Multi-Level Three-Phase Voltage Sourced Inverters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1979-1988, May. 2013.
- [117] M. Narimani and G. Moschopoulos, "A New Interleaved Three-Phase Single-Stage Pfc Ac-Dc Converter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 2, pp. 648-654, Feb. 2014.
- [118] P. U.R and A. Rathore, "Current-Fed Interleaved Phase-Modulated Single-Phase Unfolding Inverter: Analysis, Design and Experimental Results," *IEEE Trans. Ind. Electron.*, vol. PP, no. 99, pp. 1-1, 2013.
- [119] Z. Yu, J. Zhenhua, and Y. Xunwei, "Control Strategies for Battery/Supercapacitor Hybrid Energy Storage Systems," in *2008. IEEE Energy 2030 Conference*, pp. 1-6.
- [120] J. Leuchter, P. Bauer, and V. Stekly, "Battery-Supercapacitors Mixed as Electrical Power Buffers," in *2010 5th IET International Conference on Power Electronics, Machines and Drives*, pp. 1-6.
- [121] F. Liu, J. Liu, and L. Zhou, "A Novel Control Strategy for Hybrid Energy Storage System to Relieve Battery Stress," in *2010 2nd IEEE International Symposium on Power Electronics for Distributed Generation Systems*, pp. 929-934.
- [122] P. A. Cassani and S. S. Williamson, "Design, Testing, and Validation of a Simplified Control Scheme for a Novel Plug-in Hybrid Electric Vehicle Battery Cell Equalizer," *IEEE Trans. Ind. Electron.*, vol. 57, no. 12, pp. 3956-3962, Dec. 2010.
- [123] J. Jang and J. Yoo, "Equivalent Circuit Evaluation Method of Lithium Polymer Battery Using Bode Plot and Numerical Analysis," *IEEE Trans. Energy Convers.*, vol. 26, no. 1, pp. 290-298, Mar. 2011.

- [124] M. Gholizadeh and F. R. Salmasi, "Estimation of State of Charge, Unknown Nonlinearities, and State of Health of a Lithium-Ion Battery Based on a Comprehensive Unobservable Model," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1335-1344, Mar. 2014.
- [125] R. Smolenski, M. Jarnut, G. Benysek, and A. Kempinski, "Ac/Dc/Dc Interfaces for V2g Applications-Emc Issues," *IEEE Trans. Ind. Electron.*, vol. 60, no. 3, pp. 930-935, Mar. 2013.
- [126] K.-W. Hu and C.-M. Liaw, "On a Bidirectional Adapter with G2b Charging and B2x Emergency Discharging Functions," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 243-257, Jan. 2014.
- [127] H. Qian, J. Zhang, J.-S. Lai, and W. Yu, "A High-Efficiency Grid-Tie Battery Energy Storage System," *IEEE Trans. Power Electron.*, vol. 26, no. 3, pp. 886-896, Mar. 2011.
- [128] M. N. Kheraluwala, R. W. Gascoigne, D. M. Divan, and E. D. Baumann, "Performance Characterization of a High-Power Dual Active Bridge Dc-to-Dc Converter," *IEEE Trans. Ind. Appl.*, vol. 28, no. 6, pp. 1294-1301, 1992.
- [129] H. Bai and C. Mi, "Correction to "Eliminate Reactive Power and Increase System Efficiency of Isolated Bidirectional Dual-Active-Bridge Dc-Dc Converters Using Novel Dual-Phase-Shift Control" [Nov 08 2905-2914]," *IEEE Trans. Power Electron.*, vol. 27, no. 9, pp. 4177-4177, 2012.
- [130] B. Sahan, A. N. Vergara, N. Henze, A. Engler, and P. Zacharias, "A Single-Stage Pv Module Integrated Converter Based on a Low-Power Current-Source Inverter," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2602-2609, Jul. 2008.
- [131] X. Hu, K. J. Tseng, Y. Liu, S. Yin, and M. Zhang, "A High Frequency Isolated Current-Fed Bidirectional Dc/Ac Converter for Grid-Tied Energy Storage System," in *ECCE Asia Downunder (ECCE Asia), 2013 IEEE*, pp. 291-296.
- [132] D. N. Zmood and D. G. Holmes, "Improved Voltage Regulation for Current-Source Inverters," *IEEE Trans. Ind. Appl.*, vol. 37, no. 4, pp. 1028-1036, Jul. 2001.
- [133] S. A. S. Grogan, D. G. Holmes, and B. P. McGrath, "High-Performance Voltage Regulation of Current Source Inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 9, pp. 2439-2448, Sep. 2011.
- [134] J. D. Ma, B. Wu, N. R. Zargari, and S. C. Rizzo, "A Space Vector Modulated Csi-Based Ac Drive for Multimotor Applications," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 535-544, Jul. 2001.

- [135] S. V. Papaefthymiou, E. G. Karamanou, S. A. Papathanassiou, and M. P. Papadopoulos, "A Wind-Hydro-Pumped Storage Station Leading to High Res Penetration in the Autonomous Island System of Ikaria," *IEEE Trans. Sustainable Energy*, vol. 1, no. 3, pp. 163-172, Oct. 2010.
- [136] C. Mi, L. Ben, D. Buck, and N. Ota, "Advanced Electro-Thermal Modeling of Lithium-Ion Battery System for Hybrid Electric Vehicle Applications," in *2007 IEEE Vehicle Power and Propulsion Conference*, pp. 107-111.
- [137] K. Jonghoon, S. Jongwon, C. Changyoon, and B. H. Cho, "Stable Configuration of a Li-Ion Series Battery Pack Based on a Screening Process for Improved Voltage/Soc Balancing," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 411-424, Jan. 2012.
- [138] A. Emadi, L. Young Joo, and K. Rajashekara, "Power Electronics and Motor Drives in Electric, Hybrid Electric, and Plug-in Hybrid Electric Vehicles," *IEEE Trans. Ind. Electron.*, vol. 55, no. 6, pp. 2237-2245, Jun. 2008.
- [139] X. Hu, K. J. Tseng, and M. Srinivasan, "Optimization of Battery Energy Storage System with Super-Capacitor for Renewable Energy Applications," in *2011 IEEE 8th International Conference on Power Electronics and ECCE Asia*, pp. 1552-1557.
- [140] Y. W. Li, B. Wu, D. Xu, and N. R. Zargari, "Space Vector Sequence Investigation and Synchronization Methods for Active Front-End Rectifiers in High-Power Current-Source Drives," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1022-1034, Mar. 2008.
- [141] J. He, Y. W. Li, D. Bosnjak, and B. Harris, "Investigation and Active Damping of Multiple Resonances in a Parallel-Inverter-Based Microgrid," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 234-246, Jan 2013.
- [142] M. Borrega, L. Marroyo, R. Gonzalez, J. Balda, and J. L. Agorreta, "Modeling and Control of a Master-Slave Pv Inverter with N-Paralleled Inverters and Three-Phase Three-Limb Inductors," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2842-2855, 2013.
- [143] J. F. Conroy and R. Watson, "Low-Voltage Ride-through of a Full Converter Wind Turbine with Permanent Magnet Generator," *Renewable Power Generation, IET*, vol. 1, no. 3, pp. 182-189, Sep. 2007.
- [144] W. Li, C. Abbey, and G. Joos, "Control and Performance of Wind Turbine Generators Based on Permanent Magnet Synchronous Machines Feeding a Diode Rectifier," in *2006 37th IEEE Power Electronics Specialists Conference*, pp. 1-6.

- [145] T. H. Nguyen and D.-C. Lee, "Advanced Fault Ride-through Technique for Pmsg Wind Turbine Systems Using Line-Side Converter as Statcom," *IEEE Trans. Ind. Electron.*, vol. 60, no. 7, pp. 2842-2850, 2013.
- [146] S. Alepuz, A. Calle, S. Busquets-Monge, S. Kouro, and W. Bin, "Use of Stored Energy in Pmsg Rotor Inertia for Low-Voltage Ride-through in Back-to-Back Npc Converter-Based Wind Power Systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1787-1796, 2013.
- [147] A. Nabae, I. Takahashi, and H. Akagi, "A New Neutral-Point-Clamped Pwm Inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518-523, 1981.
- [148] J. Rodriguez, L. Jih-Sheng, and F. Z. Peng, "Multilevel Inverters: A Survey of Topologies, Controls, and Applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724-738, 2002.
- [149] N. Celanovic and D. Boroyevich, "A Comprehensive Study of Neutral-Point Voltage Balancing Problem in Three-Level Neutral-Point-Clamped Voltage Source Pwm Inverters," *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 242-249, 2000.
- [150] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930-2945, 2007.
- [151] H. D. G. and L. T. A., *Pulse Width Modulation for Power Converters : Principle and Practice*. New York, NJ:Wiley, 2003.
- [152] A. J. Korn, M. Winkelkemper, and P. Steimer, "Low Output Frequency Operation of the Modular Multi-Level Converter," in *2010 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 3993-3997.
- [153] S. P. Engel and R. W. De Doncker, "Control of the Modular Multi-Level Converter for Minimized Cell Capacitance," in *2011 14th European Conference on Power Electronics and Applications*, pp. 1-10.
- [154] X. She, R. Burgos, G. Wang, F. Wang, and A. Q. Huang, "Review of Solid State Transformer in the Distribution System: From Components to Field Application," in *2012 IEEE Energy Conversion Congress and Exposition*, pp. 4077-4084.