

**DEVICE DESIGN, CHARACTERIZATION AND
MODELING OF INDUCTORS AND INTERCONNECTS
FOR RFIC APPLICATIONS**

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CONTENTS

ACKNOWLEDGEMENTS	i
SUMMARY	iv
LIST OF FIGURES.....	vi
LIST OF TABLES.....	xiii
LIST OF SYMBOLS	xiv
Chapter 1 - Introduction.....	1
1.1 Motivation	1
1.1.1 Business Trends for Wireless Communication Products	1
1.1.2 Economic and Technological Perspectives	3
1.1.3 Active Devices in Current Silicon Technologies	8
1.1.4 Major Road Blocks in Silicon-based RFIC Designs	9
1.2 Objectives	12
1.3 Major Contributions of the Thesis.....	13
1.4 Organization of the Thesis.....	15
Chapter 2 - Literature Review	17
2.1 Integrated Spiral Inductors on Silicon.....	17
2.1.1 Figure of Merits for Spiral Inductors.....	17
2.1.1.1 Inductance Value, L.....	18
2.1.1.2 Quality Factor, Q-factor	21
2.1.2 Advantages in using Silicon-based Spiral Inductors.....	25
2.1.3 Identifying Loss Mechanisms in Silicon-based Spiral Inductors	26
2.1.3.1 Metallization Resistive Loss.....	26
2.1.3.2 Substrate Capacitive and Resistive Loss	28
2.1.3.3 Substrate Eddy Current.....	29
2.1.4 Q-Factor Enhancement Techniques	30
2.1.4.1 Q-Factor Enhancement using Processing Technologies ..	31
2.1.4.2 Q-Factor Enhancement using Active Inductors	38
2.1.4.3 Q-Factor Enhancement using Coupled Spiral Coils.....	39
2.1.4.4 Q-Factor Enhancement using Layout Optimization.....	40
2.1.4.5 Q-Factor Enhancement using Inductor Device Model	41
2.1.4.6 Summary of Q-Factor Enhancement Techniques.....	43
2.2 RF Interconnects on Silicon	44
2.2.1 Transmission Line Concept.....	46
2.2.1.1 Transmission Line Constants	48
2.2.1.2 Transmission Line Impedances	49
2.2.1.3 Reflection and Voltage Standing Wave Ratio.....	50
2.2.1.4 Frequency-Dependent Charge Distribution.....	51
2.2.1.5 Effects of Dielectric on Interconnects	53
2.2.2 Backend Interconnect Schemes for Silicon Technologies	54
2.2.3 Existing Methodologies to Tackle Post Layout Parasitics	56
2.3 On-Wafer RF Characterization.....	60
2.3.1 Error sources and Calibration for RF measurements	61
2.3.2 Calibration Techniques.....	65
2.3.2.1 SOLT	65
2.3.2.2 TRL.....	66

2.3.2.3	LRM	66
2.3.2.4	LRRM.....	67
2.3.2.5	Summary of Calibration Techniques.....	67
2.3.3	RF Probes	69
2.3.4	De-embedding, Extending Measurement Plane to Devices	72
2.3.4.1	One-Step OPEN De-embedding.....	72
2.3.4.2	Two-Step OPEN and SHORT De-embedding	74
Chapter 3	- Physical Layout Design Optimization of Spiral Inductors ..	76
3.1	Test Structure Fabrication and Inductors' Figure of Merits	78
3.2	Effects of Core Diameter	80
3.3	Effects of Metal Conductor Spacing.....	87
3.4	Effects of Metal Conductor Width.....	91
3.5	Giga-Hertz Amplifier using Optimized Integrated Inductors.....	102
3.6	Comparing Research Works on Inductor Layout Optimization	106
3.7	Design Optimization Methodology for Copper Spiral Inductors ...	109
3.7.1	Effects of Core Diameter.....	109
3.7.2	Effects of Metal Conductor Spacing	113
3.7.3	Effects of Metal Conductor Width	114
Chapter 4	- Modeling Symmetrical Spiral Inductors.....	119
4.1	Test Structure Design Considerations and Experimental Setup	120
4.2	RF Sub-Circuit Model and Extraction Strategy.....	123
4.3	Model Accuracy and Continuity.....	127
4.4	Design Trade-offs for Symmetrical Inductors	131
4.5	Comparing Research Works on Modeling Spiral Inductors.....	138
Chapter 5	- Modeling Differential Spiral Inductors.....	140
5.1	Design of Test Structures and Experimental Setup	141
5.2	Figure of Merits for Differential Spiral Inductors	146
5.3	RF Sub-Circuit Model and Extraction Strategy.....	147
5.4	Model Accuracy, Continuity and Design Trade-Offs.....	150
5.5	Models Verification using Differential Giga-Hertz Amplifier	161
5.6	Comparing Research Works on Modeling Differential Inductors...	165
Chapter 6	- Accurate and Scalable RF Interconnect Model	167
6.1	Design of Test Structures and Experimental Setup	167
6.2	Proposed Figure of Merit for RF Interconnects.....	169
6.3	Proposed Sub-circuit Model for RF Interconnects	173
6.4	Accuracy and Continuity of the RF Interconnect Model.....	175
6.5	Model Verification using Giga-Hertz Amplifiers.....	181
6.6	Model Verification using Voltage Controlled Oscillator	188
6.7	Comparing Research Works on Interconnect Modeling	191
6.8	RF Interconnects in Aluminum and Copper Technologies	193
Chapter 7	- Conclusions and Recommendations	197
7.1	Conclusions.....	197
7.2	Recommendations for Further Research	201
Author's Publications	202
Bibliography	203

SUMMARY

Escalating demands for personal wireless communication equipment have spearheaded development of affordable RF System-on-Chip (SoC) solutions. Silicon is believed to be the most suitable material that can satisfy the demands of this rapidly growing wireless market. Advancements in technology have continued to enhance the cutoff frequencies of active devices such as MOSFETs and SiGe HBTs. Nonetheless, low resistive bulk silicon and high resistive metallization have made on-chip inductors and interconnects major obstacles to achieving exemplary circuit characteristics at giga-hertz frequencies.

Physical design parameter optimization of conventional spiral inductors is performed in this work as all other known performance enhancement techniques for inductors have intolerable trade-offs. For the first time, conventional spiral inductors for both aluminum and copper metallization technologies are designed to achieve similar inductance values as an experimental control to investigate how its core diameter, conductor spacing and width affect their performances. Core diameter must be sufficiently large to minimize the formation of conductor eddy current. Conductor spacing should be minimal as it offers larger inductance value while consuming smaller silicon area. Optimization of conductor width has enabled inductors over a wide range of inductance values to have large quality factors at the circuit operating frequency.

Findings obtained from optimizing conventional spiral inductors have allowed small but streamlined sets of symmetrical and differential inductor test structures to be fabricated for the development of scalable RF SPICE models. These scalable inductor models have extended ground-breaking analysis of design trade-offs at frequencies up to 10 GHz, comparing inductors with identical inductance values. Large-width designs are found to favor inductors with small inductance values due to huge reduction in resistive loss. As inductance increases, trade-offs between resistive and substrate loss result in optimal

widths such that using much larger widths waste chip area and degrade quality factor. When operating frequency increases, these optimal conductor widths decrease, improving the performance and reduce the size of symmetrical and differential inductors. Brilliant circuit predictions for a giga-hertz differential amplifier reveal high levels of accuracy and scalability for the proposed scalable RF inductor models.

While metallization in the form of inductors are “friends” that store magnetic energy, as interconnects, they are however, “foes” to RFIC designers. Without considering these interconnect parasitics in the design phase, fabricated RF circuits suffer power loss and shifts in circuit operating frequencies. To minimize design iteration cycle for silicon-based RFIC, RF interconnect test structures are designed, characterized and modeled to predict their parasitic effects at radio frequencies. A new figure of merit, intrinsic factor, I_F , has been proposed in this research work to provide a convenient indication as to how interconnects affect the performance of RFICs. The proposed double- π interconnect model displayed excellent continuity and scalability across various physical dimensions of the metal lines. Circuit verifications revealed outstanding correlations between SPICE simulated and on-wafer measured circuit characteristics. The proposed methodology of tackling backend interconnects has demonstrated possibilities in achieving cost-effective one-pass design success for silicon-based RFICs when accurate device and interconnect models are used.

LIST OF FIGURES

Figure 1.1 - Worldwide SoC sales from 1999 to 2009.	2
Figure 1.2 - Percentage breakdown of worldwide SoC sales by applications.	3
Figure 1.3 - Average mask cost versus technology nodes.	4
Figure 1.4 - RF SoC design methodology.	7
Figure 2.1 - Positive and negative mutual inductance components in a rectangular inductor.	18
Figure 2.2 - Mutual inductance between two metal segments, A and B.	19
Figure 2.3 - Parallel RLC circuit.	22
Figure 2.4 - Formation of image current and its magnetic flux interaction with that of the inductor.	30
Figure 2.5 - Cross-sectional view (a) and performance (b) of inductor fabricated using MMIC technology.	31
Figure 2.6 - Cross-sectional view (a) and performance (b) of spiral inductor using 4-Level metallization.	32
Figure 2.7 - Performance comparison of Cu spiral Inductors with different metal thickness (a) and inductors with silicon and quartz substrates (b).	33
Figure 2.8 - Comparing inductor performance on SOI and bulk silicon.	34
Figure 2.9 - Measured Q-factor of square spiral inductors using SOI CMOS process.	34
Figure 2.10 - SEM photo (a) and performance (b) for the 1-turn 3D copper coil inductor.	35
Figure 2.11 - 3-dimensional illustration (a) and measured Q-factor (b) of the toroidal inductor.	35
Figure 2.12 - Cross-sectional view (a) and Q-factor comparison (b) for spiral inductors with and without eddy-current blocking structures.	36
Figure 2.13 - Polysilicon patterned shield (a), die photos of test structures (b) and L & Q versus frequency plots (c) for inductors with different polysilicon shield patterns.	37
Figure 2.14 - High-Q active inductor with RC feedback cascode network (a) and its performance (b).	38
Figure 2.15 - Test setup for tunable inductor (a) Q-factor vs phase in variable phase shifter (b).	39
Figure 2.16 - Optimized layout (a) and Q-factor (b) for varying width spiral inductors.	40
Figure 2.17 - Physical inductor model for optimization (a) and Q-factor for 10 nH inductor as a function of number of turns and conductor width (b).	41
Figure 2.18 - Cross-sectional view of on-chip interconnects	51
Figure 2.19 - Cross-sectional view of the charge distribution in an interconnect at different frequencies. (The dots and crosses indicate charge concentration of different polarity).	51

Figure 2.20 - Aluminum and copper backend interconnect process flows.....	54
Figure 2.21 - Backend cross-sectional schematics for 0.18 μm and 0.13 μm RFCMOS process.....	55
Figure 2.22 - Fully integrated RLCK solution for full-chip device-level parasitic extraction [47].	58
Figure 2.23(a) - Error adapters in two-port measurements.....	62
Figure 2.23(b) - Signal flow graph showing the error sources in two-port measurements.	63
Figure 2.24 - Infinity probes with SHORT, OPEN, LOAD and THRU standards (a) - (d) on impedance standard substrate and magnitude of S11 versus frequency on OPEN standard after calibration (e).	69
Figure 2.25 - RF Infinity Probes (a), small contact marks allowing pads of 50 x 50 μm (b), microstrip to probe tips provided shielding to DUT (c), nickel alloy probe tip allow stable and low contact resistance compared tungsten probe tip (d). Photos reproduced with permission from Cascade Microtech Inc.	70
Figure 2.26 - Equivalent circuits for DUT and OPEN de-embedding structure.....	72
Figure 2.27 - 2-Port Pi-network.	73
Figure 2.28 - Equivalent circuits for DUT, OPEN and SHORT de-embedding structures.....	74
Figure 2.29 - 2-Port Tee-network.	75
Figure 3.1 - Inductance and Q-factor versus frequency for 3-turn spiral inductors with different core diameters.....	80
Figure 3.2 - Die photos of spiral inductors with identical conductor length (1000 μm), and width (8 μm) but different core diameters (a) 10 μm , (b) 50 μm , (c) 100 μm and (d) 150 μm	81
Figure 3.3 - Inductance, Q-factor and series resistance versus frequency for inductors with identical conductor length (1000 μm) and width (8 μm) but different core diameters.....	82
Figure 3.4 - Inductance, Q-factor and series resistance versus frequency for inductors with identical conductor length (2000 μm) and width (8 μm) but different core diameters.....	83
Figure 3.5 - Inductance, Q-factor and series resistance versus frequency for inductors with identical conductor length (3500 μm) and width (8 μm) but different core diameters.....	84
Figure 3.6 - Formation of conductor eddy current in the core turns of spiral inductors.	85
Figure 3.7 - Inductance, Q-factor and series resistance versus frequency for inductors with identical conductor length (2000 μm) and width (4 μm) but different core diameters.....	86
Figure 3.8 - Inductance, Q-factor and series resistance versus frequency for inductors with identical conductor length (2000 μm) and width (16 μm) but different core diameters.....	86

Figure 3.9 - Die photos of spiral inductors with identical conductor length (2000 μm), width (8 μm) and core diameter (100 μm) but different metal-to-metal spacing of 3 (a), 6 (b), 9 (c) and 12 μm (d).	87
Figure 3.10 - Inductance, Q-factor and series resistance versus frequency for inductors with identical conductor length (2000 μm), width (8 μm) and core diameters (100 μm) but different spacing.....	88
Figure 3.11 - Inductance, Q-factor and series resistance versus frequency for inductors with identical conductor length (2000 μm), width (16 μm) and core diameters (100 μm) but different spacing.....	88
Figure 3.12 - Inductance, Q-factor and series resistance versus frequency for inductors with identical conductor length (2000 μm), width (1.5 μm) and core diameters (100 μm) but different spacing.....	89
Figure 3.13 - Inductance and Q-factor versus frequency for 1-8 turns inductors with width and core diameter of 12 and 75 μm respectively.	91
Figure 3.14 - Inductance and Q-factor versus frequency for 8-turn inductors with core diameter and spacing of 75 and 1.5 μm respectively for widths of 6, 8, 12 and 16 μm	93
Figure 3.15 - Flow chart summarizing the design methodology for optimizing the physical dimensions of spiral inductors.	94
Figure 3.16 - Inductance at low frequency versus total conductor length for inductors with identical diameter of 100 μm but different widths of 2, 4, 8, 12, 16 and 24 μm	95
Figure 3.17 - Die photos of 1.6 nH spiral inductors with identical core diameter (100 μm) but different widths of 4 μm (a), 8 μm (b), 16 μm (c) and 24 μm (d).	96
Figure 3.18 - Inductance and Q-factor versus frequency for inductors with identical inductance (1.6 nH) and core diameter (100 μm) but different widths.....	96
Figure 3.19 - Inductance and Q-factor versus frequency for inductors with identical inductance (2.8 nH) and core diameter (100 μm) but different widths.....	97
Figure 3.20 - Inductance and Q-factor versus frequency for inductors with identical inductance (4.4 nH) and core diameter (100 μm) but different widths.....	98
Figure 3.21 - Inductance and Q-factor versus frequency for inductors with identical inductance (6.2 nH) and core diameter (100 μm) but different widths.....	98
Figure 3.22 - Inductance and Q-factor versus frequency for inductors with identical inductance (8.2 nH) and core diameter (100 μm) but different widths.....	99
Figure 3.23(a) - Q-factor performance versus width for inductors with identical inductances and inductance versus width for inductors with Q_{peak} at 2.5 GHz.....	99
Figure 3.23(b) - Q-factor versus inductance for sets of inductors with optimized conductor width and fixed conductor width of 4 μm at 2.5 GHz.....	100
Figure 3.24 - Circuit schematic of a simple giga-hertz amplifier utilized to demonstrate performance enhancements when optimized inductors are used in RFICs design.....	102

Figure 3.25 - Die photos showing on-wafer RF S-parameters and high frequency noise characterization of amplifiers with non-optimized inductors (a) and optimized inductors (b).....	104
Figure 3.26 - Measured 2-port S-parameters and noise figure of amplifiers with and without optimized spiral inductors.....	105
Figure 3.27 - Inductance, Q-factor and series resistance for copper spiral inductors with identical conductor length (1000 μm) and width (8 μm) but different core diameters.....	110
Figure 3.28 - Inductance, Q-factor and series resistance for copper spiral inductors with identical conductor length (3500 μm) and width (8 μm) but different core diameters.....	111
Figure 3.29 - Inductance, Q-factor and series resistance for copper spiral inductors with identical conductor length (2000 μm) and width (4 μm) but different core diameter.	112
Figure 3.30 - Inductance, Q-factor and series resistance for copper spiral inductors with identical conductor length (2000 μm) and width (16 μm) but different core diameter.	112
Figure 3.31 - Inductance, Q-factor and series resistance for copper spiral inductors with identical conductor length (2000 μm), width (8 μm) and core diameter (100 μm) but different conductor spacing.....	113
Figure 3.32 - Inductance and Q-factor for copper spiral inductors with identical inductance (1.5 nH) and core diameter (100 μm) but different widths.....	115
Figure 3.33 - Inductance and Q-factor for copper spiral inductors with identical inductance (4.2 nH) and core diameter (100 μm) but different widths.....	116
Figure 3.34 - Inductance and Q-factor for copper spiral inductors with identical inductance (7.8 nH) and core diameter (100 μm) but different widths.....	116
Figure 3.35 - Comparing width for Q_{Peak} at 2.5 GHz and corresponding Q-factor value for aluminum and copper spiral inductors.....	117
Figure 4.1 - Physical layout scheme of symmetrical inductor for 0.18 μm RFCMOS technology.	122
Figure 4.2 - On-wafer RF characterization of a 2.5-turn symmetrical inductor with infinity probes.....	122
Figure 4.3 - SPICE-Compatible RF sub-circuit model for Symmetrical Spiral Inductors.....	123
Figure 4.4 - Model extraction strategy for symmetrical spiral inductors.	124
Figure 4.5 - Simulated versus measured inductance L, Q-factor for 2.5-turn symmetrical inductor with core diameter and width of 60 and 8 μm respectively.....	128
Figure 4.6 - Box plots showing deviations between SPICE model simulated and measured inductance and Q-factor at 2.45 and 5.05 GHz for all symmetrical inductors in the test element group.....	128
Figure 4.7- RF symmetrical inductor model continuity – simulated (surface) and measured (dots) inductance and Q-factor versus diameter and width at 2.45 GHz for 1.5-turn (a), 2.5-turn (b), 3.5-turn (c), 4.5-turn (d), 5.5-turn (e) and 6.5-turn (f) symmetrical inductors.....	130

Figure 4.8 - Inductance versus Q-factor for sets of 2.5-turn symmetrical inductors with core diameters from 30 to 180 μm and different widths at 2.45 GHz.	131
Figure 4.9 - Inductance and Q-factor versus frequency for 2 nH symmetrical inductors at 2.45 (a), 5.05 (b) and 10.05 GHz (c).	134
Figure 4.10 - Q-factor versus conductor width for 1 nH (a), 2 nH (b) and 4 nH (c) symmetrical inductor at operating frequencies of 2.45, 5.05 and 10.05 GHz.	136
Figure 4.11 - Optimal width for symmetrical inductor at operating frequencies of 2.45, 5.05 and 10.05 GHz and comparing conventional spiral (Chapter 3, Figure 3.23a) and symmetrical spiral inductor at 2.45 GHz.	137
Figure 5.1 - Layout scheme of differential inductor in 0.18 μm RFCMOS process.	141
Figure 5.2 - Die photos showing differential inductor layout in GSG configuration, inductor (a) open (b) and short calibration structures (c).	144
Figure 5.3 - Differential inductor layout in GS configuration, inductor (a) and open calibration structure (b).	144
Figure 5.4 - Differential inductance and Q-factor versus frequency for same differential inductor in GSG and GS layout configurations.	145
Figure 5.5 - SPICE-compatible RF sub-circuit model for differential inductor.	147
Figure 5.6 - Differential inductor RF model parameter extraction strategy.	148
Figure 5.7 - Simulated versus measured inductance due to single-ended excitation, L , differential inductance L_{DIFF} and quality factor Q_{DIFF} for 6-turn differential inductor with core diameter and width of 180 and 12 μm respectively.	151
Figure 5.8 - Box plots showing deviations between SPICE model simulated and measured differential inductance and quality factor at 2.45 and 5.05 GHz for all inductors in the test element group.	152
Figure 5.9 - RF differential inductor model continuity – simulated (surface) and measured (dots) differential inductance and quality factor versus diameter and width at 2.45 GHz for 2-turn (a), 4-turn (b), 6-turn (c), 8-turn (d) differential inductors.	153
Figure 5.10 - Differential inductance versus quality factor at 2.45 GHz for all inductors in the test element group. As an example, w4n2 refers to 2-turn inductors with width of 4 μm	154
Figure 5.11 - Differential inductance and quality factor versus frequency for 1.0 nH (a) and 5.0 nH (b) differential inductors at 2.45 GHz. In the legend, for example, W4 D132 refers to inductor with 4 μm width and diameter of 132 μm	155
Figure 5.12 - Differential quality factor versus conductor width for 1.0 nH (a), 3.0 nH (b) and 5.0 nH (c) differential inductors at various operating frequencies of 2.45, 5.05, 7.45 and 10.05 GHz.	158
Figure 5.13 - Optimal conductor width (for high Q_{DIFF}) versus differential inductance at operating frequencies of 2.45, 5.05, 7.45 and 10.05 GHz. Width of 2 and 32 μm are extrapolated for plots of 10.05 and 2.45 GHz respectively.	159

Figure 5.14 - Comparing optimal conductor width (for high quality factor) between differential and single ended spiral inductors (Chapter 3, Figure 3.23a) versus normalized inductance at 2.45 GHz.	160
Figure 5.15 - Circuit schematic of a 2.4 GHz single-ended-to-differential amplifier with differential Inductor.	161
Figure 5.16 - Die photos showing on-wafer multi-port RF circuit measurements of differential amplifiers with differential inductor (a) and symmetrical spiral Inductors (b) using Cascade Microtech Infinity GSSG probes.	162
Figure 5.17 - Simulated (.s) and measured (.m) 3-Port S-parameters versus frequency characteristics for giga-hertz amplifier with differential inductor.	163
Figure 5.18 - Comparing measured performance of giga-hertz amplifiers using differential inductor and symmetrical spiral inductor as the output matching load inductor.	164
Figure 6.1 - Die -photos showing on-wafer RF characterization of interconnects. (a) Interconnect test structure with Cascade Microtech RF Infinity probes. (b) Interconnects 800 μm in length with different widths and open calibration structure.	168
Figure 6.2 - Inductive source degeneration impedance matching without (a) and with (b) consideration of interconnect metallization.	170
Figure 6.3 - Double- π RF sub-circuit model for interconnects.	173
Figure 6.4 - Model parameter extraction procedure for double- π RF interconnect model.	174
Figure 6.5 - Measured vs simulated parasitic inductance (a), series resistance extracted from Y_{12} (b), Q-Factor (c) and Intrinsic Factor, I_F (d) vs frequency for interconnect with length and width of 800 μm and 20 μm respectively using the proposed double- π RF interconnect model.	175
Figure 6.6 - Single- π lumped element RF sub-circuit model for interconnects.	176
Figure 6.7 - Measured vs simulated series resistance extracted from Y_{12} (a) and Intrinsic Factor, I_F (b) vs frequency for interconnect with length and width of 800 μm and 20 μm respectively using a single- π lumped element RF sub-circuit model.	176
Figure 6.8 - Box plots showing deviation between simulated and measured parasitic inductance and Intrinsic Factor, I_F at 2.45 and 5.05 GHz for the metal-6 interconnect test structures.	179
Figure 6.9 - Double- π RF interconnect model continuity – simulated and measured interconnect inductance versus length for different widths at 2.45 GHz.	179
Figure 6.10 - Double- π RF interconnect model continuity – simulated and measured Intrinsic Factor, I_F versus length for different widths at 2.45 GHz.	180
Figure 6.11 - Schematic of a simple giga-hertz amplifier circuit to verify the accuracy of the double- π RF interconnect model.	181
Figure 6.12 - Die photos showing on-wafer circuit characterization of giga-hertz amplifiers with different interconnect widths of (a) 1.5 μm and (b) 10 μm	182

Figure 6.13 - Magnitude of measured S-parameters versus frequency for the 2 amplifier circuits with interconnect widths of 1.5 and 10 μm respectively.....	183
Figure 6.14 - Schematic of the giga-hertz amplifier circuit showing the lengths of metallization interconnects in various parts of the circuit.....	184
Figure 6.15 - Schematic of the giga-hertz amplifier circuit showing representation of metallization interconnects with conventional RC extraction.	184
Figure 6.16 - Magnitude of measured and simulated S-parameters versus frequency for giga-hertz amplifier circuit with interconnect width of 1.5 μm using different interconnect schemes.	185
Figure 6.17 - Magnitude of measured and simulated S-parameters versus frequency for giga-hertz amplifier circuit with interconnect width of 10 μm using different interconnect schemes.	186
Figure 6.18 - Schematics of voltage controlled oscillator (a) and buffer amplifier (b) of a simple giga-hertz voltage controlled oscillator with interconnect width of 10 μm to verify the accuracy of the double- π RF interconnect model.	189
Figure 6.19 - Die photo of the giga-hertz voltage controlled oscillator with interconnect width of 10 μm to verify the accuracy of the double- π RF interconnect model.	190
Figure 6.20 - Measured and simulated (SIM) oscillation frequency versus control voltage for giga-hertz voltage controlled oscillator using double- π RF interconnect model.	190
Figure 6.21 - Comparing extracted low frequency resistance for aluminum (Al) and copper (Cu) top metal interconnects with conductor lengths from 100 to 800 μm and widths of 1.5, 5 and 10 μm	195
Figure 6.22 - Comparing extracted inductance at 2.45 GHz for aluminum (Al) and copper (Cu) top metal interconnects with conductor lengths from 100 to 800 μm and widths of 1.5, 5 and 10 μm	195
Figure 6.23 - Comparing extracted Intrinsic factor at 2.45 GHz for aluminum (Al) and copper (Cu) top metal interconnects with conductor lengths from 100 to 800 μm and widths of 1.5, 5 and 10 μm	196

LIST OF TABLES

Table 1.1 - Active device technology requirements for 0.8 to 10 GHz transceivers.....	8
Table 2.1 - Modeling criteria for interconnects.....	46
Table 2.2 - Interconnect critical lengths in free space, silicon dioxide and silicon.....	47
Table 2.3 - Summary of calibration techniques for RF measurements.....	68
Table 3.1 - Comparing various research works on layout optimization for spiral inductors.....	108
Table 4.1 - Interconnect characteristics for 0.18 μ m, 0.13 μ m and 65 nm RFCMOS technology.....	125
Table 4.2 - Comparing various research works on modeling and optimizing the design of spiral inductors.....	139
Table 5.1 - Comparing various research works on modeling and optimizing the design of differential spiral inductors.....	166
Table 6.1 - Measured vs simulated gain and peak gain frequency for giga-hertz amplifiers with different interconnect widths.....	187
Table 6.2 - Comparing various research works on modeling RF interconnects.....	192

LIST OF SYMBOLS

L	- Inductance
Q	- Quality Factor
R	- Series Resistance
f	- Frequency
ω	- Angular frequency ($2 \times \pi \times$ frequency)
ξ_{PM}	- Peak magnetic energy
ξ_{PE}	- Peak electric energy
ξ_{LOSS}	- Energy loss per cycle
ξ_{AM}	- Average magnetic energy
ξ_{AE}	- Average electric energy
f_0	- Resonant frequency
V_p	- Peak voltage
ρ	- Resistivity
δ	- Skin depth
σ	- Conductivity
μ	- Permeability
λ	- Wavelength
c	- Speed of light
ϵ_r	- Relative permittivity
ϵ_0	- Permittivity of free space
μ_r	- Relative permeability
γ	- Propagation coefficient
α	- Attenuation coefficient
β	- Phase change coefficient
v_p	- Velocity of propagation
Z_0	- Characteristic impedance
Z_{in}	- Input impedance
Z_L	- Impedance along the transmission line
Γ	- Reflection coefficient
S_{DIFF}	- Differential one-port S-parameters
L_{DIFF}	- Differential inductance
Q_{DIFF}	- Differential quality factor
S_{DS21}	- Differential mode to single-ended gain
S_{CS21}	- Common mode to single-ended gain
CMRR	- Common mode rejection ratio
I_F	- Intrinsic factor

Chapter 1 - Introduction

Increasing demands for personal mobile communication equipment have motivated recent research activities to focus on the development of inexpensive, small size, low power consumption and low noise level transceivers. Silicon, with its mature technology, low fabrication cost as well as high packing density is recognized as the only suitable material able to satisfy the needs of this rapidly growing communication market. Nonetheless, several roadblocks such as the availability of high performance integrated inductors, understanding and predicting the effects of RF interconnects as well as difficulties in achieving high-yield RF semiconductor manufacturing processes continue to hinder full exploitations of the silicon technologies.

1.1 Motivation

1.1.1 Business Trends for Wireless Communication Products

The growth of wireless communication has been spectacular if not phenomenal over the past ten years. High density chip integration providing low cost RF solutions is one of the key reasons that contribute to the thriving wireless industry. Single on-chip technology of integrating components onto a common silicon substrate drives the semiconductor industry to an extraordinary rate of evolution. As semiconductor manufacturers continue to embed more functionality into their products with advancing technologies, system-on-chip (SoC) sales are booming, from 345 million units sold in 1999 to 945 million units in 2004, more than 174 % growth in 5 years as shown in Figure 1.1. Going forward, sales forecast looks very positive and it is expected that more than 2.2 billion SoC units worth US\$ 43.2 billion will be sold in 2009 [1].

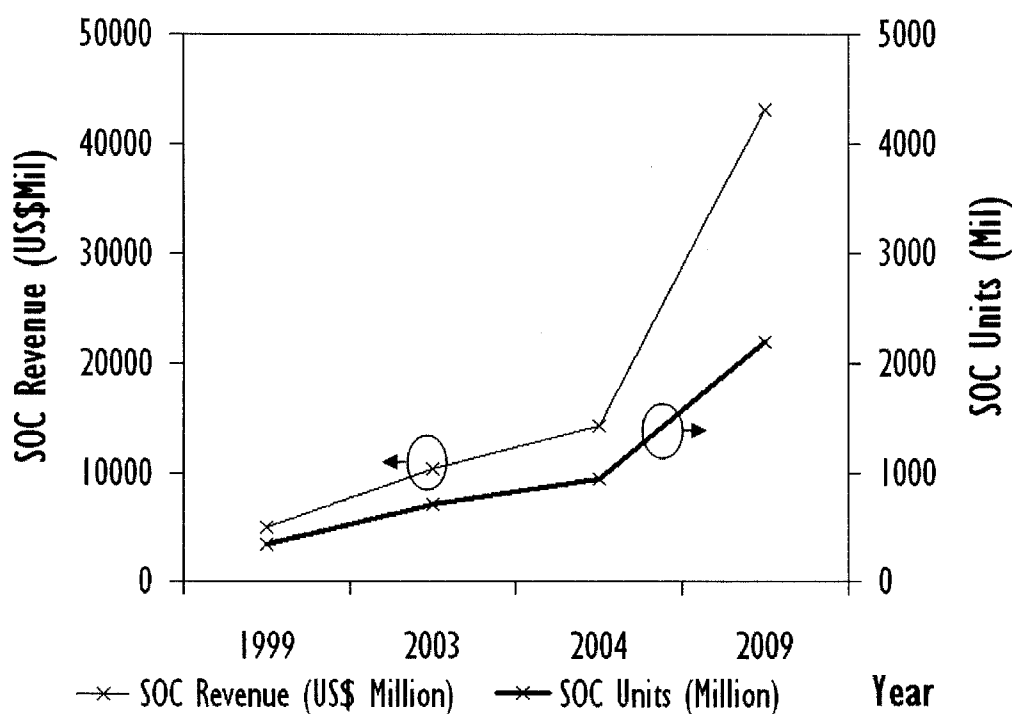


Figure 1.1 - Worldwide SoC sales from 1999 to 2009.

This predicted strong sales performance of SoC components is fuelled by three main factors:

1. Higher average selling prices compared to standalone chips.
2. Aggressive infiltration into existing markets of standalone chips, such as micro-processor unit (MPU), application-specific integrated circuit (ASIC) and digital signal processor (DSP).
3. Emergence and introduction of new end-use markets such as ultra-small mobile gadgets and automobile gadgetry previously seen as impossible to manufacture.

Analyzing the worldwide SoC market in Figure 1.2 [2], 38.5 % of the worldwide market share in 1999 was taken by communication products. In 2004, communication products commanded 57.6 % market share, overtaking the consumer segment by more than 17 %. Beyond 2009, communication products are expected to be the main driving force for the whole SoC market. Behind this flourishing wireless communication market growth is the allocation of the radio spectra, Global System for Mobile Communication (GSM). GSM is currently the dominant format for digital cellular phones, with a global market share of more than 80 % [3], [4]. Having made huge presence in various part of Europe, GSM

continues to gain grounds in emerging markets such as China, India, Africa and Latin America. Some estimates have even shown that there are currently 2 billion GSM users worldwide, with up to 500 million more customers signing up every year [5], [6].

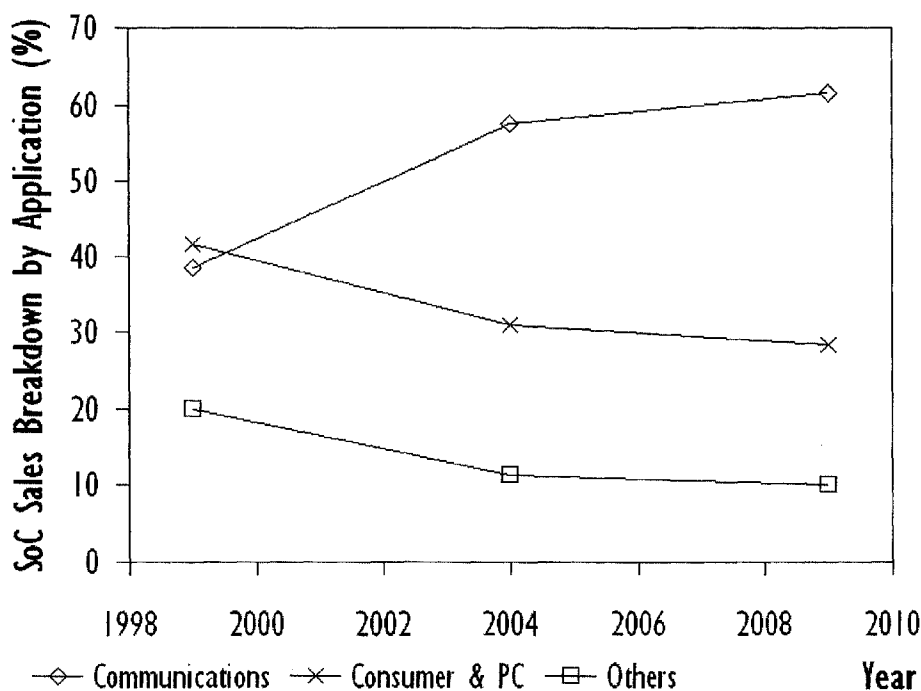


Figure 1.2 - Percentage breakdown of worldwide SoC sales by applications.

It is obvious that SoC is one of the key factors contributing to chip resurgence and massive market growth, but its potential has yet to be fully utilized. Nonetheless, the definition of SoC remains vague, adjusting periodically to technological breakthroughs and differing from one company or industry to another. In an ideal scenario, true SoCs would have everything on a single chip, excluding devices that require large physical forms such as microphones, speakers and camera lenses. Although today's technology still can't live up to this definition, there is little doubt that SoC will continue to play vital roles in many applications that are targeted at the mobile communication industry.

1.1.2 Economic and Technological Perspectives

From an economic point of view, time-to-market and cost effectiveness in product development are the most important aspects to consider in today's competitive IC business

environment. It is therefore the same reasons why SoC is becoming a popular trend now. As an example, most components on the printed circuit board (PCB) for a mobile phone are discrete passive elements typically contributing to about 10 % of the board cost. The required assembly cost is even more substantial, about 30 % of total board cost. Integration of the passive elements into the chip can reduce both component and assembly cost significantly. The use of existing integration technology also suggests that fewer ICs are required to implement a product. As such, total cost of IC packaging and testing decrease radically and with a smaller component count, PCB sizes will reduce considerably converting into more cost savings.

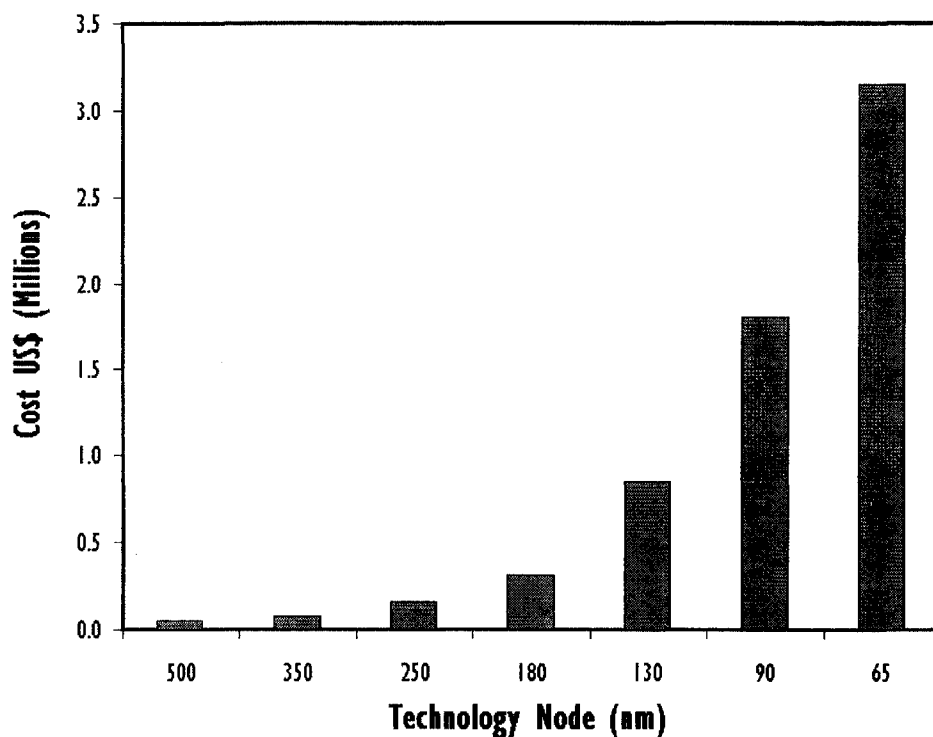


Figure 1.3 - Average mask cost versus technology nodes.

With the escalating mask cost for advanced technological nodes as shown in Figure 1.3 [7], reducing the number of design iterations becomes ever more critical. Recycling and reusing existing silicon-verified circuit intellectual properties (IPs) is now playing a role of increasing importance for SoC product development from a cost management viewpoint. The sharp increase in mask costs is primarily due to the fact that feature sizes with sub-wavelength resolution in the 0.18 μm and below technological nodes are much

smaller than the wavelength of the light use for exposure in the photolithography process. For these masks to deliver sub-wavelength resolutions, elaborate mask-enhancement techniques such as coating of light phase shifting material and optical proximity corrections are required. Hence, the creation of advanced masks is a technically challenging and expensive endeavor requiring new generations of expensive mask writing, inspection and repair tools in every three years to keep up with the technological and manufacturing requirements. To sum up, SoC product development approach not only offers lower implementation costs through component integration but also shorter design cycle and development time by reusing silicon-verified IPs, novel circuits and system architectures.

Single on-chip integration also offers several advantages from a technological perspective namely, power saving, reliability, improved matching, design flexibility and simplification for testing. Traveling RF signals between components on the PCB experience power loss and shifts in operating frequencies when overcoming large parasitic resistances, inductances and capacitances. Caused by bond pads, bond wires, IC packages, PCB traces and discrete packages, such performance degradations can be minimized through component integration when the number of transitions and interfaces between components and ICs are reduced. In short, components and ICs integrations provide more flexibility in designs, enhance system reliability, simplify and shorten the time for IC testing and therefore reduce manufacturing cost extensively.

Nonetheless, for silicon-based RF/Mixed-Signal SoC to succeed, new design methodologies have to be adopted. A modified methodology of [8] is proposed in Figure 1.4. First and foremost, the physical layouts of devices have to be optimized for RF operations. Trade-offs between device performance, layout style of device terminals, physical design parameters and area consumption are carefully considered for application and frequency specific functions. Next, essential devices for developing scalable RF

models are included in a RF test chip based on requirements from RFIC designers. Meanwhile, layouts of these devices are actually generated from parameterized cells since they are eventually customized in the device libraries of process design kits. Upon completion of test chip fabrication, extensive on-wafer device characterization is performed. Accurate and scalable device models with process statistical emphasis are subsequently developed. These SPICE-compatible device models are then consolidated to form silicon-verified device libraries in feature-rich process design kits that have interactive device search engine to help short-list suitable devices based on user-input criteria. Physical verification tools such as layout versus schematics checks, design rule checks and RF layout parasitic extraction essentially ensure error-free IC layout and provide insights as to how post layout parasitics affects the final performance of circuits. Therefore, having design automations with powerful design kits and verification tools coupled with accurate statistical emphasized device models allow successful, cost-effective and efficient one-pass silicon-based RFIC designs.

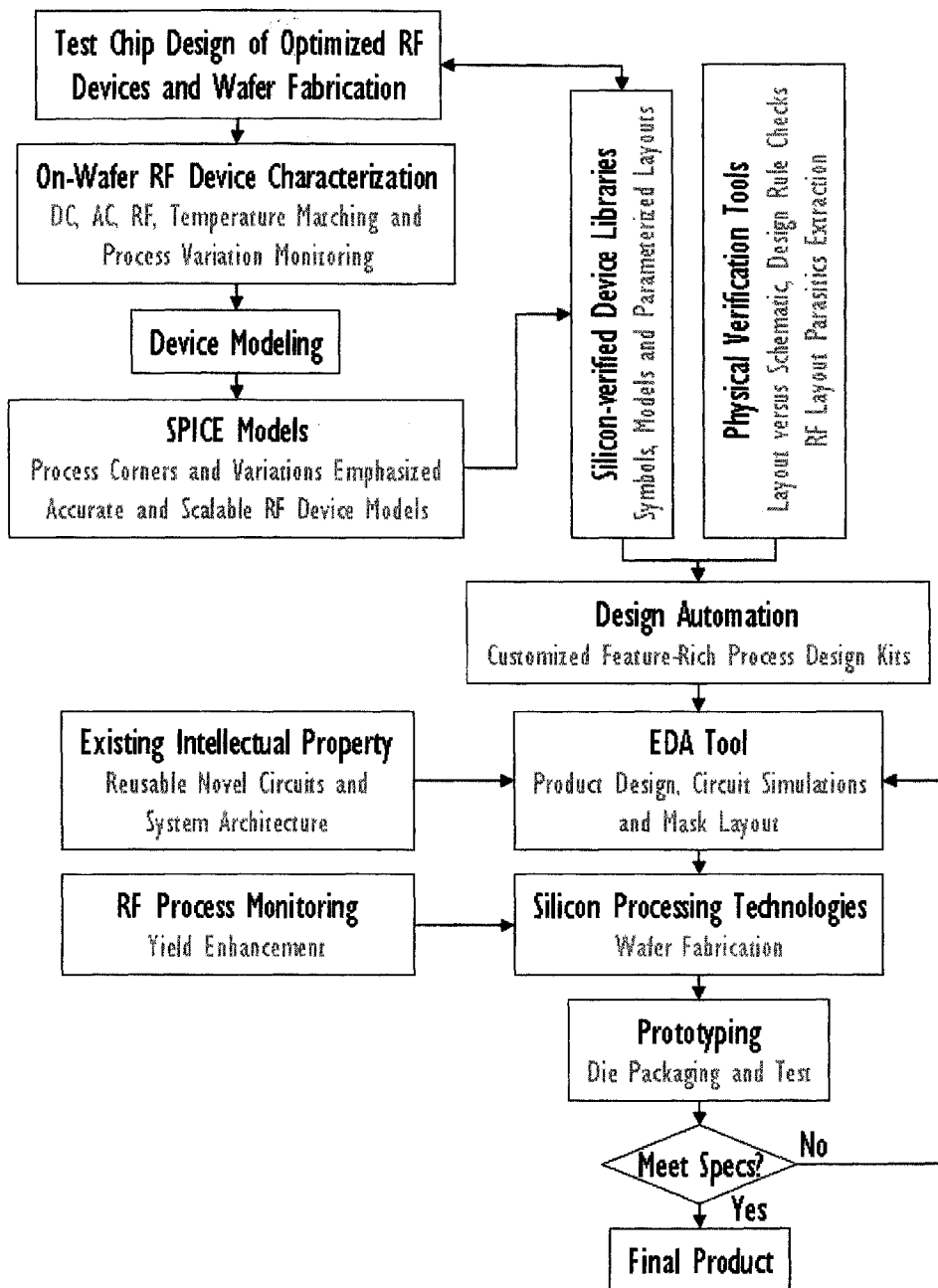


Figure 1.4 - RF SoC design methodology.

1.1.3 Active Devices in Current Silicon Technologies

MOSFETs generally have low power consumption, especially in its standby mode when it is not switching. As a result, it offers very effective solutions for implementing digital functions and circuitries in battery-operated devices. Continual down-scaling of the gate length to nanometers regime allow MOSFETs to have higher unity gain frequency [9], making silicon-based RFICs attractive from integration, power, and cost standpoints. The advancements in new technology nodes with smaller device dimensions and lower supply voltages are primarily driven by rapid growth in microprocessor, telecommunications and wireless applications which consistently demand for more functionalities on smaller chip area without draining battery power and penalizing the performance. Table 1.1 summarizes the active device technology requirements for 0.8 to 10 GHz transceivers from the 2007 International Technology Roadmap for Semiconductor [10].

Table 1.1 - Active device technology requirements for 0.8 to 10 GHz transceivers.

Year of Production		2007	2008	2009	2010	2011
Technology Node		65 nm	57 nm	50 nm	45 nm	40 nm
NPN	Emitter Width (nm)	130	120	100	100	100
	Peak F_t (GHz) [$V_{bc}=1V$]	90	90	100	100	110
	Peak F_{max} (GHz)	170	180	190	200	210
	BV_{ceo} (V)	3.1	3.1	2.9	2.9	2.8
	NF_{min} (dB) at 5 GHz	0.26	0.24	0.20	< 0.2	< 0.2
	I_c ($\mu A/\mu m$) at 50 GHz F_t	28	22	16	15	14
NMOS	V_{dd} (V)	1.2	1.1	1.1	1.0	1.0
	I_{ds} ($\mu A/\mu m$)	13	11	9	8	7
	Peak F_t (GHz)	170	200	240	280	320
	Peak F_{max} (GHz)	200	240	290	340	390
	NF_{min} (dB)	0.25	0.22	0.20	< 0.2	< 0.2

Today, heterogeneous RF subsystems are losing popularity. This is because the communication industry is migrating from integrating multiple costly technologies to utilizing a single low-cost, high-volume processing technology to provide cost-effective

RF solutions. With the emergence of high performance SiGe hetero-junction bipolar transistors [11] and cost-reductions in SiGe processing technology, silicon is even more ready to challenge III-V compound semiconductors' turfs, up to 5 GHz. The goal for RFICs manufacturers is to integrate the RF front end with the analogue/digital base-band processor on a single chip so that a complete radio-on-a-chip solution can be delivered to the communication market. Although packing a complete radio transceiver and DSP base-band functionalities on single chip may be a tricky task because of technological barriers such as noise coupling issues between RF and digital blocks, products with integrated RF front ends manufactured using silicon technologies are already available in the market.

1.1.4 Major Road Blocks in Silicon-based RFIC Designs

Tough challenges lie ahead for RFIC designers when they choose to develop their wireless integrated circuits using silicon technologies. The current deep-submicron CMOS processes continue to use highly conductive silicon substrates for latch-up immunity under tighter design rules. Integrated inductors as well as circuit interconnects fabricated on such lossy substrate suffer from undesirable energy dissipation in terms of capacitive and magnetic losses. In addition, resistive loss of metallization at giga-hertz frequency range not only further degrade the performance of the inductors but introduces more design difficulties as circuit engineers need to carefully consider the effects of the circuit interconnects. Without in-depth studies and good solutions to address these challenges, RFIC designers will have to rely on many costly and time-consuming design iterations before they can succeed in delivering a RFCMOS circuit capable of satisfying the desired specifications.

On-chip inductors, typically used in impedance matching networks, are essential components for major building blocks of a transceiver. Being the largest silicon area-consuming device in an integrated circuit meant for radio frequencies operation, the

number of spiral inductors employed predominantly determines the overall chip area required for the product. Huge device dimensions, lossy nature of the silicon substrate together with high resistive metallization have imposed critical design constraints which are yet to be identified and characterized. The electrical characteristics of such silicon-based integrated inductors are frequency dependent since these parasitics are inevitable part of its design architecture. With exhaustive studies and comprehensive understanding of the trade-offs involved in designing inductors, this research aims at developing a systematic methodology for designing optimized inductors with excellent performance at application specific operating frequencies. Availability of such methodology fully exploits the capabilities and advantages offered by these integrated inductors, ensuring efficient development of useful, accurate and scalable symmetrical and differential spiral inductor device models for circuit simulations.

Interconnects are necessary for providing electrical connections between devices in any circuits. For low frequencies analogue designs, the RC delay attributable to parasitic resistance of the metallization and the associated parasitic capacitances due to surrounding dielectric is an important factor to consider when routing critical signal path. In RF designs, high frequency properties of metal interconnect cannot be ignored. They include non-negligible parasitic inductance, high-resistive skin effects as well as substrate losses. Such effects lead to power losses and undesirable shifts in the circuit's peak performance frequency, resulting in severe circuit performance degradations. The last portion of this research aims to understand these radio frequencies effects and their correlations to circuit performance. Appropriate test structures will be designed and characterized so that accurate and scalable RF interconnect models can be developed. With these SPICE-compatible interconnect models, post layout simulations of RFICs will reveal very accurate predictions of the actual circuit performance. Establishing such correlations are

essential so as to minimize costly design iterations and also, to shorten time-to-market cycle, arriving at a one-pass RFIC design success.

1.2 Objectives

Section 1.1 presented the motivations for pursuing the topic of SoC integration for RF applications, from the economic and technological perspectives. RF SoC integration encompasses a wide span of disciplines and in each of these aspects, requires devotion of huge research and development resources. This research will only focus on studying and developing solutions to address the major obstacles mentioned in Section 1.1.4.

The objectives of this research work are summarized as follows:

1. To identify the loss mechanisms that degrades the performance of silicon-based on-chip spiral inductors.
2. To design, understand, explore and optimize the physical dimensions of conventional spiral inductors thereby improving their performance.
3. To develop a new methodology for designing conventional spiral inductors with optimized performance at application specific frequency and demonstrate its circuit level impact.
4. Based on the findings derived from the third objective, with regards to symmetrical and differential spiral inductors, the following are to be achieved:
 - a. To streamline inductor testchip designs aim at reducing testchip size and hence fabrication and test costs.
 - b. To develop scalable and accurate SPICE-compatible models which must be verify at circuit level.
 - c. To further extend optimization of these inductors to operating frequencies beyond 2.4 GHz.
5. To propose new figure of merits for RF interconnects.
6. To develop a scalable and accurate SPICE-compatible model for RF interconnects.
7. To determine the correlations between the interconnects' physical dimensions and the performance of RF circuits.

1.3 Major Contributions of the Thesis

In this work, a ground-breaking experimental technique of investigating effects of spiral inductors' physical design parameters has been proposed. Designing sets of inductors with similar inductances by maintaining identical conductor length facilitated unbiased experimental comparisons which help revealed pioneering findings. It has been demonstrated that the selection of inductor's core diameter is of utmost importance, as it greatly affects the inductor's performance and physical size. To attain larger inductance values, and to have smaller silicon area, the conductor-to-conductor spacing is best to be kept at the smallest value permitted by the layout rules. A novel optimization methodology has successfully aligned the peak quality factor frequency of the aluminum and copper-based spiral inductors, over a wide range of inductance values, for circuit operating frequencies of up to 2.4 GHz. Giga-hertz amplifier using such optimized inductors is shown to allow superior gain, better input/output matching characteristics and lower noise figure. These results are discussed in Chapter 3 and published in the IEEE Transactions on Electron Devices.

The layout optimization technique in Chapter 3 institutes a framework that streamlines test chip design considerations for developing symmetrical and differential inductor SPICE models, establishing design boundaries that reduces testchip size and ensures final device libraries contain inductors having fine inductance steps. For the first time, unbiased performance comparisons with identical inductances are made possible at frequencies up to 10 GHz because these inductor models have excellent accuracy and scalability. Optimal conductor widths for operating frequencies above 2.4 GHz have been determined and it has been found that at these frequencies, further reduction of width maintains performance improvement and reduces device size significantly. This work is outlined in Chapter 4 and 5 and has been published in the IEEE Transactions on Electron Devices.

Fabricated RF circuits will suffer unknown amount of power loss and shifts in operating frequencies if interconnects are not considered during circuit simulations. To tackle this issue, RF interconnect test structures are designed, characterized and modeled to predict their RF characteristics. Proposed in this research work is a new figure of merit called Intrinsic Factor, which conveniently guides circuit designers in choosing appropriate interconnects with the smallest parasitics for device routing. The SPICE simulator-compatible double- π interconnect model adopted in this work accurately emulate the RF characteristics of metal lines, exhibiting continuity and scalability across the physical dimensions of interconnects. It offers prior knowledge of RFICs' final performance after layout with interconnects, which will help avoid costly design iterations and reduce time-to-market for new RF products. This work is presented in Chapter 6 and published in IEEE Transactions on Microwave Theory and Techniques.

1.4 Organization of the Thesis

Chapter 1 presents the background and motivation for this research work. Present and future trends for SoC technology are reviewed from both the economic and technological perspectives. Advancements in active devices for silicon technologies are also highlighted. Major roadblocks hindering exploitations of silicon technologies for RFIC applications define the scope and objectives of this research work.

Various loss mechanisms that affect the performance of spiral inductors are analyzed in Chapter 2. The literature review presented summarizes the current problems and various techniques used in today's technology to improve the performance for silicon-based integrated inductors. Important figure of merits such as inductance and quality factor are discussed. Transmission line theories for interconnects and existing methodologies that manage post layout parasitics have been reviewed. On-wafer RF characterization of silicon devices, which includes test instrument calibration and test structures de-embedding techniques, are discussed towards the end of this chapter.

Chapter 3 presents experimental setups that help evaluate and study the effects of various physical dimensions such as core diameter, spacing and width for conventional spiral inductors. A new methodology is proposed to optimize the physical layout of spiral inductors such that its performance is aligned to the operating frequencies of RF circuitries. This methodology provides insights to the trade-offs between the performance and area that is consumed by an integrated inductor, for up to 2.4 GHz. Giga-hertz amplifiers are used to demonstrate the impact and circuit improvements when such optimized inductors are utilized in silicon-based RFIC designs.

Chapters 4 and 5 extended the work in Chapter 3, demonstrating how streamlined testchips of symmetrical and differential inductors can be designed to build accurate and scalable inductor models that cater for a wide range of application frequencies. The

physical layouts of these symmetrical and differential inductors, for a particular application frequency, are efficiently optimized by using their scalable models. These highly accurate models have provided new insights to the trade-offs between performance and area, for both the differential and symmetrical spiral inductors, up to 10 GHz operations. A single-ended input to differential output giga-hertz amplifier has been used to investigate and demonstrate model accuracy and scalability for the symmetrical and differential inductors.

The focus of Chapter 6 is to investigate and predict the detrimental effect of introducing interconnects in RF circuit designs. A new figure of merit for interconnects is proposed for the first time. Interconnect test structures for developing SPICE-compatible RF interconnect models are designed and fabricated. A scalable and accurate SPICE model is presented and correlations between the measured and simulated circuit performances of giga-hertz amplifiers are studied. The recommended SPICE model is also demonstrated to work for transient simulations when it improved the associations between the measured and simulated results for a voltage-controlled oscillator.

Chapter 7 concludes the findings for this work and proposes topics for further research.

Chapter 2 - Literature Review

2.1 Integrated Spiral Inductors on Silicon

Inductors are passive electronic components that store energy in the form of magnetic flux. In its simplest form, an inductor consists of a wire loop or coil. Its inductance is dependent on the total conductor length of the coil and also the magnetic properties of the material around which the coil is wound. Inductors when connected in series or parallel configurations can provide discrimination against unwanted signals and they are essentially used in matching networks, resonators in Voltage Control Oscillators (VCOs) and degenerator in Low Noise Amplifiers (LNAs).

Discrete inductors are usually in the form of solenoid coils because of the large mutual coupling between turns and the ease of inserting high-permeability (μ) material inside the coil to increase the inductance, L and quality factor, Q . In silicon technology, conventional 3-dimensional coils are difficult to realize as there are limitations to the maximum number of metal layers in the existing process flows. The inter-metal dielectric between metal layers results in huge overlap capacitances and thus lowers the maximum usable frequency considerably. Quality factor of such coils also suffer due to large via resistances. Spiral planar inductors are therefore more compatible with the back-end metallization schemes of present silicon technologies.

2.1.1 Figure of Merits for Spiral Inductors

The important parameters used in defining the performance of an inductor are its inductance value, quality factor and self-resonant frequency. Quantitatively, the impedance of a real inductor increases with frequency until it reaches self-resonance, whereby the parasitic capacitances resonate with the inductor. Beyond its self-resonant frequency, the inductor behaves like a capacitor and its impedance decreases with frequency.

2.1.1.1 Inductance Value, L

The inductance value of a rectangular planar spiral inductor can be accurately estimated using the procedures outlined in the Greenhouse's paper [12]. Accordingly, the overall inductance of a monolithic inductor is given by the sum of all the self-inductance of individual segments, plus the sum of all positive mutual inductances between adjacent segments, minus the sum of all negative inductances between segments on opposite sides of the spiral. Figure 2.1 identifies the respective inductance components in the inductor.

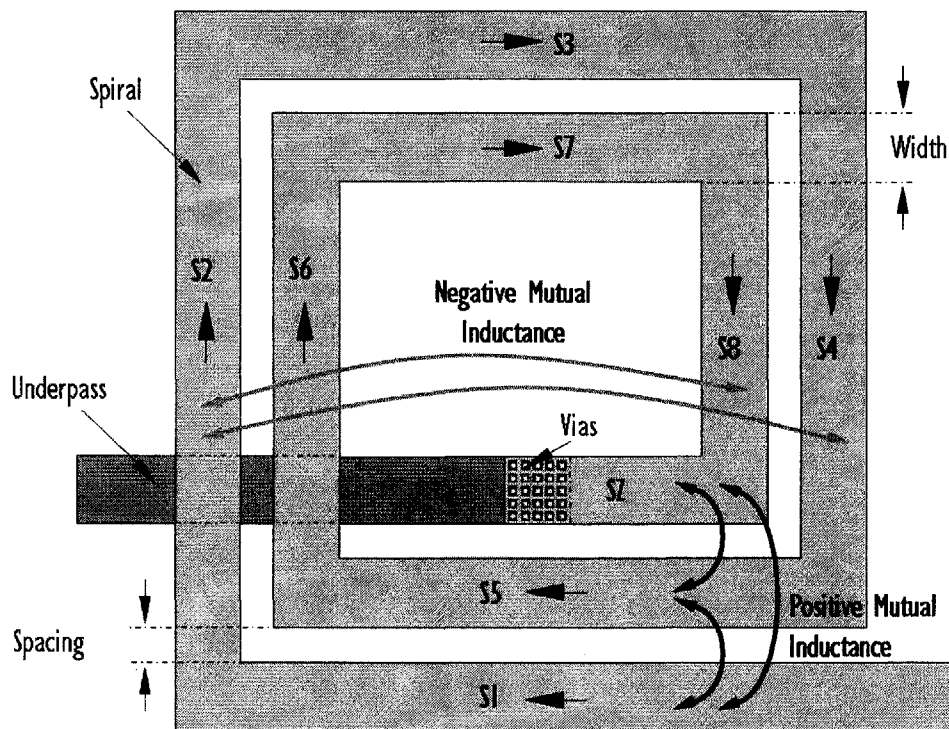


Figure 2.1 - Positive and negative mutual inductance components in a rectangular inductor.

In silicon processing technology, all metal line segments have a rectangular cross section and for a relative permeability of aluminum as 1.000021, the self-inductance of a line segment for a lossless substrate can be computed using Equation 2.1 [12],

$$L_{self} = 0.002l \left[\ln \left(\frac{2l}{w+t} \right) + 0.50049 + \left(\frac{w+t}{3l} \right) \right] nH \quad (2.1)$$

where l is the length, w is the line width and t the thickness of the metal line. All the dimensions for length are given in centimeters.

The mutual inductance between any two line segments can be computed using the following equations [12],

$$M(l, d, w) = 2 \cdot l \cdot Q(l, d, w) \text{ nH} \quad (2.2)$$

where l is the length of each segment, d is the centre to centre separation between lines and w is the width of the metal line. The function Q in Equation 2.2 is defined as,

$$Q(l, d, w) = \ln \left(\frac{l}{GMD(d, w)} + \sqrt{1 + \frac{l^2}{GMD^2(d, w)}} \right) - \sqrt{1 + \frac{GMD^2(d, w)}{l^2}} + \frac{GMD(d, w)}{l} \quad (2.3)$$

and the geometric mean distance GMD of two lines is,

$$\ln GMD(d, w) = \ln d - \left[\frac{1}{12 \left[\frac{d}{w} \right]^2} + \frac{1}{60 \left[\frac{d}{w} \right]^4} + \frac{1}{168 \left[\frac{d}{w} \right]^6} + \frac{1}{360 \left[\frac{d}{w} \right]^8} + \dots \right] \quad (2.4)$$

For metal lines of unequal length as shown in Figure 2.2, the mutual inductance is calculated using,

$$2 \cdot M_{A,B} = [M(b + p, d, w) + M(b + q, d, w)] - [M(p, d, w) + M(q, d, w)] \quad (2.5)$$

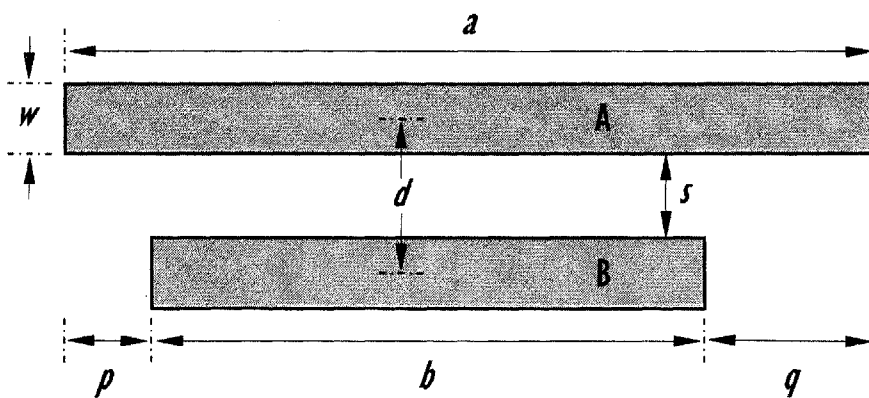


Figure 2.2 - Mutual inductance between two metal segments, A and B.

The mutual inductance of two metal segments is positive if the currents are flowing in the same direction and negative if currents are in the opposite direction. With reference to Figure 2.1, for a rectangular planar inductor with two complete turns and eight segments,

its total inductance is equal to the sum of the self-inductances, L of each segments and all the mutual inductances, M between the segments as described in Equation 2.6.

$$L_{\text{total}} = \sum L + \sum M$$

$$L_{\text{total}} = L_1 + L_2 + L_3 + L_4 + L_5 + L_6 + L_7 + L_8 + 2[(M_{1,5} + M_{2,6} + M_{3,7} + M_{4,8}) - (M_{1,7} + M_{1,3} + M_{5,7} + M_{5,3} + M_{2,8} + M_{2,4} + M_{6,8} + M_{6,4})] \quad (2.6)$$

where L_X refers to the self-inductance of segment X and $M_{X,Y}$ refers to the mutual inductance between segments X and Y .

Such equations can be implemented in MATLAB scripts to evaluate the inductance of various inductor geometries. Through this winding geometry trade-off study, it has been found that inductive characteristics of spiral inductors can be improved if there is no winding of metal conductors in the centre of the spiral. This is so because negative mutual coupling effect reduces when distance between the four segments (S6, S7, S8 and SZ in Figure 2.1) with opposite current flow increases. However, the core diameter is expected to become larger which inevitably increases the overall size of the inductor.

The width of these metal segments should be large so that resistances of the metal segments are kept low. Nonetheless, having a large width reduces the inductance per unit conductor length and increases the parasitic shunt capacitances of the inductor, which in turn degrades the resonant frequency as well as quality factor of the inductor. In addition to the above findings, metal spacing between conductors should be kept as close as possible, i.e. the minimum design rule for the process. This will save on the silicon area occupied by the inductor and promote constructive mutual coupling, thereby increasing the overall inductance of the inductor. Such preliminary analyses reveal some ideas as to how the physical layout of spiral inductors can be optimized. Even so, all the physical design parameters are inter-related and hence, to understand the effects of each design parameters would require in-depth studies especially for inductors fabricated using high resistive metallization on lossy silicon substrates.

2.1.1.2 Quality Factor, Q-factor

The efficiency of an inductor is determined by its quality factor or Q-factor. Basic physical definitions for the Q-factor are defined as follows:

$$2\pi \times \frac{\text{Energy Stored}}{\text{Energy Dissipated per Cycle}} \quad (2.7a)$$

$$\text{or } \omega \times \frac{\text{Energy Stored}}{\text{Average Power Dissipated}} \quad (2.7b)$$

It is interesting to note that the expression for quality factor is dimensionless and proportional to the ratio of energy stored to energy dissipated per unit time cycle. The quality factor expressions shown in Equations 2.7a and 2.7b are general and fundamental definitions, which can be applied to different systems. These definitions are fundamental because they do not specify the type or form in which the energy is stored or dissipated. Coincidentally, for electrical systems, both Equations 2.7a and 2.7b define the quality factor for a LC tank. The subtle distinction in quality factor between an inductor and a LC tank therefore lies in the intended form of energy storage.

For a LC tank, the Q-factor serves to provide an indication of how much energy is lost as it is being transferred between the capacitor and the inductor. The energy stored in a LC tank is actually the sum of the average magnetic and electric energies, and for a lossless LC tank, this energy is constant because it oscillates between magnetic and electric forms. As such, it can be equal to the peak magnetic energy, or the peak electric energy [13]. The rate of this oscillation is known as the resonant frequency of the tank. Since there is no energy dissipation, the Q-factor is infinite for a lossless LC tank.

On the contrary, an inductor is designed primarily to store magnetic energy and hence only energy stored in the magnetic field is of interest. All other energies stored in the form of electric field or those dissipated due to parasitic resistances are counterproductive. Therefore, the quality factor of an inductor is proportional to the net magnetic energy

stored, which is the difference between the peak magnetic and electric energies. Also, the inductor is said to be at self-resonance, when its peak magnetic and electric energies are equal. Hence, at this self-resonant frequency, the inductor's quality factor vanishes to zero and no net magnetic energy is obtainable from the inductor to any external circuit. Above its self-resonant frequency, the inductor behaves like a capacitor.

To demonstrate the subtle distinction between these two cases mentioned above, consider a simple parallel RLC circuit to be first modeled as a real inductor with substrate parasitics, R and C, and subsequently modeled as a LC tank. Figure 2.3 shows the circuit of a parallel RLC tank.

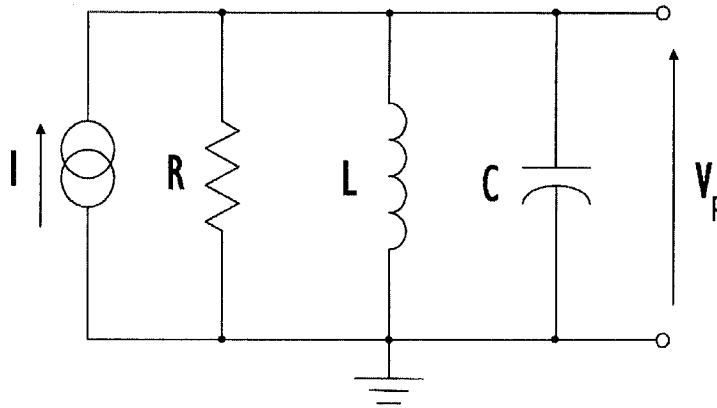


Figure 2.3 - Parallel RLC circuit.

The following show the expressions for the electric and magnetic energies, which are required to derive the quality factor for both cases, as an inductor and as a LC tank. The peak magnetic energy of the circuit shown in Figure 2.3 is given by,

$$\begin{aligned}
 \xi_{\text{PM}} &= \frac{1}{2}LI^2 \\
 &= \frac{1}{2}L\left(\frac{V_p}{X_L}\right)^2 \\
 &= \frac{1}{2}L\left(\frac{V_p^2}{\omega^2L^2}\right) \\
 &= \frac{V_p^2}{2\omega^2L}
 \end{aligned} \tag{2.8}$$

The peak electric energy is given by,

$$\begin{aligned}\xi_{PE} &= \frac{1}{2} CV^2 \\ &= \frac{1}{2} CV_p^2\end{aligned}\quad (2.9)$$

The energy loss per cycle is,

$$\begin{aligned}\xi_{LOSS} &= \frac{2\pi}{\omega} |I|^2 R \\ &= \frac{2\pi}{\omega} \left(\frac{V_p}{\sqrt{2R}} \right)^2 R \\ &= \frac{\pi}{\omega} \times \frac{V_p^2}{R}\end{aligned}\quad (2.10)$$

The average magnetic energy is given by,

$$\xi_{AM} = \frac{V_p^2}{4\omega^2 L} \quad (2.11)$$

The average electric energy is given by,

$$\xi_{AE} = \frac{1}{4} CV_p^2 \quad (2.12)$$

And the resonant frequency is given by,

$$f_o = \frac{1}{2\pi\sqrt{LC}} \quad (2.13)$$

where V_p represents the peak voltage across the circuit terminals of Figure 2.3. Using the expressions from Equations 2.8 to 2.13, the Q-factor for an inductor and the LC tank are defined as follow:

$$\begin{aligned}Q_{\text{Inductor}} &= 2\pi \cdot \frac{\text{Peak Magnetic Energy} - \text{Peak Electric Energy}}{\text{Energy Loss Per Cycle}} \\ &= \frac{R}{\omega L} \left[1 - \left(\frac{\omega}{\omega_o} \right)^2 \right]\end{aligned}\quad (2.14)$$

With reference to a spiral inductor built on silicon, C can be regarded as representing the parasitic capacitances of the substrate. R on the other hand represents the resistance of the substrate underneath the inductor. Quality factor of the inductor, Q_{Inductor} as shown in Equation 2.14, is equal to zero when the inductor is operating at its resonant frequency

(i.e. $\omega = \omega_0$). This self-resonance phenomenon occurs due to the undesirable energy dissipation or energy loss into the conductive silicon substrate.

$$\begin{aligned}
 Q_{LC \text{ Tank}} &= 2\pi \cdot \frac{\text{Average Magnetic Energy} + \text{Average Electric Energy}}{\text{Energy Loss Per Cycle}} \Bigg|_{\omega = \omega_0} \\
 &= 2\pi \cdot \frac{\text{Peak Magnetic Energy}}{\text{Energy Loss Per Cycle}} \Bigg|_{\omega = \omega_0} \\
 &= \frac{R}{\omega_0 L} \tag{2.15} \\
 \text{or} \quad &= 2\pi \cdot \frac{\text{Peak Electric Energy}}{\text{Energy Loss Per Cycle}} \Bigg|_{\omega = \omega_0} \\
 &= \omega_0 RC
 \end{aligned}$$

The Q-factor of the LC tank circuit is very important in electronic communications because it determines the 3 dB bandwidth of resonant circuits. This bandwidth of a LC tank defines the amount of signal that can be transmitted and the amount of noise, which can be attenuated by a circuit.

Both definitions in Equations 2.14 and 2.15 are important and their applications are actually determined by the intended function of a circuit. However, to evaluate the Q-factor of an on-chip inductor as a single element, the definition of Equation 2.14 will be used. Nonetheless, in actual device measurements, both L and Q are extracted from measured S-parameters after employing proper test structure de-embedding techniques.

2.1.2 Advantages in using Silicon-based Spiral Inductors

High quality factor integrated inductors are essential components to monolithic integration of RF circuits on silicon. Due to the enormous market potential of wireless communication, improving performances of RF circuit elements for the cellular bands have generated a lot of interests among researchers in this field. Though expensive, traditional substrate materials such as GaAs or quartz have provided superior microwave performance for the realization of both active and passive elements over the years. However, in reality, cost is the key concern in bringing high frequency personal communication equipment into the consumer market.

The silicon technology has offered an effective solution. Silicon's ever-improving capabilities, driven by rapid microprocessor development, are making itself more cost efficient than the GaAs technology for RF applications up to 5 GHz. Beside affordable manufacturing costs, other advantages included the following:

- Good conductor of heat
- High level of integration through multi-level interconnect metallization
- Availability of CMOS, BJT, BiCMOS and SiGe transistors
- Excellent planarity for all existing bonding technologies
- Possibility of system-on-chip, SOC solutions

In comparison to GaAs or quartz substrates, silicon does not exhibit any outstanding microwave properties. Silicon substrates for CMOS applications are predominantly lossy and hence, will without doubt degrade the inductor's quality factor at high frequencies. This situation is expected to be even more critical as the CMOS technology node scales down further. In these advanced nodes, silicon substrates with increasingly higher conductivity would have to be used to eliminate latch-up occurrences at tighter design rules. Despite having poor microwave properties, the communication industry is tolerant towards the silicon technology since manufacturing cost is simply too attractive. Hence,

the challenging task of exploiting the benefits of the silicon technology for RFIC applications has attracted and motivated a lot of fellow researchers and engineers over the last ten years.

2.1.3 Identifying Loss Mechanisms in Silicon-based Spiral Inductors

In-depth understandings as to why the silicon technology produces inferior inductors have to be attained before embarking on any further research to improve their performances. Loss mechanisms in silicon-based integrated inductors can be classified into four categories, namely, metallization resistive loss, substrate capacitive and resistive losses as well as formation of substrate eddy current. These are the main reasons why performance of silicon-based inductors is sometimes not acceptable and accurate predictions of quality factor are often difficult to make even with reliable electromagnetic simulation tools.

2.1.3.1 Metallization Resistive Loss

At low frequencies, the current flow within a metal conductor trace is uniform and its series resistance (R) can be easily determined by,

$$R = \rho \frac{l}{A} \quad (2.16)$$

where ρ is the resistivity of the metal used, l refers to the length and A the cross-sectional area of the metal conductor. However, at high frequencies, the induced electromotive force (EMF) causes a non-uniform current distribution in the inductor. This non-uniform current flows along the conductor surface, effectively reduces the cross-sectional area of the conductor. As a result, there is an increase in the series resistance, which causes a net reduction in the quality factor of the inductor. This phenomenon is known as the skin effect and it is directly proportional to the operating frequency.

Skin depth, δ is defined [14] as,

$$\begin{aligned}\delta &= \sqrt{\frac{2}{\omega\mu\sigma}} \\ &= \frac{1}{\sqrt{\pi f\mu\sigma}}\end{aligned}\quad (2.17)$$

where f refers to the frequency, σ is the conductivity and μ is the permeability of the metal conductor. Since skin depth, δ , is inversely proportional to frequency, at higher frequencies, δ decreases and this suggests that there is lesser low resistive path within the conductor for current to flow easily. Hence, resistance of the conductor increases with operating frequency.

From Equation 2.17, the skin resistance, R_{skin} (Ω/m^2), can be defined as,

$$\begin{aligned}R_{\text{skin}} &= \frac{1}{\sigma\delta} \\ &= \sqrt{\frac{\pi f\mu}{\sigma}}\end{aligned}\quad (2.18)$$

Increasing the metal thickness of the inductor coil can minimize resistive losses, thereby improving the inductor's quality factor. This is especially so for the CMOS technology because the metal thickness is typically between 0.25 μm to 0.7 μm . Many experimental results have shown that the Q-factor improves significantly when the metal thickness increases from 0.25 μm to 1.0 μm . This is due to massive reduction in the series resistance of the metal coil at low frequencies.

However, because of skin effect, the Q-factor will only increase at a much slower rate when the metal thickness continues to increase any further. According to [15], the skin depth of aluminum is about 2.5 μm at 2 GHz. This suggests that when the metal thickness is thinner than 2.5 μm , current still flows uniformly in the metal coil. When the metal conductor thickness is greater than the skin depth (i.e. 2.5 μm), current will only flow along the surface of the metal at a depth of only 2.5 μm . In addition, it also shows that the

series resistance (R_s) does not decrease with any further increase in the metal thickness. In general, to avoid skin effects at any desired operating frequencies, the inductor's metal thickness should be as large as possible so that high quality factor can be achieved.

2.1.3.2 Substrate Capacitive and Resistive Loss

The conventional silicon-based spiral inductor is usually fabricated using top and second highest metal layers and it sits on top of the inter-metal dielectric layers (which are made up of silicon dioxide) and the silicon substrate. The layers of silicon oxide and the substrate itself contribute to unwanted capacitive coupling, which degrades the self-resonant frequency of the inductor. The self-resonant frequency, f_0 , [16] of an inductor is defined as the frequency at which parallel resonance is achieved between the device's inductance and its parasitic capacitances and resistances. Here, the parasitic capacitances refer to the oxide capacitance between the inductor and silicon substrate and capacitance of the silicon substrate. The parasitic resistance, on the other hand, refers to the resistance of the silicon substrate. Ideally, the substrate and the oxide layer should not be capacitive and should have infinite resistivity so as to minimize unwanted substrate coupling. Inductors built on such ideal substrate will have high quality factor and high self-resonant frequency.

The presence of these parasitic components promotes undesirable energy dissipation and loss into the silicon substrate, which will also degrade the Q-factor of the inductor. The distributed structure of spiral inductors together with the complexity of all these parasitic components make it difficult to estimate both Q-factor and f_0 of the inductor. Even with tedious and time consuming electromagnetic field simulations, accurate predictions still require well-calibrated technology files that completely describe all the materials properties present in the architecture of the spiral inductor. Therefore, to understand the effects of these parasitics and their impact on the overall device performance, actual

device characteristics are very much preferred so that these measured data can help develop a physical, accurate and scalable inductor model.

2.1.3.3 Substrate Eddy Current

Figure 2.4 shows the top and cross-sectional views of an inductor fabricated on silicon substrate. Inductors experience magnetic losses when they are built flatly on a highly conductive silicon substrate. According to Faraday's law, an image current or eddy current is induced in the substrate underneath the spiral coil when a current, I_{spiral} is flowing in the inductor. Since the silicon substrate has low resistivity, this image current can flow easily. In compliance with Lenz's law, the direction of flow for this induced current is opposite to that of the inductor. This generates an opposing parasitic magnetic field in the substrate, which interacts with the magnetic field of the inductor and results in a degradation of the inductor's overall useful inductance. Formation of image current in the substrate and its magnetic flux interaction with that of the inductor is illustrated in Figure 2.4.

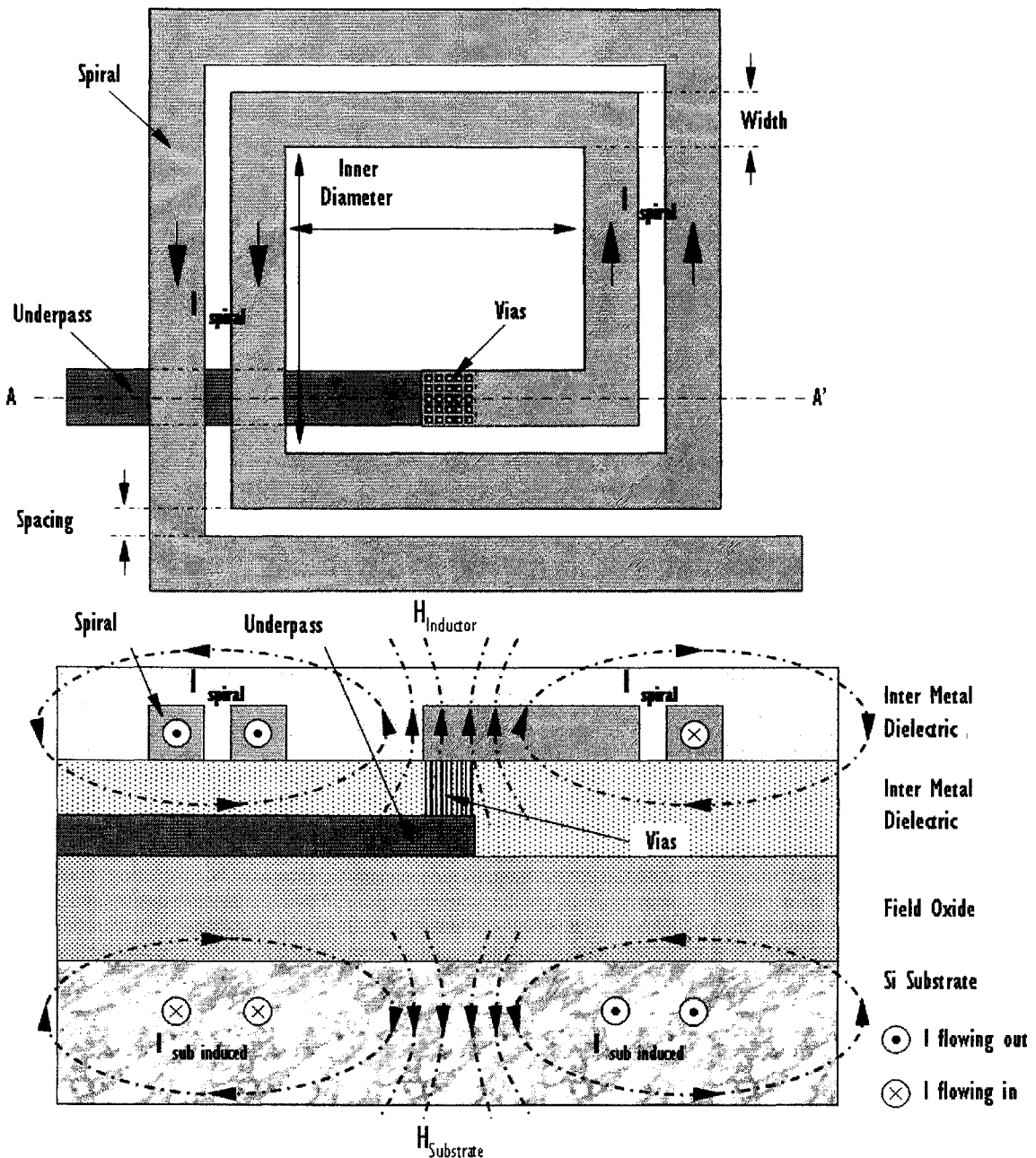


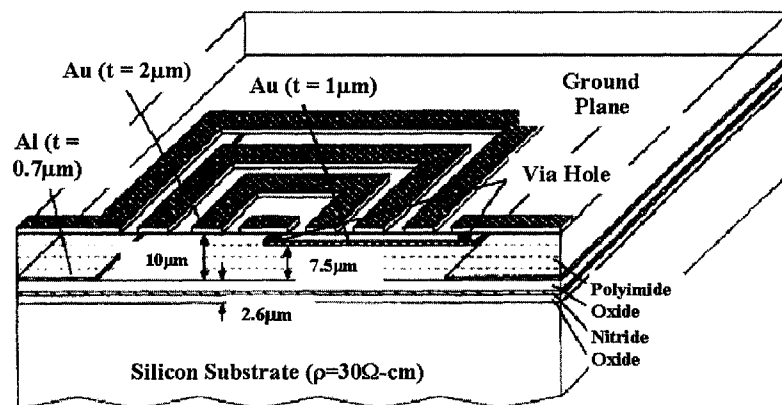
Figure 2.4 - Formation of image current and its magnetic flux interaction with that of the inductor.

2.1.4 Q-Factor Enhancement Techniques

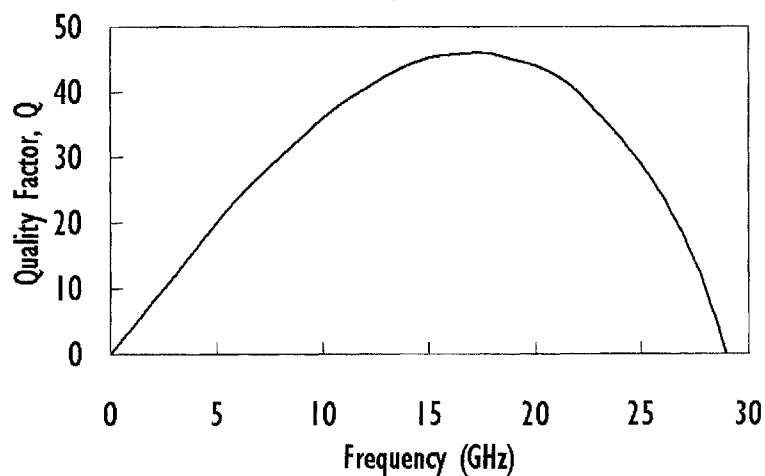
Numerous techniques have been used to enhance the performance of on-chip silicon-based spiral inductors since its implementation. A number of researchers have come up with techniques to improve the Q-factor of the spiral inductor with many reported breakthroughs. The following sections will consolidate some of these methods and techniques that are found to have improved the performance of the spiral inductors.

2.1.4.1 Q-Factor Enhancement using Processing Technologies

Kamogawa [17] presented a high-Q inductor fabricated on a conductive Si substrate using monolithic microwave integrated circuit (MMIC) technology. Figure 2.5(a) illustrates the architecture of this inductor. Conductor resistive loss is minimized by the implementation of Gold (Au) metallization while substrate losses and the parasitic capacitance are eliminated by the special dielectric stack and ground plane placed between the spiral and the substrate. The special polyimide layer with low dielectric constant further reduces the shunt capacitance to the ground plane, allowing the inductor to have a high resonant frequency. Figure 2.5(b) shows the Q-factor plot of this inductor. Indeed, good inductive characteristics are observed, but fabrication of such inductor can be expensive, involving non-standard CMOS process flows.



(a)



(b)

Figure 2.5 - Cross-sectional view (a) and performance (b) of inductor fabricated using MMIC technology.

In another publication [18], Joachim, Mehmet and Keith presented a high Q-factor, three-layer metal inductor, fabricated using the multi-level interconnect technology available in the CMOS process. Figure 2.6(a) shows the cross-sectional view of this inductor with stacked metal layers. The spiral of the inductor is actually made up of Metal 2, Metal 3 and Metal 4, shorted using Via 2 and Via 3, to reduce the conductor series resistance. In Figure 2.6(b), Q-factor of the inductor improves significantly due to a huge reduction in series resistance of the spiral coil. Nevertheless, the whole inductor structure is brought closer to the silicon substrate and inevitably increases the parasitic capacitance. This not only degrades the inductor's Q-factor at higher frequencies but also causes a reduction in its self-resonant frequency. Such techniques work well for small inductors but may not be applicable to large-inductance inductors since they require much bigger area, suggesting that their parasitic capacitance would be too huge to allow for high Q-factor and self-resonant frequency.

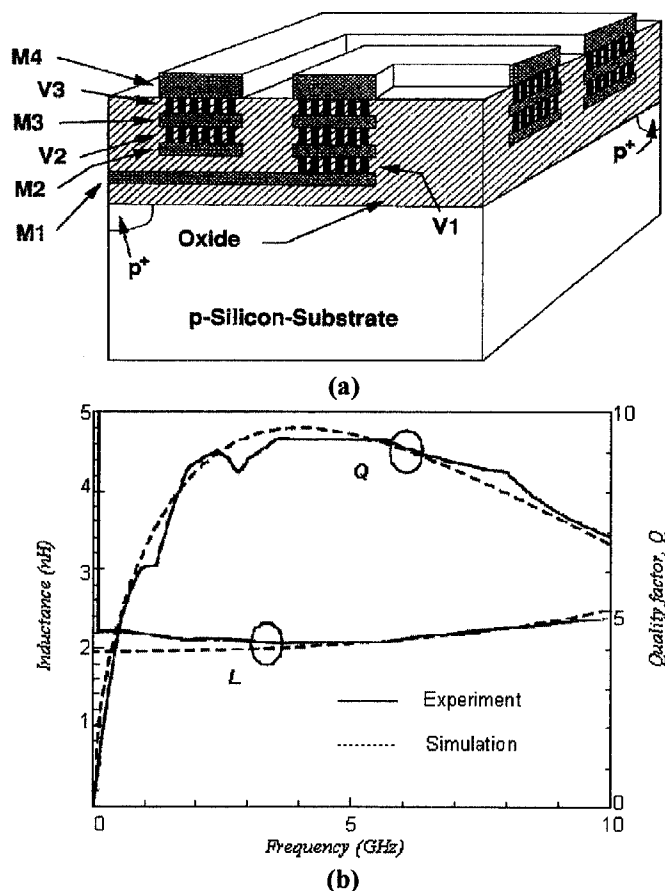


Figure 2.6 - Cross-sectional view (a) and performance (b) of spiral inductor using 4-Level metallization.

Daniel and Joachim also investigated the performance of inductors fabricated on quartz substrates as well as those fabricated using the copper damascene interconnect technology [19]. The copper damascene process has been fully capitalized to improve the performance of spiral inductors by allowing the use of metallization with lower resistivity and ability to fabricate thicker multi-level metal layers. It has been demonstrated in Figure 2.7(a) that the inductor with thicker top metal ($4\ \mu\text{m}$) has a better Q-factor at all frequencies. Improvements in the inductor's Q-factor and resonant frequency are also remarkable when its silicon substrate is replaced with a lossless quartz substrate. Eliminating substrate loss completely, Figure 2.7(b) shows the Q-factor and inductance comparison for inductors with silicon and quartz substrate.

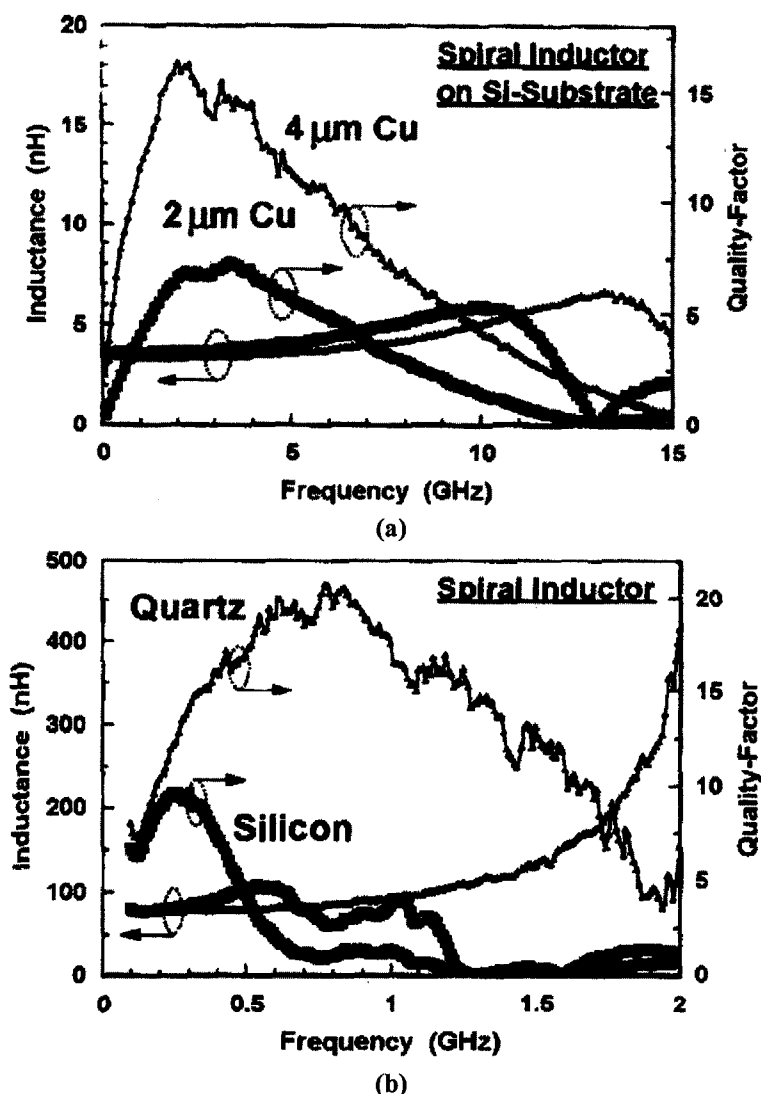


Figure 2.7 - Performance comparison of Cu spiral Inductors with different metal thickness (a) and inductors with silicon and quartz substrates (b).

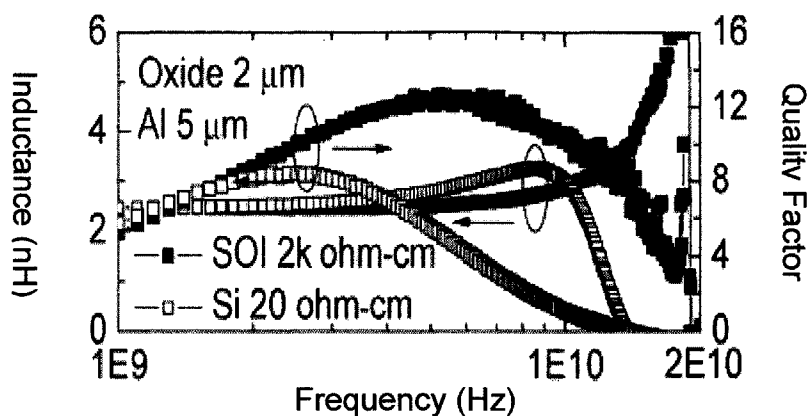


Figure 2.8 - Comparing inductor performance on SOI and bulk silicon.

In 2006, Xi’an Jiao Tong University in China examined the performance of spiral inductors fabricated using silicon-on-insulator (SOI) technology [20]. They have reported that spiral inductors on high resistive SOI (2 kΩ-cm) substrates out-performed those designed on conventional bulk silicon (20 Ω-cm). Shown in Figure 2.8, the 2.3 nH spiral inductor on high-resistive SOI substrate has maximum Q-factor value that is 50 % larger compared to the spiral inductor constructed on conventional bulk silicon substrate. In the same year, University of California uses high Q-factor inductors in SOI CMOS technology to achieve a low power 700 MHz VCO with a phase noise performance of -121 dBc/Hz at 600 MHz offset [21]. They also testified that the high resistive substrate allows 2.5 to 8.5-Turn square spiral inductors to have high Q-factor as summarized in Figure 2.9.

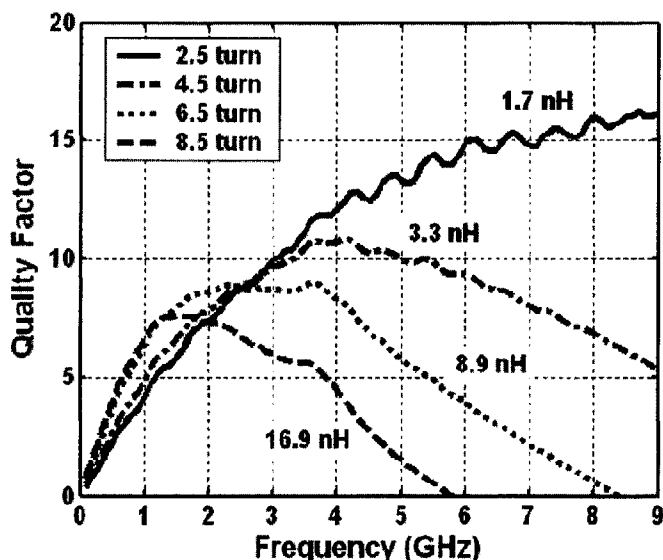


Figure 2.9 - Measured Q-factor of square spiral inductors using SOI CMOS process.

A research group from the University of California, Berkeley, has reported the successful implementation of a monolithic 3-dimensional copper coil inductor [22]. Thick copper traces of the coil are fabricated using electroplating process. Alumina is used as the core material because of its negligible loss tangent at high frequencies [23]. Compared to conventional spiral inductors, this 3-dimensional copper coil inductor achieves superior performance with Q values up to 30 at 1 GHz. Figure 2.10(a) shows a SEM picture of a 1-turn inductor with probe pad structure and Figure 2.10(b) depicts the inductance and Q-factor plots for this inductor.

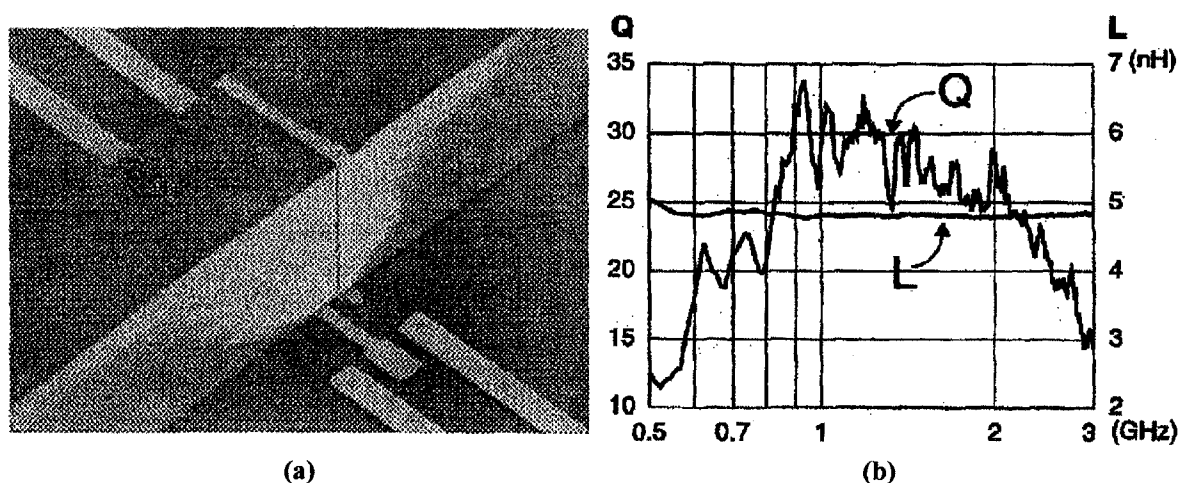


Figure 2.10 - SEM photo (a) and performance (b) for the 1-turn 3D copper coil inductor.

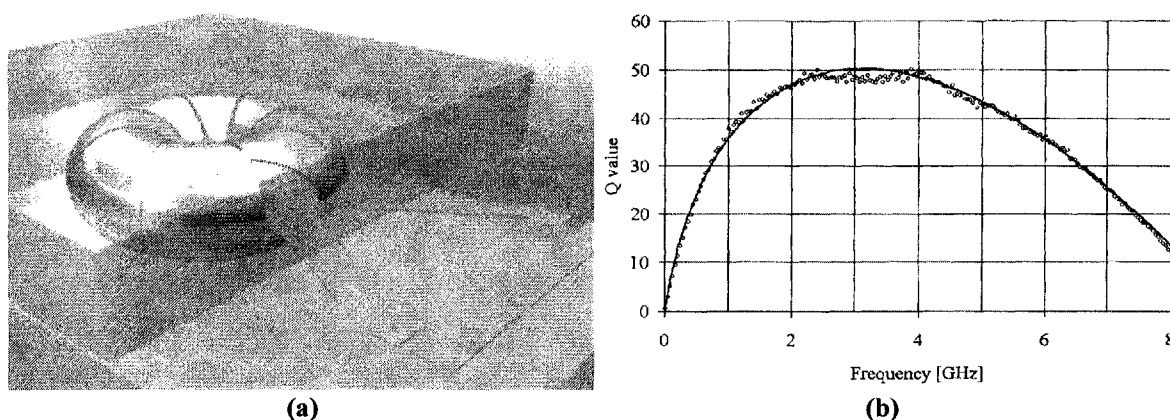


Figure 2.11 - 3-dimensional illustration (a) and measured Q-factor (b) of the toroidal inductor.

Another team from the Nokia research centre in Finland has also developed a novel 3-dimensional toroidal inductor using their polymer replication technique [24]. This inductor was put together on silicon substrate, with gold as the primary material for the coil. The characteristic of the toroidal inductor has been excellent, with very high Q-
 Device Design, Characterization and Modeling of Inductors and Interconnects for RFIC Applications — 35

factor of 50 at 3 GHz. Figure 2.11 portrays a 3-dimensional illustration as well as the measured performance of the toroidal inductor. The performances of 3-dimensional inductors developed by University of California and Nokia have been exemplary. Nonetheless, integration of their fabrication techniques into the current CMOS process flow, without affecting the final process yield, is expected to be very challenging.

Mernyei, Darrer, Pardoen and Sibrai reported a new technique to improve the Q-factor of spiral inductors by reducing the substrate magnetic loss, which is primarily caused by induced eddy currents from the inductor's magnetic field. This is achieved by inserting n^+ regions (narrow strips) in the top p^+ layer, perpendicular to the eddy-currents flow. P-N-P junctions are thus created and can be used to eliminate the eddy current closed loop paths in the top heavily doped p^+ layer [25]. Figures 2.12(a) and 2.12(b) show the spiral inductor with eddy-current blocking structures and the Q-factor comparison of the inductors respectively. Sp1 refers to 2-turn and Sp2 refers to 3-turn spiral inductors. Figure 2.12(b) reveals that the inductors with eddy-current blocking structures perform much better with higher Q values as compared to their counterparts. In existing CMOS process flow that starts with P-substrate, high resistive N-well can be used as the blocking structures.

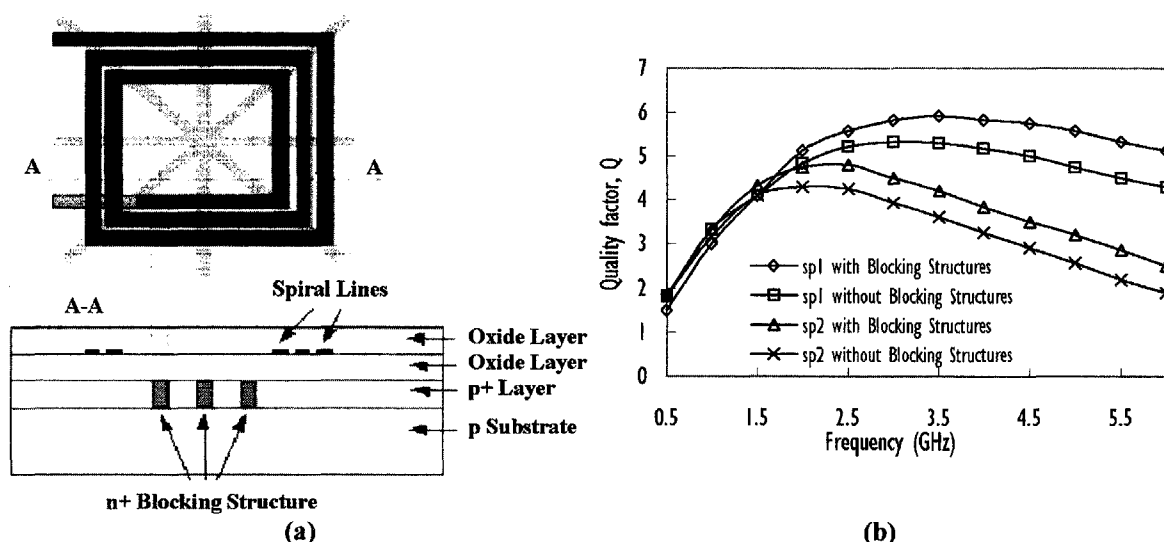


Figure 2.12 - Cross-sectional view (a) and Q-factor comparison (b) for spiral inductors with and without eddy-current blocking structures.

In 1998, Patrick Yue and Simon Wong [26] presented a shielded inductor, which improves the inductor's Q-factor. The implementation of such inductors also saw reduction in substrate coupling between two adjacent inductors by as much as 25 dB at 1-2 GHz. These shielded inductors are fabricated by inserting a patterned polysilicon ground shield between the spiral inductor and the silicon substrate. This ground plane helps to terminate the electric field of the inductor before it penetrates into the substrate, thereby eliminating unwanted substrate losses. Figure 2.13(a) reveals the patterned shield used. Figure 2.13(b) shows the die photos of test structures with patterned ground shield, shown with and without the inductor.

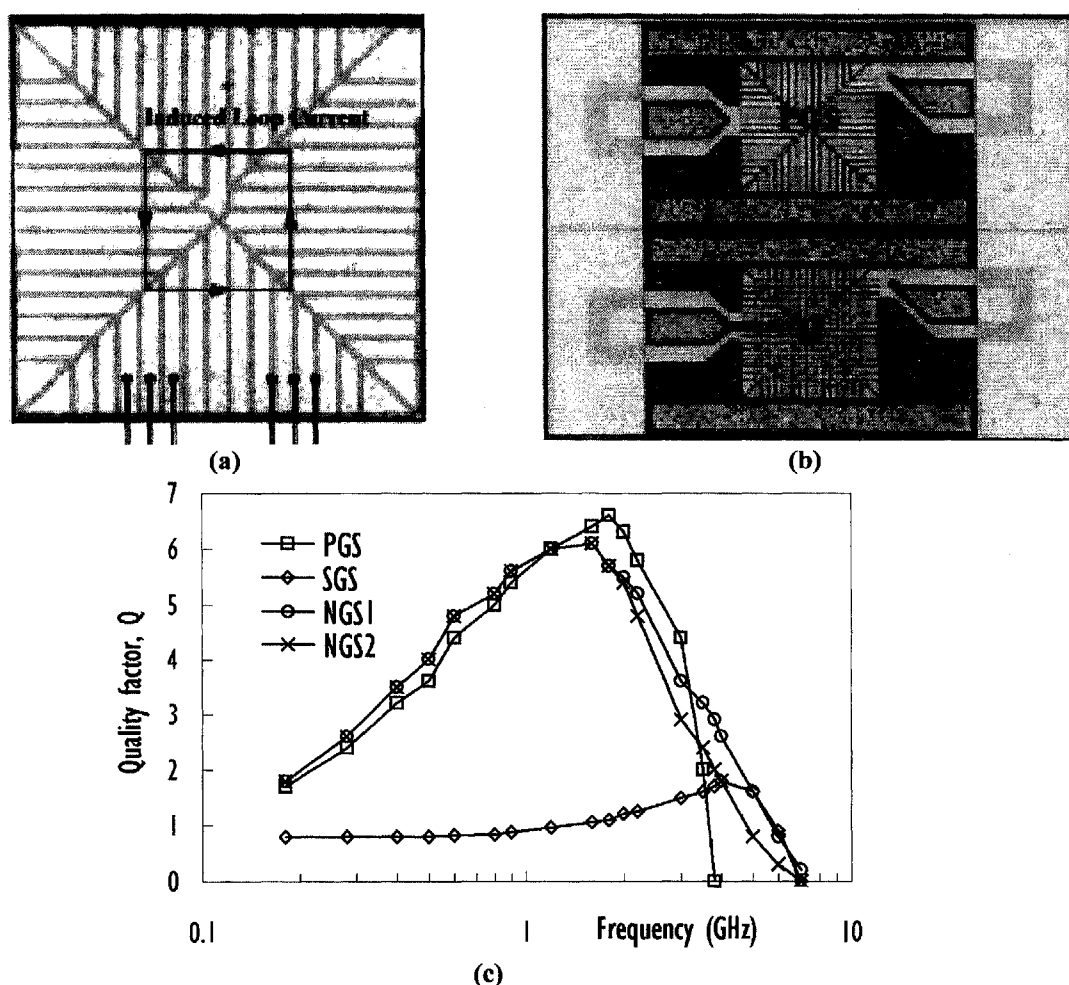


Figure 2.13 - Polysilicon patterned shield (a), die photos of test structures (b) and L & Q versus frequency plots (c) for inductors with different polysilicon shield patterns.

The ground shield is patterned so that it hinders the formation of closed loop current paths in the substrate and prevents negative mutual coupling between the induced substrate

current and the current flowing in the inductor such that the inductor's magnetic field and its overall inductance are not reduced (See Figure 2.4). Figure 2.13(c) shows Q-factor of four inductors, namely, with patterned ground shield (PGS), with solid ground shield (SGS), without ground shield and a substrate resistivity of $19 \Omega\text{-cm}$ (NGS1), and without ground shield and a substrate resistivity of $11 \Omega\text{-cm}$ (NGS2). The inductor with PGS yields the highest Q-factor due to the elimination of eddy currents while the SGS exhibits the lowest Q-factor because the induced eddy currents are not eliminated. Increasing the substrate resistivity also helps to minimize losses in the substrate. Nonetheless, the Q-factor improvement using PGS is not significantly high and occurs near the resonant frequency of the inductor.

2.1.4.2 Q-Factor Enhancement using Active Inductors

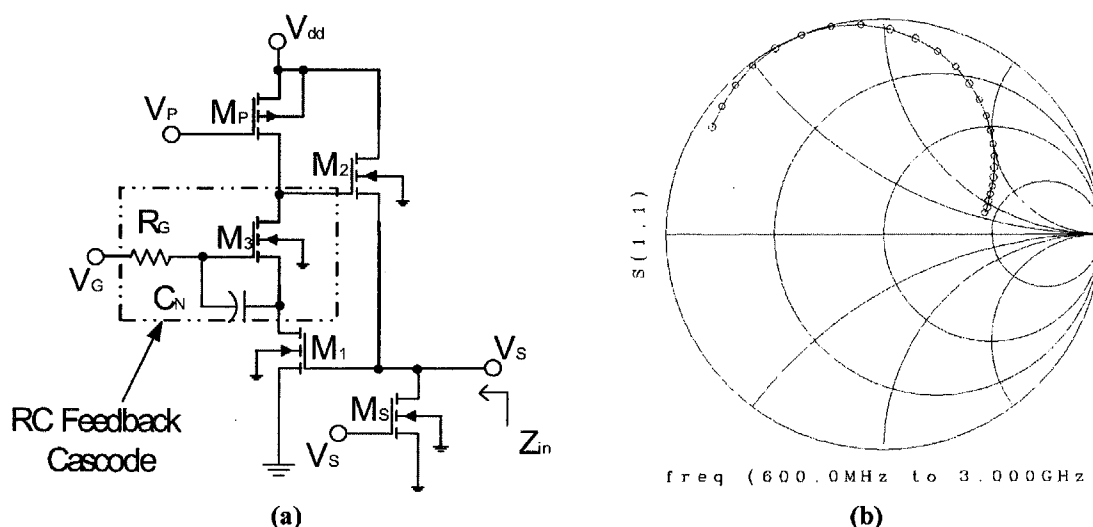


Figure 2.14 - High-Q active inductor with RC feedback cascode network (a) and its performance (b).

Jhy-Neng Yang from National Chiao Tung University and his fellow researchers design a CMOS broadband amplifier with high Q-factor active inductors as shown in Figure 2.14 [27]. Adopting common-gate configuration and high Q-factor active inductors, the broadband amplifier has achieved high power gain, wider bandwidth and better matching characteristics. In the absence of passive inductors, the chip area is significantly reduced though circuit complexity increases. It would be interesting to compare and evaluate the circuit improvements against an amplifier that uses passive inductors. Active inductors do

offer advantages such as high Q-factor with small area consumption. Nevertheless, implementations of such circuitries are time-consuming and not easily portable across different technological nodes. This could be a big hindrance since huge libraries of active inductors are required for circuit performance optimization. Also, active inductors are sensitive to biasing circuitries; consume additional power and introduce noise sources which may result in severe system level performance degradations. Because of these reasons, they are generally not popular among RFIC design companies.

2.1.4.3 Q-Factor Enhancement using Coupled Spiral Coils

A novel tunable inductor is presented by Pehlike at the International Electron Device Meeting in 1997 [28]. The inductor architecture consists of coupled RF and drive coils which employs phase shifting of the mutual components, demonstrating inductance tuning and significant decrease in resistive losses. Extremely high Q-factor of about 2000 can be achieved using this elaborate technique. Figures 2.15(a) and (b) illustrate the test setup for the tunable inductor and the measured Q-factor versus phase shifts of the variable phase shifter.

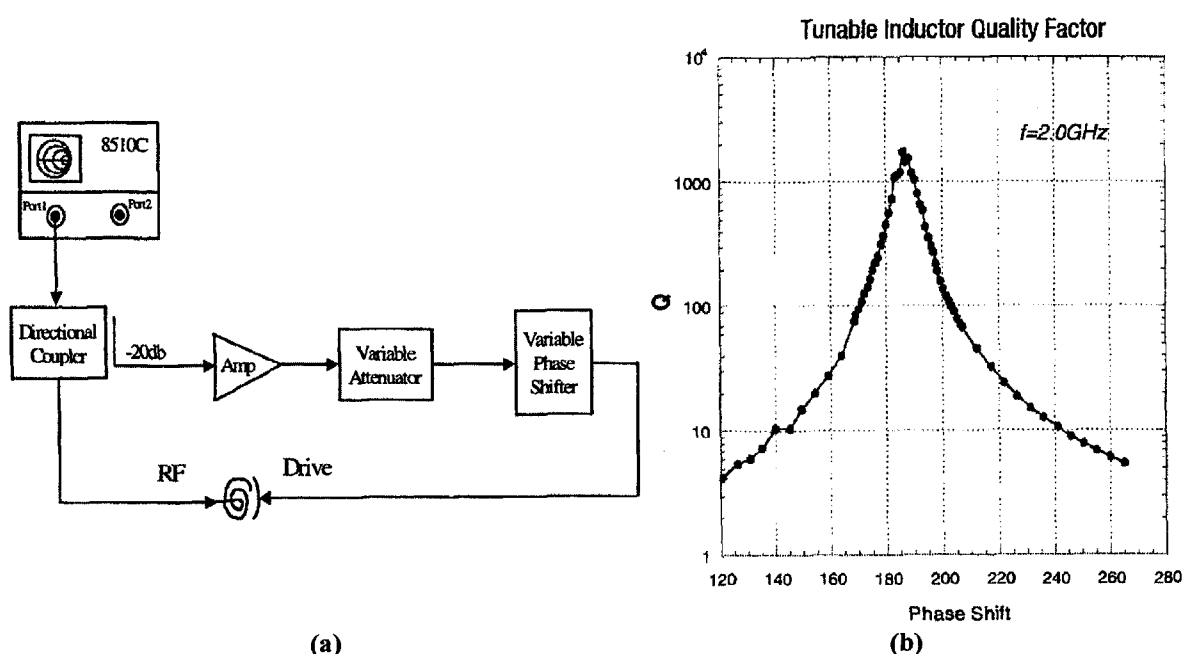


Figure 2.15 - Test setup for tunable inductor (a) Q-factor vs phase in variable phase shifter (b).

Although the results look very impressive, allowing inductance tuning with high Q-factor, there are several drawbacks in this technique. Besides the RF and drive inductor coils, implementation of this method requires more components and circuitries, suggesting even larger silicon area and power consumption as compared to using active or passive inductors. The active devices essential in realizing the phase shifting signal in the driving coil will also contribute to an expected increase in both power consumption and noise levels of the entire system. Performance of this inductor is also sensitive to the relative phase difference between signals flowing in the RF and driving coils revealing little circuit tolerance allowance during implementation.

2.1.4.4 Q-Factor Enhancement using Layout Optimization

Lopez-Villegas, J. Samitier, C. Cane, and P. Losantos, presented a method to improve the Q-factor of RF integrated inductors by optimizing the inductor's layout [29]. This method has been applied to the design of square spiral inductors using a silicon-based multi-chip module (MCM) technology and silicon micro-machining post processing. Essentially, the layout is optimized by using a variable width spiral coil inductor shown in Figure 2.16(a) to achieve high Q-factor.

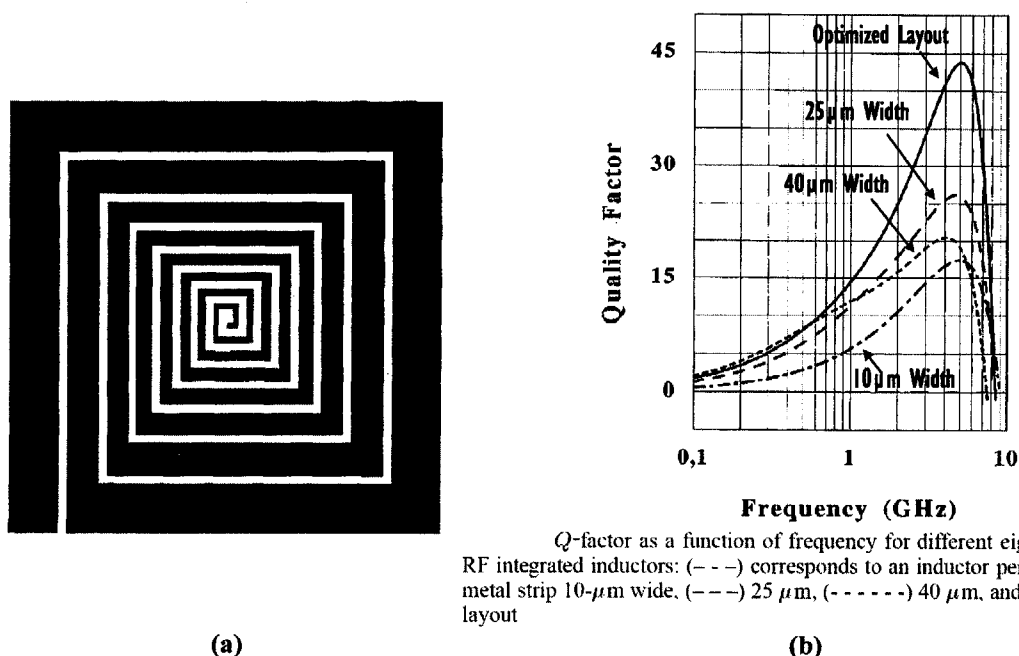


Figure 2.16 - Optimized layout (a) and Q-factor (b) for varying width spiral inductors.

From Figure 2.16(b), it is shown that this optimized inductor produced the best performance in a wide range of frequencies around 3.5 GHz. However, the drawback of this method is that it is only effective when applied to inductors whose fabrication process involves silicon substrate removal. Silicon substrate underneath the spiral coil has been removed to minimize substrate losses at radio frequencies. The inductance values for the four inductors, which must be similar to form a good basis for performance comparison, are not made known in this publication. The design of this experiment has likely led to an unfair evaluation of four inductors having completely different inductance values since the per unit length inductance is inversely proportional to the inductor's conductor width.

2.1.4.5 Q-Factor Enhancement using Inductor Device Model

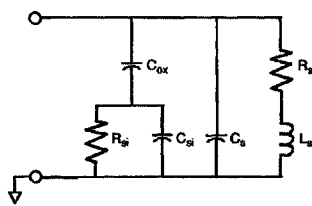
$$R_s = \frac{\rho \cdot l}{w \cdot \delta \cdot (1 - e^{-t/\delta})} \quad (1)$$

$$C_s = n \cdot w^2 \cdot \frac{\epsilon_{ox}}{l_{ox,metal}} \quad (2)$$

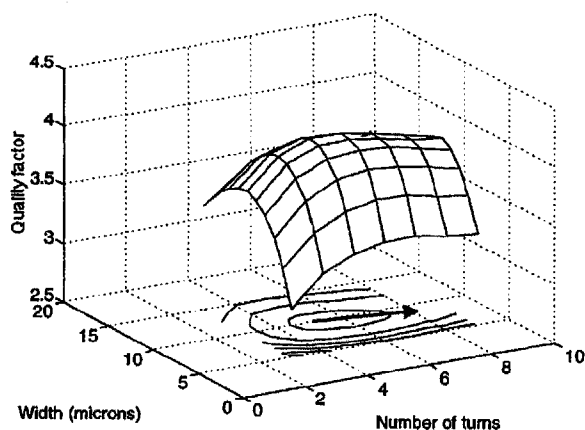
$$C_{ox} = \frac{1}{2} \cdot l \cdot w \cdot \frac{\epsilon_{ox}}{t_{ox}} \quad (3)$$

$$C_{st} = \frac{1}{2} \cdot l \cdot w \cdot C_{sub} \quad (4)$$

$$R_{st} = \frac{2}{l \cdot w \cdot G_{sub}} \quad (5)$$



(a)



(b)

Figure 2.17 - Physical inductor model for optimization (a) and Q-factor for 10 nH inductor as a function of number of turns and conductor width (b).

J.E. Post proposed optimizing the physical layout of spiral inductors [30] through analysis of physical model, as shown in Figure 2.17(a). This lumped element empirical model for silicon-based spiral inductors is developed by Simon Wong and Patrick Yue [31]. The simplicity of the physical model enables a computational procedure for efficient layout selection, optimizing both Q-factor and self-resonant frequency. Figure 2.17(b) shows that utilizing the proposed optimization algorithms, the highest Q-factor for a 10 nH inductor can be located. The best width and number of turns is found to be about 10 μm and 6 turns respectively.

This technique of optimizing the performance of spiral inductor is indeed convenient but puzzling as to how physical designs of inductors with different number of spiral turns and widths can be generated to yield identical inductances of 10 nH at a particular operating frequency. Another drawback of this approach is its reliance on the validity of the proposed spiral inductor model, which depends on whether a comprehensive testchip (with inductors fully permuted having different turns, width and core diameter designs) has been used for the inductor model development. Nonetheless, even with these concerns, three other papers [32] - [34] with more efficient optimization algorithms that made use of the same physical spiral inductor model were subsequently published.

In another recent research paper published in 2008, S. K. Mandal [35] improves the work of T. Liu [36] and R. Bhattacharya [37] and proposed combining both artificial neural networks (ANN) and particle-swarm optimization (PSO) techniques to optimize and synthesize the layout of spiral inductors. In his research, the PSO optimizer generates a swarm of particles, each representing a combination of inductor layout parameters. The ANN then evaluates each of these combinations and produces the inductance, Q-factor and self-resonant frequency based on a set of predetermined design criteria. This technique of synthesizing the spiral inductors is highly efficient as characteristics of four hundred inductors have been used to train the ANN. Nonetheless, one of the major drawbacks in this research work lies on the characteristics of the four hundred inductors. They were obtained from electromagnetic simulations and not real measured data. Testing the trained ANN model with another one hundred simulated inductors yielded poor prediction accuracy with errors in inductance, Q-factor and self-resonant frequency up to 15 %, 8 % and 8.5 % respectively. Finally, critical to RF circuit designers, it must be highlighted that such ANN models are not SPICE-compatible and therefore cannot be employed in commercial circuit simulators.

2.1.4.6 Summary of Q-Factor Enhancement Techniques

Several techniques to enhance the Q-factor of inductors have been reviewed. Improvements using novel silicon processing technologies and advanced materials are the most outstanding. Although great achievements were accomplished but most cannot be adopted in existing RFCMOS process flows because of reliability issues and expected increase in process complexities which will have detrimental impacts on process yield and manufacturing costs. Spiral inductors fabricated on SOI technology seems promising but require in-depth comparison studies to justify the use of SOI wafers which typically cost five to ten times more expensive than conventional bulk silicon wafers [38], [39].

Both active inductors and coupled RF coils approaches result in inductors having very high Q-factors but they require active devices for implementation which will exceed the system level power consumption and noise level budgets. Huge libraries of such inductors are necessary for circuit optimization but designing them is tedious and will likely require multiple design iterations, a time consuming and costly development cycle. Because of this, they do not allow ease of portability across different technological nodes, for example from 0.25 μm to 0.18 μm RFCMOS process.

On a separate note, layout-optimized inductors with varying width are novel but optimizing the physical layout of inductors should be made on the basis of comparing inductors with similar inductance values as the Q-factor is also largely dependent on the inductance behavior. Unless this important point is ensured, how such optimization methodology works remains vague. Last but not least, layout versus performance optimization of inductors using device models requires reliable models that can accurately predict the actual measured characteristics of inductors when their physical design parameters such as core diameter and conductor width are modified accordingly.

2.2 RF Interconnects on Silicon

Interconnects exist to serve the essential task of providing electrical connections for devices and they can be classified into different levels. As an example, at the lowest level, on-chip backend metallization interconnects provide electrical linkage between semiconductor devices such as capacitors, resistors, MOS and bipolar junction transistors. In the higher levels, interconnects are backplanes or gateways providing infrastructure for high speed, large bandwidth data transfer between networks. Hence, interconnects come in different forms and sizes, and one way of defining interconnect is as follows:

- Level 1 Interconnect: On-Chip
- Level 2 Interconnect: Multi-Chip Modules (MCM Package)
- Level 3 Interconnect: Printed Circuit Board (PCB)
- Level 4 Interconnect: BackPlane (Package)
- Level 5 Interconnect: Rack, Connect Systems (Package)

Sizes of interconnect increase as the interconnect level escalates and interconnects with the smallest dimensions can be found at the lowest level, in this case, on a semiconductor chip. At various levels in the hierarchy, due to different requirements and operating frequencies, interconnects are designed and modeled differently. Modeling techniques such as electromagnetic (EM) simulation using HFSS (High-Frequency Structure Simulation) [40], circuit model using partial element equivalent circuits (PEEC) and passive device physical modeling can be applied to different levels of the hierarchy. This research work investigates and focus on interconnects at the on-chip level meant for radio frequency operations.

From Chapter 1, it is clear that growing demands from consumer market will continue to motivate the exploitation of silicon-based RF SoC. Nonetheless, further explorations of silicon technologies for wider range of possible RF applications reveal that interconnects, just like inductors, are fast becoming technological bottle-necks limiting any potential utilization. This is because CMOS on-chip interconnects are fabricated using resistive

aluminum or copper metallization, isolated by silicon oxide on lossy silicon substrates. Such interconnects have detrimental effects on circuits, and as frequency increases, undesirable parasitic responses, both inductive and resistive in nature as well as capacitive coupling to the substrate become even more pronounced, leading to significant deteriorations in circuit performance as well as shifts in circuit frequency response. This section will review the theories of transmission lines and provide a background understanding of existing techniques adopted to rectify these issues. There will also be a quick review and comparison between aluminum and copper backend interconnect schemes for existing silicon technologies.

2.2.1 Transmission Line Concept

The most important difference between transmission line theory and circuit theory is electrical size. Circuit analysis assumes that the physical length of an electrical connection is much smaller than the electrical wavelength of the propagating signal, while transmission lines are much shorter, just fractions of a wavelength, or many wavelengths [41]. Hence, for transmission line structures with physical dimensions which are considerably smaller than the wavelengths of the signals being transmitted, they may be acceptably described with line voltages and currents. And if the signal level is fairly constant along the entire length of the interconnect, it can be treated as a lumped element and not a transmission line.

When the signal is sinusoidal, it is generally agreed in [42] that the signal does not change much in time over an interval equal to one twentieth of the period, T , of the signal. Considering a sinusoidal signal, $x(t) = A\sin(\omega t)$, where $\omega = 2\pi f$ is the radian frequency of the signal and $f = 1/T$ is its frequency so that $x(t) = A\sin(2\pi t/T)$. The maximum changes occur when the signal goes from a time, $t = -\alpha T/2$ to $t = +\alpha T/2$ where α is the fraction of the period. So in one twentieth of the period ($\alpha = 0.05$) the signal can change by 16 % of its maximum possible change in value. Hence, when the interconnect line is less than $1/20^{\text{th}}$ of the wavelength, λ , of the signal, it is regarded as safe to use a lumped circuit model for the interconnect. Table 2.1 below summarizes the modeling criteria for interconnects.

Table 2.1 - Modeling criteria for interconnects.

Signal Type	Model Requirement	
	Transmission Line model	Lumped model
Sinusoidal	Length $> \lambda/10$	Length $< \lambda/20$

Using the criteria in Table 2.1, critical lengths of interconnects can be computed over frequency,

$$\text{Critical length} < \lambda / 20$$

$$\text{Critical length} < c / (\text{frequency} * 20)$$

where $\lambda = c / \text{frequency}$ and $c = \text{speed of light (in free space)} \cong 3e+08 \text{ m/sec}$

Table 2.2 - Interconnect critical lengths in free space, silicon dioxide and silicon.

Frequency (GHz)	2.5	5.0	7.5	10	20	50
Critical Length= $\lambda/20$ in free space (μm)	6000	3000	2000	1500	750	300
Critical Length= $\lambda/20$ in SiO ₂ , $\epsilon_r=3.9$ (μm)	3038	1519	1013	759	380	152
Critical Length= $\lambda/20$ in Si, $\epsilon_r=11.9$ (μm)	1739	870	580	435	217	87

As the frequency increases, wavelength becomes smaller correspondingly. It is therefore necessary to set up a complete electromagnetic field solution to analyze such line structures. If it is assumed that small line dimensions prevail, then a number of useful results must be obtained on a voltage and current basis. The theory thus developed is called the distributed circuit theory [42]. When the operating frequency for silicon-based RFICs move into the giga-hertz range, the physical dimensions of interconnects will approach an order of magnitude in relation to the wavelength of the transmitted signals. At such frequencies, transmission line effects may begin to impede with the proper operation of the signal propagating across the chip.

High frequency response of an interconnect line depends on the source resistance and termination resistance looking in and out of the interconnect structure [43]. When the source resistance is much larger than the interconnect line impedance, only a small portion of the applied voltage will be placed on the line initially. The voltage will slowly increase, in an exponential fashion until reaching steady state over time. In such cases, the interconnect line effect is negligible and the line could be approximated by a lumped RLC physical model. If the source resistance is reduced and the line's response begins to include more and more ringing over time, this demonstrates the delay through the transmission line. In such cases, transmission line is a better approximation and these kind of structures can be approximated by cascading several interconnect lump models to achieve reasonable accuracy.

2.2.1.1 Transmission Line Constants

In a uniform transmission line, the line parameters are defined as follows:

Resistance per unit length	= R'
Inductance per unit length	= L'
Conductance per unit length	= G'
Capacitance per unit length	= C'

R' , L' , G' and C' are referred to as resistance, inductance, conductance and capacitance per unit length respectively. In most radio frequency transmission lines, the effects due to L' and C' tend to dominate because of the relatively high inductive reactance and capacitive susceptance. They are generally refer to “loss-free” or “lossless” lines although in practice some information about R' or G' maybe necessary to determine the actual power loss. The lossless concept is useful and offer relatively good approximation. The propagation of a wave along the line is characterized by the propagation coefficient, γ ,

$$\gamma = \sqrt{(R' + j\omega L')(G' + j\omega C')} \quad (2.19)$$

or

$$\gamma = \alpha + j\beta \quad (2.20)$$

where, α = attenuation coefficient, in Nepers per meter.

β = phase change coefficient, in degrees, or radians, per meter.

ω = angular frequencies in radians per second

At sufficiently high radio frequencies, Equations 2.19 and 2.20 yield

$$\beta = \omega\sqrt{L'C'} \quad (2.21)$$

β is called the “wave number”. From the relationship of propagation velocity, the signal velocity propagation can be written as

$$v_p = \omega / \beta \text{ (m/sec)} \quad (2.22)$$

Using equation 2.21, v_p can be expressed as

$$v_p = 1 / \sqrt{L'C'} \text{ (m/sec)} \quad (2.23)$$

The velocity of propagation is also given in terms of the absolute permeability, μ and permittivity, ϵ of the medium through which the wave passes,

$$v_p = 1/\sqrt{\mu\epsilon} = c/\sqrt{\mu_r\epsilon_r} \quad (\text{m/sec}) \quad (2.24)$$

where, $c = 2.99793 \times 10^8$ m/sec, the velocity of light in free space.

μ_r = relative permeability of the medium through which the wave passes

ϵ_r = relative permittivity of the medium through which the wave passes

From equation 2.24, it is important to note that the wave propagation speed is dependent on the dielectric medium.

2.2.1.2 Transmission Line Impedances

The characteristic impedance, Z_0 of a transmission line is generally given by

$$Z_0 = \sqrt{\frac{R' + j\omega L'}{G' + j\omega C'}} \quad (2.25)$$

At high radio frequencies this simplifies to

$$Z_0 = \sqrt{\frac{L'}{C'}} \quad (2.26)$$

Changing Z_0 requires a change in the physical dimensions of the transmission line. The impedance looking into a transmission line varies with the distance progressed along the line. By setting down the distance limits (d) into expressions for the voltage and current at any point along the line, for a specific impedance Z_L , the following expression for the input impedance of the line is given by

$$Z_{in} = Z_0 \left(\frac{Z_L \cosh \gamma d + Z_0 \sinh \gamma d}{Z_0 \cosh \gamma d + Z_L \sinh \gamma d} \right) \quad (2.27)$$

Equation 2.27 is a general expression for Z_{in} and for lossless lines, it simplifies to

$$Z_{in} = Z_0 \left(\frac{Z_L + jZ_0 \tan \beta d}{Z_0 + jZ_L \tan \beta d} \right) \quad (2.28)$$

Using equation 2.28, the shorted-circuit (at the far end of the transmission line) case where $Z_L = 0$, gives

$$Z_{sc} = jZ_0 \tan \beta d \quad (2.29)$$

And for open-circuit (at the far end of the transmission line) case, where $Z_L = \infty$, gives

$$Z_{oc} = -jZ_0 \cot \beta d \quad (2.30)$$

When the line is terminated with a load impedance exactly equal to the characteristic impedance (Z_0) of the line itself, it is a perfectly broadband matched. The denominator is equal to the numerator in the right-hand parentheses of equation 2.27 and hence

$$Z_{in} = Z_0 \quad (2.31)$$

This completely matched condition is often used in test and measurement procedures.

2.2.1.3 Reflection and Voltage Standing Wave Ratio

In all cases, unless the line is in completely matched condition, the load termination will reflect some of the energy originally injected into the transmission line. When a signal is reflected back to the launching point, interference between the incident and reflected waves, traveling at the same velocity but in opposite directions, causes a standing-wave field pattern to be formed. The voltage reflection coefficient, Γ , ratio of reflected to incident voltage at the load is given by

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \quad (2.32)$$

The ratio of maximum to minimum amplitude of the standing wave is called the Voltage Standing Wave Ratio (or VSWR) given by

$$\text{VSWR} = \frac{1 + |\Gamma|}{1 - |\Gamma|} \quad (2.33)$$

For matched condition, $\Gamma = 0$ and $\text{VSWR} = 1$. The reflection coefficients and standing wave ratios for short-circuit and open-circuit terminated conditions are -1 and $+1$ respectively, and in both cases mentioned above, the VSWR is infinite.

2.2.1.4 Frequency-Dependent Charge Distribution

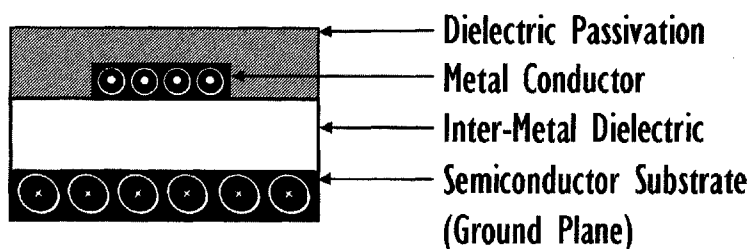


Figure 2.18 - Cross-sectional view of on-chip interconnects

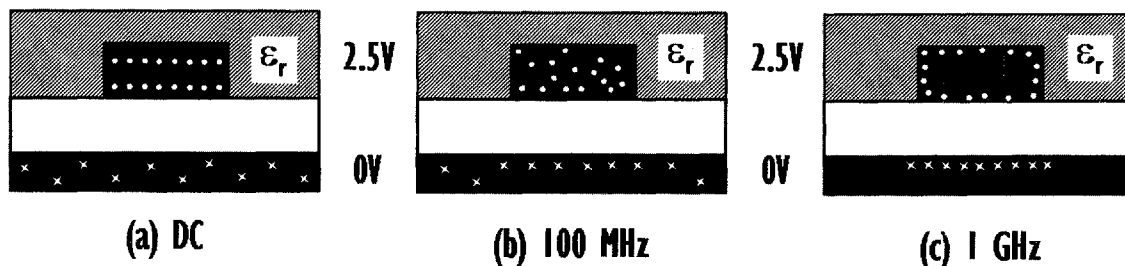


Figure 2.19 - Cross-sectional view of the charge distribution in an interconnect at different frequencies. (The dots and crosses indicate charge concentration of different polarity).

On-Chip interconnects are essentially planar structures with cross-sectional view as shown in Figure 2.18. Such lines have frequency dependent behaviors and Figure 2.19 shows the charge distribution of the interconnect structure under different operating conditions. When a positive DC voltage is applied on the top conductor, positive charges on the top conductor generally arranged in a fairly uniform distribution as illustrated in Figure 2.19(a). The bottom conductor, which is the ground plane, has balanced negative charges, so that the electric field lines begin on the positive charges and terminate on the negative

charges. The negative charges on the ground plane are uniformly distributed over the entire ground plane.

As frequency of the signal propagating in the interconnect increases, the charges do not have sufficient time to rearrange and they are not distributed homogeneously. Such effect is observed at 100 MHz, as shown in Figure 2.19(b). This phenomenon becomes more prominent when the frequency of the signal is at 1 GHz as depicted in Figure 2.19(c). The electromagnetic fields, being time varying, are not able to penetrate the conductor as before due to skin effects. As such, charges in the top conductor are only distributed with respect to the depth of penetration into the conductor. Consequently, current flow is mostly concentrated near the surface of the conductor and the effective cross-sectional area of the conductor for current to flow is reduced and hence, resistance of the conductor increases significantly. On the other hand, charge distribution is not uniform over the whole ground plane and charges are concentrated under the strip. This effect increases the resistance of the ground plane and the electric energy stored in the dielectric.

Redistribution of the charges results in a change of the conductor's inductance with frequency. At low frequencies, for the same current, magnetic energy is stored inside as well as outside of the conductors. At intermediate frequencies, the inductance reduces with frequency and only at sufficiently high frequencies, the magnetic field becomes confined to the region outside the conductors and the inductance remains approximately constant. As frequency continues to increase, parasitics become more pronounced and the inductance starts to increase. Nonetheless, the most significant frequency dependent effect is the resistance of the interconnect, which increases approximately as the square root of frequency (refers to Equation 2.18).

2.2.1.5 Effects of Dielectric on Interconnects

On-chip interconnects are usually constructed within insulating materials such as silicon dioxide. Presence of such insulating material between conductors alters the electrical characteristics of the interconnect. Application of an electric field across the dielectric moves the centers of positive and negative charges, changing the amount of energy stored in the electric field. The extra energy storage property is described by the relative permittivity, ϵ_r , which is a ratio of the material's permittivity to that of free space, ϵ_0

$$\epsilon_r = \frac{\epsilon}{\epsilon_0} \quad (2.34)$$

Relative permittivity of materials used in on-chip interconnects, varies from 3.5 - 3.9 for doped silicon dioxide (eg boro-phospho-silicate glass (BPSG), fluorine-doped silicate glass (FSG) etc) to 11.9 for silicon. When interconnect is enclosed by more than one medium i.e. a non-homogeneous transmission line, the effective permittivity, ϵ_{eff} , has to be used. ϵ_{eff} will change with frequency as the proportion of energy stored in the different regions changes. This effect is called dispersion and can cause an input pulse to spread out as the different frequency components of the pulse travel at different speeds.

A similar effect on energy storage in the magnetic field occurs for a few materials. The magnetic properties of materials are due to the magnetic dipole moments resulting from alignment of electron spins. In most materials, the electron spins occur in pairs with opposite polarity and the net outcome is zero magnetic moment. However, when the net outcome is not zero, this remaining net magnetic moment will align with a magnetic field and provides a mechanism for additional storage of magnetic energy. The relative permeability, μ_r , describes this effect. Nearly all materials used with interconnects have $\mu_r=1$.

2.2.2 Backend Interconnect Schemes for Silicon Technologies

Up to the 0.18 μm technology node for CMOS processing technology, aluminum (doped with small amount of copper) has always been the preferred metallization choice for interconnections between devices. Nonetheless, as device/metallization feature size continues to shrink with demands for faster and better chip performance, limitations of the aluminum metallization become more evident. Aluminum's high resistivity, less inferior electromigration properties and difficulties in etching very fine aluminum lines have exposed its weaknesses with copper metallization schemes emerging as the backend interconnect for 0.13 μm CMOS technological nodes and beyond. Comparing the traditional backend interconnect technology whereby aluminum is deposited on inter-metal dielectric (IMD, doped silicon dioxide), patterned and etched forming the desired metal lines, copper metallization, on the other hand, uses damascene processes as shown in Figure 2.20 [44].

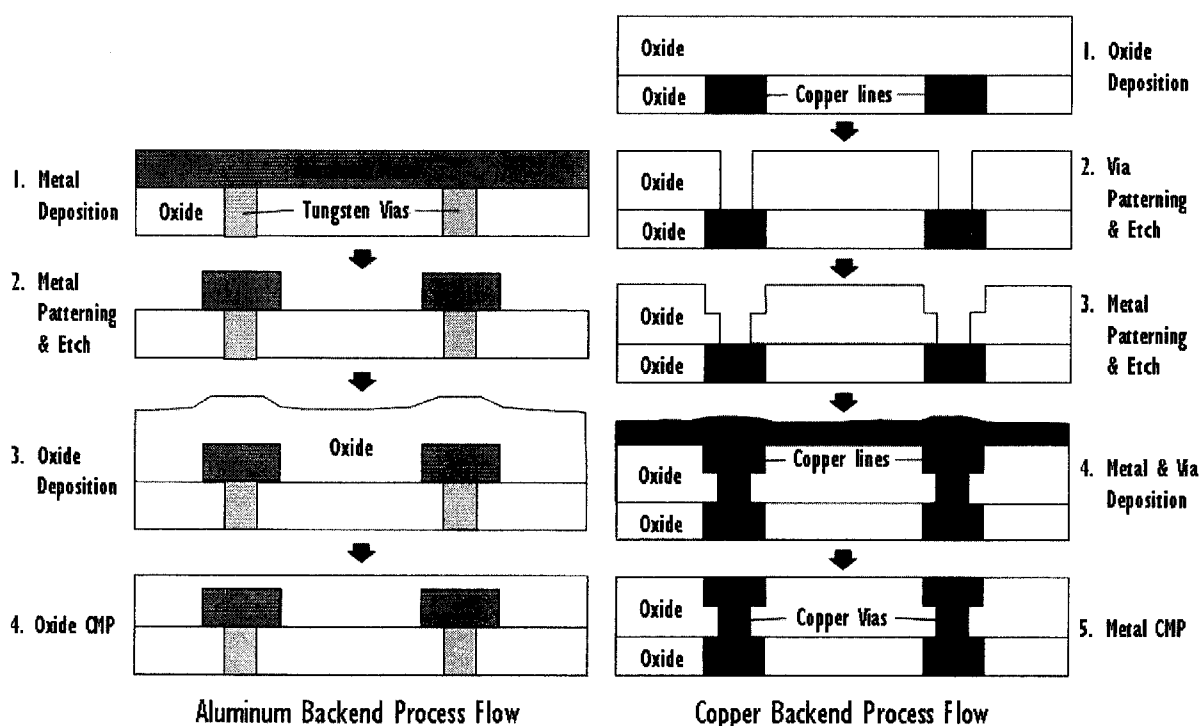


Figure 2.20 - Aluminum and copper backend interconnect process flows.

In a dual-damascene process, IMD is first deposited and patterned to define the locations for the vias and metal lines. A thin layer of barrier material such as tantalum or tantalum

nitride is subsequently lay upon to prevent copper diffusion into the critical gate oxide, causing catastrophic device failures. On top of the barrier metal is a copper seed layer which serves as a base for the succeeding deposition of copper through electroplating. When the metal and via regions are completely plated with copper as shown in step 4 of Figure 2.20, chemical mechanical polishing (CMP) process is used to remove the excess metallization, forming the desired metal lines.

Figure 2.21 shows a comparison of the cross-sectional backend interconnect schematics for 0.18 μm and 0.13 μm RFCMOS technologies used in this research project. These RFCMOS processes are modified from the standard logic process with additional plug-in analogue/RF modules like low ($300 \Omega/\square$) and high sheet rho ($1 \text{ K}\Omega/\square$) polysilicon resistors, metal-insulator-metal (MIM) capacitors, deep Nwell option (for suppressing substrate noise coupling) and most important of all, thick top metallization to achieve high Q-factor inductors and low-loss interconnects.

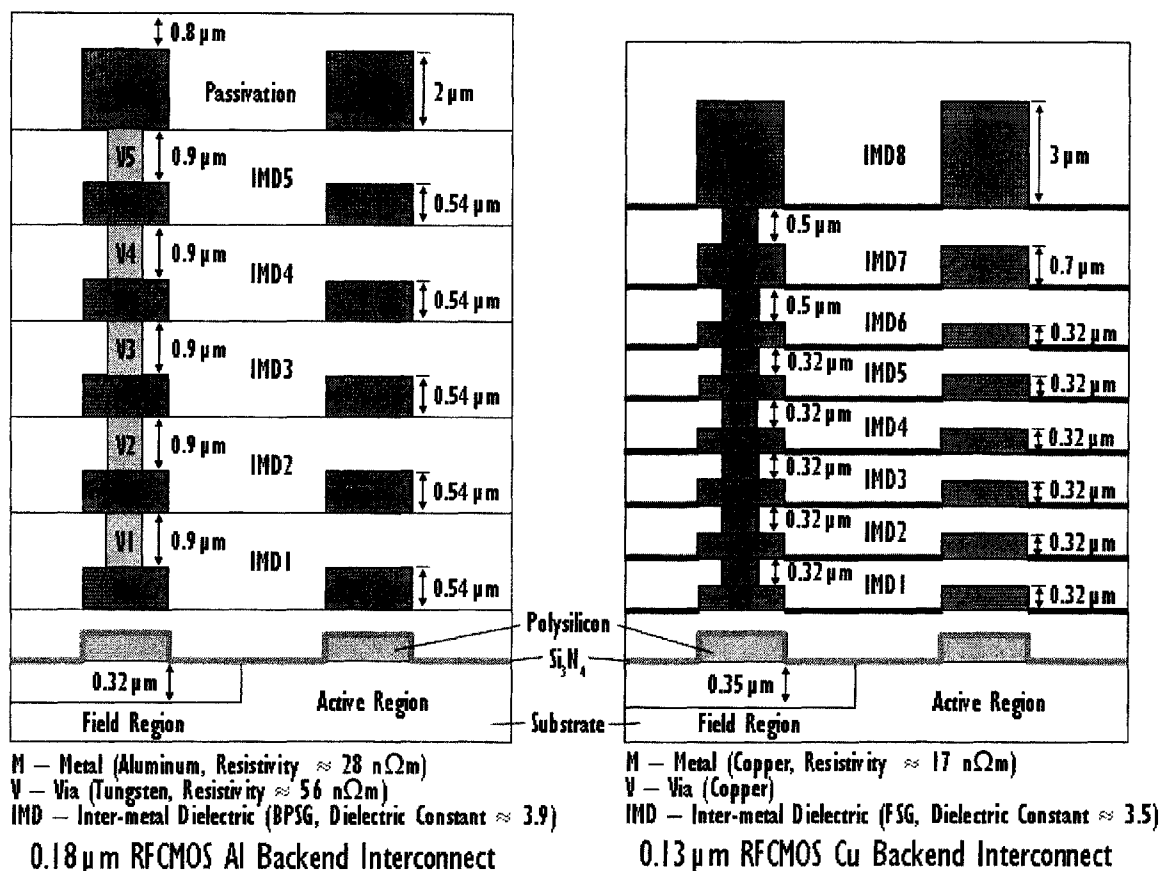


Figure 2.21 - Backend cross-sectional schematics for 0.18 μm and 0.13 μm RFCMOS process.

2.2.3 Existing Methodologies to Tackle Post Layout Parasitics

Silicon-based RF designs are now conceptualized on CAD tools that utilize feature-rich process design kits (PDKs) with accurate and scalable device models developed based on extensive and reliable on-wafer RF device characterization. Despite having accurate device models that are capable of predicting device degradation effects at radio frequencies, a typical RFIC still requires several design iterations before it can comply with the design specifications. These design iterations can be avoided if metallization interconnects, which become parts of the circuit when they are used to provide electrical connections between devices, are carefully considered during post-layout circuit simulations. Interconnects have detrimental effects on circuits, and as frequency increases, undesirable parasitic responses, both inductive and resistive in nature as well as capacitive coupling to the substrate are even more pronounced, leading to significant deteriorations in circuit performance as well as shifts in circuit frequency response.

Most silicon foundries provide extensive information on the interconnect characteristics for their technology, but these interconnects are generally characterized at low frequencies. Simple Resistance-Capacitance (RC) post layout extraction approach cannot accurately emulate and predict effects such as substrate losses, inductive parasitics and skin effects of metallization at radio frequencies. Several techniques have been proposed to model skin effects of interconnects or inductors at high frequencies but most of these methods contain resistive elements described by frequency dependent equations and therefore cannot be implemented in existing SPICE-compatible simulators [45]. Other methods include using EM simulators to perform post layout simulations so that high frequency effects of the interconnects will be taken into considerations [46]. These methodologies may offer good accuracies if the technology files are well-calibrated against the manufacturing process. Accurate simulations are generally very time-consuming and integrating these EM tools

into existing commercial SPICE simulators has proved to be a very challenging and daunting task with top companies paying millions of dollars to own such solutions.

One example of such expensive software module in Cadence, a very popular commercial CAD tool among RFIC design companies, is its recently released, state-of-the-art post-layout parasitic extraction tool, Assura [47]. Prior to parasitic extraction, layout of the full chip first undergoes a layout-versus-schematic (LVS) check as outlined in Figure 2.22. Then, parasitic extraction based on pre-defined rules and technology files is executed. In this parasitic extraction flow, additional parasitic extraction (Assura RCX-PL) which invokes parasitic inductance and inductive mutual coupling extraction enhances the standard resistance-capacitance parasitic extraction scheme for RFIC applications. These parasitics are then back-annotated and updated onto the circuit schematic for post layout simulations and analysis of changes in the circuit performance due to layout parasitics. Although such automated design tools can save RF circuit designers a lot of time and hassle of considering the effects of each individual interconnection, there are drawbacks and they are:

1. Failure to consider skin effects i.e. the increase of metallization series resistance at giga-hertz frequencies. Such inadequacies can, for example, lead to incorrect prediction of amplifier's gain at operating frequency.
2. Lumping and combining parasitics to emulate interconnects. This is incorrect at giga-hertz frequencies which will be further discussed in Chapter 6.
3. A very expensive tool and to achieve highly accurate circuit predictions, still requires foundries or RFIC design companies to calibrate and verify the technology files by running experiments to determine if the extracted parasitics at giga-hertz frequencies are correct.
4. Very time consuming extraction flow especially for complex chips, which cannot be tolerated under hectic development schedule.

5. Significant increase in the complexity of the circuit schematic after parasitic extraction which could potentially give rise to solution convergence failures for time domain simulations.

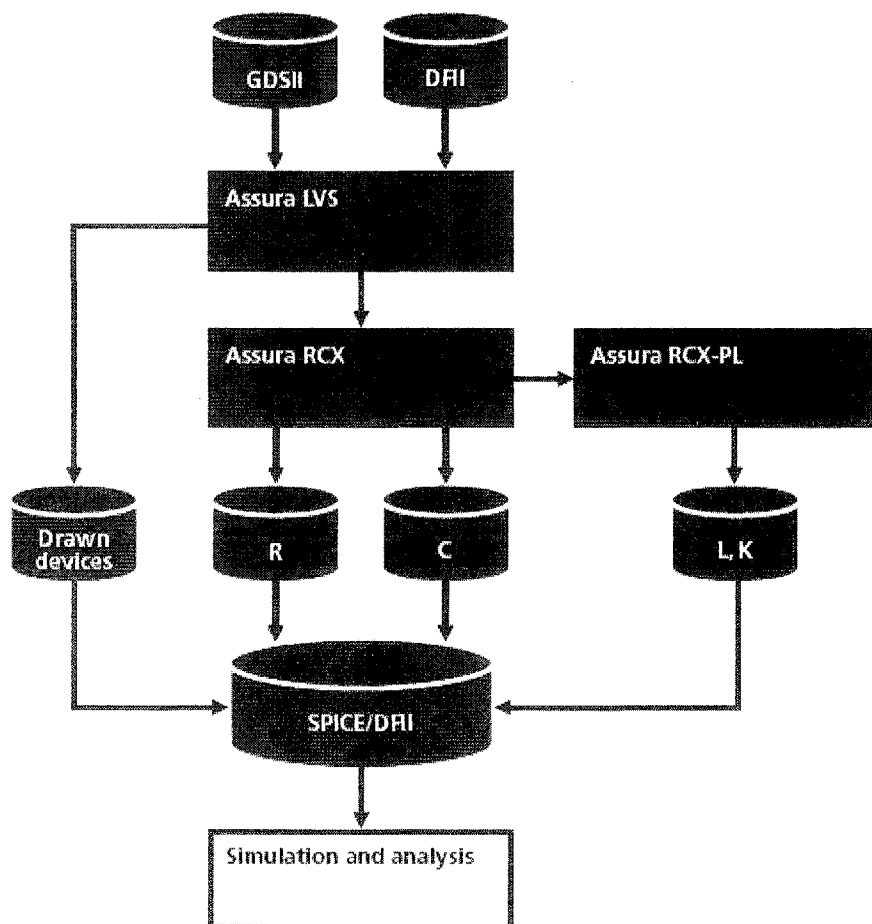


Figure 2.22 - Fully integrated RLCK solution for full-chip device-level parasitic extraction [47].

For experienced RFIC designers without elaborate CAD tools support, they often have to over-design their circuits to cater for performance degradation and shifts in circuit frequency response. They would then continue to rely on costly and time consuming design iterations until their designs are eventually within specifications. Therefore, accurate and scalable SPICE-simulator compatible RF interconnect models are necessary to help cope with the escalating demands of designing RFICs with higher operating frequencies on cost-effective silicon technologies. Armed with these interconnect models, circuit designers can quickly take preventive measures prior to circuit fabrication if the RF interconnects are found to have adverse effects on their circuits during post-layout

simulations, thereby reducing the number of design iterations, saving development cost as well as shortening the product time-to-market cycle.

2.3 On-Wafer RF Characterization

The main aim of performing on-wafer RF characterization is to allow better understanding of all active and passive devices' characteristics at radio frequency operation and develop realistic RF SPICE-compatible device models based on the measurement results. Such approach to device modeling is expensive since capital and knowledge intensive investments are required. A basic RF test setup which includes DC analyzer, vector network analyzer, probe station and engineering software for test and model development typically cost around US\$1million. Costly test chip fabrications, hiring engineers with RF characterization and modeling experience, and replacing expensive RF probes due to wear and tear all result in high operating cost for developing RF device models. Though expensive, measurement-based modeling approach is still very popular among established semiconductor manufacturing and fab-less IC design companies as compared to other techniques such as electromagnetic simulations mainly because highly accurate device models are required. In a long term perspective, huge cost savings from shorter RFIC development cycles through minimal design iterations actually far exceed the investments and operational costs required to develop measurement-based RF SPICE models and this is the reason why some fabless RFIC giants like Qualcomm, Broadcom, Mediatek invest and build up their own in-house device modeling capabilities.

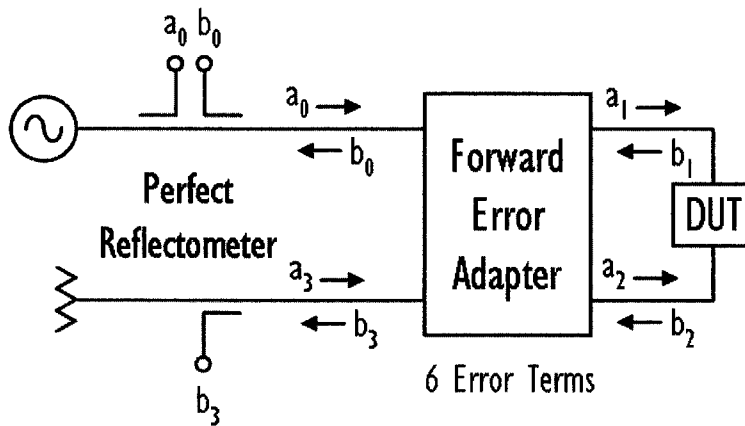
Before accurate RF measurements can be made, the test system must first be calibrated. Calibrations correct or "zero" the imperfections in the test system by measuring known quantities called standards. The RF characteristics of these standards are known beforehand and by measuring these standards as the device under test (DUT), the test system's imperfection can be isolated, quantified and mathematically improved. This section will review test instrument calibration techniques, past and existing RF probe technologies and extending measurement reference planes to devices for on-wafer RF measurements.

2.3.1 Error sources and Calibration for RF measurements

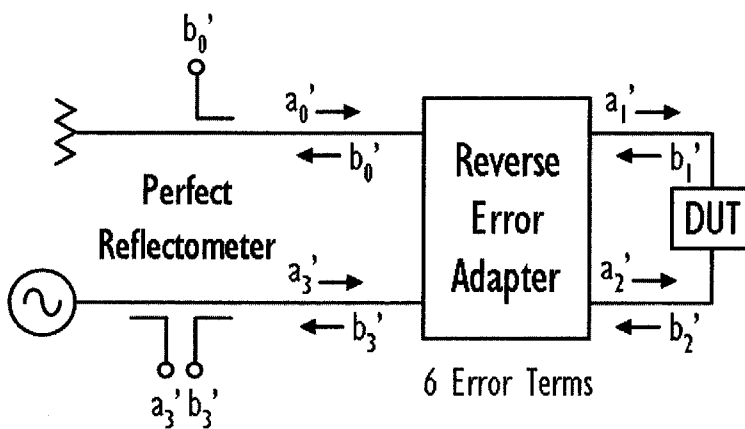
A RF test system essentially has two types of error sources, namely random and systematic errors. Random errors are not predictable and can happen irregularly during measurements. They come from the electronic components that are present within the test instruments. For example, thermal excitation of carriers and minority carriers drifting across PN junctions are noise sources that can be triggered by changes in room temperature and these errors manifest as low-levels signals spuriously emerging from the noise floor. On the other hand, RF errors which occurred predictably and repeatedly are referred to as systematic errors. Examples of such sources of errors come from parasitic inductance from cables and parasitic capacitance from bias tees. Systematic errors are easier to tackle since adopting calibrations techniques on known standards help identify the error coefficients and move the measurement reference plane to the probe tips before performing on-wafer RF measurements. Random errors, however, can be prevented by observing strict test procedures such as proper warming up of test instruments prior to system calibration and measurement, and during measurements, maintain a test setup that is in thermal equilibrium and perform periodic system stability checks to ensure validity of the instruments' calibrated state.

Calibration essentially extracts error coefficients of an error model which is used to describe the source of errors in a RF test system. To implement this, a fictitious error adapter is placed between the two-port DUT and the 'perfect reflectometer' measurement ports as shown in Figure 2.23(a) [48]. The corresponding signal flow graphs are illustrated in Figure 2.23(b). As an example, considering the forward signal flow graph, it comprises of six terms namely directivity, source match, reflection tracking, load match, transmission tracking and isolation, each representing an error source. Employing calibration standards, one at a time at each port allow six calibration measurements, which help solve six equations for six error terms at each port. For example, measuring the

return loss at port 2 help to find the reflection terms E_{DR} , E_{SR} and E_{RR} . Connecting a thru' standard between port 1 and 2 give the forward and reverse transmission terms E_{LF} , E_{LR} , E_{TF} and E_{TR} . Isolation measurement will reveal the crosstalk error terms E_{XF} and E_{XR} but they are generally small and often ignored.



Forward Model



Reverse Model

Figure 2.23(a) - Error adapters in two-port measurements.

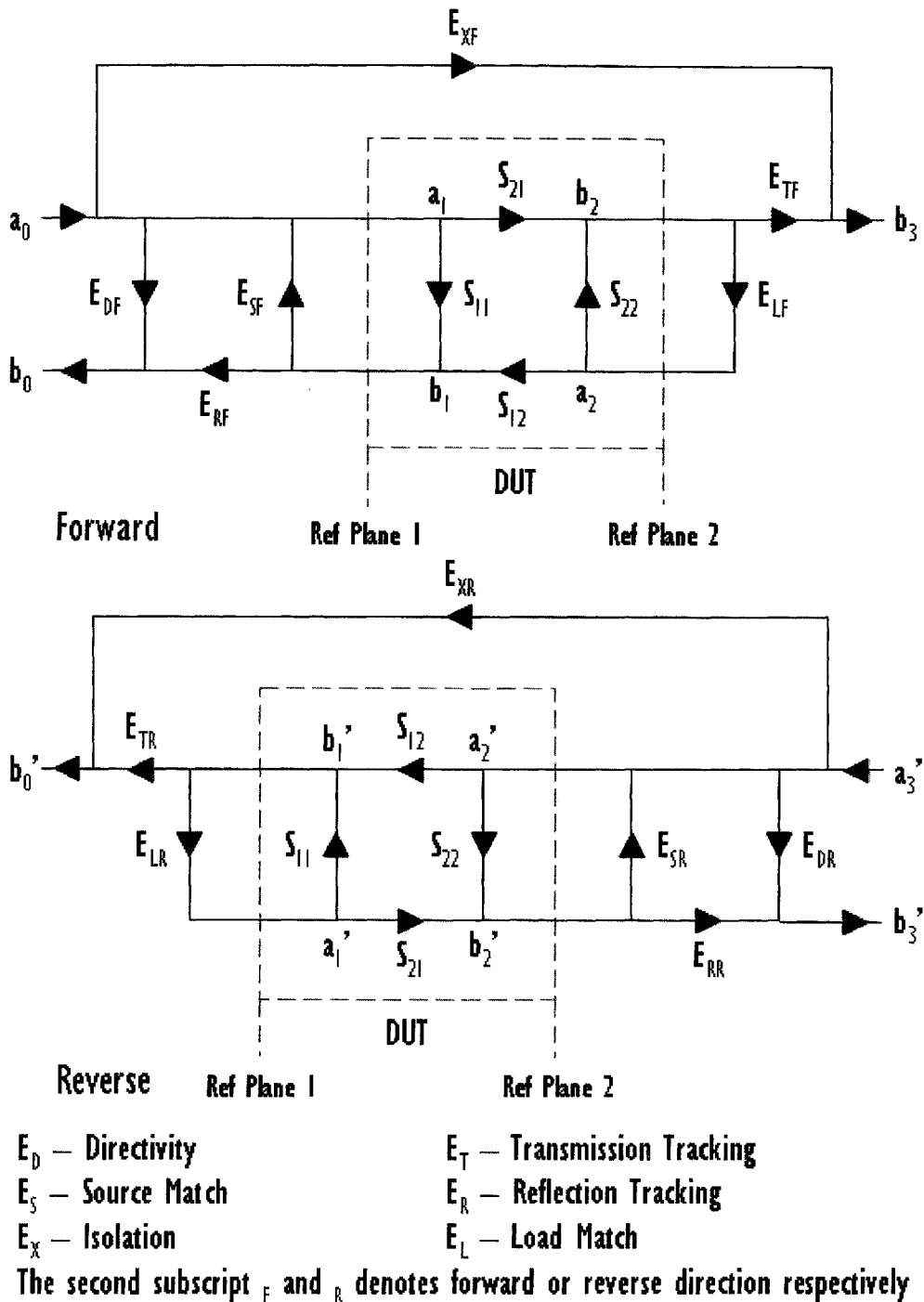


Figure 2.23(b) - Signal flow graph showing the error sources in two-port measurements.

The following equations are then used to calculate and correct the measured S-parameters for the DUT after solving for all the error coefficients,

$$S_{11,DUT} = \frac{\left[\left(\frac{S_{11M} - E_{DF}}{E_{RF}} \right) \left(1 + \frac{S_{22M} - E_{DR}}{E_{RR}} E_{SR} \right) \right] - \left[\left(\frac{S_{21M} - E_{XF}}{E_{TF}} \right) \left(\frac{S_{12M} - E_{XR}}{E_{TR}} \right) E_{LF} \right]}{\left[1 + \left(\frac{S_{11M} - E_{DF}}{E_{RF}} \right) E_{SF} \right] \left[1 + \left(\frac{S_{22M} - E_{DR}}{E_{RR}} \right) E_{SR} \right] - \left[\left(\frac{S_{21M} - E_{XF}}{E_{TF}} \right) \left(\frac{S_{12M} - E_{XR}}{E_{TR}} \right) E_{LF} E_{LR} \right]} \quad (2.35)$$

$$S_{12}^{\text{DUT}} = \frac{\left[1 + \left(\frac{S_{11M} - E_{DR}}{E_{RR}} \right) (E_{SR} - E_{LR}) \right] \left[\frac{S_{21M} - E_{XR}}{E_{TR}} \right]}{\left[1 + \left(\frac{S_{11M} - E_{DF}}{E_{RF}} \right) E_{SF} \right] \left[1 + \left(\frac{S_{22M} - E_{DR}}{E_{RR}} \right) E_{SR} \right] - \left[\left(\frac{S_{21M} - E_{XF}}{E_{TF}} \right) \left(\frac{S_{12M} - E_{XR}}{E_{TR}} \right) E_{LF} E_{LR} \right]} \quad (2.36)$$

$$S_{21}^{\text{DUT}} = \frac{\left[1 + \left(\frac{S_{22M} - E_{DR}}{E_{RR}} \right) (E_{SR} - E_{LR}) \right] \left[\frac{S_{21M} - E_{XF}}{E_{TF}} \right]}{\left[1 + \left(\frac{S_{11M} - E_{DF}}{E_{RF}} \right) E_{SF} \right] \left[1 + \left(\frac{S_{22M} - E_{DR}}{E_{RR}} \right) E_{SR} \right] - \left[\left(\frac{S_{21M} - E_{XF}}{E_{TF}} \right) \left(\frac{S_{12M} - E_{XR}}{E_{TR}} \right) E_{LF} E_{LR} \right]} \quad (2.37)$$

$$S_{22}^{\text{DUT}} = \frac{\left[\left(\frac{S_{22M} - E_{DR}}{E_{RR}} \right) \left(1 + \frac{S_{11M} - E_{DR}}{E_{RF}} E_{SF} \right) \right] - \left[\left(\frac{S_{21M} - E_{XF}}{E_{TF}} \right) \left(\frac{S_{12M} - E_{XR}}{E_{TR}} \right) E_{LF} \right]}{\left[1 + \left(\frac{S_{11M} - E_{DF}}{E_{RF}} \right) E_{SF} \right] \left[1 + \left(\frac{S_{22M} - E_{DR}}{E_{RR}} \right) E_{SR} \right] - \left[\left(\frac{S_{21M} - E_{XF}}{E_{TF}} \right) \left(\frac{S_{12M} - E_{XR}}{E_{TR}} \right) E_{LF} E_{LR} \right]} \quad (2.38)$$

The above methodology is error-free only if the calibration standards are ideal. However, in reality, the calibration standards are never ideal. A true open or short reflects 100 % of the incident signal, while a perfect load termination absorbs all the incident energy. An ideal thru connects two ports together with no physical length and loss. Even with the best conductor, a thru standard still have skin effects when operating frequency increases, resulting in conductor loss in the high RF regime. Nonetheless, correction factors for these calibration standards known as calibration coefficients made up for the standards' deficiencies. Incorporated into vector network analyzer, these coefficients allow for corrections of the deficiencies, making the standards appear as perfect to the network analyzer. For on-wafer RF measurements, values of these coefficients usually depend on the construction and physical dimensions of the RF probe as well as the calibration standards and they are normally supplied by probe manufacturers such as Cascade Microtech Inc.

2.3.2 Calibration Techniques

Various RF calibration techniques are available in the literature but this section focuses on four common techniques which are widely used in the industry, explaining their limitations and briefly describes their theories.

2.3.2.1 SOLT

Short-Open-Load-Thru (SOLT) calibration fundamentally solves for all twelve error terms shown in Figure 2.23(b). Short-Open-Load measurements at each port are sufficient to solve for six terms. A forward reflection calibration determines E_{DF} , E_{SF} , E_{RF} while reverse reflection calibration solves for E_{DR} , E_{SR} and E_{RR} . Thru standard takes care of the remaining terms such as transmission frequency response in both directions i.e. E_{TF} and E_{TR} . With the thru connected, use one port to measure the match presented by the other port and measuring in each direction provides the load terms, E_{LF} and E_{LR} . After removing the thru and terminating both ports, measuring the insertion loss will reveal any leakage between ports, thereby giving the isolation terms E_{XT} and E_{XR} , completing all the twelve error terms.

The twelve calibration measurements provide more information than required to determine the twelve terms in the error model. Since 3 of the error terms in the model are solved twice, the equation set is over-determined and this may be a big shortcoming for the SOLT calibration technique. Calibration validity can be dubious if solving different equations for the same error terms yields unequal results. Accuracy of the standards is also another fundamental limitation of the SOLT method. Well-comprehended understandings of the standards' characteristics lead to highly precise calibration. Nonetheless, small divergence from ideal scenarios can lead to large errors, manifested in regions of the smith chart far from the calibration standard [49]. Also, repeatable behavior

of these standards after multiple usages is highly questionable and accurate characterization of these standards up to 20 GHz is extremely laborious [50].

2.3.2.2 TRL

Thru-Reflect-Line (TRL) [51] calibration technique is based on the transmission line standards, with a short transmission line serving as its thru standard. The reflect standard can be either an open or a short and only the sign of its reflection coefficient is required. Perfect open or short is not required for the reflect but open is preferred since it operates over a much wider bandwidth. The precision standard for this calibration technique is the line. Its characteristic impedance determines the reference impedance for the entire RF test system. However, deviations in the conductor etching process could result in slight variations of the characteristic impedance and this can lead to measurement errors. TRL's inability to correct for line loss contributed by the metal conductor's resistivity and skin effects are its major negative aspects.

2.3.2.3 LRM

The Line-Reflect-Match (LRM) [52] method employs a precision load to define the system characteristic impedance. Either an open or short can be used as the reflect. As in SOLT, the load must be well-defined if not, the calibration sensitivity is degraded. The line standard sets the electrical reference plane for the measurement system. Contrary to SOLT, neither the open's capacitance nor the short's inductance are required to be known prior to calibration because of the mathematics involved [53]. Having the same reflect and load standards to calibrate both ports give the most accurate results. The match, unique for LRM technique, is also its main weakness as parasitic inductance may potentially corrupt the calibration accuracy.

2.3.2.4 LRRM

The Line-Reflect-Reflect-Match (LRRM) is almost identical to LRM but uses the additional reflect to alleviate LRM's principal flaw, which is the parasitic inductance in the match (load) standard. Another key benefit of the LRRM calibration technique is that the match does not have to be the system's characteristic impedance. Like LRM, the short and open standards in LRRM do not have to be well-defined. Characterizing the line necessitates only to finding its electrical delay and loss and all other information related to the standards is not essential to obtain quality calibrations.

The primary advantage offered by LRRM is accurate characterization of the match standard's parasitic inductance, overcoming the weakness in LRM. RF measurement of the match is only performed at one port, and as such; there are no discrepancies from using different match standards on opposite ports. LRRM also avoids the problem of RF probe placement inconsistencies which lead to variations in the standard's parasitic inductance. Calibrating with one match standard measured on one port eliminates differences in inductances measured on both ports.

The match standard's parasitic inductance is evaluated by focusing on the open since it is the most repeatable standard. The open should exhibit no conductance upon calibration. If after calibration, the measurement displays negative conductance, the match is deemed to have some inductance. LRRM iteratively adjusts the match's calibration coefficient until the open's conductance equals to zero. Nonetheless, the match measured on one port is assumed to behave identically on the other port. This can lead to error in the return loss measurement, S_{11} and S_{22} when the two ports are actually not the same.

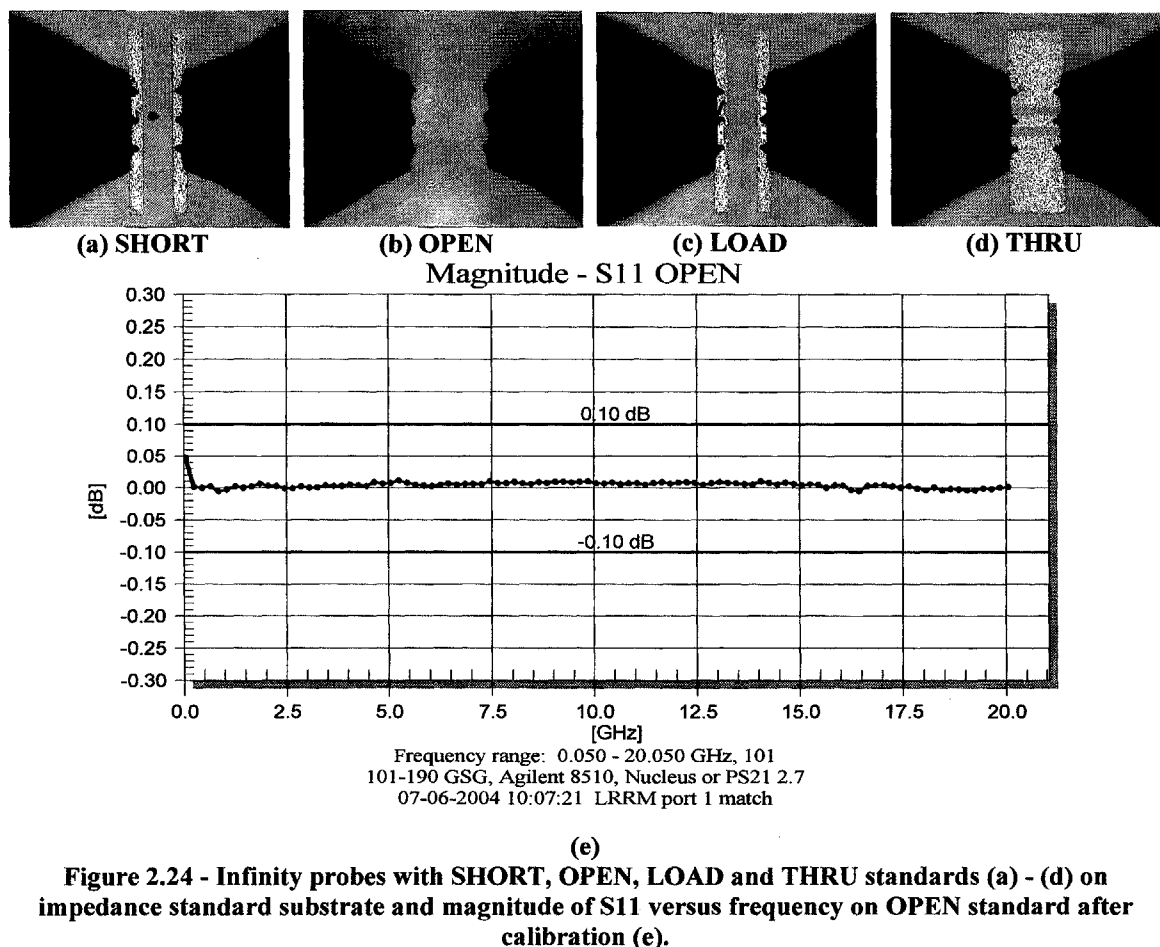
2.3.2.5 Summary of Calibration Techniques

Calibration removes systematic errors from the test systems, ranging from cable and probe losses to connector reflections and vector network analyzer (VNA) imperfections. In

practice, choosing which calibration method is often determined by the type of standards which can be fabricated reliably for that particular test setup. At high frequencies, if good line definitions are available, TRL is preferred but for on-wafer measurements, cumbersome long and lossy line structures must be included in the testchip and wafer if it is required to cover the lower frequency spectrum. If high quality broadband standards are available, SOLT is preferred. For on-wafer RF measurements with fixed pitch probes, LRRM using Impedance Standard Substrate (ISS) is preferred and widely adopted in the industry. Table 2.3 consolidates the four calibration techniques discussed in this section. Figure 2.24, on the other hand, shows LRRM calibration of Infinity Probes up to 20 GHz using ISS supplied by Cascade Microtech Inc.

Table 2.3 - Summary of calibration techniques for RF measurements.

Calibration Method	SOLT	TRL	LRM	LRRM
Ideal Standards Required	Short, Open, Load, Thru	Line	Line, Match	Line, Match's Resistance
Non Ideal Standards Required	None	Thru, Reflect	Reflect (Open or Short)	Reflect, Match's Inductance
Advantages	Precise Coaxial Standards easy to build	Transmission line standards, easy to understand and fabricate	Only Load must be well-defined, accurate Results derived from same Reflect and Load standards use on both ports	Automatic calibration of match's parasitic Inductance and Match need not be Z_0
Disadvantages	Over-determination of Error Terms, very sensitive to accuracy of standards and can be reliable only up to 20 GHz.	Sensitive to Z_0 of Lines and require additional lines structures on substrate for on-wafer tests	Parasitic Inductance may corrupt the load	Both Ports using 1 match can give rise to error if they are not identical



(e)
Figure 2.24 - Infinity probes with SHORT, OPEN, LOAD and THRU standards (a) - (d) on impedance standard substrate and magnitude of S11 versus frequency on OPEN standard after calibration (e).

2.3.3 RF Probes

Before the introduction of RF probes, knowing the behavior of a device on the wafer is a burdensome process which involves dicing up the wafer, mounting dies onto test fixtures. Even then, discriminating the responses of bonding wires and PCB traces from the devices when characterized using a calibrated instrument becomes the next obstacle for test engineers. Such practices are impractical for high-volume production test since preparations of the test fixtures are tedious and time-consuming.

As technology advances, RF probes are used to launch RF signals into devices on the wafers. In particular, air coplanar probes with different probe tip materials have been widely used. Flexible beryllium-copper probe tips are popular for probing gold pads on fragile GaAs substrates since they do not damage the pads. Stiff tungsten RF probes, on the other hand, are popular among engineers characterizing silicon-based devices.

Nonetheless, over-traveling action of these probes on the test pads are required to break through the aluminum oxide layer to ensure low contact resistance. As such, larger pad designs that not only waste expensive test chip space but introduce huge pad parasitics are required to accommodate the over-traveling actions of these RF probes. Also, during test, aluminum oxide buildup can vary the contact resistance and the residual oxide material accumulated on the tungsten probe tips would degrade its contact resistance with extended use. These are common issues encountered when using RF probes with tungsten tips.

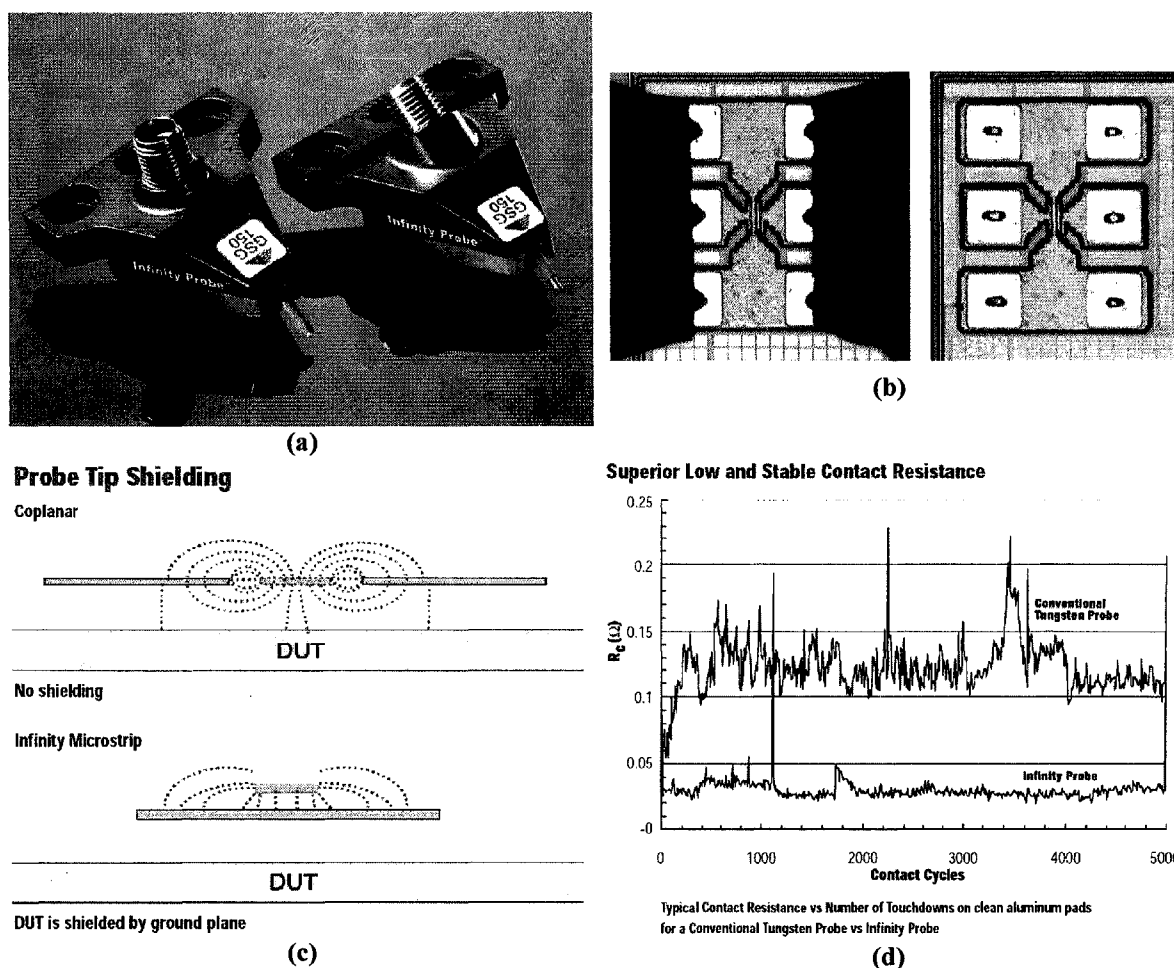


Figure 2.25 - RF Infinity Probes (a), small contact marks allowing pads of 50 x 50 μm (b), microstrip to probe tips provided shielding to DUT (c), nickel alloy probe tip allow stable and low contact resistance compared tungsten probe tip (d). Photos reproduced with permission from Cascade Microtech Inc.

A new RF probe, named Infinity Probe [54], sets high benchmarks for the RF device characterization and modeling community when it was launched in 2003 by Cascade Microtech Inc. This revolutionary probe combines extremely low contact resistance on

aluminum pads with unsurpassed RF measurement accuracy to provide highly reliable and repeatable measurements. Unlike air coplanar probes, adopting lithography thin-film construction process and microstrip design up to the probe tips, Infinity Probe has superior field confinement that suppresses unwanted transmission modes and coupling to nearby devices. Non-oxidizing nickel alloy tips together with innovative force delivery system allow small contact marks to be made on pads with only contact resistance of less than 0.05Ω . The use of such probes allows smaller pads to be designed, thereby reducing the pad parasitics and test chip size required for device characterization and modeling. Figure 2.25 illustrates the various features of the Infinity probe discussed in this sub-section.

2.3.4 De-embedding, Extending Measurement Plane to Devices

RF engineers are interested in the intrinsic characteristics of the devices such as its doping level, transit frequency, gain, inductance, Q-factor, etc. It is not possible to place RF probes directly on the devices to measure its performance. Instead, on-wafer characterization of devices requires probe pads and interconnects to access the DUT. The disadvantage is that parasitics of the pads and interconnects are often very much larger than the device itself. The procedure of calibration as discussed in Section 2.3.1 defines the reference plane at the probe tips. To reveal the intrinsic DUT's RF behavior, probe pads and interconnects (test leads) must be de-embedded by shifting the electrical reference plane from the RF probes to the device under test.

In short, preparation to characterize a DUT on the wafer involves a two-step process. First, the vector network analyzer is calibrated, setting the reference plane to the probe tips. Then the device is measured together with a set of dummy or calibration structures to move the electrical reference plane from the probe tips to the DUT. This section outlines a few methods to de-embed the probe pad and test lead parasitics, and these techniques can be applied to both passive and active devices. In general, the test structures for de-embedding should have the same metal pattern as the DUT layout and because substrate resistivity and inter-metal dielectric thickness vary across the wafer, these de-embedding structures must be located near the DUT.

2.3.4.1 One-Step OPEN De-embedding

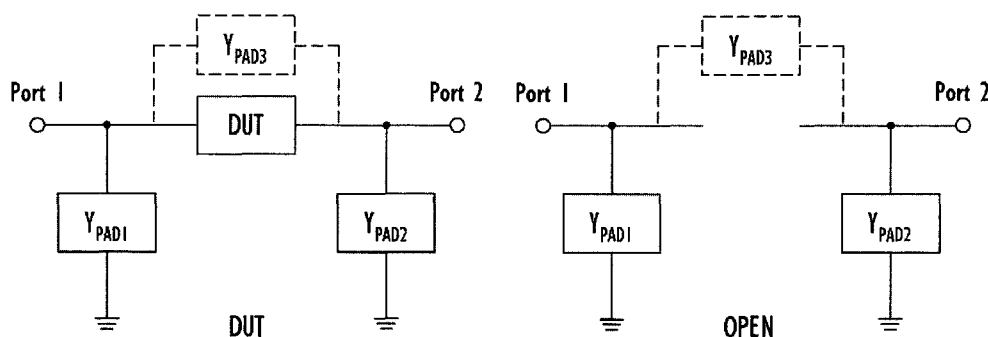


Figure 2.26 - Equivalent circuits for DUT and OPEN de-embedding structure.

OPEN structures are used to de-embed the shunt capacitances of the pad and test leads (if any). Figure 2.26 shows the equivalent circuits for a device under test and its corresponding OPEN de-embedding test structure on silicon. De-embedding with only an OPEN structure is valid when test leads are part of the device as in the case of spiral inductors and interconnects or for the case whereby lengths of the test leads are short with respect to the wavelength of the RF signal. Pad capacitance is formed by the oxide layers that are sandwiched between metal layers and the substrate. Its capacitance value is a function of the pad size, the oxide dielectric constant and thickness while resistance value is depend on the resistivity of the substrate. Based on two-port network theories, to de-embed these shunt capacitance and resistance, simply subtract the measured admittance matrix of the OPEN structure from those of the DUT as shown in Equation 2.39.

$$\text{Device } Y = \text{DUT } Y - \text{OPEN } Y \quad (2.39)$$

where subscript Y refers to the measured admittance matrices for the test structures.

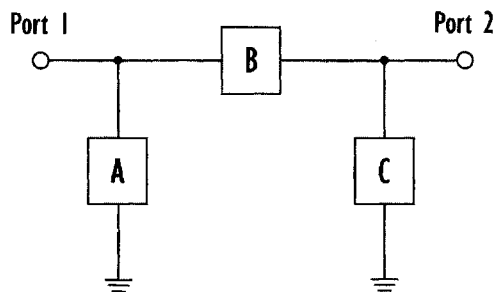


Figure 2.27 - 2-Port Pi-network.

To help understand how the admittance matrix works, Figure 2.27 shows a Pi-network and its corresponding admittance Y-matrix can be defined as,

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} A+B & -B \\ -B & C+B \end{bmatrix} \quad (2.40)$$

Therefore,

$$\begin{aligned} A &= Y_{11} + Y_{12} \text{ or } Y_{11} + Y_{21} \\ B &= -Y_{12} \text{ or } -Y_{21} \\ C &= Y_{22} + Y_{12} \text{ or } Y_{22} + Y_{21} \end{aligned} \quad (2.41)$$

2.3.4.2 Two-Step OPEN and SHORT De-embedding

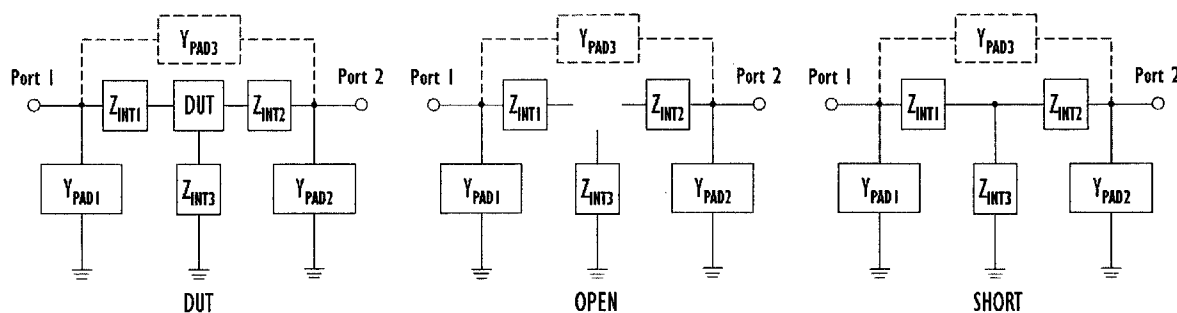


Figure 2.28 - Equivalent circuits for DUT, OPEN and SHORT de-embedding structures.

Having an additional SHORT de-embedding test structure to the previous method enhances the measurement accuracy of the intrinsic device by removing series parasitics such as contact resistances associated to probing, series resistances and inductances associated with the test leads. A two-step de-embedding technique is necessary when the test leads' inductances and resistances affect the characteristics of the devices significantly. Such scenarios occur for devices such as transistors since they are very small compare to the overall RF test structure. Figure 2.28 shows the equivalent circuits for the DUT, OPEN and SHORT de-embedding structures. To move the reference plane to the device, the S-parameters of these three structures have to be measured separately. The admittance matrices of the DUT and SHORT are subtracted with admittance matrices of the OPEN structure. These two steps help to remove the shunt parasitics of the pad from the DUT and the SHORT structures. Thereafter, the two resultant admittance matrices are converted to impedances matrices for removal of series parasitic components as outlined in Equation 2.42.

$$\begin{aligned}
 A_Y &= \text{DUT}_Y - \text{OPEN}_Y \\
 B_Y &= \text{SHORT}_Y - \text{OPEN}_Y \\
 \text{Device}_Z &= A_Z - B_Z
 \end{aligned}
 \tag{2.42}$$

where subscript Y and Z refer to the measured admittance and impedance matrices respectively for the test structures.

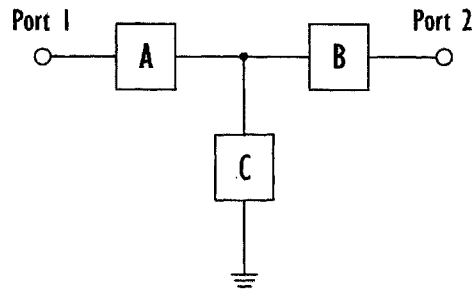


Figure 2.29 - 2-Port Tee-network.

To help understand how the impedance matrix works, Figure 2.29 shows a Tee-network where its corresponding impedance Z-matrix can be written as,

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} A+C & C \\ C & B+C \end{bmatrix} \quad (2.43)$$

Therefore,

$$\begin{aligned} A &= Z_{11} - Z_{12} \text{ or } Z_{11} - Z_{21} \\ B &= Z_{22} - Z_{12} \text{ or } Z_{22} - Z_{21} \\ C &= Z_{12} \text{ or } Z_{21} \end{aligned} \quad (2.44)$$

Chapter 3 - Physical Layout Design Optimization of Spiral Inductors

Exploitation of the mature and cost-effective silicon technologies requires the availability of optimized integrated inductors with high Q-factors to enhance the performance of RF circuits. Resistive metallization and lossy silicon substrate continue to be major roadblocks to achieving high performance integrated inductors. Therefore, thorough studies to develop reliable methodologies for optimizing the physical layout of spiral inductors are essential even though it requires huge amount of test chip resources. Know-how in designing inductors will bring about long term benefits such as reduction in circuit design iterations which help shorten the product time-to-market cycle, cost-effectiveness in using silicon die area for products and improvements in circuit performance to satisfy stringent system level specifications.

In the past decade, many techniques have been proposed to optimize the physical layout of silicon-based spiral inductors. One popular approach adopted by many research groups is to optimize layout of the inductor by making use of device models as discussed in Section 2.1.4.5. Such convenient optimization algorithms are however limited by the validity of these models in making accurate predictions of the spiral inductors' behavior at high frequencies when their physical design parameters such as core diameter, conductor spacing and width are modified accordingly. Another notable methodology optimizes the physical layout of spiral inductors by having variable conductor width at different turns of the inductor as presented in Section 2.1.4.4. This scheme, though novel, focuses just on Q-factor optimization without explicitly reporting that similar inductance values are ensured while comparing the performances of inductors with different designs. Comparing inductors with the same inductance values is critical since Q-factor is determined by both the inductive and resistive behavior of the spiral inductors.

In this chapter, a novel yet simple to understand methodology is proposed for the first time to quantitatively show how each physical design parameters of core diameter, conductor spacing and width affect the performance of silicon-based spiral inductors. The methodology further outlines a design flow that optimizes the physical layout of the spiral inductor, demonstrating for the first time, alignment of the inductor's peak Q-factor response to the operating frequency of the circuit. The use of such optimized inductors is demonstrated to improve the performance of a giga-hertz amplifier. Most importantly, the experiments reported in this chapter compare inductors with identical inductance values.

3.1 Test Structure Fabrication and Inductors' Figure of Merits

The spiral inductor test structures are fabricated in a 6-metal layer 0.18 μm RFCMOS process technology with plug-in analogue/RF modules such as deep-Nwell, MIM capacitor and 2 μm thick top metal back-end-of-line process flow outlined in Section 2.2.2. The circular spiral coil of the inductor is constructed utilizing metal 6 while metal 5 is used for its underpass. On-wafer RF device measurements are performed using Agilent 8510C Vector Network Analyzer and Cascade Microtech RF Infinity probes. The wafer and RF probes are shielded within the Micro-chamber of Cascade Microtech S300 semi-automated probe station during the measurements. Two-port S-parameters of the inductors are extracted over the frequency range from 50 MHz to 20.05 GHz. P+ taps are included in the ground frame of the 6-pad GSG test structures to ensure proper grounding of the substrate. To facilitate de-embedding of pad capacitance without the inductors, open calibration structures are fabricated next to the device. Parasitics of the test pads are accurately de-embedded by subtracting Y-parameters of the open calibration structures from the spiral inductor test structures, as discussed in Section 2.3.4.1.

From the de-embedded Y parameters, inductance, L and quality factor, Q of integrated inductors are determined by [31],

$$L = \frac{\text{Im ag} \left[\frac{1}{Y_{11}} \right]}{2 \times \pi \times \text{Frequency}} \quad (3.1)$$

$$Q = -\frac{\text{Im ag} [Y_{11}]}{\text{Real} [Y_{11}]} \quad (3.2)$$

And series resistance, R, for spiral inductors can be expressed as follows [55],

$$R = \text{Real} \left[-\frac{1}{Y_{12}} \right] \quad (3.3)$$

L and Q are both extracted from Y_{11} and not Y_{12} parameters since it is important to include and consider the effects of the lossy silicon substrate when evaluating the overall performance of the spiral inductors. On the contrary, parasitic series resistance, R associated with the metallization is extracted from Y_{12} parameter to show the skin effects of metallization at radio frequencies excluding substrate losses. However, this is only valid within the frequency range or sizes of the inductors such that a simple lumped element pi model is valid in predicting the behavior of the spiral inductors.

A novel and simple layout optimization technique to systematically investigate effects of core diameter, metallization spacing and width on the performance of integrated spiral inductors will be demonstrated in the following sections. For each of these three physical design parameters, this methodology focuses on careful considerations in designing the test structures which ensure unbiased performance comparison of spiral inductors with similar inductance values. Experiments that compare characteristics of inductors with different inductance values offer little understanding as to how the core diameter, metallization spacing and width would affect the behavior of these spiral inductors since Q-factor of an inductor is determined by both its resultant magnetic energy storage capability and resistive loss as shown in Equation 3.2. Last but not least, the proposed methodology also exploits the understanding of the inductor's resistive and substrate losses with respect to its physical layout so that its peak Q-factor can be aligned at the operating frequency of the circuit.

3.2 Effects of Core Diameter

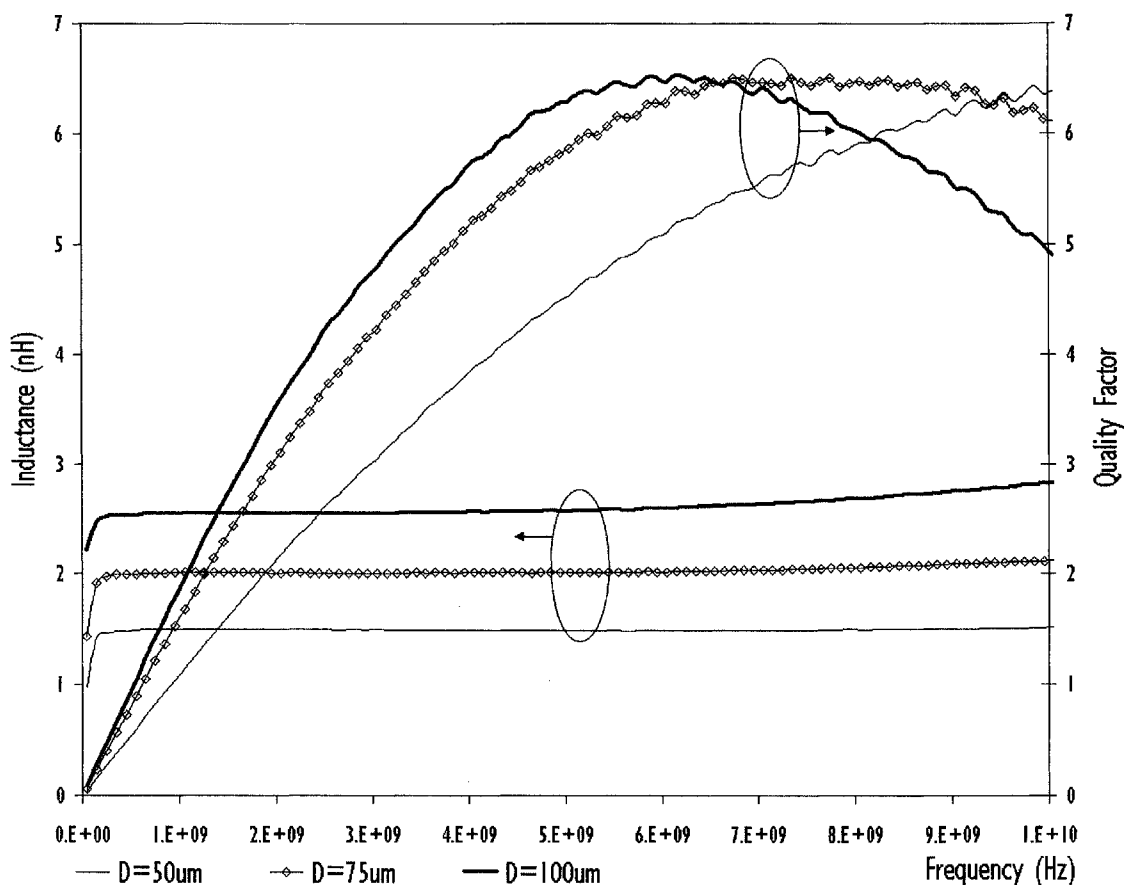


Figure 3.1 - Inductance and Q-factor versus frequency for 3-turn spiral inductors with different core diameters.

The inner core diameter of spiral inductor is an important physical design parameter to consider since it determines the overall size of the inductor. Being the largest device in RFICs, the number of inductors used would most probably establish the final product die size. Resultant effects on device characteristics and area consumption due to core diameter are at trade-offs and this must be well-comprehended in RFIC designs. When 3-turn spiral inductors with different inner diameters (50, 75 and 100 μm) and fixed conductor width are fabricated and characterized, they yield different inductance values as plotted in Figure 3.1. Because the inductance values are different, effects of core diameter on the performance of inductors cannot be differentiated and analyzed. As such, to investigate the impact of the core diameter, a few sets of test structures are designed with fixed width and total conductor lengths to obtain spiral inductors with similar inductance

values. Figure 3.2 illustrates die photos of integrated inductors designed with different core diameter values of 10, 50, 100 and 150 μm but with fixed width, spacing and total conductor length of 8, 1.5 and 1000 μm respectively.

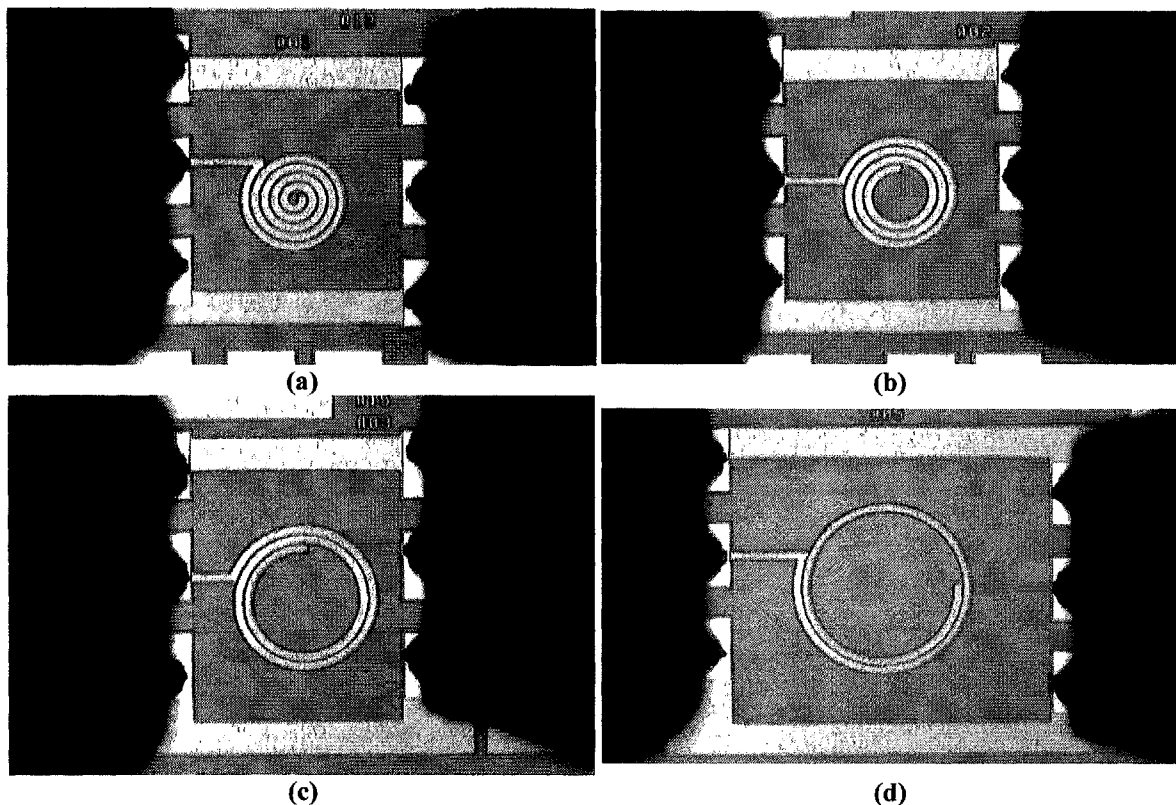


Figure 3.2 - Die photos of spiral inductors with identical conductor length (1000 μm), and width (8 μm) but different core diameters (a) 10 μm , (b) 50 μm , (c) 100 μm and (d) 150 μm .

Since the total conductor lengths and widths are kept constant for all four test structures, they have almost the same low frequency inductance and resistance values as shown in Figure 3.3. It is very critical to monitor the series resistance plots at low frequencies so as to be sure that any enhancements to the Q-factor is a result of design improvement and not due to inconsistent probe contact resistances when measuring these inductors. It is also important to emphasize again that if the number of turns for the inductor is fixed instead of the total conductor length, it would be impossible to obtain inductors having the same inductance values since their total conductor lengths would be different. From Figure 3.3, at 3 GHz, where the inductance values are almost identical, Q-factor improves significantly by more than 57 % when the core diameter of the spiral inductors increases

from 10 to 100 μm . At 7.5 GHz, when the inductance values defer by about 0.2 nH, the same amount of increase in diameter result in a noteworthy 73 % enhancement in Q-factor.

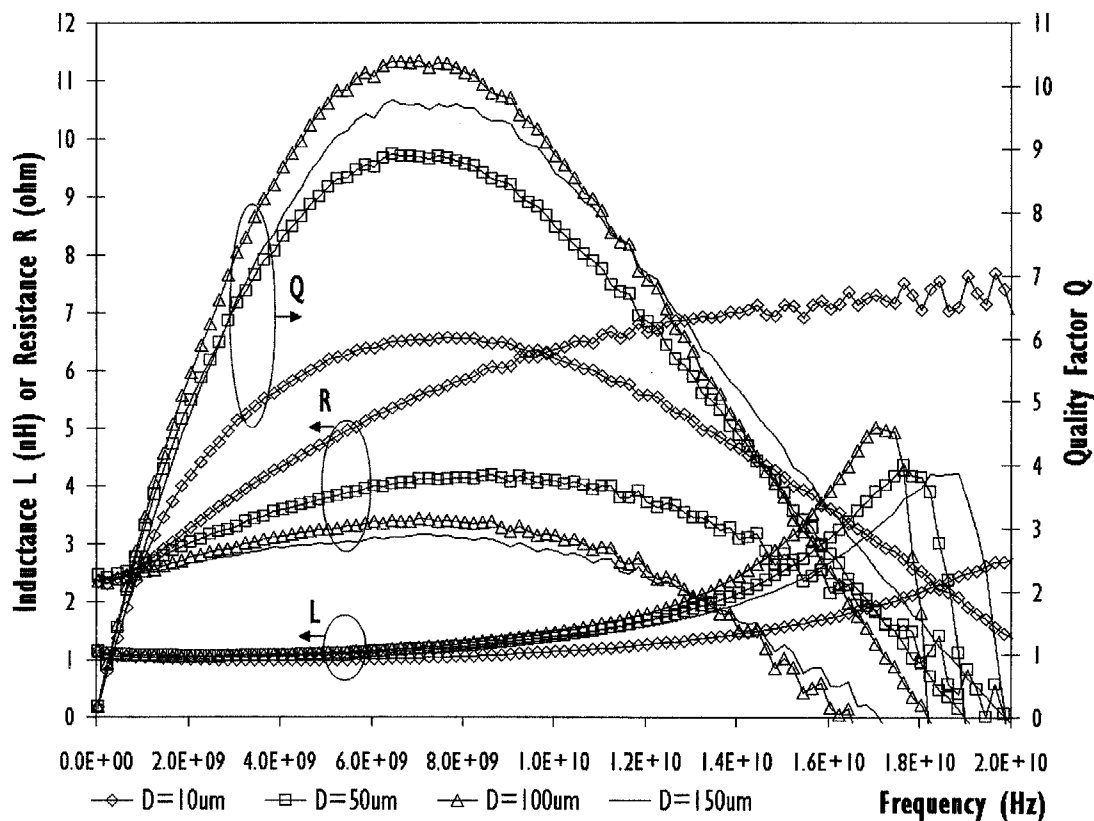


Figure 3.3 - Inductance, Q-factor and series resistance versus frequency for inductors with identical conductor length (1000 μm) and width (8 μm) but different core diameters.

Figure 3.4 shows that when the total conductor length is increased to 2000 μm , identical observations of similar inductances and low frequency series resistances are noted for all the integrated inductors with different core diameters. At 3 GHz, Q-factor improved by 46 % when diameter increased from 10 to 100 μm . Figure 3.5, on the other hand, further demonstrates that for spiral inductors with 3500 μm in total conductor length, at 2 GHz, the Q-factor can improve by more than 30 % when 100 μm as opposed to 10 μm is used as the diameter of the spiral inductors. Experimental results from these three sets of inductors with similar inductance values reveal that core diameter have great influence over the Q-factor of spiral inductors because at high frequencies, inductors with large core diameter tend to have smaller series resistance as shown in all the series resistance versus

frequency plots. For the width of 8 μm , the optimal diameter value noted from the experimental results is about 100 μm and further increments of core diameter value do not enhance the Q-factor.

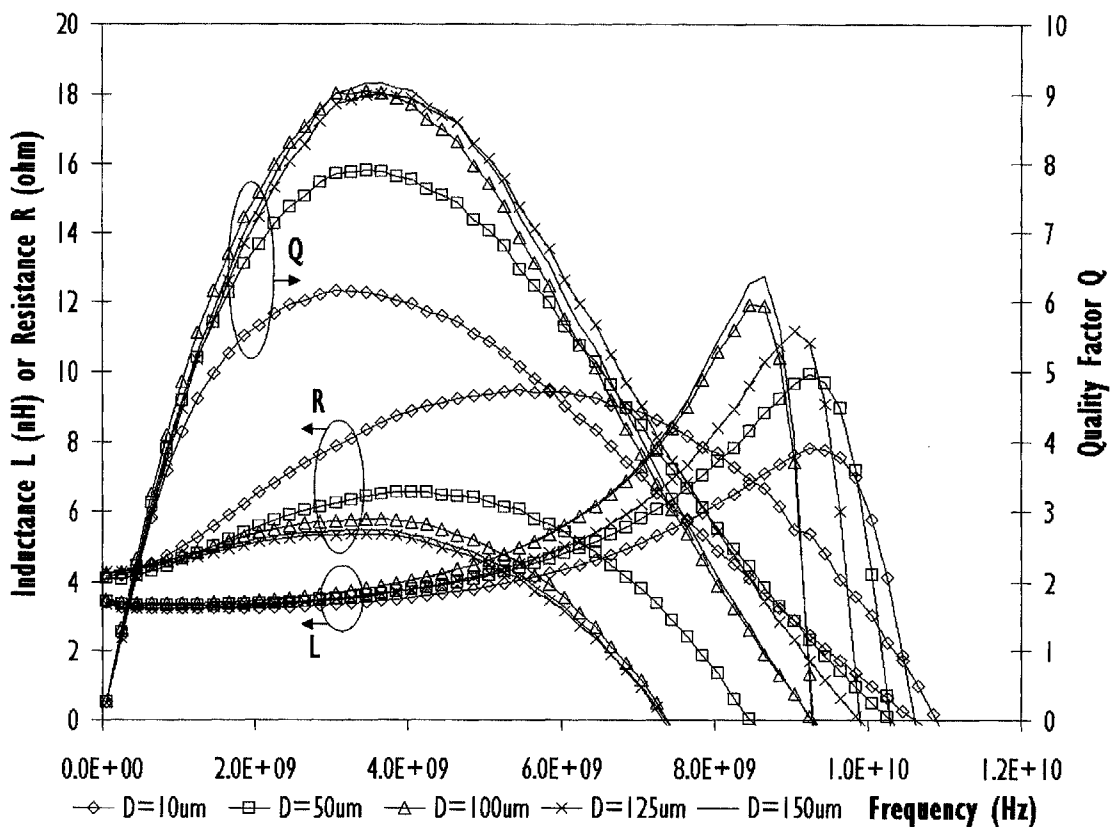


Figure 3.4 - Inductance, Q-factor and series resistance versus frequency for inductors with identical conductor length (2000 μm) and width (8 μm) but different core diameters.

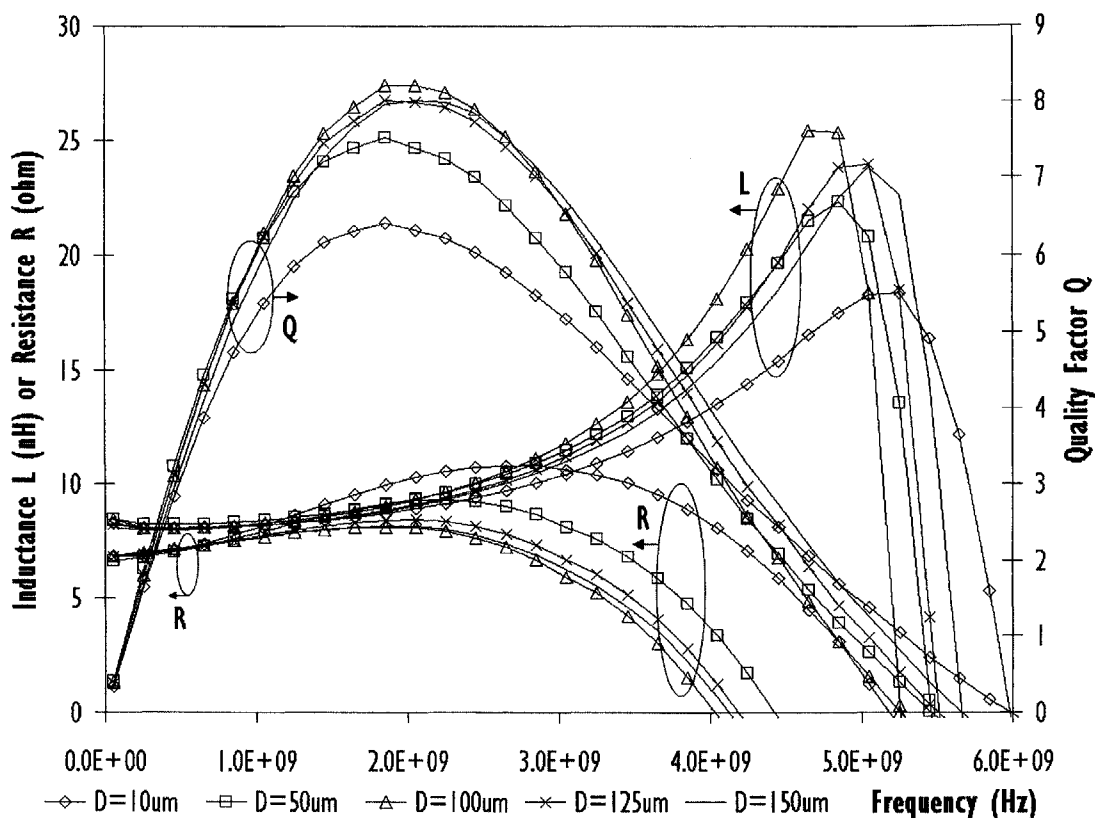


Figure 3.5 - Inductance, Q-factor and series resistance versus frequency for inductors with identical conductor length ($3500 \mu\text{m}$) and width ($8 \mu\text{m}$) but different core diameters.

The interactions between the inductor's core diameter and its high frequency resistive behavior can be explained by the formation of conductor eddy current. The circular inductor shown in Figure 3.6 carries a current, I_{spiral} , and generates an associated magnetic field, B_{spiral} that has a maximum intensity at the center of the spiral. For the case of a large-width inductor with a very small core diameter, an enormous part of this magnetic field does not pass through the center of the spiral but rather through its inner turns. In accordance to Faraday's and Lenz's laws, an electric field is magnetically induced on these inner turns, producing circular eddy currents, I_{eddy} , which flow in the direction opposing the original change in magnetic field. The magnitude of this induced electric field is proportional to the derivative of $B(t)$ with respect to time, as such, this effect is very significant at giga-hertz frequencies. The formation of such eddy currents causes a non-uniform current flow in the inner turns of the spiral, increasing the series resistance, which in turn reduce the Q-factor of the spiral inductor [56].

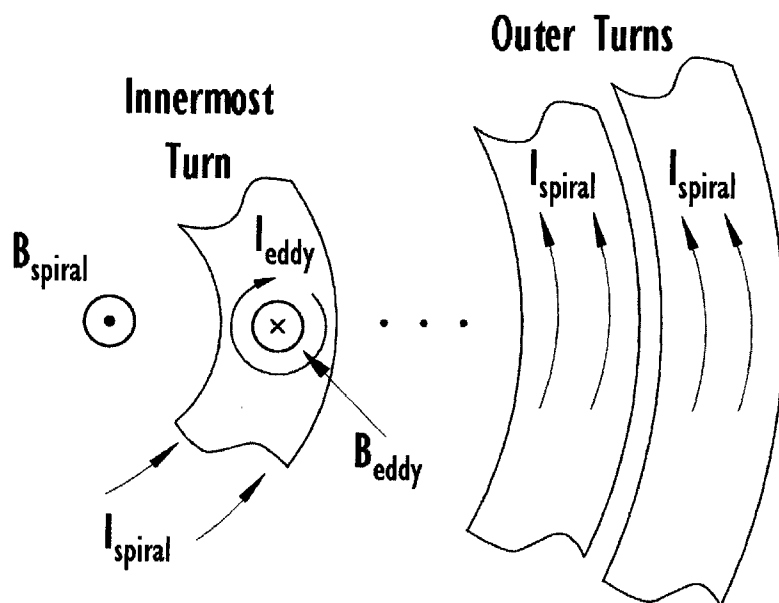


Figure 3.6 - Formation of conductor eddy current in the core turns of spiral inductors.

Interestingly, when a smaller conductor width of $4\ \mu\text{m}$ is used for inductors with total conductor length of $2000\ \mu\text{m}$, the conductor eddy current effect is not as pronounced since majority of the magnetic field passes through the hollow core of the spiral inductor and hence the core diameter has little effect on Q-factors of the integrated inductors as shown in Figure 3.7. However, at 3 GHz, for the same conductor length of $2000\ \mu\text{m}$, when $16\ \mu\text{m}$ conductor width is used, the Q-factor of the inductor improved tremendously by 34 % when diameter increases from 50 to $150\ \mu\text{m}$, compared to an improvement of only 14.5 % for the case of $8\ \mu\text{m}$ conductor width, as summarized in Figure 3.8 and Figure 3.4 respectively. While the conductor width widens, the distance between the outer turns of the inductor and its centre hollow core increases extensively. It is then more probable for the inductor's magnetic field to pass through the inner turns instead of its hollow core and therefore, for large-width inductors, core diameters should be large to avoid formation of conductor eddy current. These experiments have examined the conductor eddy current effect quantitatively and, in general, the core diameter should be sufficiently large, more than $100\ \mu\text{m}$, to minimize this adverse effect on the performance of spiral inductors.

However, for a relatively small inductor with narrow conductor width, it is not necessary to have a large core diameter since it would only waste expensive silicon real estate.

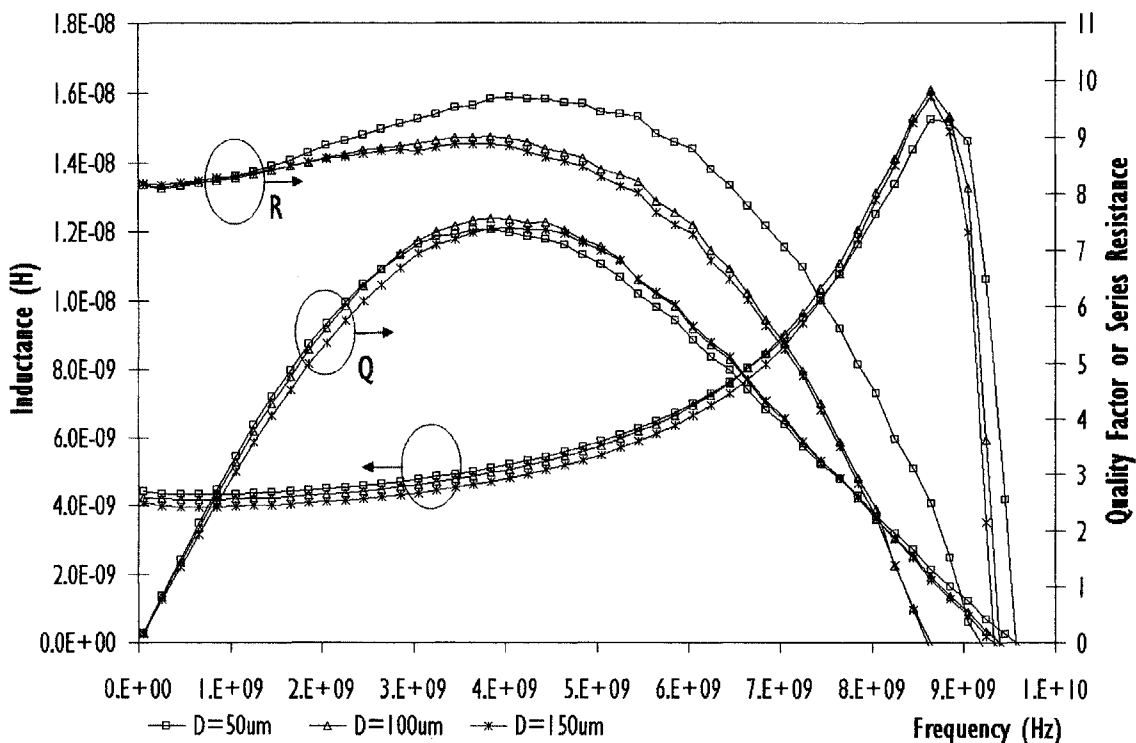


Figure 3.7 - Inductance, Q-factor and series resistance versus frequency for inductors with identical conductor length (2000 μm) and width (4 μm) but different core diameters.

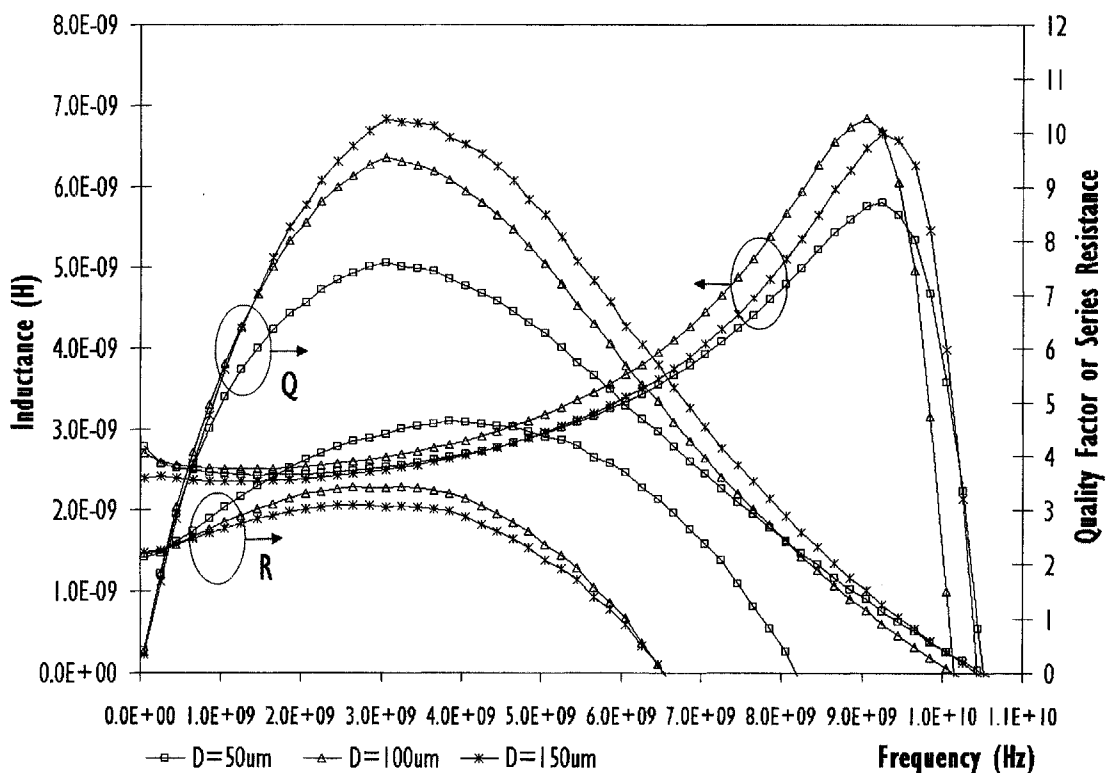


Figure 3.8 - Inductance, Q-factor and series resistance versus frequency for inductors with identical conductor length (2000 μm) and width (16 μm) but different core diameters.

3.3 Effects of Metal Conductor Spacing

To investigate the effects of conductor-to-conductor spacing on spiral inductors, four inductors with identical conductor length, width and core diameter of 2000, 8 and 100 μm respectively are designed and fabricated having different spacing of 3, 6, 9 and 12 μm . Die photos of these four inductor test structures are shown in Figure 3.9. On-wafer characterization reveals that metallization spacing does not significantly affect the Q-factor performance of spiral inductor. As depicted in Figure 3.10, as conductor spacing decreases, the inductance values increase due to more mutual inductive coupling between the conductors within the spiral coil. At low frequency, all four inductors have identical series resistance but in the higher RF regime (2 - 4 GHz), inductor with spacing of 3 μm has the largest series resistance and this resistance decreases as the conductor spacing for the inductor increases.

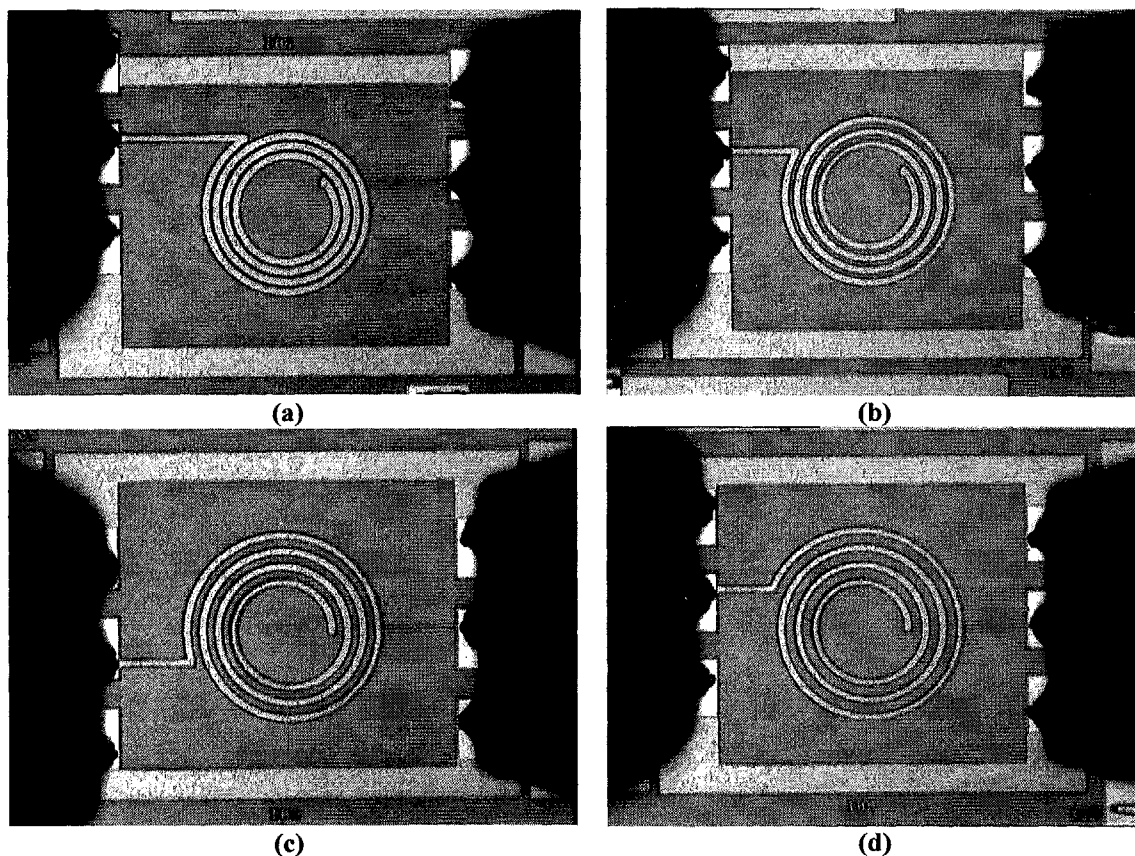


Figure 3.9 - Die photos of spiral inductors with identical conductor length (2000 μm), width (8 μm) and core diameter (100 μm) but different metal-to-metal spacing of 3 (a), 6 (b), 9 (c) and 12 μm (d).

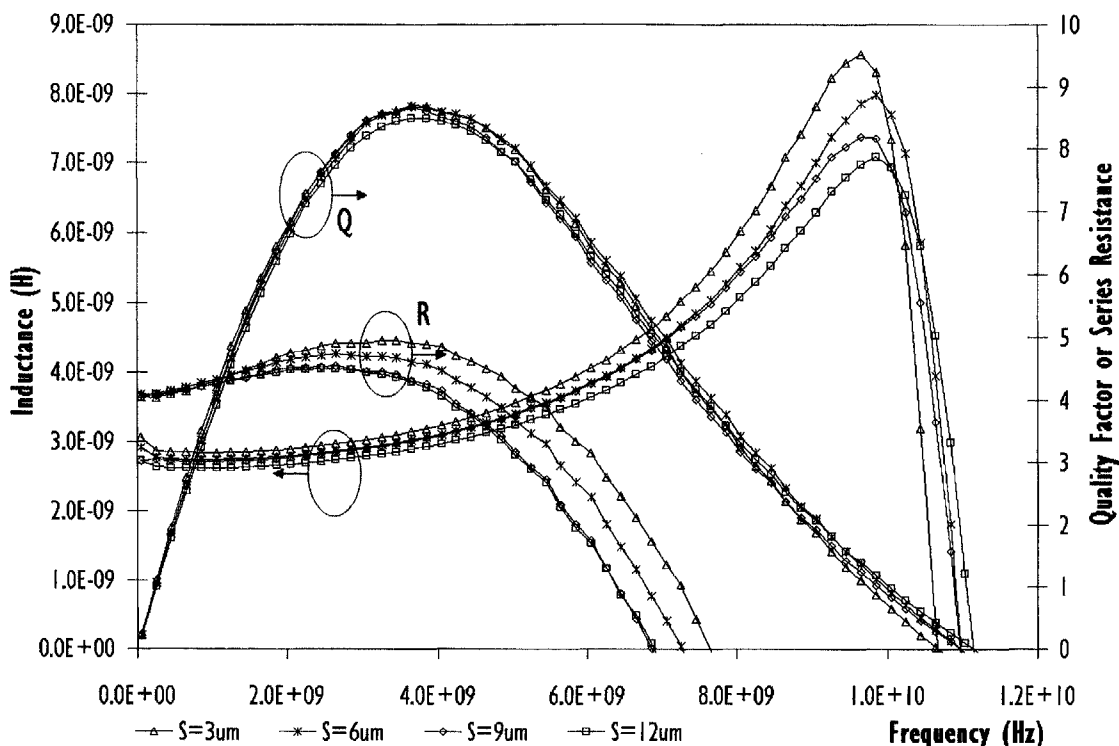


Figure 3.10 - Inductance, Q-factor and series resistance versus frequency for inductors with identical conductor length (2000 μm), width (8 μm) and core diameters (100 μm) but different spacing.

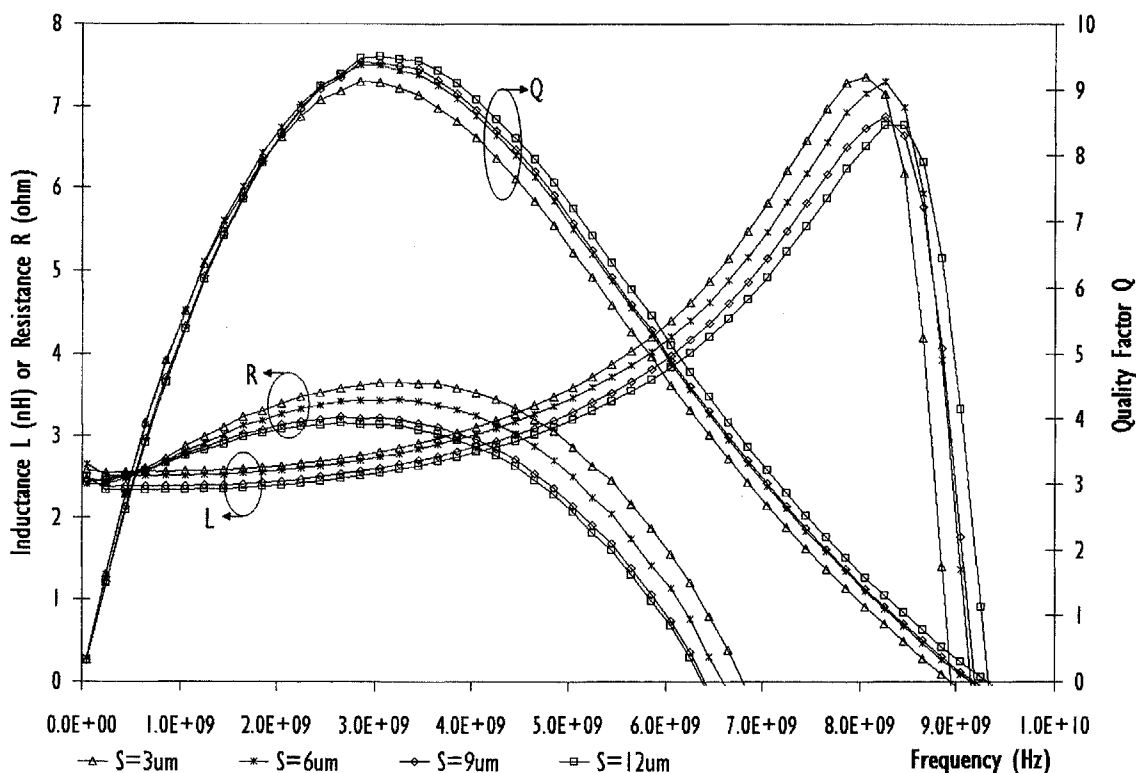


Figure 3.11 - Inductance, Q-factor and series resistance versus frequency for inductors with identical conductor length (2000 μm), width (16 μm) and core diameters (100 μm) but different spacing.

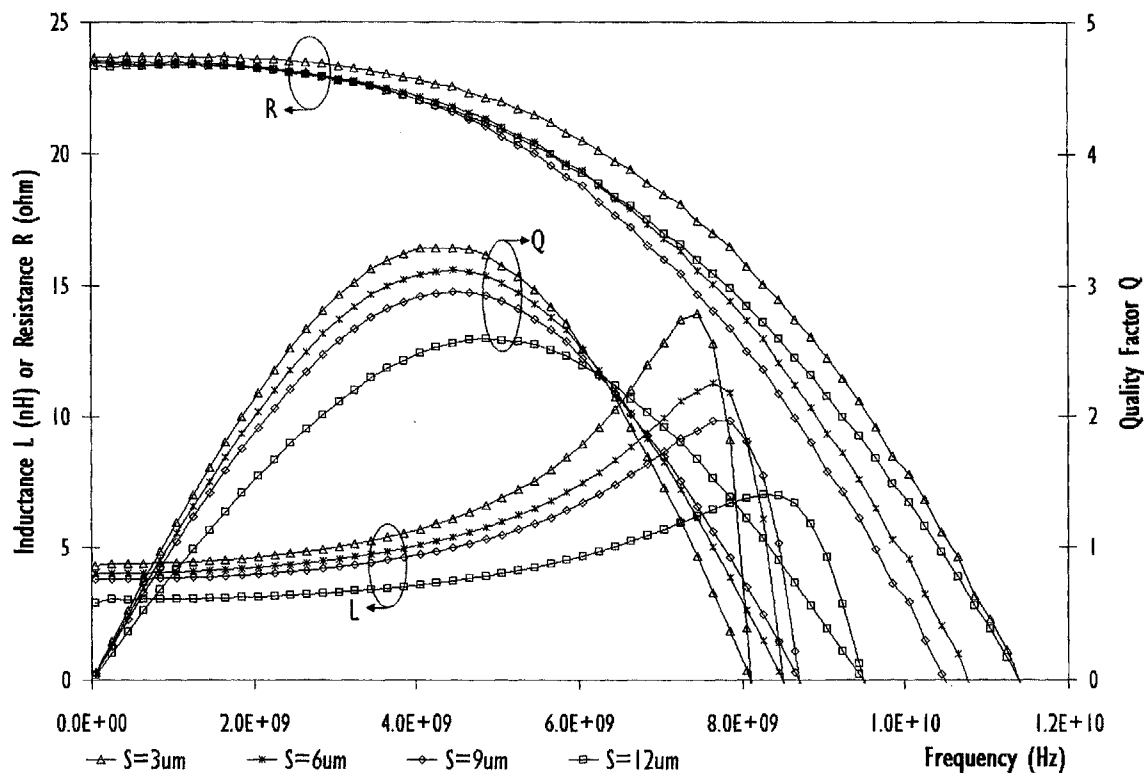


Figure 3.12 - Inductance, Q-factor and series resistance versus frequency for inductors with identical conductor length ($2000 \mu\text{m}$), width ($1.5 \mu\text{m}$) and core diameters ($100 \mu\text{m}$) but different spacing.

Such phenomenon is due to localized proximity effect whereby eddy currents are generated within the metal trace because of nearby current-carrying metal trace. Inductor with the smallest spacing possesses the largest inductance and high frequency series resistance, while the opposite is true for inductor with the largest spacing. Because Q-factor is determined by the resultant inductive and resistive behavior of the inductors, counter-compensations between inductance and series resistance are observed and as a result, the Q-factor performances for all four inductors are almost identical. Similar observations are also noted for the set of inductors with conductor width of $16 \mu\text{m}$ as shown in Figure 3.11. For the case of inductors with conductor width of $1.5 \mu\text{m}$, the influence of constructive mutual coupling under smaller spacing has huge impact on the overall inductance value of the inductor. Figure 3.12 compares and shows that with a smaller spacing, inductance per unit area occupy by the inductor is very much superior compared to inductors with large conductor to conductor spacing. Therefore, for the 0.18

μm RFCMOS technology, inductor with the smallest spacing is generally favored since it offers the highest inductance value and also occupies the least area.

3.4 Effects of Metal Conductor Width

Typical inductor device libraries offered by silicon foundries contain only inductors designed using different number of turns with fixed conductor width, spacing and core diameter. For such approach, using a fixed width and core diameter of 12 and 75 μm respectively, for example, to design inductors with different turns, one would observe that only 4-turn and 5-turn inductors (3 and 4.5 nH) have large Q-factors at the operating frequency of 2.5 GHz as shown in Figure 3.13. This is so because their peak Q-factor frequency is close to 2.5 GHz. As sizes of the inductors and their inductance values increase, their resonant frequency and peak Q-factor frequency start to decrease. Although inductance coverage for the device library is provided in this typical approach, only a few inductors will perform well at a particular frequency of interest. Similar situation, as shown in Figure 2.9, has also been observed for spiral inductors fabricated using the SOI CMOS technology.

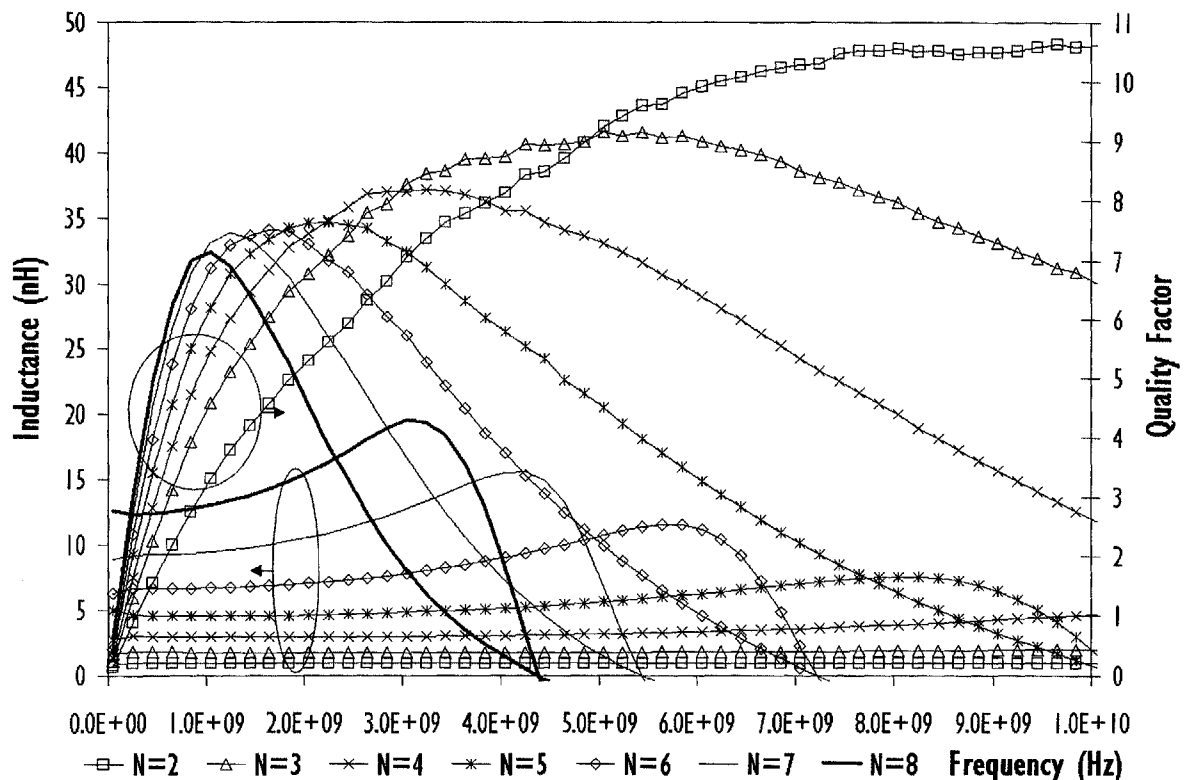


Figure 3.13 - Inductance and Q-factor versus frequency for 1-8 turns inductors with width and core diameter of 12 and 75 μm respectively.

When the inductor's width is studied in an experiment with four 8-turn spiral inductors having fixed 75 μm core diameter and 1.5 μm spacing but with different conductor widths of 6, 8, 12 and 16 μm , these four spiral inductors have very different inductance values even at low frequencies, with 16 μm width inductor having the largest inductance value, as shown in Figure 3.14. However, an interesting point to highlight is that total conductor lengths for the 4 inductors with widths of 6, 8, 12 and 16 μm are 3699, 4160, 5082 and 6005 μm respectively and their normalized unit length low frequency inductance values are actually 2.73, 2.58, 2.40 and 2.24 $\text{pH}/\mu\text{m}$ correspondingly. These observations show that as width decreases, the unit length inductance value increases. To investigate the effect of conductor width, one has to pay special attention to the unit length inductance so that inductors of different conductor width can be designed to have same inductance values and unbiased experimental comparisons can be facilitated. Hence, these results imply that the researchers in Section 2.1.4.4 [29] were likely to have qualified the performance of their proposed layout-optimized inductor in experiments that must have compared varying width and fixed width inductors having different inductance values.

The results from Figures 3.13 and 3.14 reveal that conventional design approach cannot generate high-Q inductors across a wide range of inductance values and hence circuit designers are left with few alternatives to enhance the performance and robustness of their circuits. Such scenarios are usually encountered because the conductor width, which determines the per-unit-length inductance, resistive loss as well as capacitive substrate loss of the inductor, has not been optimized for that particular application frequency. Understanding the implications of using different conductor widths will allow RF device modeling engineers to align the peak Q-factor frequency to the operating frequency of the circuit, achieving maximum performance for every inductor that is being used in RFIC designs.

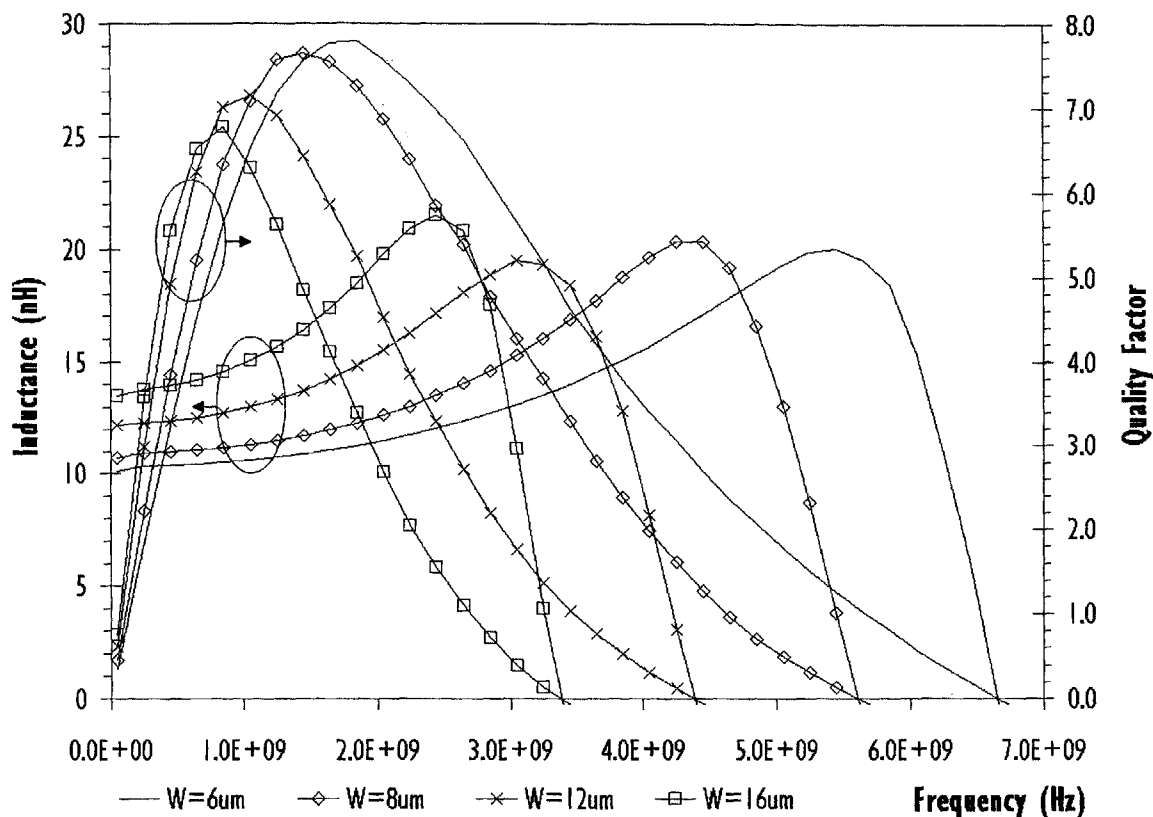


Figure 3.14 - Inductance and Q-factor versus frequency for 8-turn inductors with core diameter and spacing of 75 and 1.5 μm respectively for widths of 6, 8, 12 and 16 μm .

In this sub-section, the peak Q-factor of inductors will be aligned to the operating frequency of the circuit through a design methodology summarized in the flowchart shown in Figure 3.15. An array of inductors with different widths (2, 4, 8, 12, 16 and 24 μm) and total conductor lengths (750, 1000, 1500, 2000, 2500 and 3000 μm) are designed with fixed spacing and diameter of 1.5 and 100 μm correspondingly. The same 0.18 μm RFCMOS process is used to fabricate these inductors and they are then measured using on-wafer RF characterization procedure described in Section 3.1. Figure 3.16 consolidates the low frequency inductance versus total conductor length plot and reveals that the unit length inductance increases when the conductor width is reduced. To investigate the effect of conductor width on the performance of inductors, Figure 3.16 is utilized for interpolation of total conductor lengths such that spiral inductors with different widths will have the same inductance values. As an example, when a 1.5 nH line is drawn in the inductance versus conductor length plot, four total conductor lengths for individual widths of 4, 8, 16 and 24 μm are obtained. The interpolated total conductor lengths allows

four separate inductors to be redesigned and fabricated such that they will have the same inductance values to study and understand the impact of the conductor width.

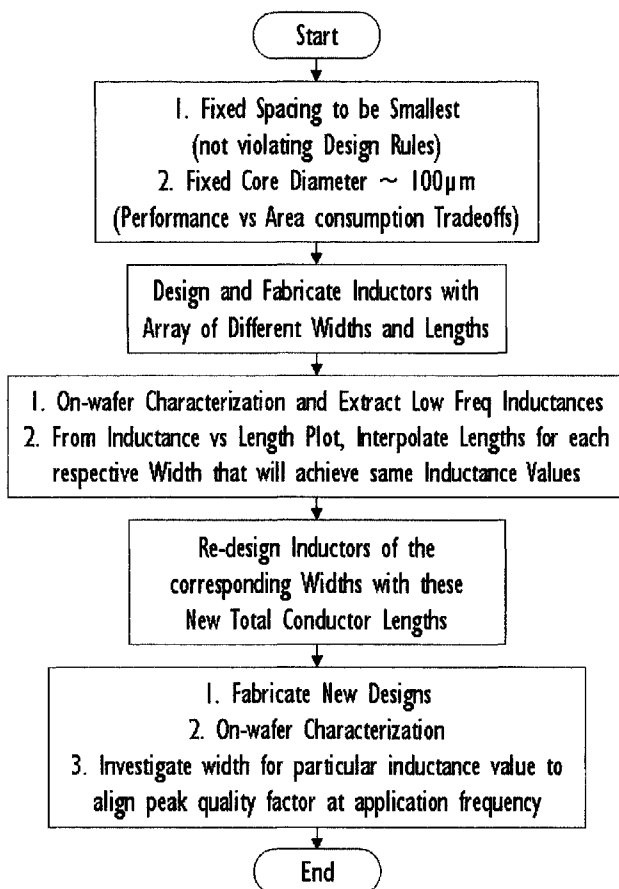


Figure 3.15 - Flow chart summarizing the design methodology for optimizing the physical dimensions of spiral inductors.

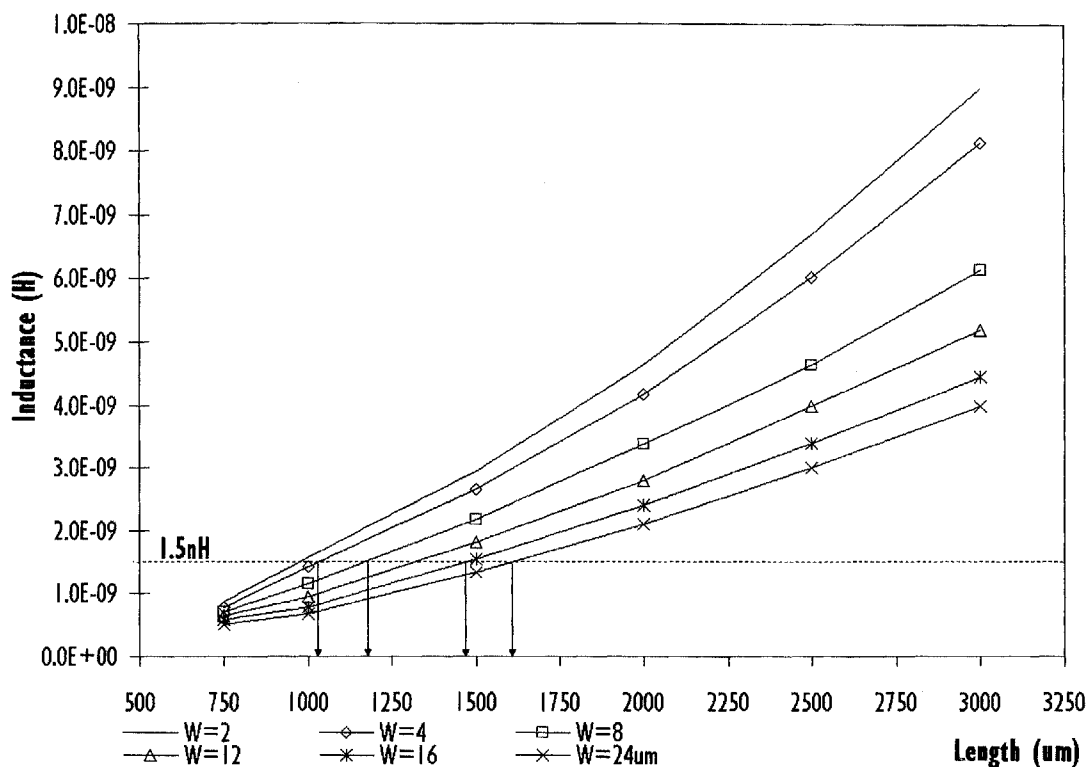


Figure 3.16 - Inductance at low frequency versus total conductor length for inductors with identical diameter of 100 μm but different widths of 2, 4, 8, 12, 16 and 24 μm .

Figure 3.17 shows die photos of these four inductors with different conductor widths and Figure 3.18 compares their inductance and Q-factor plots. The measured results reveal that at 2.5 GHz, inductances (1.6 nH) for all four inductors are very similar and the Q-factor improves by more than 84 % as the conductor width increases from 4 to 16 μm . Although the inductor with metallization width of 24 μm has a peak Q-factor frequency closer to 2.5 GHz, its Q-factor is only 5.4 % more superior and requires an additional 60 % more silicon area as compared to the inductor with 16 μm width conductor. From these results, two observations are made, the peak Q-factor frequencies of inductors can indeed be adjusted desirably through the proposed optimization technique described in Figure 3.15. The Q-factor versus area consumption trade-off is an important finding to convey to the industry since it will affect both the final performance as well as the die size of silicon-based RFICs.

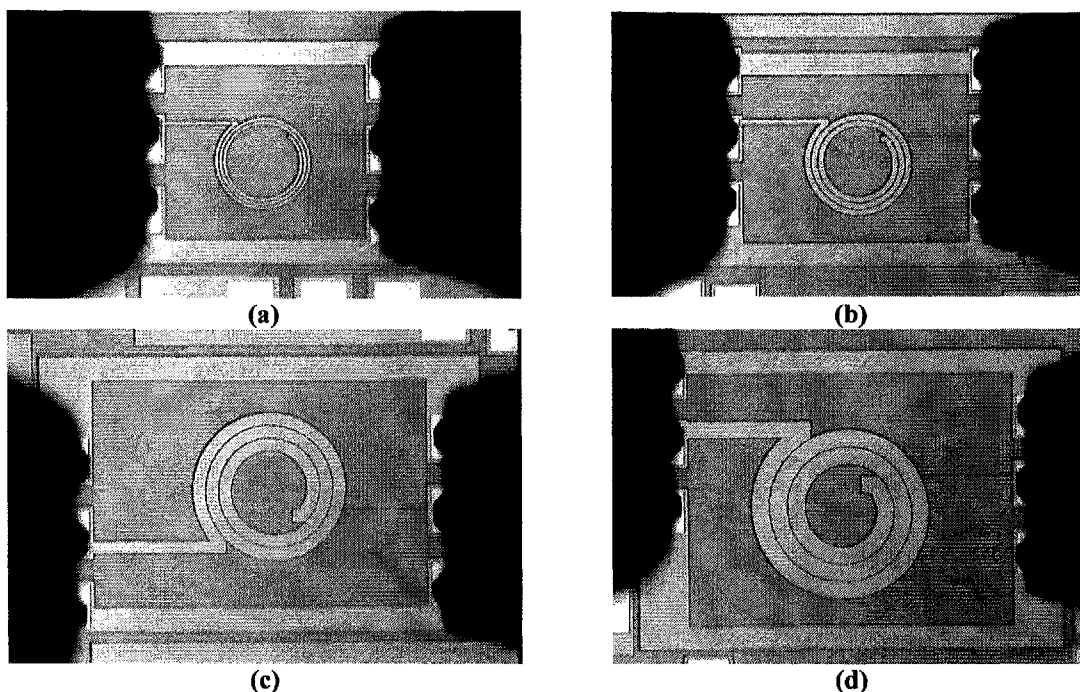


Figure 3.17 - Die photos of 1.6 nH spiral inductors with identical core diameter (100 μm) but different widths of 4 μm (a), 8 μm (b), 16 μm (c) and 24 μm (d).

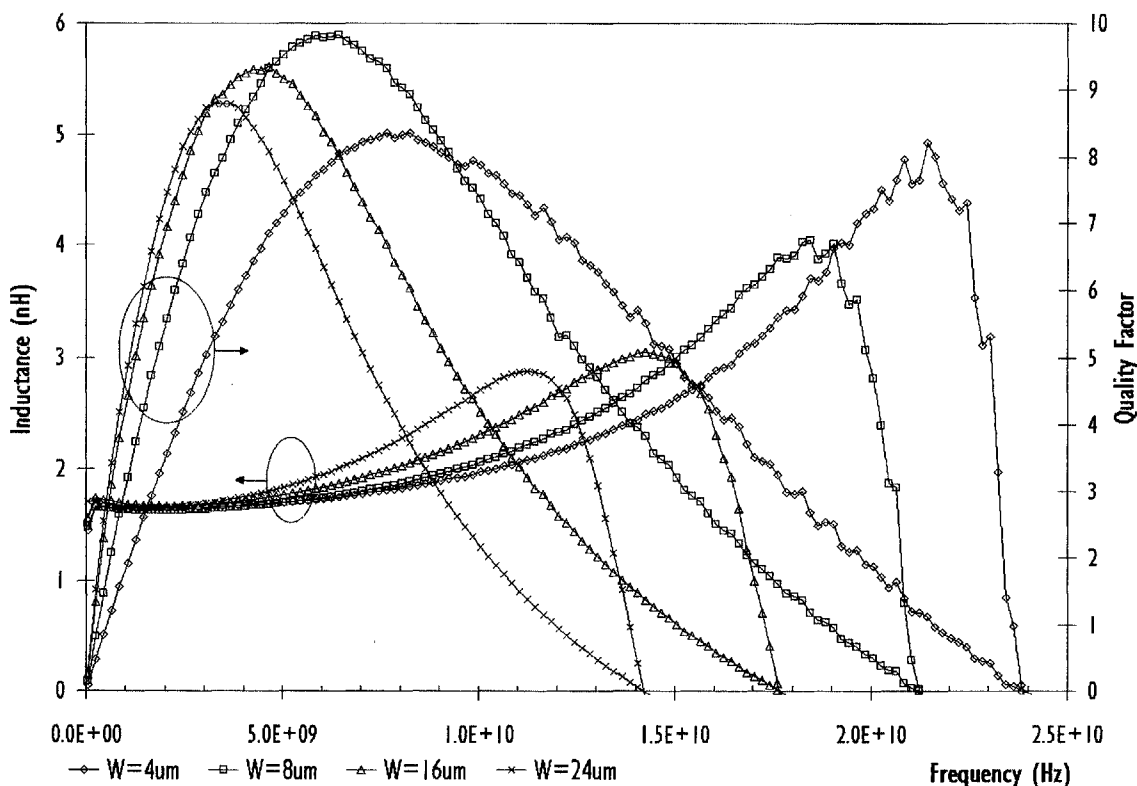


Figure 3.18 - Inductance and Q-factor versus frequency for inductors with identical inductance (1.6 nH) and core diameter (100 μm) but different widths.

This experiment is repeated to investigate 2.8 nH inductors as illustrated in Figure 3.19. At 2.5 GHz, all 4 inductors have equivalent inductance values and comparison of the Q-

factor plots reveal that the conductor width of 16 μm is more suitable for 2.5 GHz applications since it has a relatively larger Q-factor compared to width 4 and 8 μm spiral inductors. Although peak Q-factor frequency for the inductor with 24 μm width is at 2.5 GHz, trading-off a larger silicon area of more than 61 % only results in a Q-factor improvement of about 8.5 %. Figure 3.20 and Figure 3.21 consolidate the inductance and Q-factor plots for sets of 4.4 nH and 6.2 nH inductors respectively. Both plots show that at 2.5 GHz, the inductance values are all very close for the respective sets of four inductors and the most suitable width to design inductors with this range of inductance values, is about 8 μm after considering the trade-offs in Q-factor, peak Q-factor frequency response as well as the size of the inductors. For larger inductances such as the set of 8.2 nH spiral inductors depicted in Figure 3.22, inductors with 4 and 8 μm conductor width both perform well. However, if a conductor width of 6 μm is to be used, it would likely be the optimal value, generating an inductor with its peak Q-factor at 2.5 GHz.

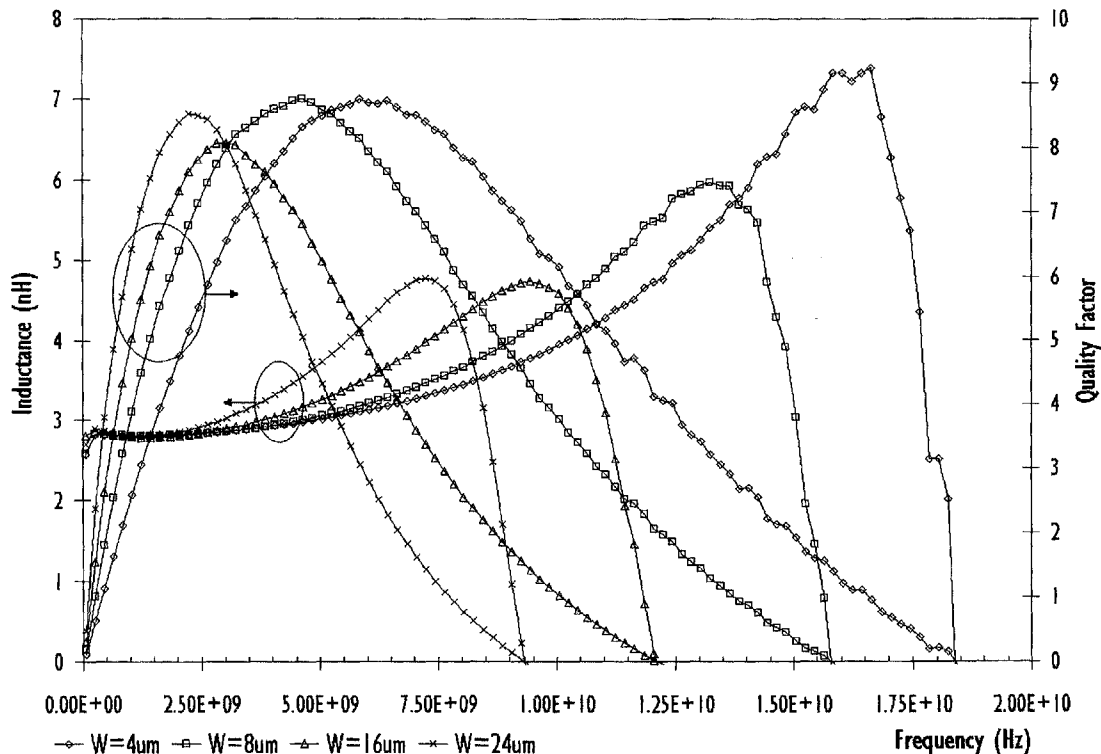


Figure 3.19 - Inductance and Q-factor versus frequency for inductors with identical inductance (2.8 nH) and core diameter (100 μm) but different widths.

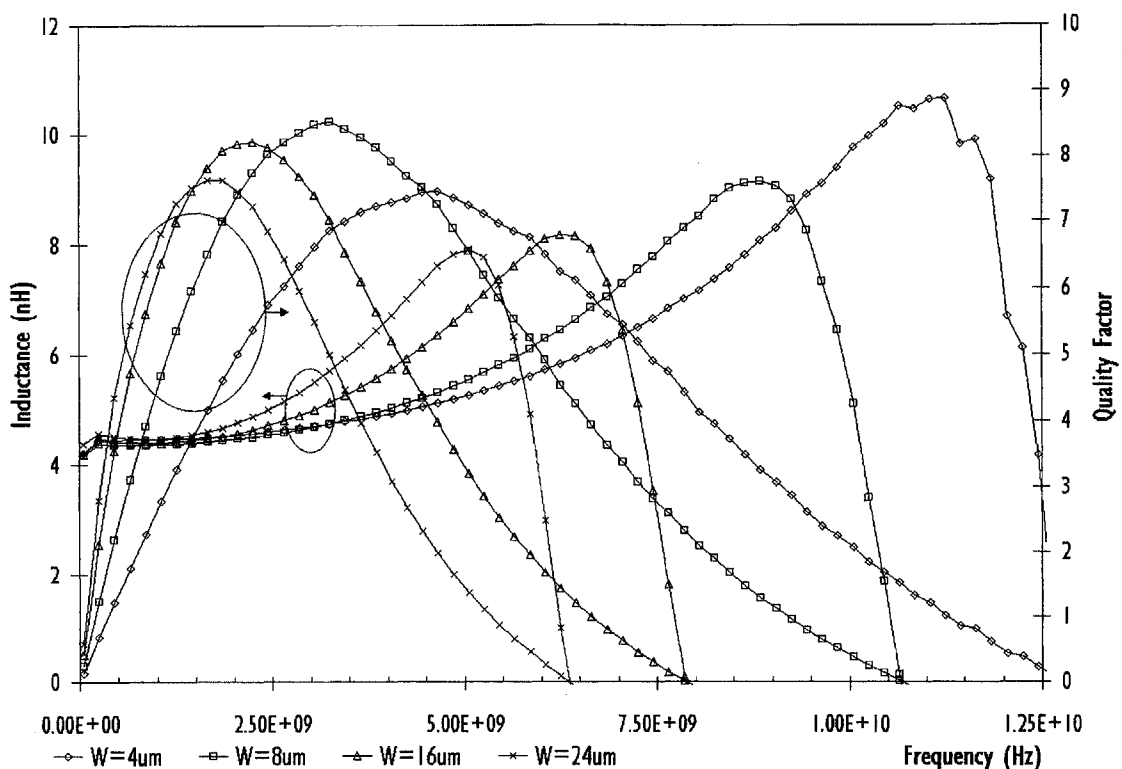


Figure 3.20 - Inductance and Q-factor versus frequency for inductors with identical inductance (4.4 nH) and core diameter (100 μm) but different widths.

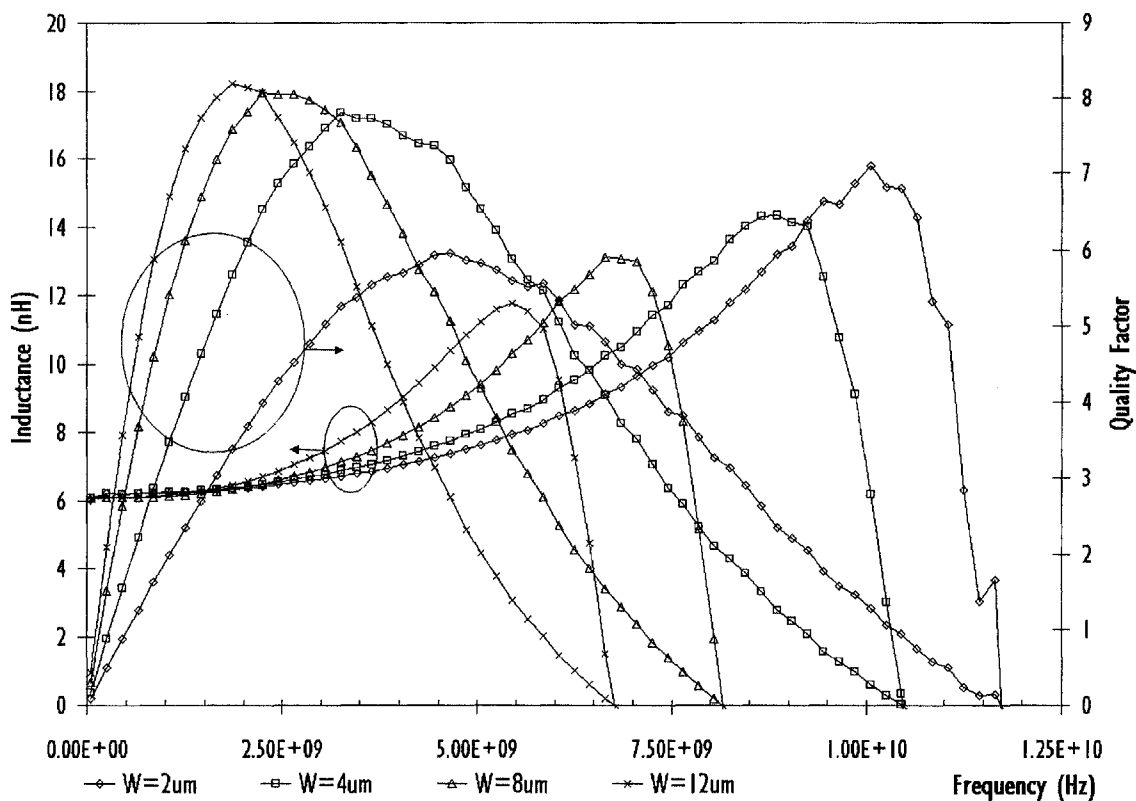


Figure 3.21 - Inductance and Q-factor versus frequency for inductors with identical inductance (6.2 nH) and core diameter (100 μm) but different widths.

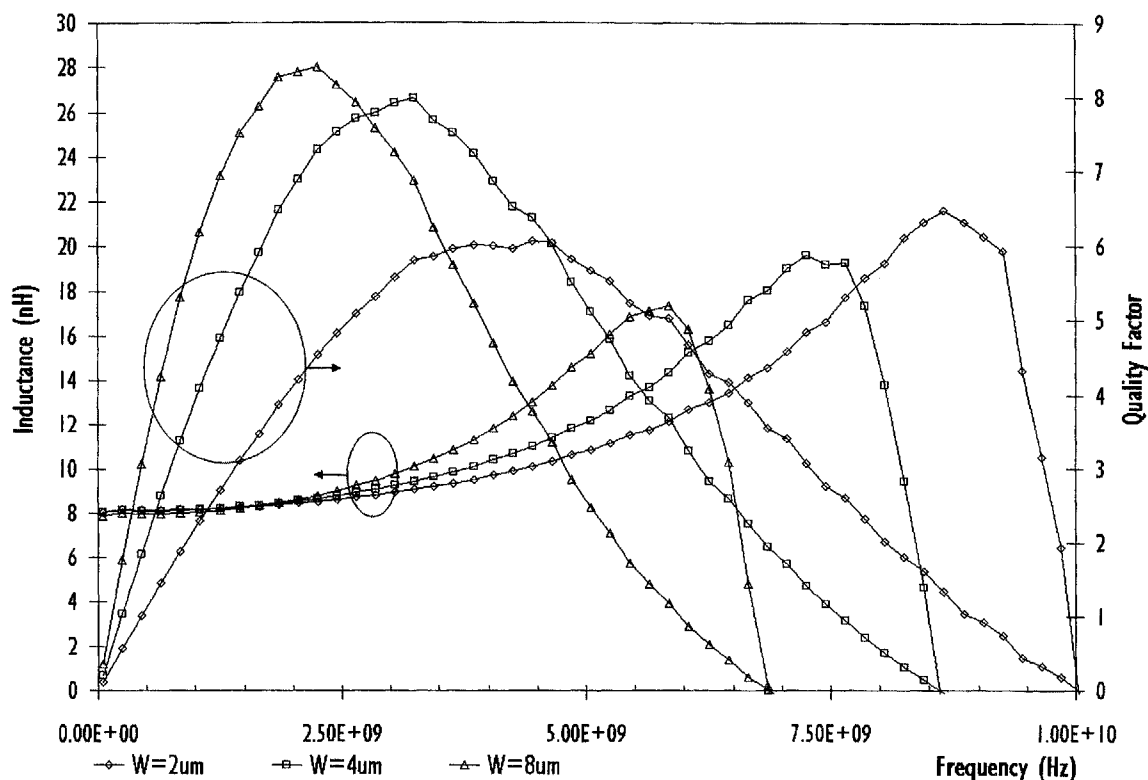


Figure 3.22 - Inductance and Q-factor versus frequency for inductors with identical inductance (8.2 nH) and core diameter (100 μm) but different widths.

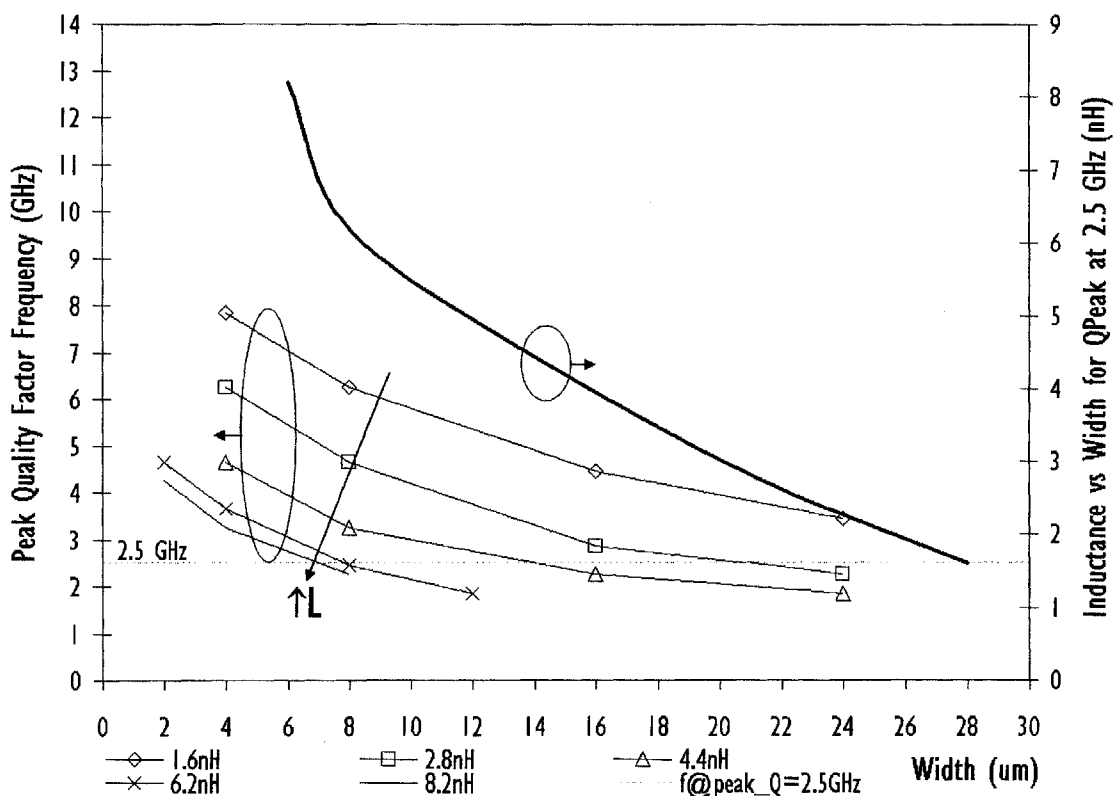


Figure 3.23(a) - Q-factor performance versus width for inductors with identical inductances and inductance versus width for inductors with Q_{peak} at 2.5 GHz.

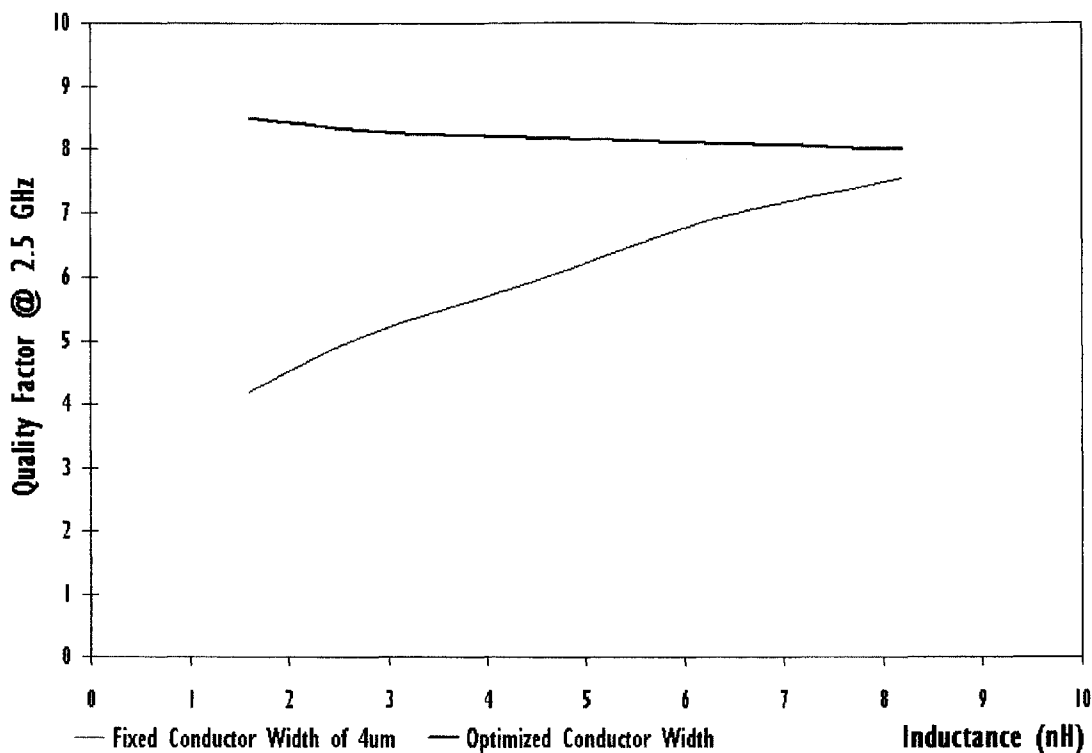


Figure 3.23(b) - Q-factor versus inductance for sets of inductors with optimized conductor width and fixed conductor width of 4 μm at 2.5 GHz.

The experimental results in this sub-section conclude that conductor width is a very important design parameter since it affects the unit length inductance value, resistive loss as well as the peak Q-factor frequency of spiral inductors. When the optimal conductor width is employed, the peak Q-factor frequency can be aligned to the circuit operating frequency and the spiral inductor's Q-factor will be desirably large. Figure 3.23(a) summarizes the correlations between Q-factor at 2.5 GHz as well as peak Q-factor frequency for different inductance values and sizes of conductor width. This plot reveals that in order to maintain the peak Q-factor frequency at 2.5 GHz, when the inductance increases, the conductor width has to be reduced to minimize the substrate loss which is more dominant than its resistive loss for large inductors. Thus, having smaller width for large inductor improves its performance and at the same time, reduces the silicon area it requires. Small inductors, on the other hand, should be designed with large conductor width since their relatively short total conductor length do not constitute to large capacitive substrate loss. Having a large conductor width, resistive loss will be reduced

drastically, achieving significant improvement in the Q-factor for small inductors. Figure 3.23(b) compares Q-factor of inductors having optimal conductor width and those with fixed width of 4 μm over the inductance range of 1.6 to 8.2 nH at 2.5 GHz. It has been demonstrated that with the optimization of inductor's width, high Q-factor can be maintained for a specific range of inductance values at the frequency of interest. Using fixed conductor width would only result in inductors having high Q-factor at certain inductance values. As shown in Figure 3.23(b), the width of 4 μm only benefits inductors with large inductance values.

Empirical formulae which provide very accurate fit to the experimental data in Figure 3.16 and Figure 3.23(a) are developed to allow ease of designing inductors with their peak Q-factor at 2.5 GHz in the 0.18 μm RFCMOS process. These formulae are shown in Equations 3.4 and 3.5 with the boundary conditions of $0.5 \leq \text{IND} \leq 9.0$ nH and $2 \leq W \leq 28$ μm , where IND and W denote the inductance and conductor width respectively. To utilize these empirical functions, for a certain required inductance value, the optimal width, W can first be evaluated using Equation 3.4.

$$W (\mu\text{m}) = 4.5445\text{E-}01 \times \text{IND}^2 - 7.8138 \times \text{IND} + 39.386 \quad (3.4)$$

$$\begin{aligned} \text{Length } (\mu\text{m}) = & 809.624 + 282.245 \times \ln(\text{IND}) - 3.640 \times W + \\ & 159.161 \times (\ln(\text{IND}))^2 + 2.653 \times W^2 + 46.717 \times \ln(\text{IND}) \times W + \\ & 52.908 \times (\ln(\text{IND}))^3 - 0.07404 \times W^3 - 1.0283 \times \ln(\text{IND}) \times W^2 + \\ & 4.562 \times (\ln(\text{IND}))^2 \times W \end{aligned} \quad (3.5)$$

Based on the optimal width derived from Equation 3.4 and the required inductance, Equation 3.5 (developed from Figure 3.16) can then be used to determine the required total conductor length for the optimized inductor. These two geometrical parameters together with core diameter of 100 μm and spacing of 1.5 μm allow optimized inductors to be easily generated for use in 0.18 μm RFCMOS circuits operating at 2.5 GHz.

3.5 Giga-Hertz Amplifier using Optimized Integrated Inductors

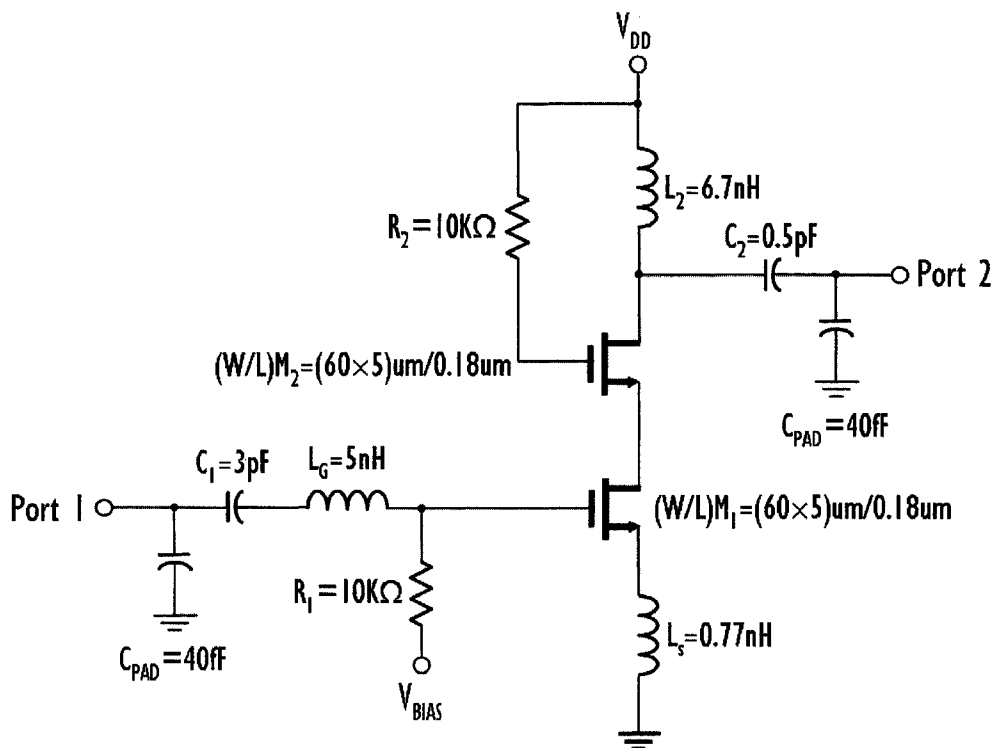


Figure 3.24 - Circuit schematic of a simple giga-hertz amplifier utilized to demonstrate performance enhancements when optimized inductors are used in RFICs design.

The proposed methodology for optimizing spiral inductors is evaluated using a giga-hertz amplifier. Figure 3.24 shows the circuit schematic of the giga-hertz amplifier utilized to demonstrate circuit performance enhancements when optimized spiral inductors are used in RFIC designs as compared to using non-optimized inductors. The amplifier is designed to operate at 2.4 GHz with an expected gain of about 14 dB. Cascode architecture is used for the amplifier design since this configuration provided better gain and input-to-output isolation characteristics. The classical inductive source degeneration input matching technique has been adopted for the input stage of the amplifier. For the gate-to-source capacitance of the input transistor M_1 , L_G , L_S and C_1 provide narrow band impedance matching of the input port to the external 50 ohm system at 2.4 GHz. V_{BIAS} provides the input biasing to the transistor M_1 and R_1 is used to isolate the RF signal path from the DC biasing path. M_2 is a common gate amplifier used to improve gain for the LNA as well as

the isolation between the input and output ports. R_2 is used to provide a stable DC biasing to the M_2 transistor and at the output stage, L_2 and C_2 are utilized for 50 ohm load matching.

Two device-identical amplifiers were fabricated, one with normal spiral inductors and another with optimized inductors having peak Q-factor at 2.4 GHz. Since the peak Q-factor of the optimized inductors are all aligned at 2.4 GHz, they generally have Q-factors at least 50 % higher than the non-optimized ones. Die photos showing on-wafer circuit measurements of the amplifiers with non-optimized and optimized inductors are shown in Figure 3.25(a) and (b) respectively. The pad capacitances have been taken into consideration during circuit simulations, as such, no pad parasitic de-embedding is required for the circuit measurements. A typical die to perform the on-wafer circuit characterization is selected based on full wafer map device characteristics obtained from RF scribeline process monitoring test structures that have been developed in the course of this research work [57]. In measuring the two-port response of the giga-hertz amplifiers, over-driving the nMOSFETs into saturation is avoided by having a low source power setting of about -20 dBm on the vector network analyzer.

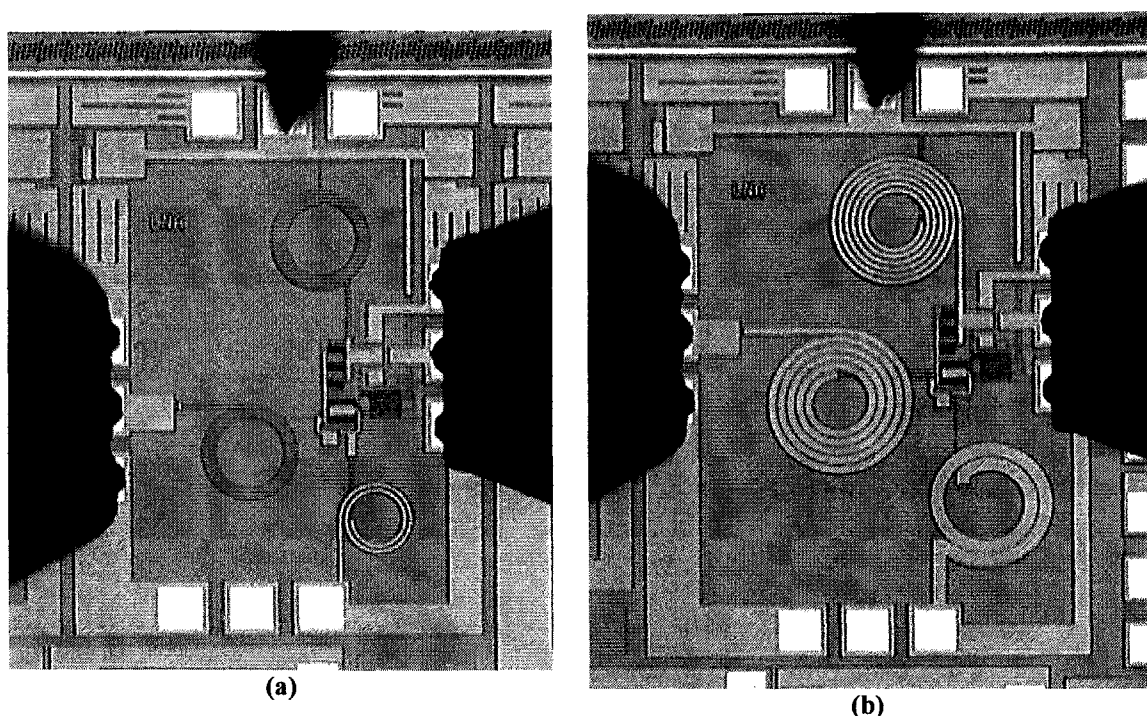


Figure 3.25 - Die photos showing on-wafer RF S-parameters and high frequency noise characterization of amplifiers with non-optimized inductors (a) and optimized inductors (b).

Figure 3.26 compares the 2-port S-parameters and high frequency noise behavior of the two amplifiers. Designs of the inductors are different for the two amplifiers, but measured circuit results reveal that both amplifiers operate at 2.4 GHz, allowing meaningful comparisons of circuit performances to be made. As opposed to using non-optimized spiral inductors, optimized inductors offer a 2.56 dB gain improvement at 2.4 GHz. Although a larger amplifier die size of 28.6 % is required, employing optimized inductors not only enhance the amplifier's gain and its narrowband input/output matching characteristics, but also allow the amplifier to operate with a much lower noise figure of about 2.5 dB instead of 3.0 dB at 2.4 GHz due to larger inductor Q-factor [58]. These circuit improvements are made possible because all loss mechanisms that would degrade the Q-factor of inductors have been carefully considered and kept minimal at 2.4 GHz. Through this circuit-level verification, the proposed methodology for optimizing the physical design parameters of spiral inductors is shown to be reliable, enhancing the circuit performance of silicon-based RFICs.

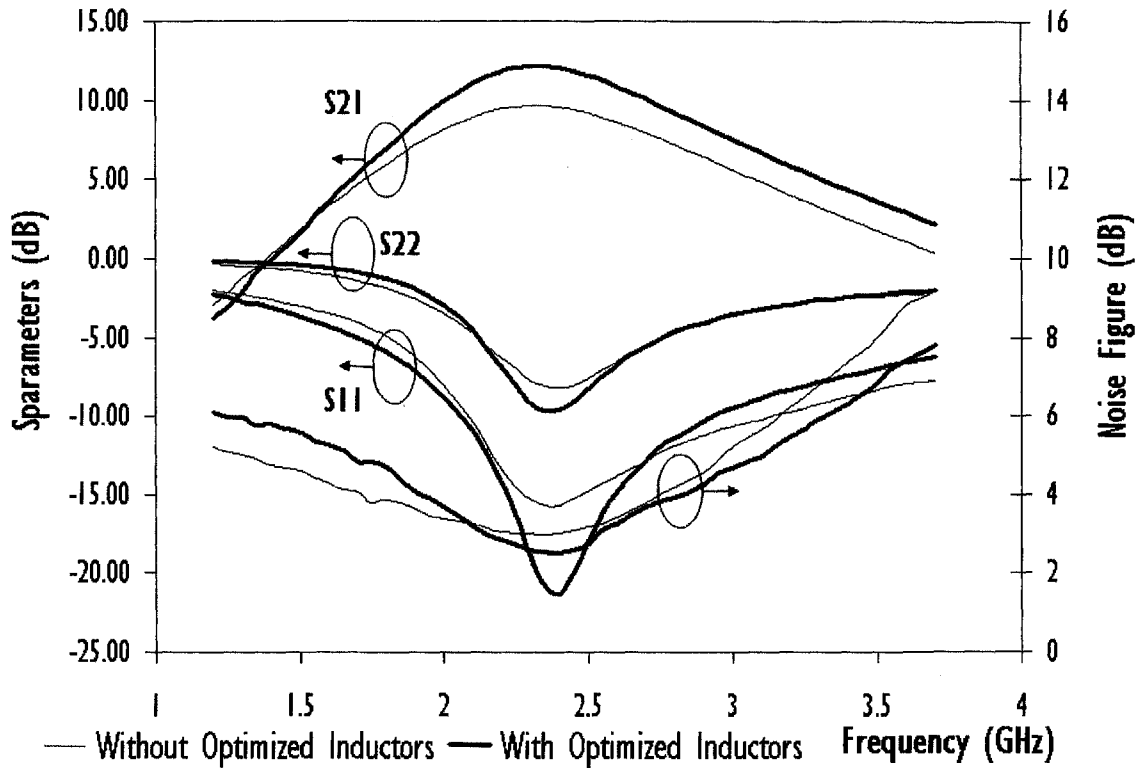


Figure 3.26 - Measured 2-port S-parameters and noise figure of amplifiers with and without optimized spiral inductors.

3.6 Comparing Research Works on Inductor Layout Optimization

For benchmarking purposes, a number of research papers are consolidated in Table 3.1 to evaluate the research contributions for this work. In contrast to other research studies, an overwhelming number of test structures were designed over 3 separate rounds of testchip fabrications so that a reliable and robust methodology can be developed to optimize the layout of spiral inductors. Unbiased experiments with spiral inductors having identical inductances at the frequency of interests help in the systematic understanding of how to optimize the core diameter and spacing for the spiral inductors. Although the proposed methodology to overcome the challenge of maintaining similar inductances for inductors with different widths seems straightforward, it is ground-breaking and novel, earning this work publication acceptance for IEEE Transactions on Electron Device.

Some research works did not have published inductance characteristics to make sure that inductors of different physical layouts have identical inductances at the same frequency to make reliable performance evaluations. One such example is the varying width inductor design [29] which drew conclusions based on the Q-factor values observed. Most researchers who adopts SPICE models for layout optimizations fail to ensure that the models they are using are highly accurate and scalable, capable of predicting the behaviors of the inductors when their physical design parameters such as core diameter, width and spacing are varied accordingly [30], [32]-[34]. These research studies also committed the error of not comparing inductors with identical inductance, simply defining the width or diameter values that would achieve the highest Q-factor. This is true only for a few particular inductance values and frequency of interest as shown in Figure 3.13. In contrast, for real circuit applications, RFIC designers actually require inductors over a wide range of inductance values to have high Q-factor.

Last but not least, as opposed to all other publications highlighted, this is the only study which has conducted circuit verifications for the layout optimization methodology, with both giga-hertz amplifiers having the same peak gain frequency of 2.4 GHz when evaluating the impact of the layout optimized inductors.

Table 3.1 - Comparing various research works on layout optimization for spiral inductors.

Author	Lopez-Villegas J.M.	X. Z. Xiong	J. E. Post	T. Wang	Y. Zhan	M. D. Rosales	This Work
Reference	[29]	[32]	[30]	[33]	[34]	[59]	
Journal/Conference	IEEE TMTT	IEEE Conf.	IEEE T Cir & Sys	IEEE Conf.	IEEE Conf.	IEEE Conf.	IEEE TED
Year of Publication	2000	2000	2000	2003	2004	2005	2005
Number of test structures used for developing layout optimization methodology.	4	3	5	4	4	4	101 (Total number of Inductors designed and tested after 3 separate rounds of test chips fabrication)
Is the optimization methodology published?	Optimization based on varying the width of the inductor	Yes	Yes (Optimization based on inductor's width) (For 5 nH @ 2.5 GHz, optimal width is 22 μm)	Yes	Yes	Optimize inductor outer diameter; investigate the effect of pattern ground shield, stacked metal and Octagonal versus square inductor	Yes (In Section 3.2 – 3.4, diameter, spacing and width are optimized systematically ensuring unbiased comparison with identical inductance values) (For 5 nH @ 2.5 GHz, optimal width is 10 μm)
Did the experiments compare inductors of different physical layouts having identical inductance values at frequency of interests?	No (The inductance versus frequency plots are not published)	No	No (The inductance versus frequency plots are not published)	No	No	No (The inductance versus frequency plots are not published)	Yes (Throughout Chapter 3, it compares inductors with identical inductance values up to 2.4 GHz)
What is the operating frequency supported by the methodology?	Unknown since no inductance plots were published	Unknown	2 GHz	Unknown	Unknown	Unknown (Measurement up to 6 GHz)	2.4 GHz (Without an accurate and scalable model, this methodology can only support up to 2.4 GHz. Chapter 4 develops a scalable model which support layout optimization up to 10 GHz)
If SPICE models are used in performing layout optimization, are there verifications studies on the scalability and accuracy of the model?	No SPICE models used	No (Nine Element lumped model is used [31], accuracy and scalability not verified)	No (Nine Element lumped model is used [31], accuracy and scalability not verified)	No (Nine Element lumped model is used [31], accuracy and scalability not verified)	No (Six Element lumped model is used, accuracy and scalability not verified)	No SPICE models used	Yes for work in Chapter 4 (In Chapter 4, a scalable inductor SPICE model has been used. Its accuracy and continuity has been scrutinized. The optimization studies are performed to make sure that)
Has the design optimization methodology been verified with test circuits and results published?	No	No	No	No	No	No	Yes (2 Amplifiers were used. Despite different designs for the inductors, the amplifiers both operate at the same centre frequencies)

3.7 Design Optimization Methodology for Copper Spiral Inductors

In the previous sections, physical designs for spiral inductors constructed using the 0.18 μm RFCMOS aluminum interconnects have been successfully optimized and its benefits demonstrated with huge improvements in circuit performance observed when using such optimized inductors. This section will focus on qualifying the validity of the proposed optimization methodology for spiral inductors fabricated using the 0.13 μm RFCMOS technology with copper backend interconnects. Essentially, all the spiral inductors designed for experiments in Section 3.2 to 3.5 were sent for fabrication using the copper backend technology. These inductors were then characterized by the same procedure outlined in Section 3.1 and the results presented and discussed in this section. The key differences between the 0.18 μm and 0.13 μm RFCMOS technologies are the materials selected for metallization and inter-metal dielectrics as well as thickness of the topmost metal layer and these have been presented and compared in Figure 2.21 of Section 2.2.2.

3.7.1 Effects of Core Diameter

Figure 3.27 and 3.28 evaluate the performance of copper spiral inductors designed with different core diameter values from 10 to 150 μm but fixed width (8 μm), spacing (1.5 μm) and total conductor lengths of 1000 and 3500 μm respectively. To guarantee fair device comparisons, the two sets of inductors correspondingly must have the same measured low frequency inductance and series resistance values as observed in the 2 plots. It has also been noted that using much thicker (3 μm) copper metallization with a lower resistivity of 17 $\text{n}\Omega\text{m}$ significantly improves Q-factor of the spiral inductors by more than 50 % when compared to their aluminum (2 μm thick, resistivity of 28 $\text{n}\Omega\text{m}$) counterparts in Figures 3.3 and 3.5. Also, the copper inductors' self-resonant frequencies are higher by about 2 GHz when comparing inductors in Figure 3.5 and Figure 3.28. This is attributed to the fact that fluorinated silica glass (FSG) oxide used as inter-metal dielectric in the

0.13 μm technology has lower dielectric constant compared to borophosphosilicate glass (BPSG) oxide in the 0.18 μm technology. Nonetheless, like aluminum spiral inductors, copper inductors also require large core diameter of at least 100 μm to suppress the formation of conductor eddy currents which have considerably reduce the Q-factor of spiral inductors.

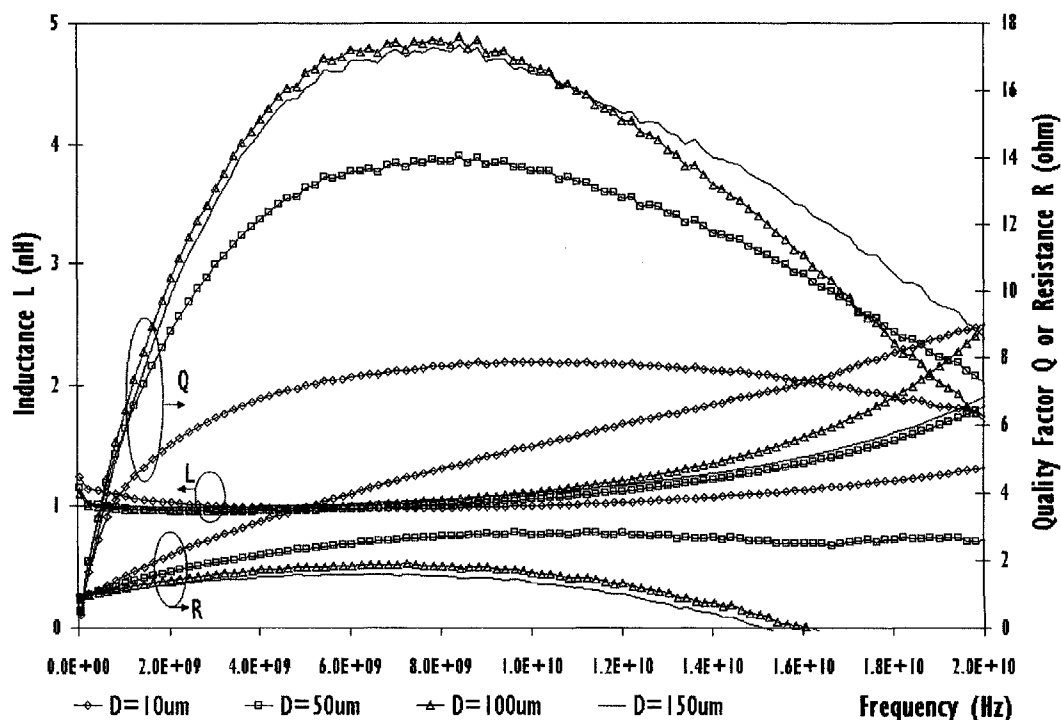


Figure 3.27 - Inductance, Q-factor and series resistance for copper spiral inductors with identical conductor length (1000 μm) and width (8 μm) but different core diameters.

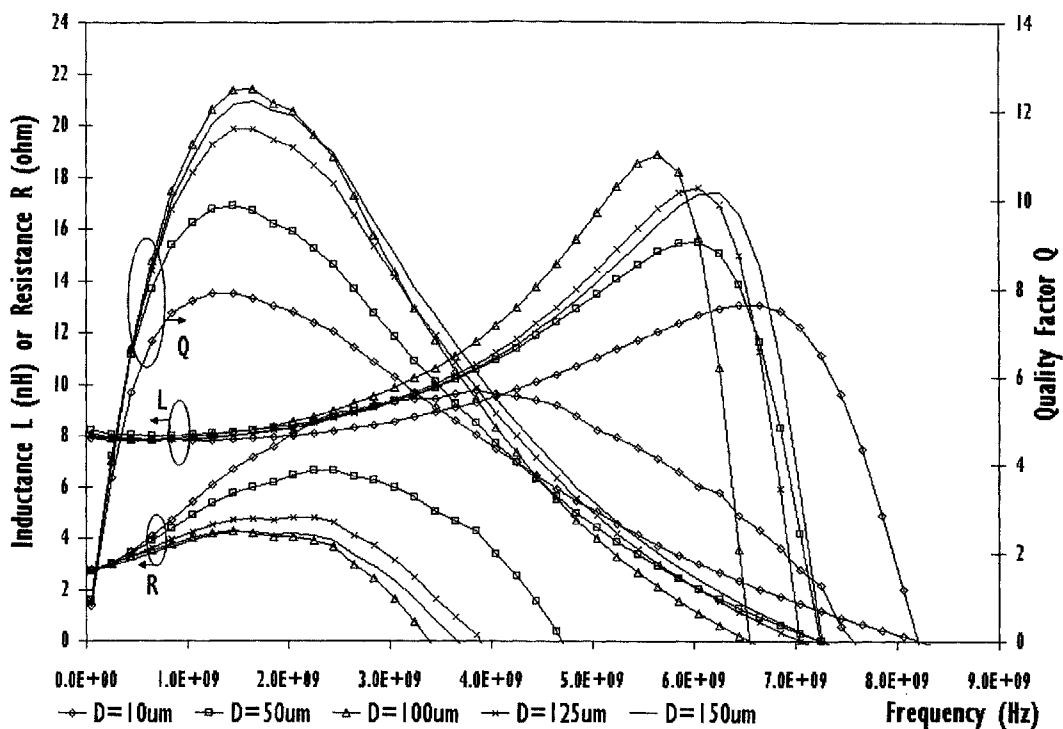


Figure 3.28 - Inductance, Q-factor and series resistance for copper spiral inductors with identical conductor length (3500 μm) and width (8 μm) but different core diameters.

Figure 3.29 and 3.30, on the other hand, investigate the correlations between different core diameters at a fixed total conductor length of 2000 μm for conductor widths of 4 and 16 μm . At 3.5 GHz, when diameter increases from 50 to 150 μm , for the set of inductors with 4 μm conductor width, Q-factor of the inductor improved by 18 %. On the contrary, for set of inductors with conductor width of 16 μm , at 2.8 GHz, increasing the same amount of core diameter results in a phenomenal Q-factor improvement of 60 %. When large conductor width is used, it is indeed a considerable distance between the outer turns and centre core of the inductor, making it more probable for the inductor's magnetic field to pass through the inner turns instead of its hollow core. Therefore, similar to large-width aluminum inductors, such copper spiral inductors should have core diameters much larger than 100 μm to avoid formation of conductor eddy current which lead to significant performance degradations.

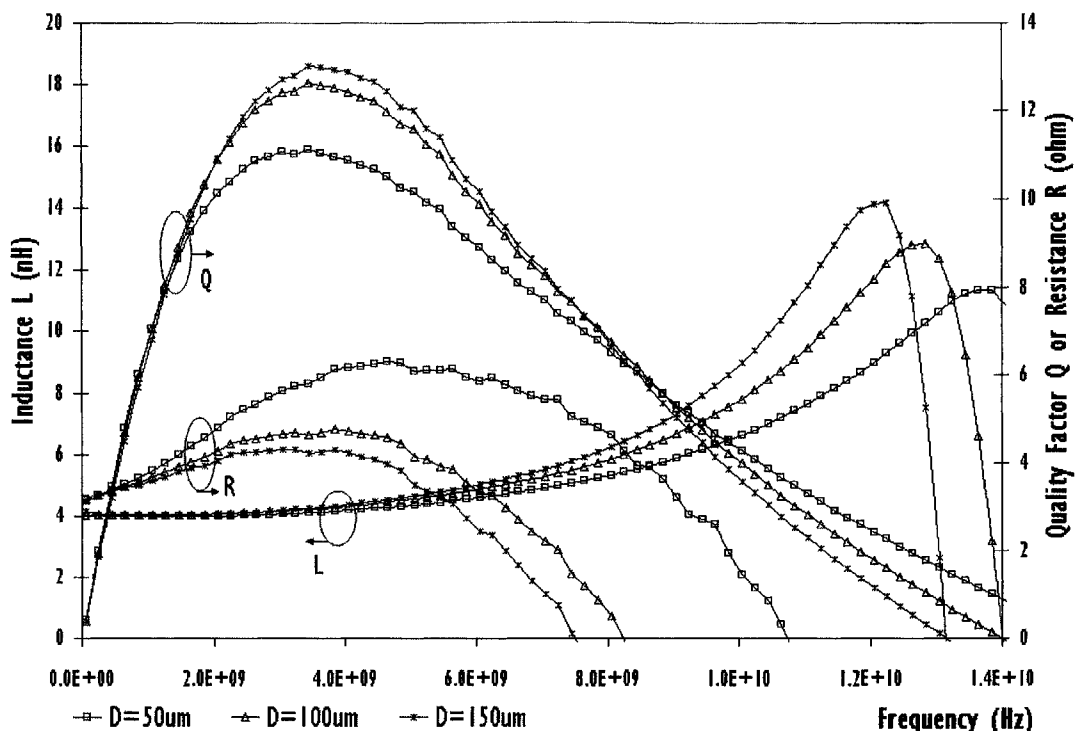


Figure 3.29 - Inductance, Q-factor and series resistance for copper spiral inductors with identical conductor length (2000 μm) and width (4 μm) but different core diameter.

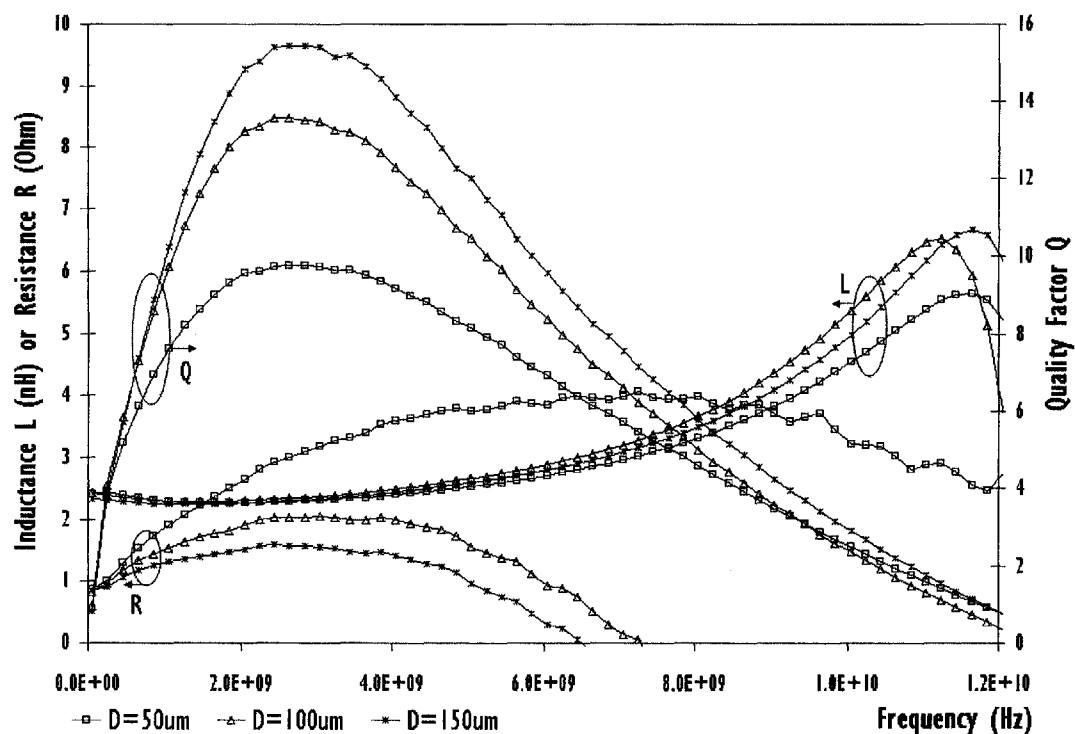


Figure 3.30 - Inductance, Q-factor and series resistance for copper spiral inductors with identical conductor length (2000 μm) and width (16 μm) but different core diameter.

3.7.2 Effects of Metal Conductor Spacing

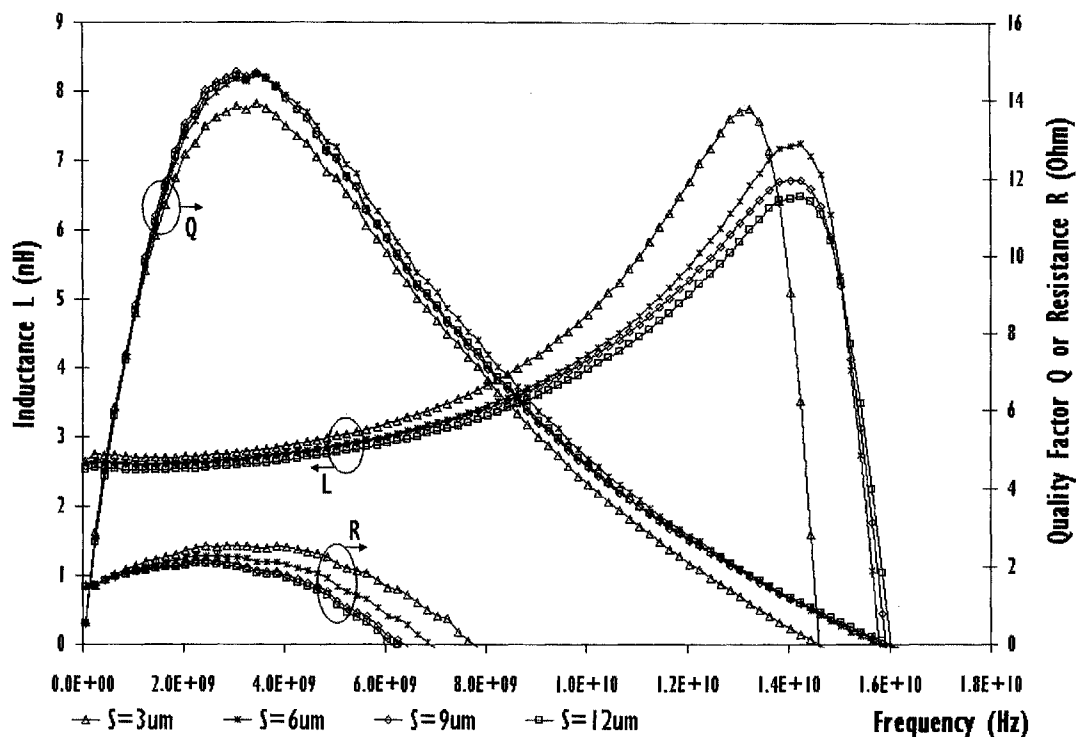


Figure 3.31 - Inductance, Q-factor and series resistance for copper spiral inductors with identical conductor length (2000 μm), width (8 μm) and core diameter (100 μm) but different conductor spacing.

To investigate the impact of metal conductor spacing for copper-based spiral inductors, four inductors with identical conductor length (2000 μm), width (8 μm) and core diameter (100 μm) but different conductor spacing of 3, 6, 9 and 12 μm are fabricated. Figure 3.31 consolidates the inductance, Q-factor and series resistance versus frequency plots for these inductors. The observations made for aluminum-based and copper-based inductors with regards to the effects of conductor spacing are identical and they can be summarized as follows:-

1. As conductor spacing decreases, the inductance values increase due to more mutual inductive coupling between the conductors within the spiral coil.
2. Beyond 2 GHz, inductor with spacing of 3 μm has the largest series resistance and this resistance decreases as the conductor spacing for the inductor increases due to localized conductor eddy current effect.

3. Inductor with the smallest spacing possesses the largest inductance and high frequency series resistance and vice versa.
4. Counter-compensations between inductance and series resistance result in Q-factor performances for all four inductors to be almost the same (For spacing of 3 μm , at the peak Q-factor frequency, Q-factor of the inductor is 7 % smaller).

Therefore, smallest conductor spacing while not violating top metal design rules is preferred in the copper backend interconnect technology, deriving maximum inductance from the available silicon real estate. This finding is in line with the aluminum-based inductors.

3.7.3 Effects of Metal Conductor Width

To verify the design optimization methodology outlined in the flowchart of Figure 3.15, spiral inductors in Section 3.4 are also fabricated in the 0.13 μm RFCMOS technology. In this sub-section, copper-based 1.6, 4.2 and 7.8 nH inductors (counterparts of 1.6, 4.4 and 8.2 nH aluminum-based inductors in Figures 3.18, 3.20 and 3.22 respectively) are consolidated in Figure 3.32, 3.33 and 3.34 correspondingly. These copper-based spiral inductors are noted to have slightly lower inductances values compared to the aluminum-based inductors, especially for inductors with high-inductance values. With aluminum and copper having almost the same permeability ($\mu_{\text{Al}} = 1.2566650 \times 10^{-6}$ H/m and $\mu_{\text{Cu}} = 1.2566290 \times 10^{-6}$ H/m [60]), this observation is likely due to thicker metallization for the two topmost metals in the copper technology. Having thicker metallization suggests larger metal cross-sectional area, thereby reducing both current density and the amount of inductance generated by the spiral coil. Nevertheless, thicker copper top metallization and its low resistivity of 17 n Ωm have significantly reduced the resistive loss, increasing the Q-factor of copper-based inductors by more than 50 % when evaluated against aluminum-based inductors ($\rho_{\text{Al}} = 28$ n Ωm).

Most important of all, from the device performance plots in Figures 3.32, 3.33 and 3.34, the peak Q-factor frequencies for copper-based inductors with different inductance values can also be adjusted desirably through the proposed optimization technique described in Figure 3.15. As an example, for 4.2 nH inductors in Figure 3.33, its peak Q-factor frequency varies from 3.5 to 1.5 GHz when the width increases from 4 to 24 μm . To align the peak Q-factor for these 4.2 nH inductors for a 2.5 GHz application, conductor width of 8 μm can be used.

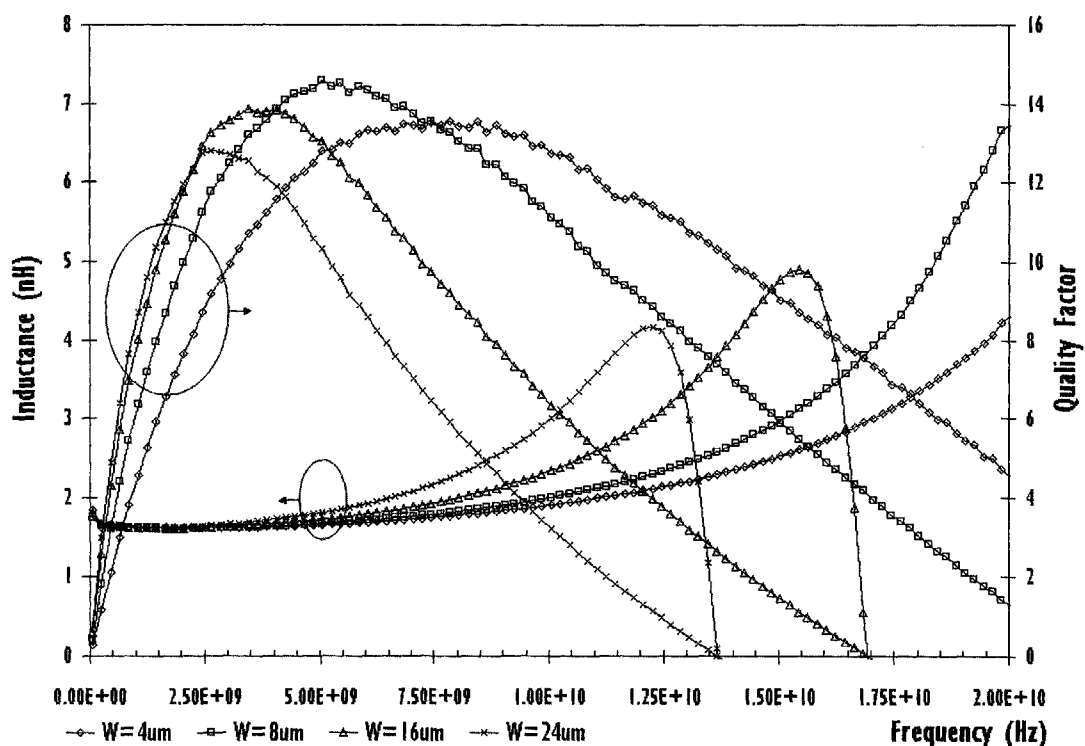


Figure 3.32 - Inductance and Q-factor for copper spiral inductors with identical inductance (1.5 nH) and core diameter (100 μm) but different widths.

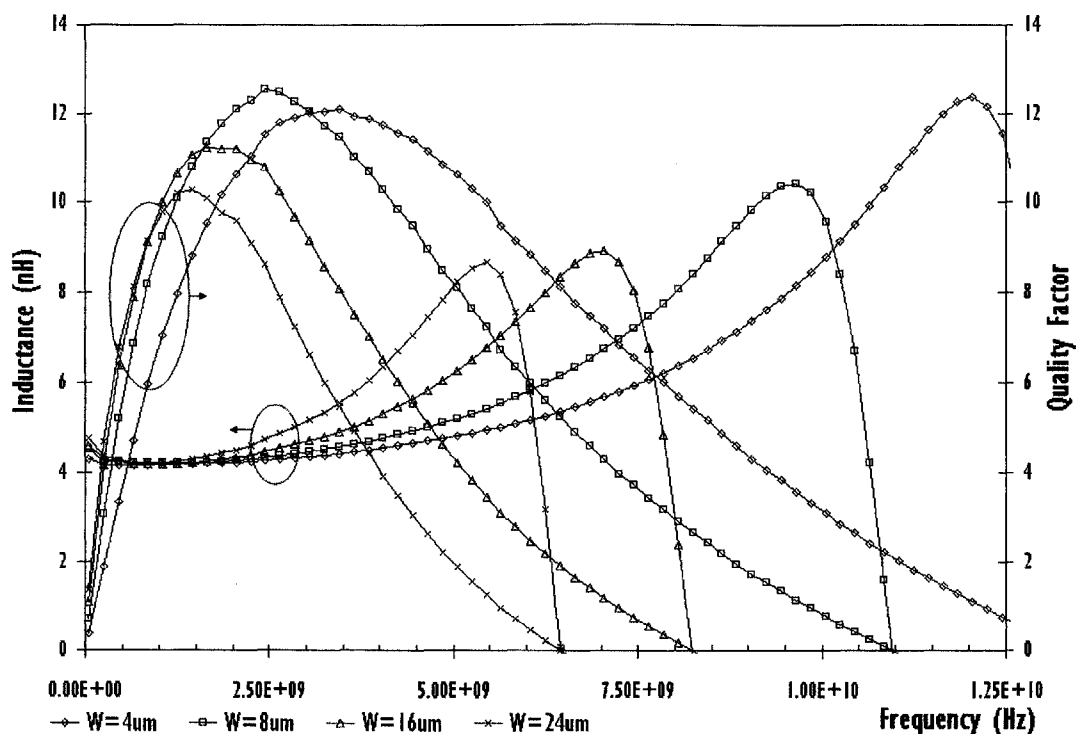


Figure 3.33 - Inductance and Q-factor for copper spiral inductors with identical inductance (4.2 nH) and core diameter (100 μm) but different widths.

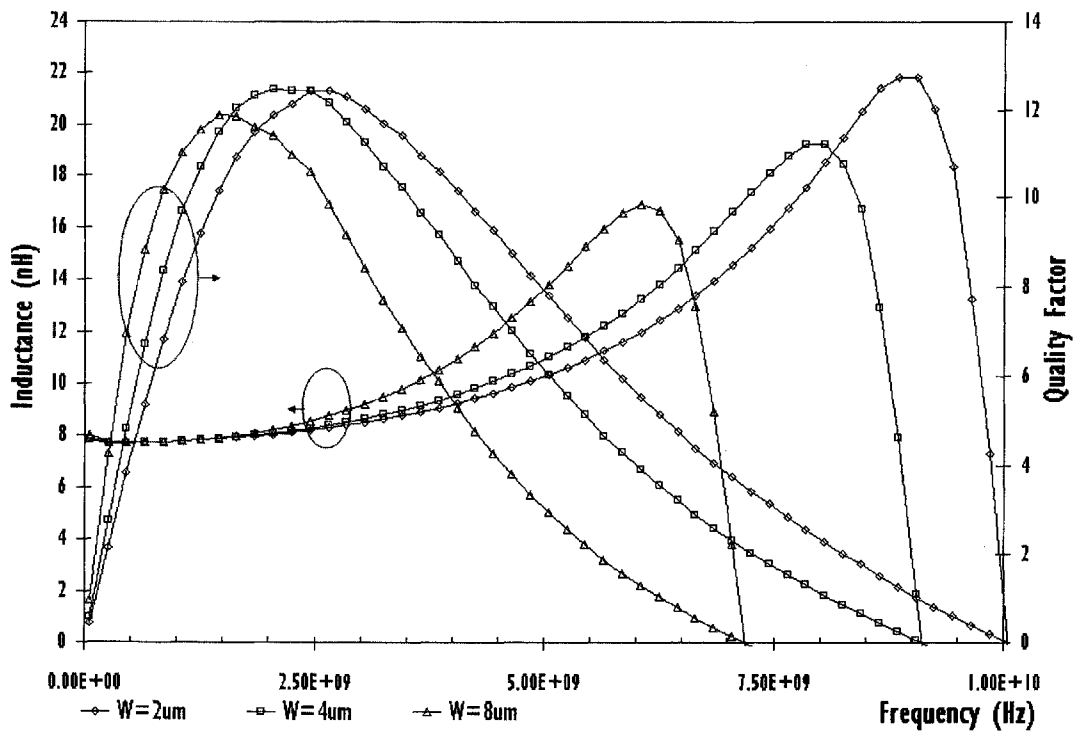


Figure 3.34 - Inductance and Q-factor for copper spiral inductors with identical inductance (7.8 nH) and core diameter (100 μm) but different widths.

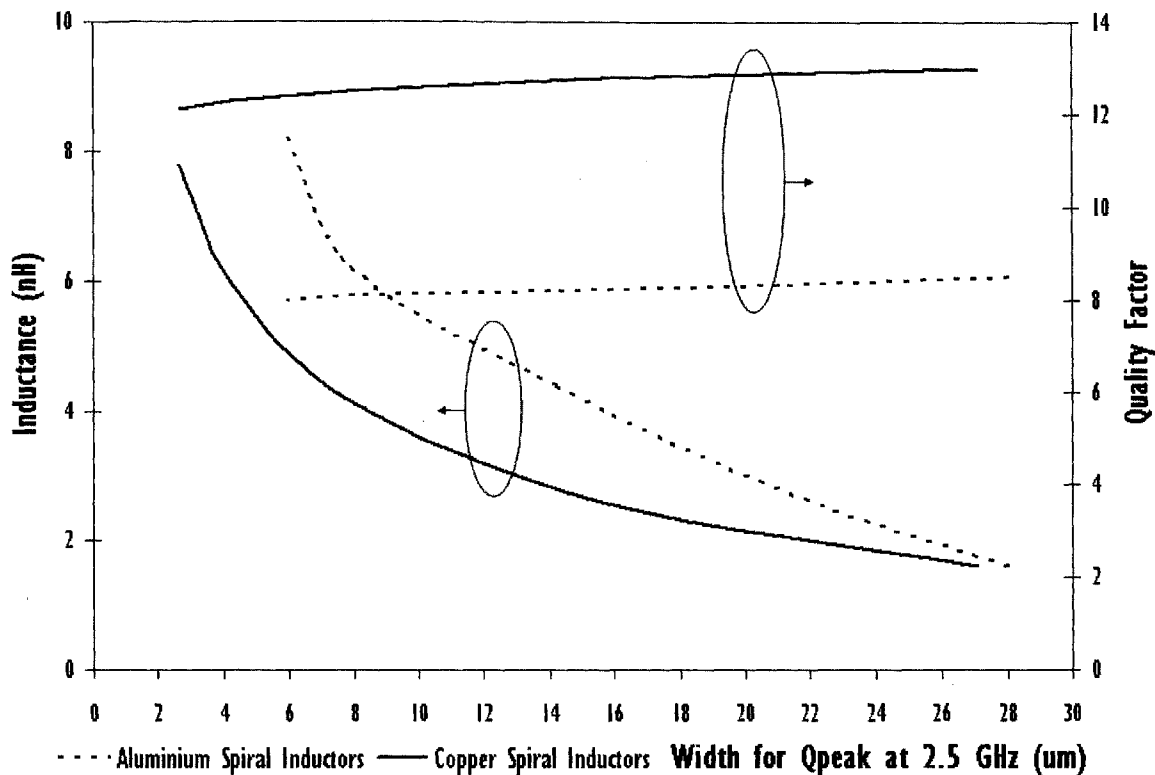


Figure 3.35 - Comparing width for Q_{peak} at 2.5 GHz and corresponding Q-factor value for aluminum and copper spiral inductors.

The novel methodology proposed in Section 3.4 not only revolutionize how RF device engineers design their spiral inductors, but has been proved to be highly trustworthy, robust and portable across both the aluminum and copper metallization technologies. As shown in Figure 3.35, for the first time, this optimization methodology has allowed meaningful technology benchmarking to be made between copper and aluminum spiral inductors by comparing over a range of inductance values, the required conductor width to achieve peak Q-factor at 2.5 GHz. Apart from achieving 50 % improvement in Q-factor and larger self resonant frequencies of more than 2 GHz, the required width for ensuring peak Q-factor at 2.5 GHz has been found to be very much smaller for copper-based spiral inductors.

For instance, to design a 7 nH inductor in the copper technology would only require half of the width compared to that of aluminum-based inductors. This finding has huge implications and numerous advantages since using smaller width not only save a lot of lateral space but with smaller widths, the per unit length inductance will be much larger,

suggesting a shorter overall conductor length to obtain the same amount of inductance. With narrower conductor widths, small core diameters can be used as conductor eddy current effect observed in Section 3.7.1 for small-width inductors will be less detrimental, significantly reducing the overall size of the inductor. In short, copper-based inductors require smaller areas and have far more superior device performance compared to aluminum-based inductors.

Chapter 4 - Modeling Symmetrical Spiral Inductors

In Chapter 3, a reliable and robust methodology has successfully optimized the physical layout of conventional spiral inductors for both the copper and aluminum metallization technologies. During the course of designing and analyzing the performance of these conventional spiral inductors, it has also been realized that this methodology can only support the physical layout optimization for spiral inductors up to 2.5 GHz. Beyond this frequency, the inductors experience self-resonance and their inductances increase at different rates, rendering fair performance comparisons with identical inductance impossible at high frequencies. As more cost-sensitive mobile communication applications turn to silicon, together with the device technology and performance advancing at an amazing pace, it is critical for device and circuit design engineers to know how to optimize the physical layout and be fully aware of the design trade-offs for spiral inductors operating at frequencies beyond 2.5 GHz.

The research outcome in Chapter 3 established fundamental knowledge, revealing that small inductors must be designed with large conductor width to suppress resistive loss achieving improvements in Q-factor. As inductance increases, the conductor width has to be reduced to minimize the substrate loss which is more dominant than its resistive loss for these large inductors. With these important understandings in mind, this chapter attempts to develop a scalable symmetrical spiral inductor device model from a streamlined set of test structures designed based on the findings in Chapter 3, so that the physical layout of symmetrical spiral inductors can be optimized up to 10 GHz. Without these prior device knowledge, to develop a decent scalable inductor model that encompasses the full design window (predicting the effects of inductor's turn, core diameter and width), enormous amount of testchip and engineering resources would be required and these resources will definitely come by with hefty price tags.

4.1 Test Structure Design Considerations and Experimental Setup

There are a few key challenges to consider and overcome when developing such an accurate and scalable inductor model. These challenges together with proposed solutions to overcome them are presented as follows:

1. Layout of the inductor's test leads must be fixed for ease of use and the input/output ports should use the highest metal layer (which is usually the thickest also) available in the processing technology. This would ensure lowest possible loss when connecting to other devices in the circuit.
2. A huge testchip with large quantities of inductors is necessary for developing a scalable device model. Hence, the inductor's layout and performance is best to be symmetrical at the input and output ports. Such kind of layout will result in much more time efficient and effective parameter extraction and model development processes. Therefore, the conventional spiral inductor layout having an asymmetrical design is not suitable and a symmetrical inductor layout shown in Figure 4.1 will be adopted for this purpose.
3. The inductor model must be able to generate inductors with fine inductance step variations, for example with 0.1 nH step size. This is absolutely necessary for device performance comparison at high frequency and circuit optimization. As revealed in Figure 3.13, varying the inductor's number of turns is not a suitable solution since the inductance steps between different turns are too large and increase at higher rates as number of turn increases. For example, from 2 to 3-turn, L increases by 0.8 nH ; from 7 to 8-turn, L increases by 3.54 nH. Therefore, instead of number of turns, core diameter of the inductor will be varied in 1 μm steps, generating sets of inductors having fine inductance variations which help facilitates performance comparisons at high frequencies.

To address the stated challenges, an extensive set of symmetrical inductor test structures has been designed. These test structures are fabricated using 0.18 μm RFCMOS processing technology. Figure 4.1 shows the layout of a 2.5-turn elliptically designed symmetrical inductor. Both input and output ports are designed with metal 6 (thickness of

2 μm) and metal 5 is used as underpasses to prevent shorting the coil. Such design has helped to achieve a very symmetrical layout, giving almost identical input and output port characteristics. Test element group consisting of 1.5 to 6.5-turn symmetrical inductors with core diameters ranging from 30 to 180 μm in steps of 30 μm is fabricated. The metal-to-metal spacing of the symmetrical inductors is fixed at 3 μm . Metal width, on the other hand, varies accordingly to the size of the inductors as stated in Figure 4.1. For example, 1.5-turn inductors are designed with widths from 8 to 32 μm and 6.5-turn inductors are designed with widths from 4 to 8 μm . From findings in Chapter 3, it would be a waste of expensive testchip resources if 6.5-turn inductors are drawn with width of 32 μm as their substrate losses will be too large, suffering self-resonance at very low frequencies and hence, completely not useful at all. Costly testchip space is better utilized if 1.5-turn symmetrical inductors are designed with widths of 32 μm which will reduce the peak Q-factor frequency and improves the Q-factor of these inductors at low GHz frequencies.

Agilent 8510C Vector Network Analyzer and Cascade Microtech Infinity probes are used to characterize these symmetrical inductors. Infinity probes are the preferred choice due to the fact that they offer low and stable contact resistance, critical in obtaining the intrinsic performance of the inductors after using a one-step open de-embedding technique. Figure 4.2 depicts a die photo showing on-wafer RF measurement of a 2.5-turn symmetrical spiral inductor using infinity probes. The methodology of characterizing these symmetrical inductors and their figure of merits are identical to those adopted for conventional spiral inductors and they have been presented and discussed in Section 3.1.

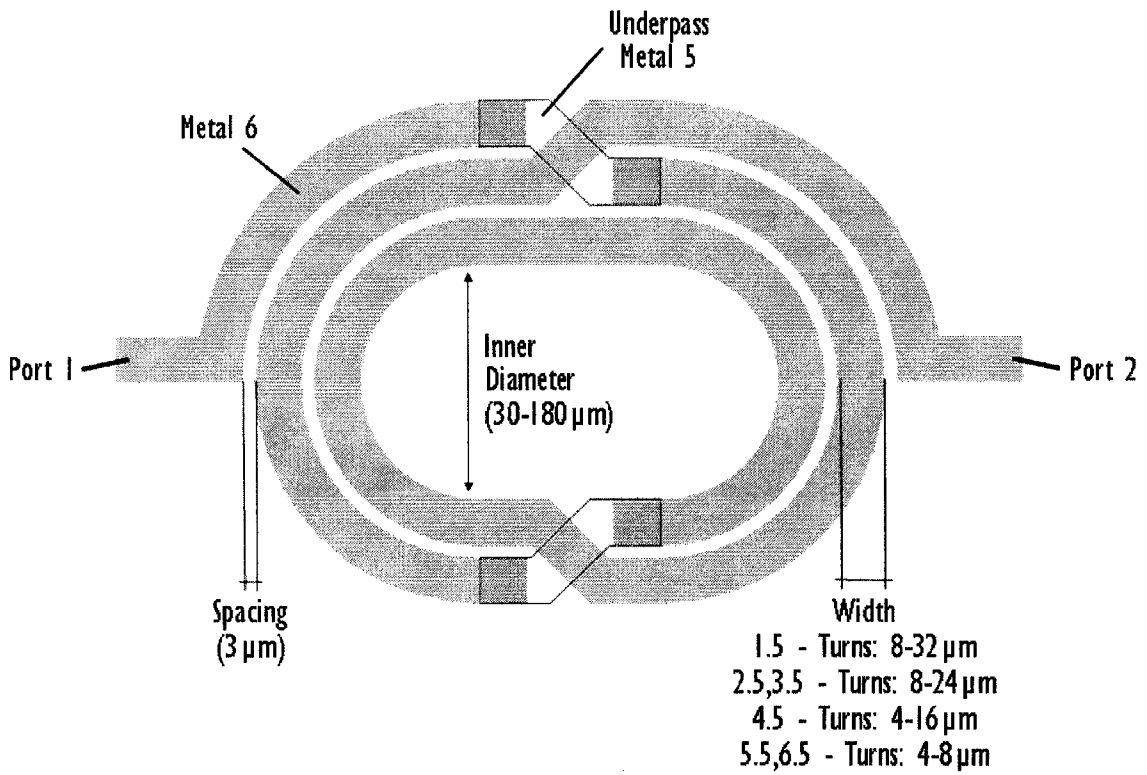


Figure 4.1 - Physical layout scheme of symmetrical inductor for 0.18 μm RFCMOS technology.

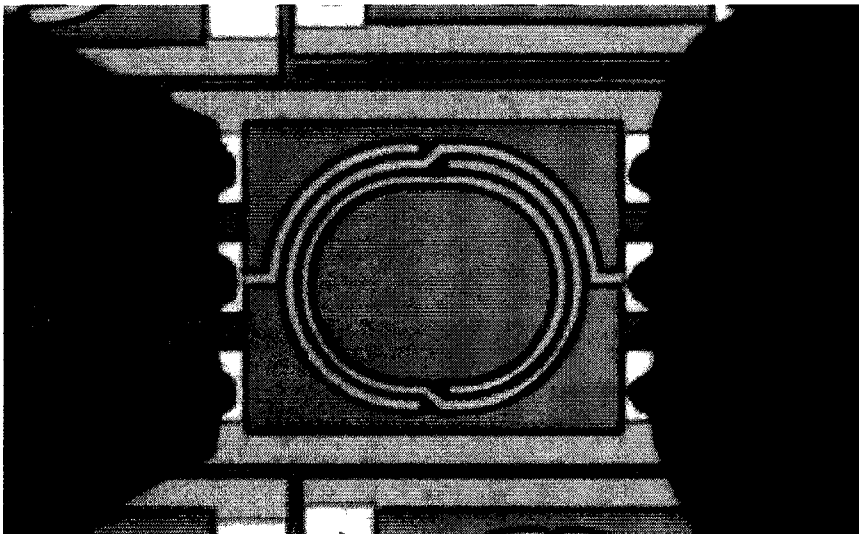


Figure 4.2 - On-wafer RF characterization of a 2.5-turn symmetrical inductor with infinity probes.

4.2 RF Sub-Circuit Model and Extraction Strategy

Figure 4.3 illustrates the proposed scalable lumped-element RF sub-circuit model for symmetrical inductors. In the sub-circuit model, L_S and R_S account for the self-inductance and resistive loss of spiral coil respectively while L_{SK} and R_{SK} model the skin effects of the metallization at giga-hertz frequencies. C_S portrays the capacitive coupling between the input and output ports. C_S portrays the capacitive coupling between the input and output ports. Substrate loss of the symmetrical inductor is modeled by C_{OX} , C_{SUB} and R_{SUB} which describe the parasitic oxide capacitance between silicon substrate and inductor, the capacitive and resistive losses of the silicon substrate respectively. Since the layout is symmetrical, the extracted model parameters such as R_S , L_S , R_{SK} , L_{SK} , C_{OX} , R_{SUB} and C_{SUB} are identical. A double- π model instead of a simple single- π model is used for the symmetrical inductors because the total conductor lengths of these inductors are typically very long and as operating frequency increases, these metallization behave like transmission lines with distributed characteristics and hence, a simple lumped element π model is insufficient to describe its behavior. Discussions explaining this phenomenon and reasons for adopting double- π -like models can also be found in Section 6.4.

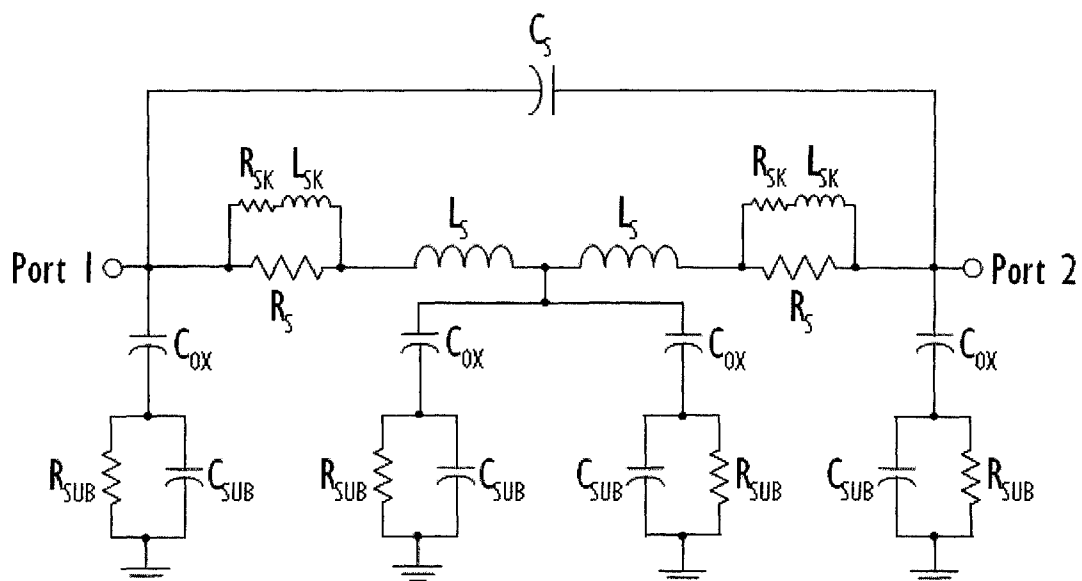


Figure 4.3 - SPICE-Compatible RF sub-circuit model for Symmetrical Spiral Inductors.

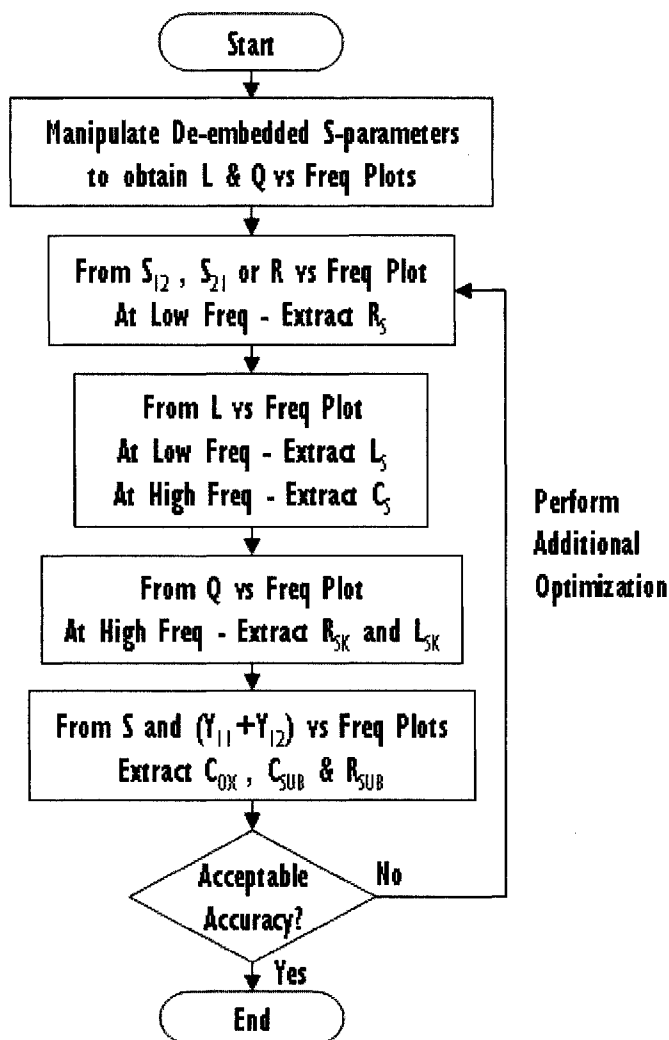


Figure 4.4 - Model extraction strategy for symmetrical spiral inductors.

Extraction strategy to obtain values of each element in the symmetrical inductor model is outlined in Figure 4.4. In this strategy, the open de-embedded Y-parameters for the symmetrical inductors, are manipulated to derive parameters such as inductance L, Q-factor and series resistance R, according to Equations 3.1, 3.2 and 3.3 respectively. Next, R_S is extracted at low frequency on the R versus frequency plot to ensure that subsequent model parameters obtained are physical and accurate. From L versus frequency plot, L_S and C_S are obtained separately focusing at the low and high frequency regions respectively. R_{SK} and L_{SK} are then acquired from Q-factor versus frequency plot, with emphasis around the peak Q-factor frequency regime to model metallization skin effects. In contrast, techniques that model skin effects using resistive elements described by frequency-dependent equations are not compatible with SPICE simulators and therefore

cannot be used in RF circuit design tools like Cadence. The subsequent step for model development would be to extract the substrate loss elements from S-parameters and Y-parameters plots. Before finally accepting the model parameters, the whole procedure is repeated a couple of times to achieve better model accuracy.

Table 4.1 - Interconnect characteristics for 0.18 μm , 0.13 μm and 65 nm RFCMOS technology.

RFCMOS Technology node	0.18 μm	0.13 μm	65 nm
Metallization material	Aluminum	Copper	Copper
Resistivity (nΩm) (approx.)	28	17	17
No. of metal layers	6	8	10
Thickness of Top metal, N (μm)	2.00	3.00	3.50
Thickness of N-1 metal (μm)	0.54	0.70	0.90
Inter-metal dielectric (IMD) material	BPSG	FSG	SiOC
IMD dielectric constant (approx.)	3.9	3.5	2.9

To extend this model from 0.18 μm RFCMOS technology to advanced nodes such as the 65 nm RFCMOS technology, key backend interconnect characteristics tabulated in Table 4.1 have to be analyzed and correlated to the model parameters. As the technology scales down, it is observed that thin aluminum is replaced with much thicker copper metallization. This reduces the resistivity (increases Q-factor) and per unit length inductance values of the metallization. Therefore, when symmetrical inductors with exactly the same design migrate from 0.18 μm to 65 nm RFCMOS technology, the model parameters, R_S , R_{SK} , L_{SK} and L_S would likely have to be trimmed down in order to have good inductance and peak Q-factor prediction. Novel inter-metal dielectric materials with much lower dielectric constants are also used in the copper backend interconnect technology. Hence, a much smaller C_{OX} value is expected to predict the larger self-resonant frequency in these advance technological nodes. These three phenomena were observed when inductors fabricated in the 0.18 μm and 0.13 μm technology are compared in Section 3.7. The smaller fringing capacitance due to IMD having low dielectric constant is counteracted by the increase in top metal thickness. Reduction in substrate resistivity to suppress the occurrence of latch-up under tighter design rules is not

substantial. As such, the values of C_S , R_{SUB} and C_{SUB} are not likely to change significantly for copper-based inductors.

In the following sections, accuracy and scalability of this model will be scrutinized extensively. Next, design trade-offs for the symmetrical inductor will be analyzed by having sets of inductors with identical inductance values but different conductor width for operating frequencies up to 10 GHz. Last but not least, a comparison will be made for this research study against other previously published work.

4.3 Model Accuracy and Continuity

To obtain measurement data for developing the symmetrical inductor model, a “golden wafer” is selected based on the measured resistivities of metal 5 and 6. Golden die is then chosen from this wafer as a die with typical inductance and Q-factor performance determined from full wafer map RF measurements on a wide-width symmetrical inductor. For most silicon foundries, device modeling workflow normally takes place immediately after a technology node has been developed, suggesting that the processing technology is likely to be still in its infancy stage. Therefore, such die selection approach prior to performing device measurements for model development is critical in prolonging validity of the SPICE model as processing technology matures along with the implementation of yield enhancement techniques.

Using inductors’ measurement data from a typical die and the proposed extraction strategy in Figure 4.4, model elements are extracted using IC-CAP, Agilent’s device measurement and modeling software. After extraction, the model parameters are each put together with empirical formulae, which best emulate their behaviors, as functions of the inductors’ turns, core diameter and width. As an example, Figure 4.5 shows how well this model can predict the measured inductance, Q-factor and series resistance for a 2.5-turn symmetrical inductor with core diameter and width of 60 and 8 μm respectively. 2.45 and 5.05 GHz have been selected to examine the accuracy as well as continuity of this scalable model. Box plots in Figure 4.6 have revealed outstanding predictability and accuracy for the symmetrical inductor model. For most of the useful inductors that have yet to operate beyond their self-resonant frequencies, model deviations between the measured and simulated inductance are within -1 % to 3 % for 2.45 and 5.05 GHz. Q-factor, on the other hand, has model deviations ranging from -3 % to 5 % for 2.45 and 5.05 GHz.

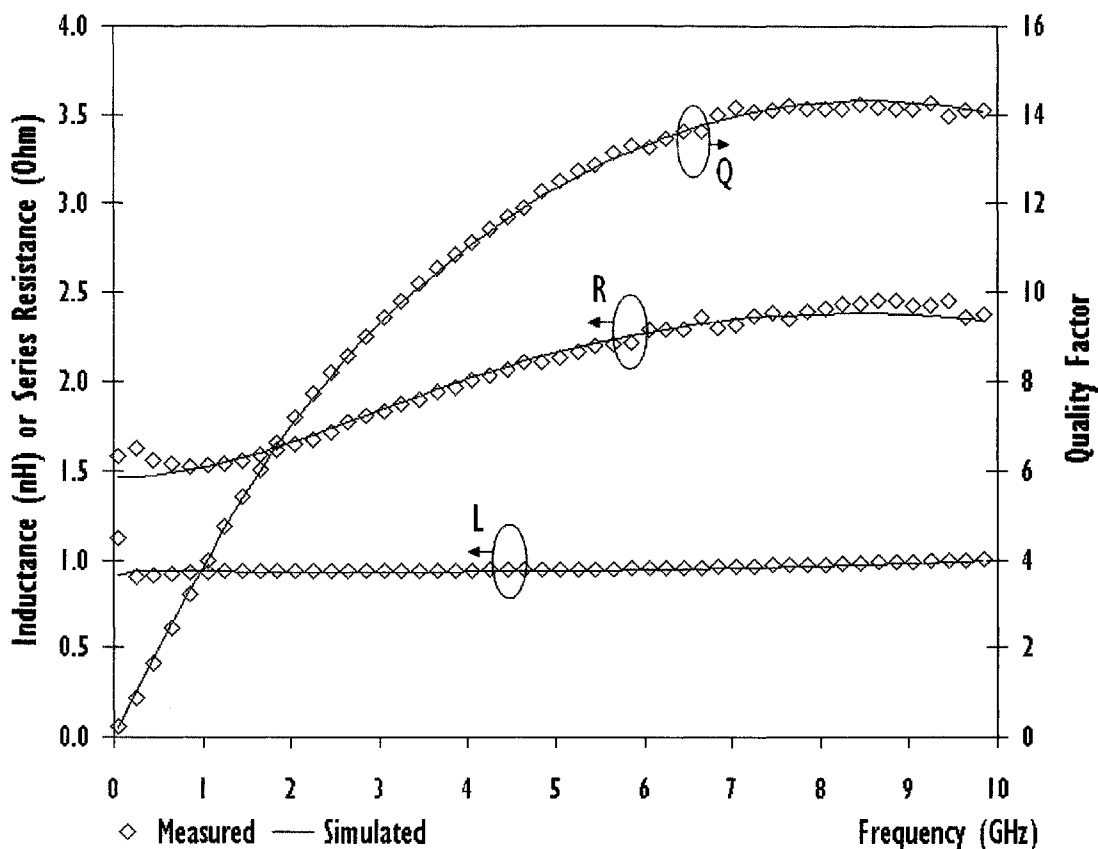


Figure 4.5 - Simulated versus measured inductance L, Q-factor for 2.5-turn symmetrical inductor with core diameter and width of 60 and 8 μm respectively.

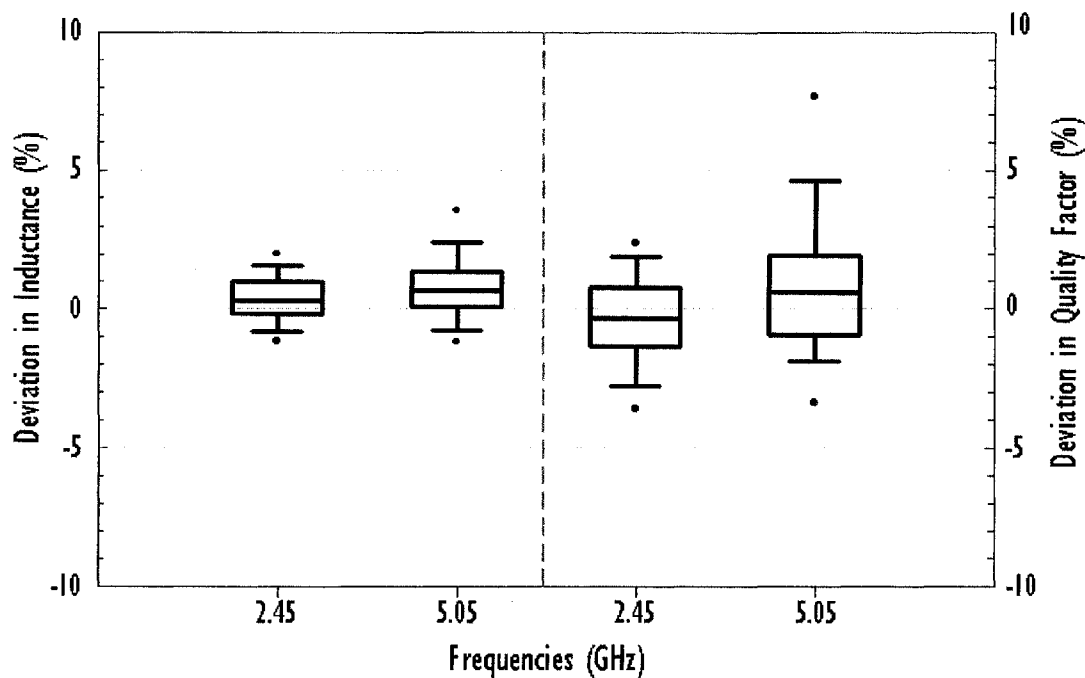


Figure 4.6 - Box plots showing deviations between SPICE model simulated and measured inductance and Q-factor at 2.45 and 5.05 GHz for all symmetrical inductors in the test element group.

The symmetrical inductor model is shown to be continuous, capable of predicting inductance and Q-factor for all the test structures with various turns, core diameters and conductor widths as illustrated in Figure 4.7. These 3-dimensional plots also disclosed excellent linearity in inductance values for all the symmetrical inductors when core diameter increased from 30 to 180 μm . Therefore, designing the test structure in this manner and changing the core diameter in steps of 1 μm will ensure the establishment of inductor device library with fine inductance steps spanning a full range of application frequencies that can address the challenges set forth in Section 4.1.

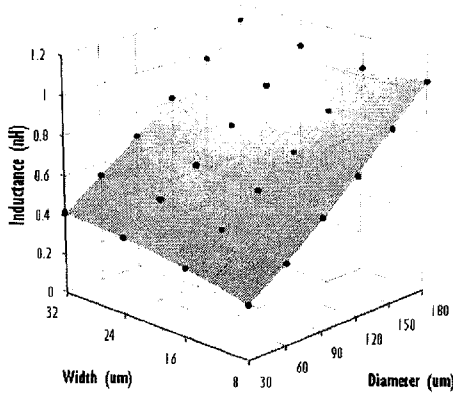


Fig 4.7 (a)

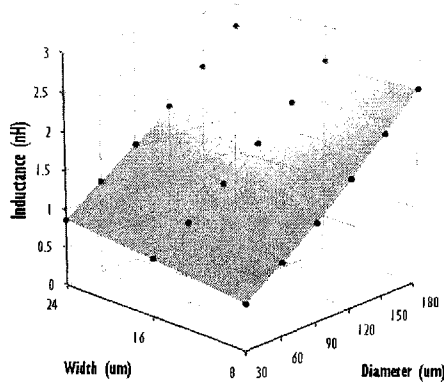
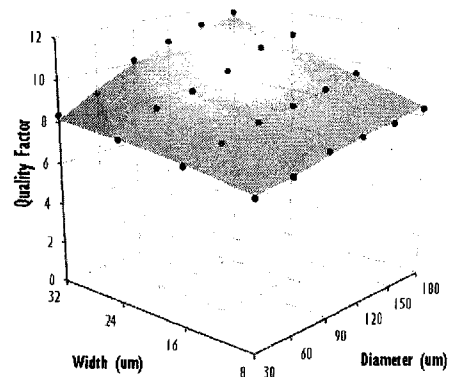


Fig 4.7 (b)

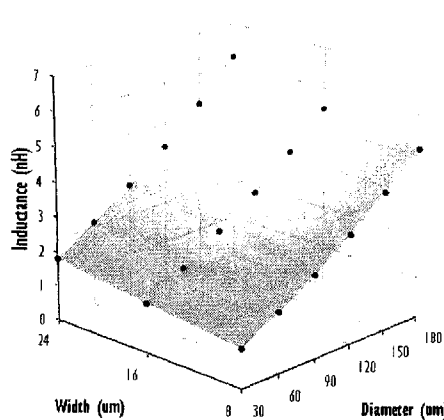
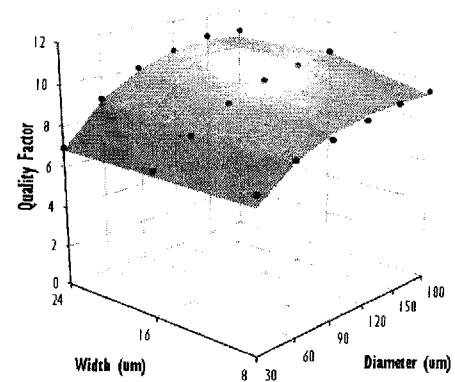
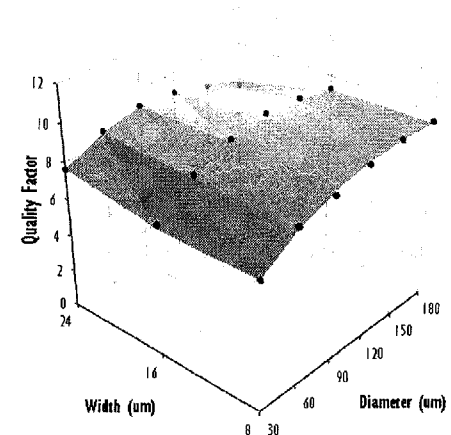


Fig 4.7 (c)



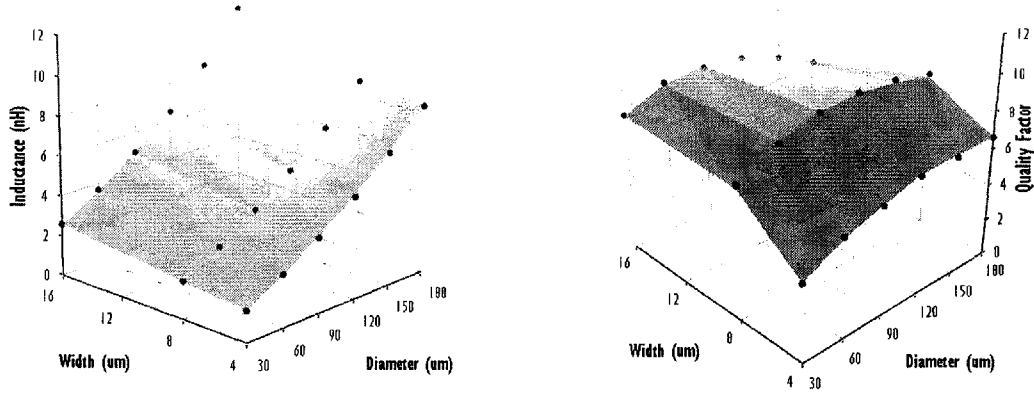


Fig 4.7 (d)

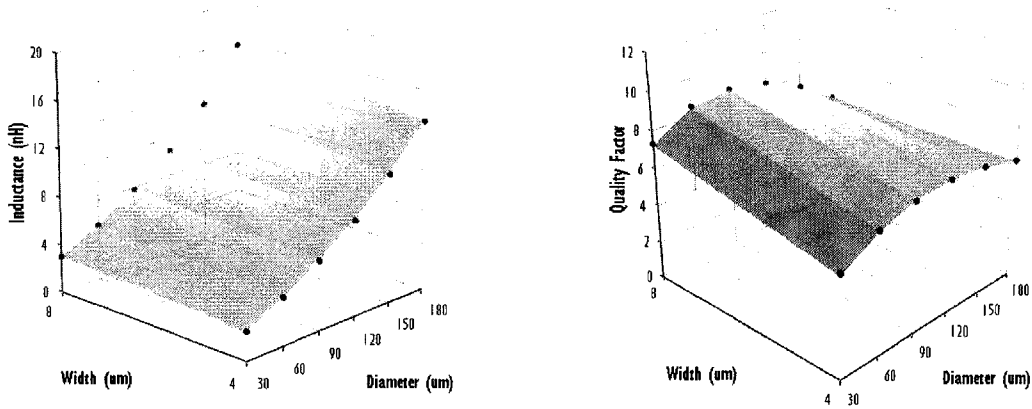


Fig 4.7 (e)

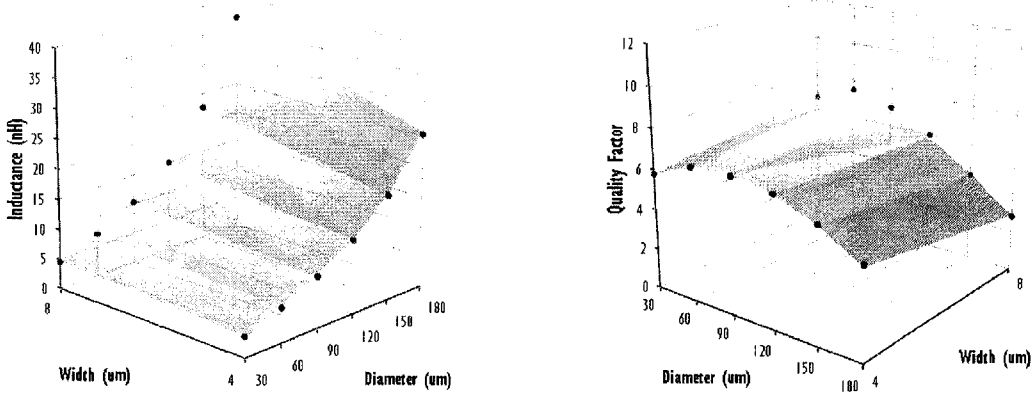


Fig 4.7 (f)

Figure 4.7- RF symmetrical inductor model continuity – simulated (surface) and measured (dots) inductance and Q-factor versus diameter and width at 2.45 GHz for 1.5-turn (a), 2.5-turn (b), 3.5-turn (c), 4.5-turn (d), 5.5-turn (e) and 6.5-turn (f) symmetrical inductors.

4.4 Design Trade-offs for Symmetrical Inductors

Figure 4.8 illustrates the inductance versus Q-factor plots for 2.5-turn symmetrical spiral inductors. On this graph, each of these plots represents a set of 2.5-turn inductors having a fixed conductor width with diameters varying from 30 to 180 μm . For instance, when diameter changes from 30 to 180 μm for the conductor width of 8 μm , inductance values from 0.6 to 2.6 nH are obtained correspondingly. Drawing iso-inductance lines across the plots in Figure 4.8 facilitate impartial performance evaluations on the effects of conductor width for the symmetrical inductors. For example, when a 2 nH iso-inductance line crosses the three plots, it is observed that for the widths of 8, 16 and 24 μm , in order to obtain inductors with exactly 2 nH at 2.45 GHz, the core diameters must be between 120 and 150 μm . Making use of the scalable symmetrical inductor model to perform 1 μm linear interpolation of the core diameter allows 3 inductors with widths of 8, 16 and 24 μm to have exactly 2 nH at 2.45 GHz.

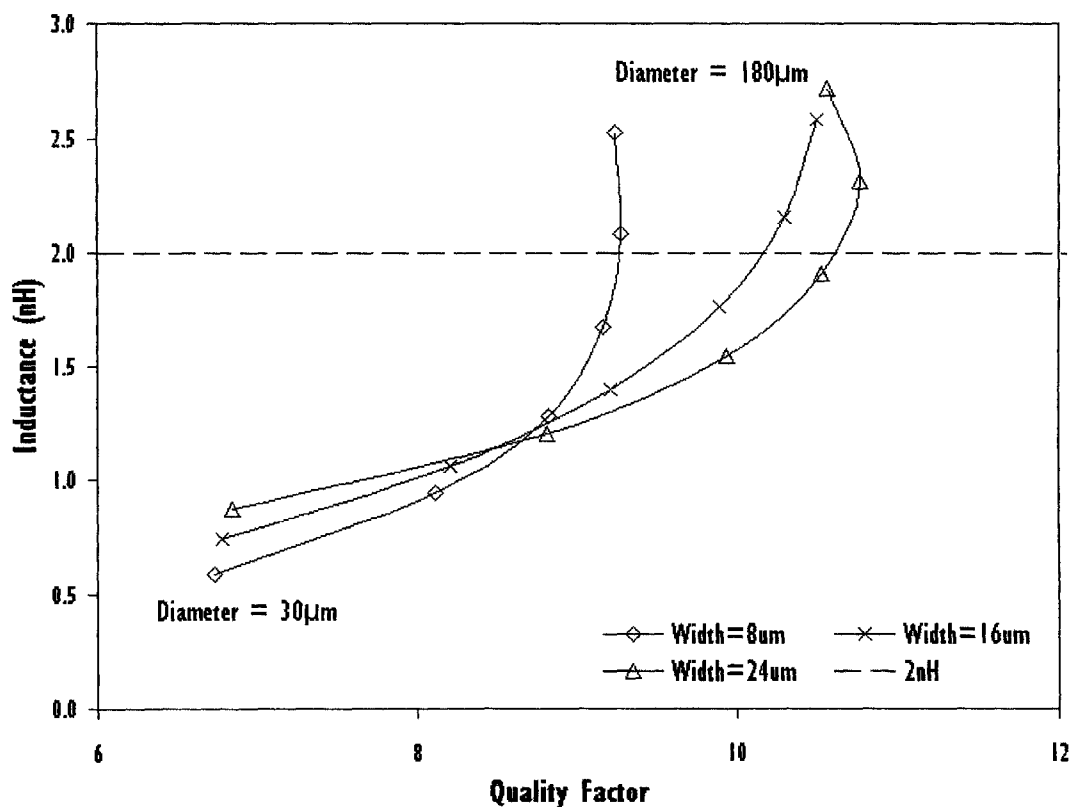


Figure 4.8 - Inductance versus Q-factor for sets of 2.5-turn symmetrical inductors with core diameters from 30 to 180 μm and different widths at 2.45 GHz.

Figure 4.9 shows the inductance and Q-factor versus frequency plots for 2 nH symmetrical spiral inductors at 2.45, 5.05 and 10.05 GHz obtained using the scalable symmetrical inductor model. These graphs have indeed revealed the fact that varying and optimizing the core diameters in 1 μm steps has successfully allowed symmetrical inductors of different conductor widths to have identical inductance values and hence, non-biased performance comparisons at application frequencies up to 10 GHz. As operating frequency increases, 2 nH symmetrical inductors with larger widths must be designed to have smaller low-frequency inductances (much less than 2 nH), taking into considerations self-resonance effects to ensure that these inductors would have exactly 2 nH at the frequency of interest, making fair device performance comparisons possible. Facilitated by the accurate and scalable symmetrical inductor model developed in Section 4.3, these innovative experimental comparisons are performed for the first time, conveniently at frequencies more than 2.5 GHz.

Figure 4.9 (a) concludes that at 2.45 GHz, use of 24 μm conductor width instead of 8 μm for 2 nH symmetrical inductor reduces the resistive loss at low frequencies, thereby improving Q-factor by about 15 %. Although implementing such design approach trade-off substantial chip area for better device performance, optimal widths exist across each operating frequencies beyond which any further use of larger width and silicon real estate would renders this technique ineffective. To illustrate this, in Figure 4.9 (c), at 10.05 GHz, using 8 μm conductor width instead of 16 μm for the 2 nH inductor results in higher Q-factor with more than 53 % improvement. Although the inductor with 8 μm conductor width has lower Q-factor at frequencies below 3 GHz, as operating frequency increases, substrate loss which is directly proportional to conductor width becomes very dominant for the large-size inductor with width of 16 μm , thereby causing fast Q-factor roll-offs. Hence, at 10.05 GHz, Q-factor for 8 μm width inductor is observed to be the most superior. To sum up, when operating frequency increases, employing narrower conductor

width and thus shorter total conductor length (narrow width conductor have larger per unit length inductance) concurrently results in smaller inductor size, lower substrate loss and better device performance all at the same time.

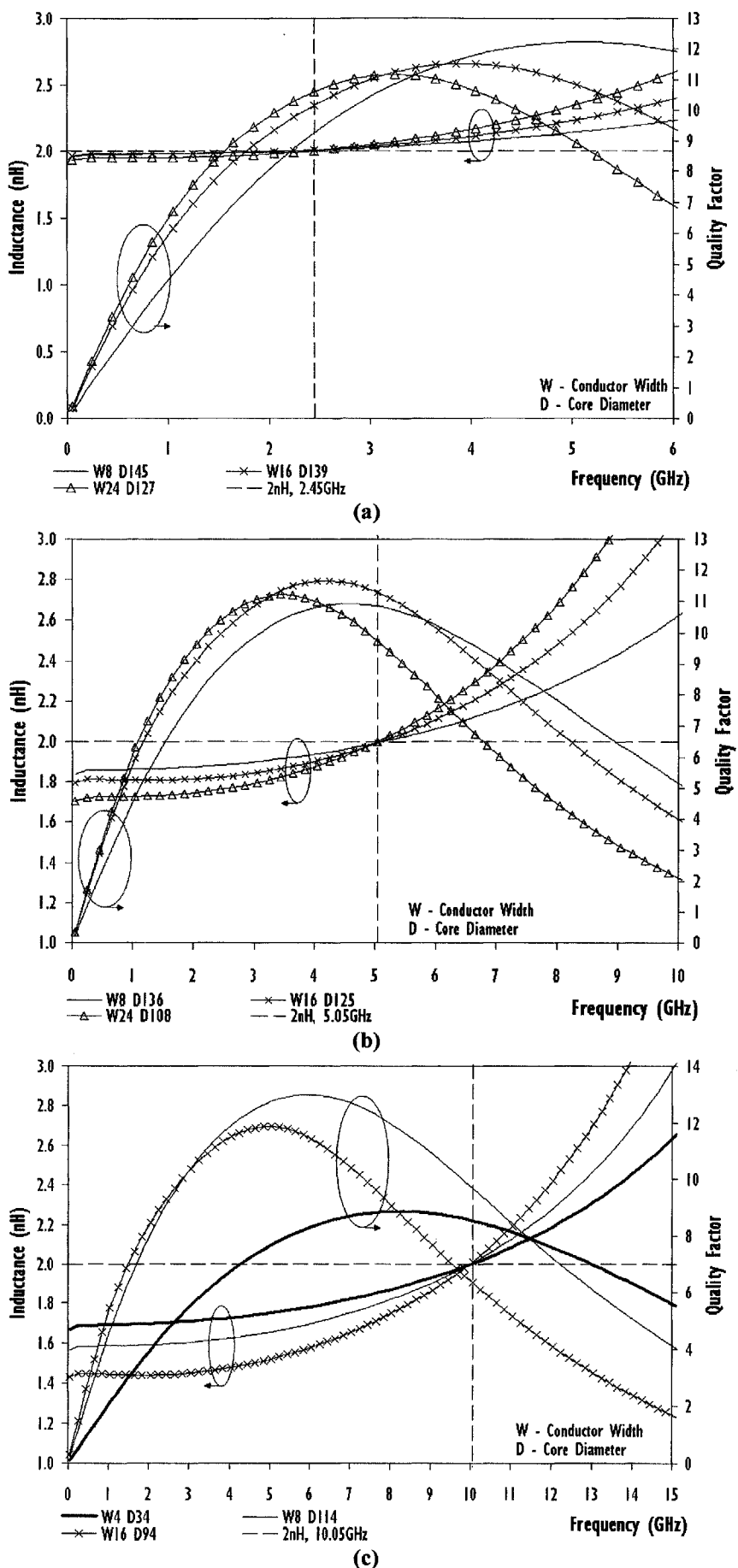
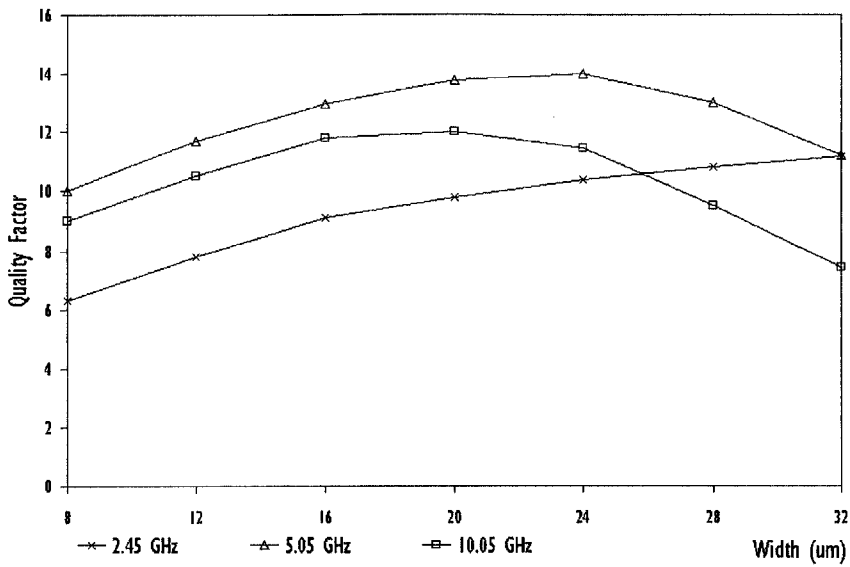


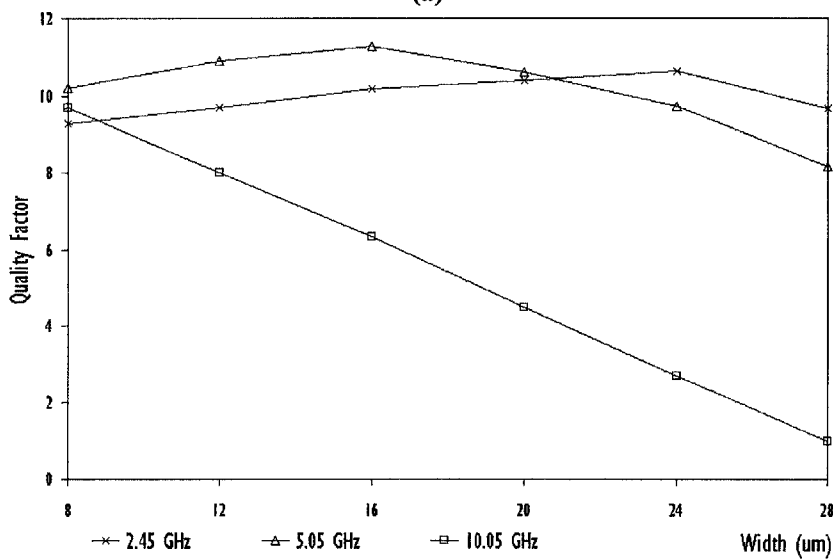
Figure 4.9 - Inductance and Q-factor versus frequency for 2 nH symmetrical inductors at 2.45 (a), 5.05 (b) and 10.05 GHz (c).

Figure 4.10 consolidates and compares 1, 2 and 4 nH symmetrical inductors at 2.45, 5.05 and 10.05 GHz, with identical inductance values, plots of Q-factor versus conductor width. For small-inductance symmetrical inductors, using large conductor width improves Q-factor for 1 nH inductors. This as explained earlier on is attributed to the reduction in resistive loss at the expense of chip area. As inductance or operating frequency increases, trade-offs between resistive and substrate loss results in the existence of optimal widths such that beyond these widths, any further use of larger conductor width do not improve Q-factor but waste expensive silicon area. This is evident for 2 and 4 nH inductors in Figure 4.10 (b) and (c) respectively, showing degradations in Q-factor for operating frequency of 10.05 GHz when conductor width of more than 8 μm is used.

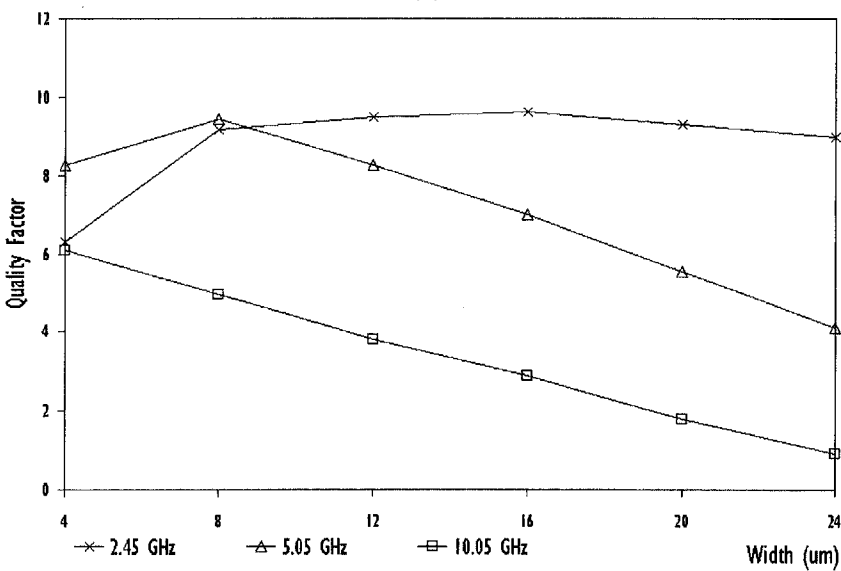
Figure 4.11 summarizes the 3 plots in Figure 4.10, describing the optimal widths which will give the highest Q-factor at various inductance values and operating frequencies. In general, as frequency or inductance increases, the optimal widths, whereby highest Q-factor can be attained from a given symmetrical inductor design, would be reduced. Figure 4.11 also compares, for the first time, at 2.45 GHz, optimal widths between conventional spiral inductors in Chapter 3 and the symmetrical spiral inductors in this chapter. Although physical designs and optimization methodologies for these 2 inductors are relatively different, they yielded almost identical optimal width versus inductance characteristics. This gives absolute confidence to the proposed methodology of using an accurate and scalable device model to extend the physical layout optimization of inductors beyond 2.45 GHz. It is also motivating to note that when operating frequencies increases, optimal widths for spiral inductors decreases. As silicon processing technologies advances with huge improvements made to the transistor's speed and cut-off frequency, RF circuits operating at higher frequencies will benefit from small-size inductors that come with high Q-factors.



(a)



(b)



(c)

Figure 4.10 - Q-factor versus conductor width for 1 nH (a), 2 nH (b) and 4 nH (c) symmetrical inductor at operating frequencies of 2.45, 5.05 and 10.05 GHz.

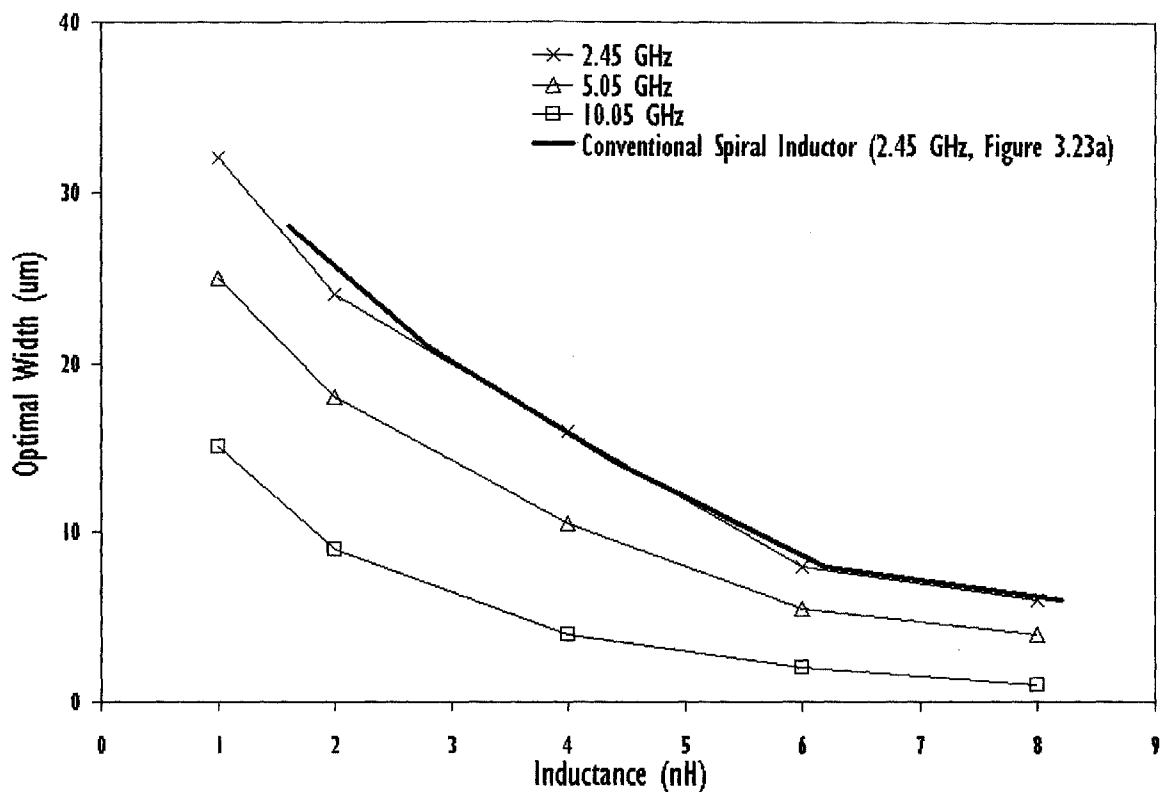


Figure 4.11 - Optimal width for symmetrical inductor at operating frequencies of 2.45, 5.05 and 10.05 GHz and comparing conventional spiral (Chapter 3, Figure 3.23a) and symmetrical spiral inductor at 2.45 GHz.

The accuracy and scalability of the symmetrical inductor model developed in this work will be verified in Chapter 5 using a differential amplifier with the device model accuracy determined based on correlations between measured and simulated circuit results.

4.5 Comparing Research Works on Modeling Spiral Inductors

Most of the research studies published in the literature utilize limited test structures to develop scalable inductor models and they fail to ensure identical inductance values for device performance comparisons across different application frequencies. On the contrary, this research work has a huge test element group of 102 inductors spanning wide-ranging physical design parameters of 1.5 to 6.5-turn, widths from 4 to 32 μm and core diameters from 30 to 180 μm , to comprehensively test the proposed extraction strategy and model development methodology for the symmetrical inductors.

Table 4.2 compares a number of research papers that were recently published in prestigious technical journals to quantify the contributions for this research work [61] - [65], [35]. Notably, this research employs the most number of test structures for model development, concurrently achieving the smallest model error. In contrast to published work that uses EM simulated inductor characteristics as the data for developing non-SPIICE compatible artificial neural network models [35], this research work has designed, fabricated and performed on-wafer RF measurements for more than a hundred symmetrical spiral inductors to develop a practical, accurate and scalable model. This symmetrical inductor model was also verified using a giga-hertz amplifier and further exploited to make ground breaking analysis in the trade-off studies between the inductor layout design and its performance up to 10 GHz.

Table 4.2 - Comparing various research works on modeling and optimizing the design of spiral inductors.

First Author	Y. Cao	J. Chen	X. Huo	W. Gao	F. Huang	S. K. Mandal	This Work
Reference	[61]	[62]	[63]	[64]	[65]	[35]	
Technical Journals	IEEE JSSC	IEEE TED	IEEE TED	IEEE TMTT	IEEE JSSC	IEEE TCAD Cir & Sys	To be Published
Year of Publication	2003	2006	2006	2006	2006	2008	
Number of test structures used for model development.	11	3	7	14	5	400 (EM Simulated data)	102 (refer to Section 4.1)
How many elements are in the proposed model?	24	12+S×10 (S=no. of Segments, a 3-turn inductor, has 62 elements, each inductor will have a different model)	20 (More elements to be added for better accuracy)	24 (All have to be extracted)	20	Unknown (Artificial Neutral Networks (ANN) models for 0.18 μm CMOS Inductors)	21 (Only 8 elements have to be extracted)
What is the operating frequency supported by the model?	10 GHz	15 GHz (acceptable model fitting up to 10 GHz)	10 GHz	20 GHz (acceptable model fitting up to 10 GHz only)	10 – 20 GHz	Up to 2.5 GHz	10 GHz (or Self-resonant, whichever is lower)
What is the model error/deviation?	Q deviation* -10.8 – 8.7 %	Only fitting results for 3 inductors (No model Deviation)	Only fitting results for 7 Inductors (No model Deviation)	Only fitting results for 3 inductors (No model Deviation)	L : 6.6 % Q : 8.9 %	L : 15 % Q : 8 % (After testing ANN-model with another 100 EM simulated inductors)	L : -1 to 3 % Q : -3 to 5 % (For all inductors at 2.45 and 5.05 GHz)
Is the model scalable to the inductor physical design parameters?	To a certain extent, but only 11 inductors with limited turns, widths and diameters	Only 3 inductors having 2.5, 3 and 5 turns	Only 7 Inductors with different turns and substrate resistivities	Only 3 inductors results are published	Only fitting results for 5 inductors	Unknown (No data published and no inductor data to compare)	Yes (102 inductors, Scalable across different Turns, Width, Diameter)
What is the performance of the model continuity for different physical dimensions?	Unknown	Unknown	Unknown	Unknown	Unknown	Unknown (No L and Q fitting plots against the physical dimensions of Inductors)	Excellent (Model is continuous Figure 4.7)
Is the model SPICE-compatible?	Yes	Yes	Yes	Yes	Yes	No (No sub-circuit models for inductors were published)	Yes
Trade-off studies between performance, layout and operating frequency at same inductance value?	No	No	No	No	No	3nH at 2.5 GHz 4nH at 1 GHz (ANN model was trained based on EM simulated inductor results)	Yes (Recommend the optimal widths for different inductance values up to 10 GHz Figure 4.10)
Has the model been verified in test circuits?	No	No	No	No	No	No	Yes (Amplifier was used, Results in Section 5.5)

*Absolute error is calculated instead of the published root mean square error

Chapter 5 - Modeling Differential Spiral Inductors

Differential modulation schemes for low cost transceivers have motivated strong research interests in silicon-based on-chip differential inductors [66] - [70]. These differentially driven symmetrical spiral inductors are extensively used in matching networks and LC tanks for differential circuits such as low noise amplifiers and voltage controlled oscillators. Inter-winding 2 coils together, differential inductor consumes smaller silicon area, in doing so reduces the overall chip size. They also exhibit higher Q-factor over a broader range of frequency, making them essential device components for radio frequency integrated circuit (RFIC) design. Despite these advantages, such inductors are not readily available in silicon-verified device libraries but only offered by established semiconductor foundries. Reliable techniques to optimize the physical design of differential inductors are also not well established in the literature.

To fully exploit the capabilities of these monolithic differential inductors, RFIC designers require a comprehensive device library in user-friendly process design kit (PDK) to achieve design success in a short development cycle. Impacts of each physical design parameters such as core diameter, methodologies to optimize these parameters and availability of silicon-verified inductor libraries having small incremental steps of inductance values are crucial criteria for successful circuit design optimization. In short, circuit designers must have accurate and scalable device models, empowering them with full flexibilities and freedom to choose and trade-off between device performance and device size conveniently. In this chapter, an accurate and scalable differential inductor model is presented to address the growing demands of differential design trends for RFICs. This scalable model allows physical layout of differential inductors to be optimized either for small area-driven or high performance-driven circuit designs at application frequencies up to 10 GHz. Accuracy of the differential inductor model is also

verified using giga-hertz differential amplifiers, revealing excellent correlations between simulated and measured circuit characteristics.

5.1 Design of Test Structures and Experimental Setup

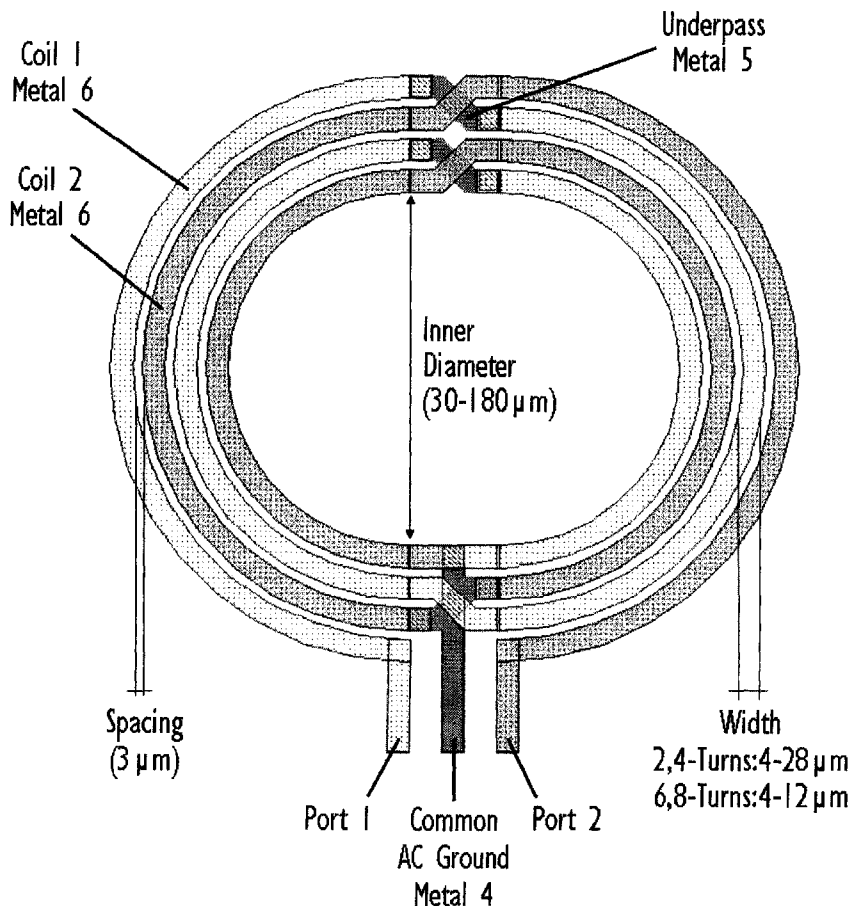


Figure 5.1 - Layout scheme of differential inductor in 0.18 μm RFCMOS process.

An extensive set of differential inductor test structures has been designed so as to extract a scalable differential inductor model and allow for application specific performance optimization. These test structures are fabricated using the same 0.18 μm RFCMOS processing technology. Figure 5.1 shows the layout of a 4-turn circular differential inductor. Its 2 spiral coils consist mainly of thick top metal 6 with metal 5 as underpasses to avoid shorting the two coils. The centre-tap, a common AC ground where the two coils are connected is routed out from the centre of the differential inductor with metal 4. To obtain experimental data required for developing the scalable RF model, test element group consisting of 2, 4, 6 and 8 even-turn differential inductors with core diameters

ranging from 30 to 180 μm in steps of 30 μm is fabricated. The metal-to-metal spacing of the differential inductors is kept constant at 3 μm . Metal width, on the other hand, varies from 4 to 28 μm for 2-turn and 4-turn inductors and 4 to 12 μm for 6-turn and 8-turn inductors, all sets spaced in steps of 4 μm .

Several objectives can be achieved by designing the test element group in this manner. One important goal is to have small incremental inductance steps within the library of differential inductors. Instead of changing the inductor's number of turns, which likely give rise to inductors with quarter, half or three-quarter turns, varying the core diameter in small steps offers much smaller, linear and gradual change in its differential inductance. Having such small incremental inductance steps within the library of inductors is essential to facilitate efficient circuit optimization; managing circuit post-layout interconnect effects as well as swift design migrations for circuits with conventional spiral inductors to differential inductors. In addition, this approach also allows the input/output leads of differential inductors to be established in a fixed orientation, making the overall chip floor-planning a convenient task for IC layout engineer (unlike changing number of turns which could lead to inductors having either quarter, half or three-quarter turns).

Inductors with large core diameters are usually preferred because they have high Q-factor due to small conductor eddy current effect as discussed in Chapter 3. Nonetheless, when circuit performance can be compromised to achieve more area efficient chip, inductors having small core diameter will be the favored choice. To cater for such design requirements, core diameter of differential inductors in this test element group were varied from 30 to 180 μm . The layouts of these inductors are permuted with different width designs, allowing performance optimization at various application frequencies for differential inductors having wide range of inductance values. More in-depth discussions will be presented in subsequent sections of this chapter.

Agilent 8510C Vector Network Analyzer and Cascade Microtech Infinity probes are used to characterize the differential inductors. Infinity probes are preferred since they have low and stable contact resistance. Wafer and RF probes are shielded within the Micro-chamber of the semi-automated probe station throughout the measurements. Two-port S-parameters of the fabricated inductors are extracted over the frequency range from 50 MHz to 20.05 GHz. Reverse side of the wafer has been back-grinded such that the substrate is grounded through the test chuck. P+ taps near the inductors are also included and connected to the ground pads to ensure effective grounding of the substrate.

Popular technique to layout full-turn differential inductors for on-wafer RF characterization is to adopt a ground-signal-ground (GSG) configuration as shown in Figure 5.2. Two calibration structures, the open (Figure 5.2(b)) and short (Figure 5.2(c)) are required to move the measurement reference plane to the inductor input/output leads depicted in the layout of Figure 5.1. An open followed by short de-embedding procedure will remove the pad capacitive parasitic, then test leads resistive and inductive parasitics respectively. Such method of characterizing the inductor will need more silicon real estate as extra set of ground pads and additional short calibration structure are required. Also, the short de-embedding procedure has high tendencies of introducing over de-embedding errors especially if high contact resistance is experienced during probing of the short calibration structure, or for the case of small inductors having resistance values comparable to the contact resistance of the RF probes. Device engineers would need extra times and attention during on-wafer probing as occurrences of such de-embedding errors may result in inductors having deceptively high Q-factor.

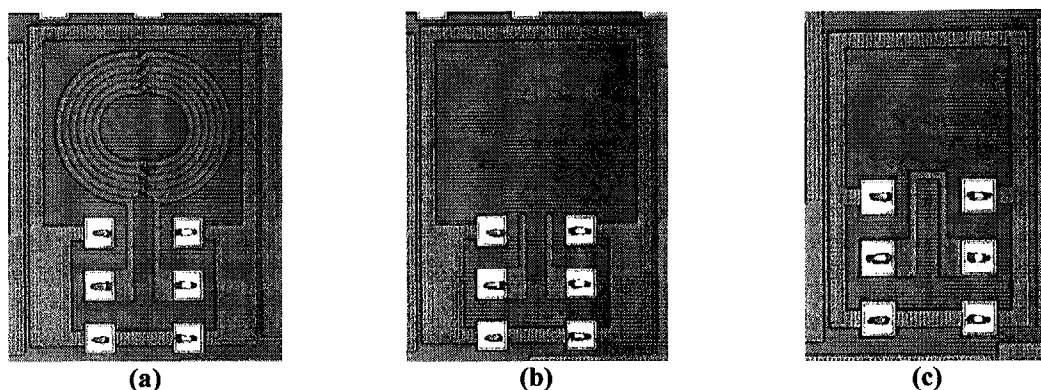


Figure 5.2 - Die photos showing differential inductor layout in GSG configuration, inductor (a) open (b) and short calibration structures (c).

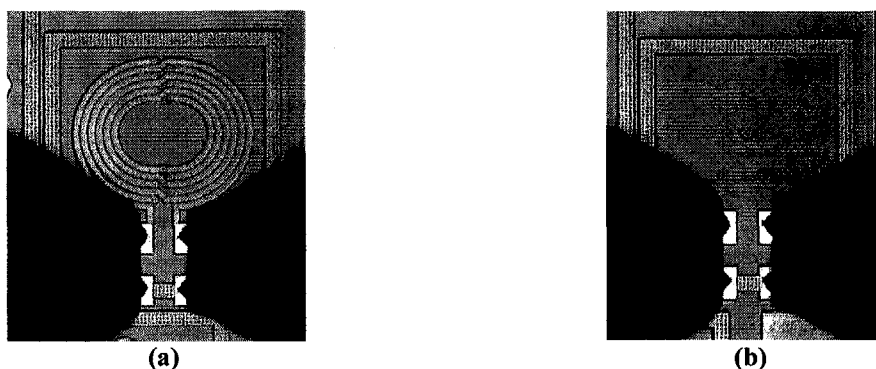


Figure 5.3 - Differential inductor layout in GS configuration, inductor (a) and open calibration structure (b).

For this work, a ground-signal (GS) configuration approach as shown in Figure 5.3 is adopted for the differential inductor. The signal pads are directly shorted to the test leads of the inductor and hence, short calibration structure is not required. Capacitive parasitics of the test pads are accurately de-embedded by subtracting Y-parameters of the open calibration structures from test structures with the inductors as outlined in Section 2.3.4. As opposed to the GSG configuration, the GS layout approach not only minimizes de-embedding errors but also yielded a significant 44 % reduction in test chip size. More importantly, reliability of the GS layout approach has been demonstrated up to 20 GHz with excellent correlations between de-embedded intrinsic characteristics of differential inductors for the two different layouts schemes as shown in Figure 5.4.

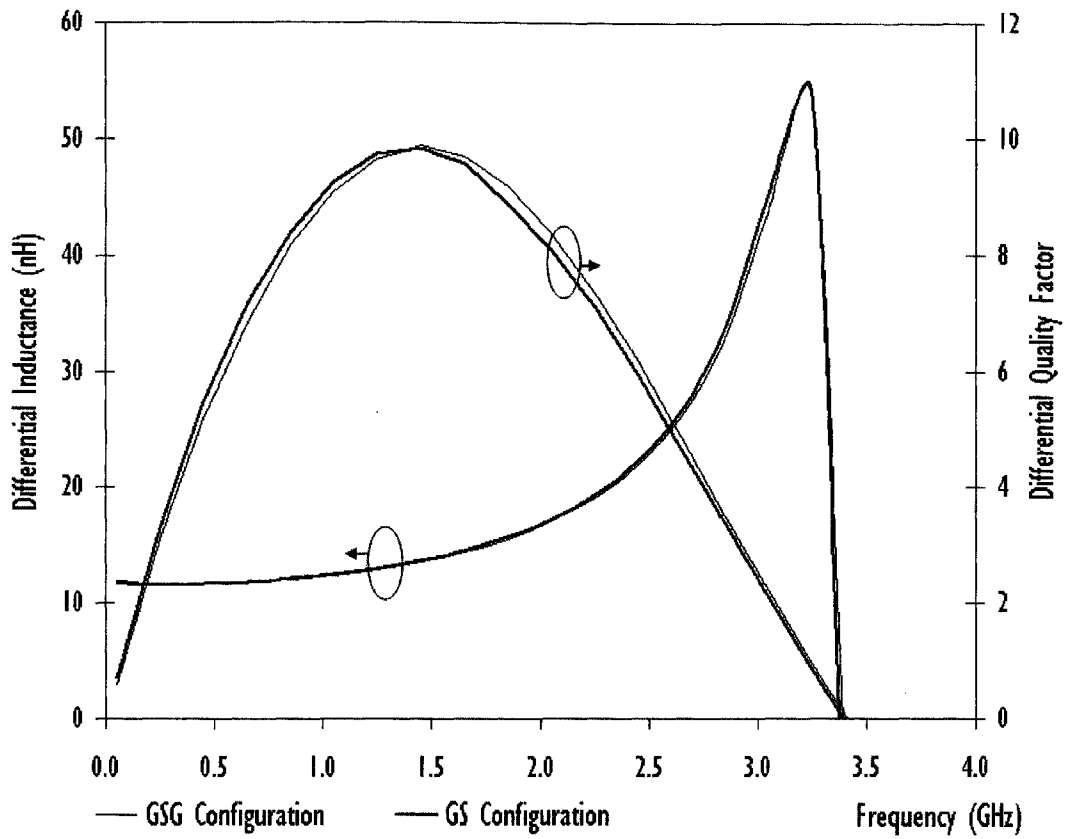


Figure 5.4 - Differential inductance and Q-factor versus frequency for same differential inductor in GSG and GS layout configurations.

5.2 Figure of Merits for Differential Spiral Inductors

Differential inductors' figure of merits, differential inductance, L_{DIFF} and differential quality factor, Q_{DIFF} used in this paper are obtained from the de-embedded S-parameters shown in Equations 5.1 to 5.4 [71], [72]. The differential one-port S-parameter is first obtained from the de-embedded S-parameters as follows:

$$S_{\text{DIFF}} = \frac{S_{11} + S_{22} - S_{12} - S_{21}}{2} \quad (5.1)$$

With Z_o as the differential system impedance, the differential Z-parameter is derived as:

$$Z_{\text{DIFF}} = \frac{2Z_o(1 + S_{\text{DIFF}})}{1 - S_{\text{DIFF}}} \quad (5.2)$$

Differential inductance and quality factor are evaluated from the differential Z-parameter as:

$$L_{\text{DIFF}} = \frac{\text{Imag}(Z_{\text{DIFF}})}{2 \times \pi \times \text{Frequency}} \quad (5.3)$$

$$Q_{\text{DIFF}} = \frac{\text{Imag}(Z_{\text{DIFF}})}{\text{Real}(Z_{\text{DIFF}})} \quad (5.4)$$

The inductance related to single-ended excitation (at Port 1) to decouple the inductive mutual coupling effects between the two spiral coils can be evaluated as:

$$L = \frac{\text{imag} \left[Z_o \times \left(\frac{1 + S_{11}}{1 - S_{11}} \right) \right]}{2 \times \pi \times \text{Frequency}} \quad (5.5)$$

5.3 RF Sub-Circuit Model and Extraction Strategy

Figure 5.5 depicts the proposed scalable lumped-element RF sub-circuit model for the differential inductors in this paper. L_S and R_S emulate the self-inductance and resistive loss of both spiral coils respectively while L_{SK} and R_{SK} model the skin effects of the metallization at giga-hertz frequencies. M_1 describes the inductive mutual coupling effects between the 2 coils. C_S accounts for the capacitive coupling between coil 1 and coil 2. R_1 models the resistive loss of the centre-tap underpass. Substrate loss of the differential inductor is taken care by C_{OX} , C_{SUB} and R_{SUB} which describe the parasitic oxide capacitance between the silicon substrate and inductor, the capacitive and resistive losses of the silicon substrate respectively.

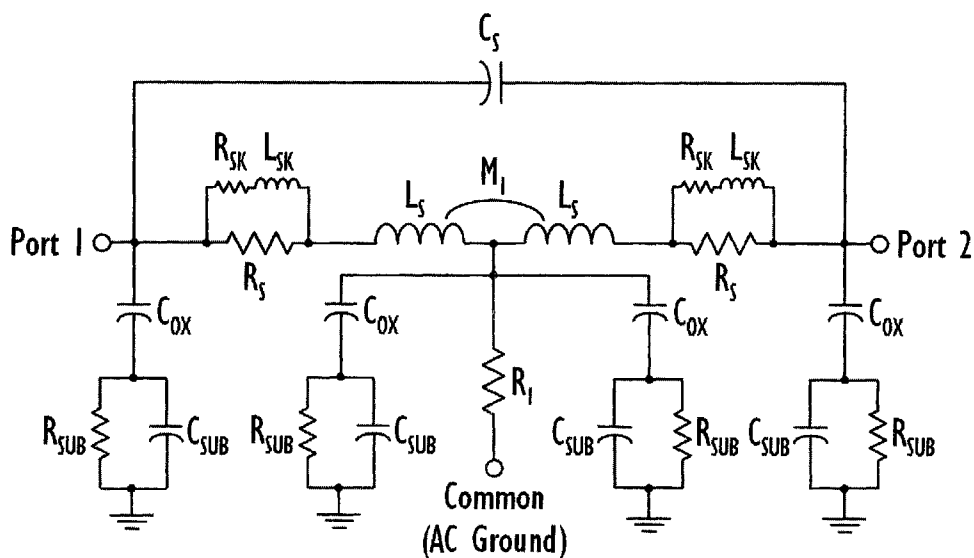


Figure 5.5 - SPICE-compatible RF sub-circuit model for differential inductor.

The model parameter extraction strategy for obtaining values of the elements in the differential inductor model is outlined in Figure 5.6. In this procedure, R_S , L_S and R_1 must be extracted first to ensure that subsequent model parameters obtained are physical and accurate. This is especially so for L_S because the measured L_{DIFF} is a contribution of both self-inductance from individual coil as well as mutual coupling effect from both spiral coils. As such, to accurately determine the amount of mutual coupling M_1 , it is essential to establish L_S first from the L versus frequency plot and then M_1 from L_{DIFF} plot. On the

other hand, elements such as R_{SK} and L_{SK} , which model the skin effects of metallization at giga-hertz frequencies, can be extracted focusing on the high frequency portion of Q_{DIFF} versus frequency plot. In contrast to techniques that model skin effects using resistive elements described by frequency-dependent equations, model developed using this approach to predict skin effects is compatible with SPICE simulators.

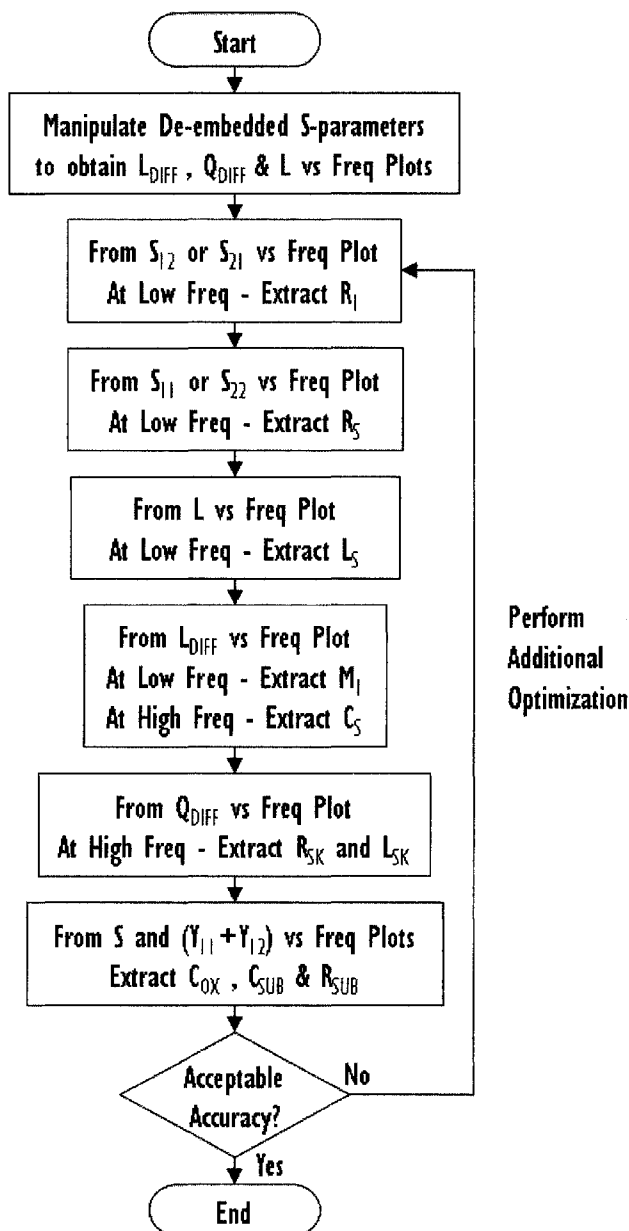


Figure 5.6 - Differential inductor RF model parameter extraction strategy.

With reference to Table 4.1, to extend this differential inductor model from 0.18 μm RFCMOS technology to advanced technological nodes such as the 65 nm technology, smaller model parameters R_s , R_{SK} , L_{SK} , L_s and R_l would have to be used for the same Device Design, Characterization and Modeling of Inductors and Interconnects for RFIC Applications — 148

inductor design because of thicker, lower resistive top copper metallization. With materials having lower dielectric constant as the IMD for copper interconnect technology, C_{OX} is also expected to be reduced. Similar to the symmetrical inductors in Chapter 4, the increase in top metal thickness and reduction in substrate resistivity is not likely going to have drastic change on M_1 , C_S , C_{SUB} and R_{SUB} .

The differential inductor model and its extraction methodology set forth in this work are both physical and simple to understand. Most published sub-circuit models are complex, lacking clear procedure for precise extraction of the mutual coupling coefficient M_1 [73] - [75]. Accurate determination of M_1 and L_S is very important especially for 1-turn differential inductors with small core diameters as they would have negative coupling coefficients for M_1 . Limited test structures with small physical design parameters variations are usually used to quantify model validity, accuracy and even scalability [75] - [76]. On the contrary, 120 inductors having wide-ranging physical design parameters, from 2-turn to 8-turn, width of 4 to 28 μm and diameter from 30 to 180 μm , are used to extensively test this methodology. It will be demonstrated in the following sections that this technique for accurate model parameter extraction results in trustworthy device models which will help establish good correlations between measured and simulated circuit behaviors.

5.4 Model Accuracy, Continuity and Design Trade-Offs

A “golden wafer” is selected based on the DC characteristics of back-end-of-line metallization for the development of this scalable differential inductor model. Full map on-wafer RF measurements with automated die alignment and wafer thickness corrections are performed on a differential inductor design to determine the “golden die”. Accurate die-to-die stepping and consistent “skating” of the RF probes on the test pads (to achieve good ohmic contact) are vital to ensure that deviations in the measured device characteristics across the wafer are predominantly due to process variations. Such full wafer map analysis assures that measurement data for all the differential inductors are obtained from a typical die and hence, device behavior associated with the 0.18 μm RFCMOS processing technology can be better represented by the RF model. This approach will prolong validity of the device models as processing technology matures over time.

With the proposed extraction strategy of Figure 5.6 and measurement data from a typical die, the sub-circuit elements in the scalable RF model are extracted using IC-CAP. These model parameters are then each formulated with empirical functions that best emulate (with the smallest error) their relationships with respect to the inductors’ turns, core diameter and width. As such, the RF model is valid only within the physical-design boundaries described by the 120 differential inductor test structures in the test element group. As an example, Figure 5.7 shows how well this model can match the measured L , L_{DIFF} and Q_{DIFF} for a 6-turn differential inductor with an inner diameter and width of 180 and 12 μm respectively. With the extraction methodology of first determining L_S using the L plot, M_1 is found to be 0.81 for this inductor when fitting L_{DIFF} at low frequency. As this model is scalable, its accuracy as well as continuity in predicting all test structures at popular application frequencies must be scrutinized carefully and 2.45 and 5.05 GHz are selected for this purpose. The box plot of Figure 5.8 indicates that majority of the useful

inductors in the test element group, that have yet to operate beyond their self-resonant frequencies, varied within -3 % to 4 % at 2.45 and 5.05 GHz respectively between the measured and simulated differential inductance. On the other hand, deviations in differential quality factor for the scalable model are observed to be within -4 % to 8 % at 2.45 and 5.05 GHz correspondingly. This differential inductor model has clearly demonstrated outstanding predictability and accuracy.

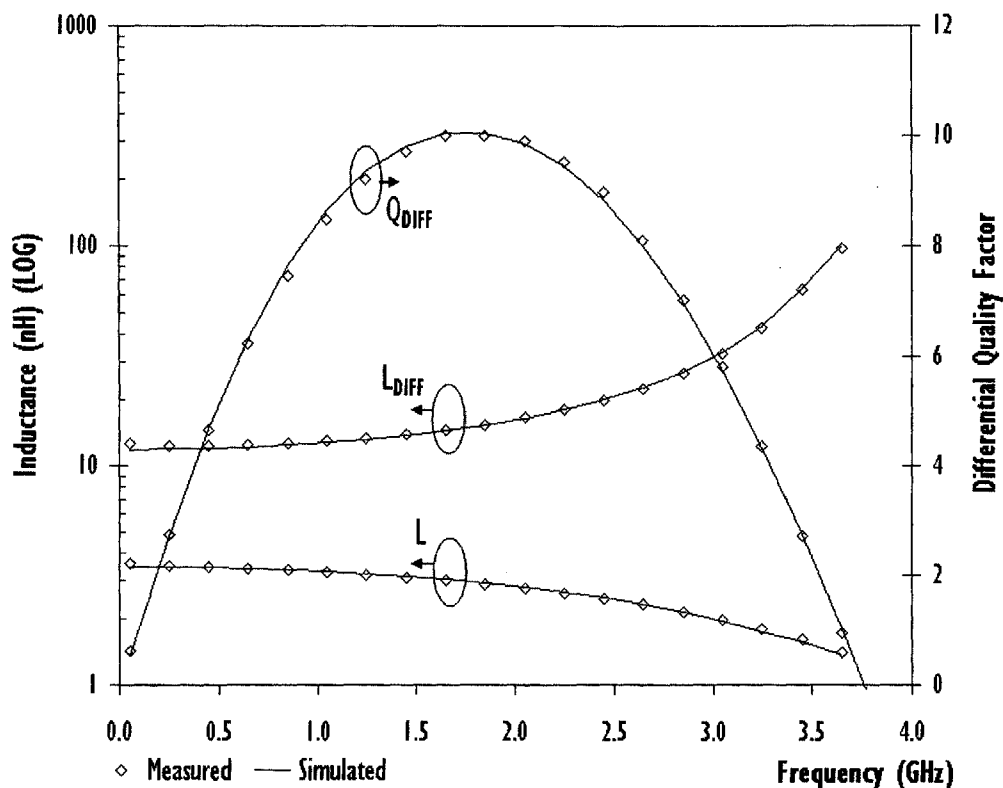


Figure 5.7 - Simulated versus measured inductance due to single-ended excitation, L , differential inductance L_{DIFF} and quality factor Q_{DIFF} for 6-turn differential inductor with core diameter and width of 180 and 12 μm respectively.

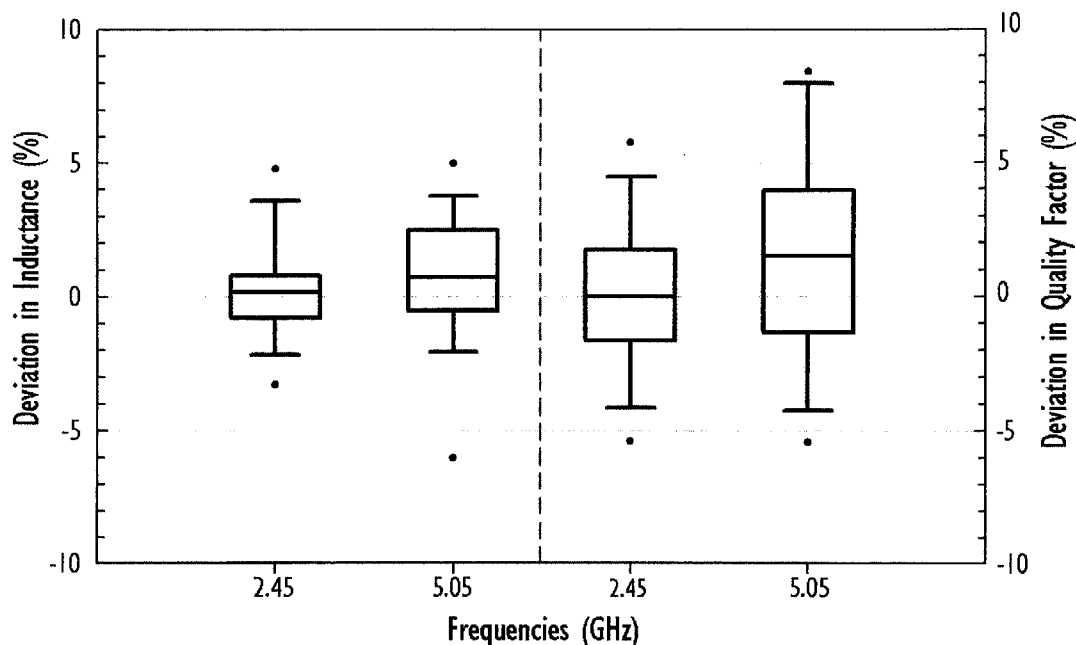


Figure 5.8 - Box plots showing deviations between SPICE model simulated and measured differential inductance and quality factor at 2.45 and 5.05 GHz for all inductors in the test element group.

3-dimensional plots of Figure 5.9 reveal that at 2.45 GHz, the scalable RF model is continuous within all the test structures having various turn, core diameter and conductor width. A huge device library with 5436 differential inductors can be derived from this scalable RF model if the core diameter and conductor width are swept in steps of 1 and 2 μm respectively. Excellent linear change in inductance has been observed for 2, 4 and 6-turn differential inductors when their core diameter increases from 30 to 180 μm . This reaffirms the fact that a library of inductors with fine inductance steps is achievable when the diameter is swept at 1 μm step. On the other hand, differential inductances for 8-turn inductors increase more abruptly because their self-resonant frequencies are close to 2.45 GHz. In fact, some of these inductors with diameters larger than 120 μm have already experienced self-resonance and are excluded from the plots shown in Figure 5.9(d).

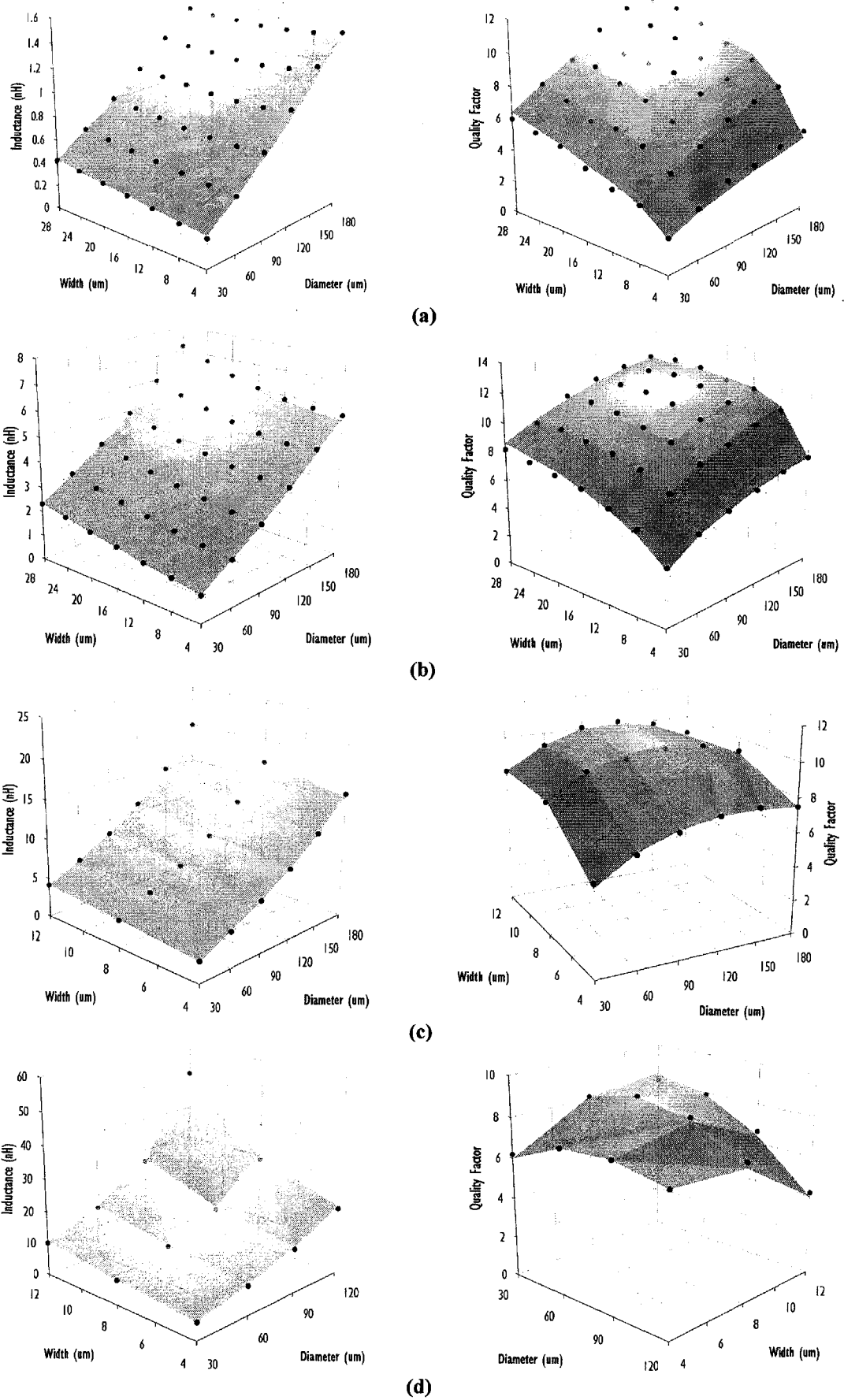


Figure 5.9 - RF differential inductor model continuity – simulated (surface) and measured (dots) differential inductance and quality factor versus diameter and width at 2.45 GHz for 2-turn (a), 4-turn (b), 6-turn (c), 8-turn (d) differential inductors.

In Figure 5.9, it is also apparent that as the conductor width widens, the differential inductance increases. This is because the overall conductor length of the inductor, which is a proportional function of width and core diameter, increases and results in larger self-inductance values. Nonetheless, the per unit length inductance of metal line is inversely proportional to its conductor width, i.e. the use of larger width leads to smaller per unit length inductance. Considering these 2 effects, to select the best width for a particular inductance value and application frequency, differential inductances for inductors of different width design must be identical to facilitate impartial performance comparisons since Q_{DIFF} is dependent on L_{DIFF} , metallization resistive loss as well as substrate losses.

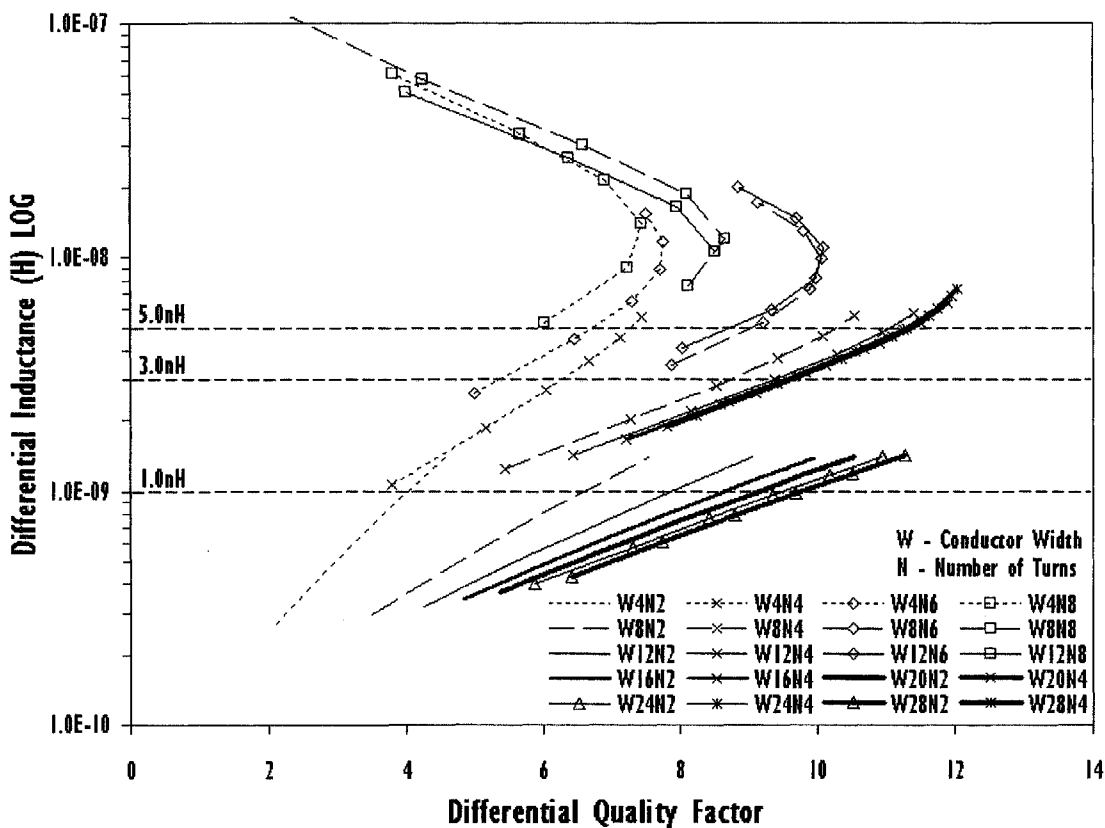


Figure 5.10 - Differential inductance versus quality factor at 2.45 GHz for all inductors in the test element group. As an example, w4n2 refers to 2-turn inductors with width of 4 μm .

For ease of understanding, the differential inductance versus quality factor plot (L_{DIFF} and Q_{DIFF} of all 120 differential inductors at 2.45 GHz) in Figure 5.10 is used for illustrations. On this graph, each of these plots represents a particular set of inductors in the test element group having diameters of 30, 60, 90, 120, 150 and 180 μm with the same number

of turn and width. Iso-inductance lines, 1, 3 and 5 nH are drawn to evaluate effects of conductor width on the performance of differential inductors. Similar to the symmetrical inductors (Section 4.4), these iso-inductance lines narrow down the range of diameter values, allowing efficient linear interpolations of core diameter (in 1 μm steps) to obtain inductors of different widths having identical inductance values at 2.45 GHz. Such interpolation and evaluation are only made possible with an accurate and scalable model.

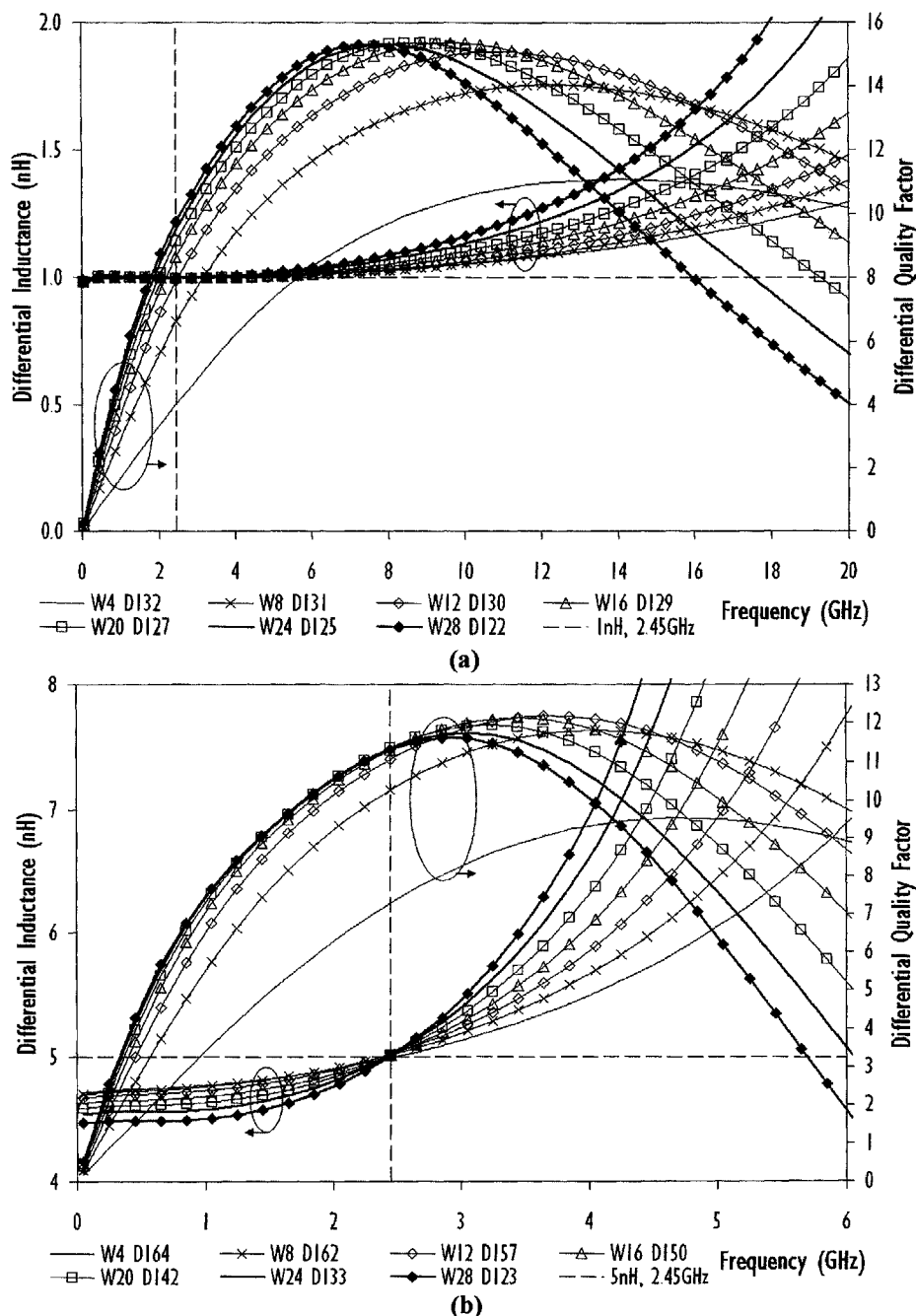


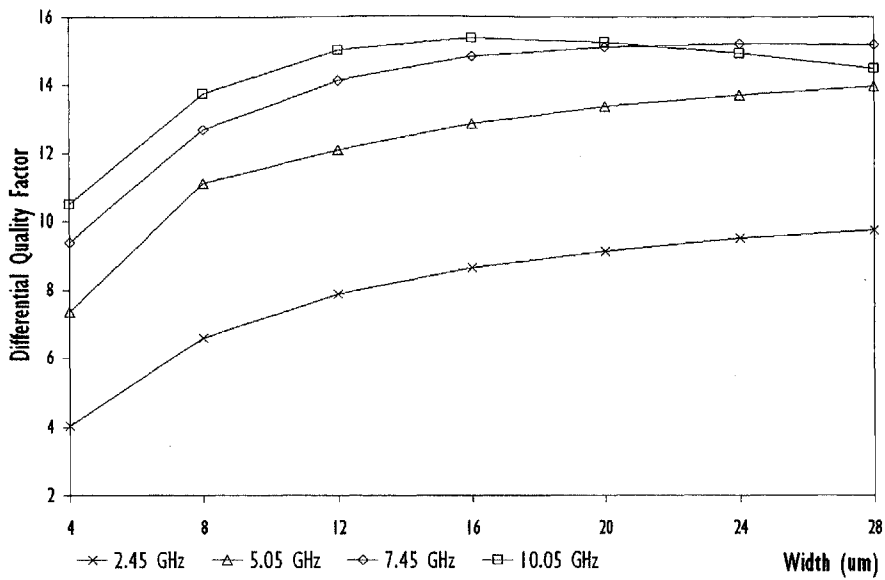
Figure 5.11 - Differential inductance and quality factor versus frequency for 1.0 nH (a) and 5.0 nH (b) differential inductors at 2.45 GHz. In the legend, for example, W4 D132 refers to inductor with 4 μm width and diameter of 132 μm .

Figure 5.11 shows the differential inductance and Q-factor versus frequency plots for 1 and 5 nH inductors at 2.45 GHz. From these 2 graphs, varying and optimizing the core diameters in 1 μm steps indeed allow inductors of different conductor widths to have identical inductance values and hence, non-biased performance comparisons. The overall conductor lengths for 1 nH inductors with widths of 4, 8, 12, 16, 20, 24 and 28 μm are evaluated to be 1004, 1092, 1180, 1269, 1351, 1433 and 1508 μm respectively, reiterating the fact that the per unit length inductance of metal line is inversely proportional to its conductor width. On the other hand, 5 nH differential inductors with widths larger than 12 μm are designed to have smaller low-frequency inductances, taking into considerations self-resonance and substrate loss effects to ensure that they would have exactly 5 nH at 2.45 GHz, making fair device performance comparisons possible. This is the first time such experimental studies and comparisons for differential inductor at frequencies of more than 2 GHz, are performed through the use of an accurate scalable differential inductor model.

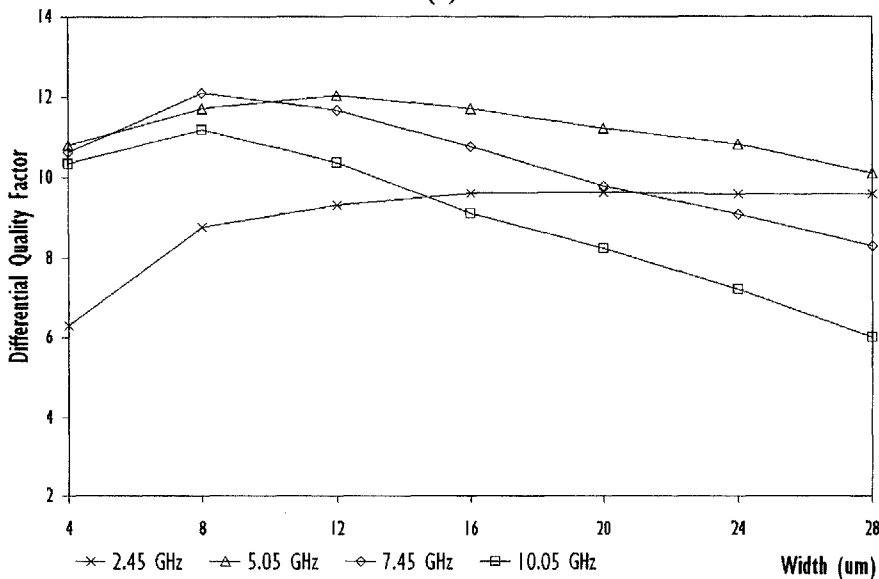
Figure 5.11 concludes that at 2.45 GHz, wider conductor width for differential inductors reduces the resistive loss at low frequencies, thereby improving Q_{DIFF} . Although implementing such design approach trade-off substantial chip area for better device performance, an optimal width exists beyond which any further use of larger width and silicon real estate would renders this technique ineffective. To demonstrate this, conductor width of 16 μm instead of 4 μm for 1 nH inductors is used. The Q_{DIFF} is noted to improve significantly from 4.0 to 8.7 (115 %), with a corresponding 73 % increase in the device size. However, an increase in width from 4 to 28 μm leads to a 142 % Q_{DIFF} improvement but expands the inductor overall size enormously by more than 158 %. For 1 nH inductors, the optimal width at 2.45 GHz is therefore 16 μm and that for 5 nH inductors is determined to be 12 μm . Large-inductance inductors generally require huge total conductor length and therefore, a sizeable chip area is necessary to generate the

required self inductance. Employing narrower conductor width and thus shorter total conductor length (narrow width conductor have larger per unit length inductance) attractively results in smaller inductor size, lower substrate loss and better device performance.

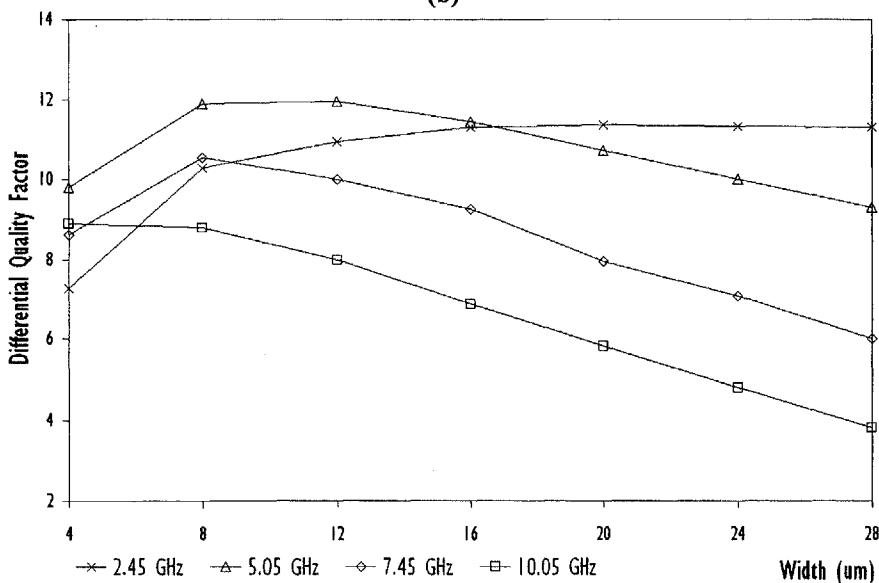
1, 3 and 5 nH iso-inductance lines for frequencies of 5.05, 7.45 and 10.05 GHz were constructed to ensure that the inductors with identical inductance values are compared. Plots of differential quality factor at these frequencies versus conductor width are consolidated in Figure 5.12. For small-inductance differential inductors, large conductor width improves Q_{DIFF} tremendously, apparent for 1 nH inductors up to 10.05 GHz. Such phenomenon as explained earlier on is attributed to the reduction in resistive loss at the expense of chip area, which for these small inductors, do not significantly degrade their high frequency performance since their overall conductor lengths are still relatively short. Meanwhile, as the differential inductance increases, the device size required for generating the required inductance values also gets larger. In this scenario, especially at the higher operating frequencies, trade-offs between resistive and substrate loss results in the existence of optimal widths such that beyond these widths, any further use of larger conductor width do not improve Q_{DIFF} but waste expensive silicon area. This is evident for 5 nH inductors in Figure 5.12(c) which show degradations in Q_{DIFF} for operating frequencies of 5.05, 7.45 and 10.05 GHz when conductor width of more than 8 μm is used. Plots in Figure 5.12 has shown that an optimal width exists which allows for trade-offs between the performance and device size.



(a)



(b)



(c)

Figure 5.12 - Differential quality factor versus conductor width for 1.0 nH (a), 3.0 nH (b) and 5.0 nH (c) differential inductors at various operating frequencies of 2.45, 5.05, 7.45 and 10.05 GHz.

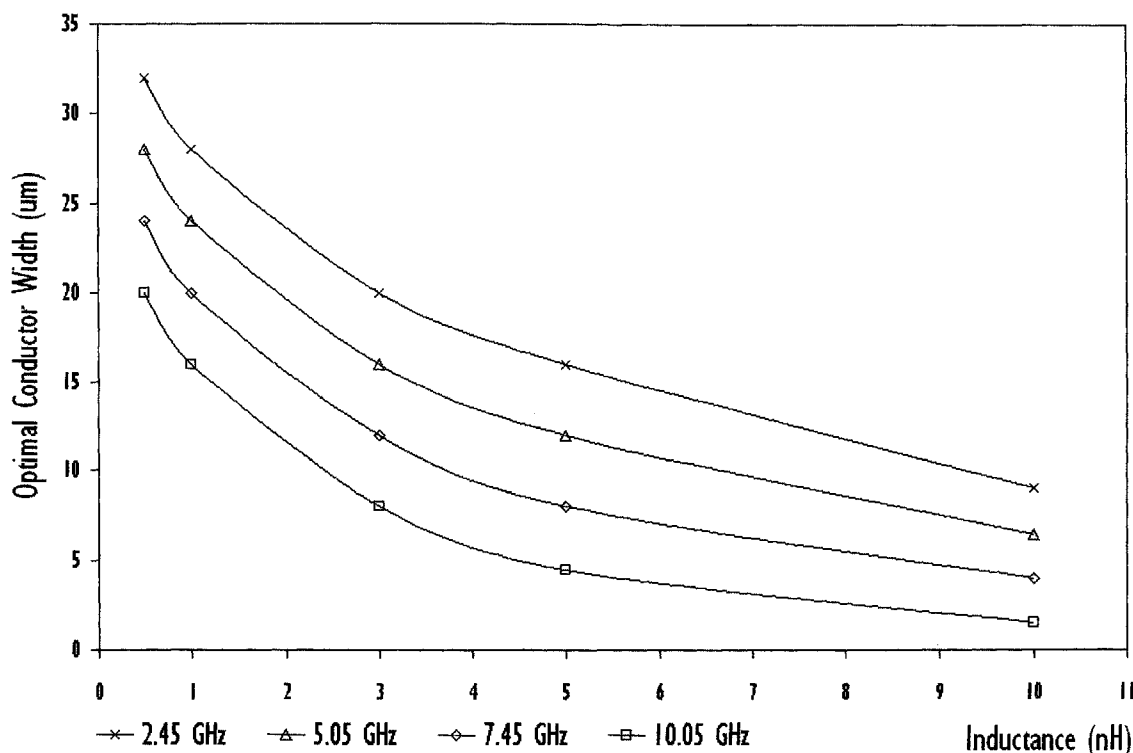


Figure 5.13 - Optimal conductor width (for high Q_{DIFF}) versus differential inductance at operating frequencies of 2.45, 5.05, 7.45 and 10.05 GHz. Width of 2 and 32 μm are extrapolated for plots of 10.05 and 2.45 GHz respectively.

If characteristics of the differential inductors in Figure 5.12 are summarized in Figure 5.13, describing the optimal widths versus inductance values at various operating frequencies, an interesting observation can be made. As inductance values or operating frequency increase, optimal conductor widths for differential inductors have to be smaller. Using narrow conductor width not only improves device performance but reduces the required total conductor length and thus overall device size of the inductor, significantly decreasing the development and production costs for silicon-based RFICs. Figure 5.14 compares the optimal width between single-ended spiral inductors in Chapter 3 and the differential inductors in this chapter at 2.45 GHz through normalization of the differential inductance ($L_{DIFF}/2$). At the same inductance value, differential inductors has huge advantage of requiring 30 % smaller optimal conductor width compared to conventional spiral inductors, suggesting further device size reduction when utilizing and optimizing differential inductors for RF circuits. Results in this section also highlighted the

possibilities of building device libraries with application-specific differential inductors having optimized layouts which will save model development time and test chip cost. However, such device libraries might not cater for circumstances in which designers are willing to compromise on having poorer circuit performance for a smaller chip size.

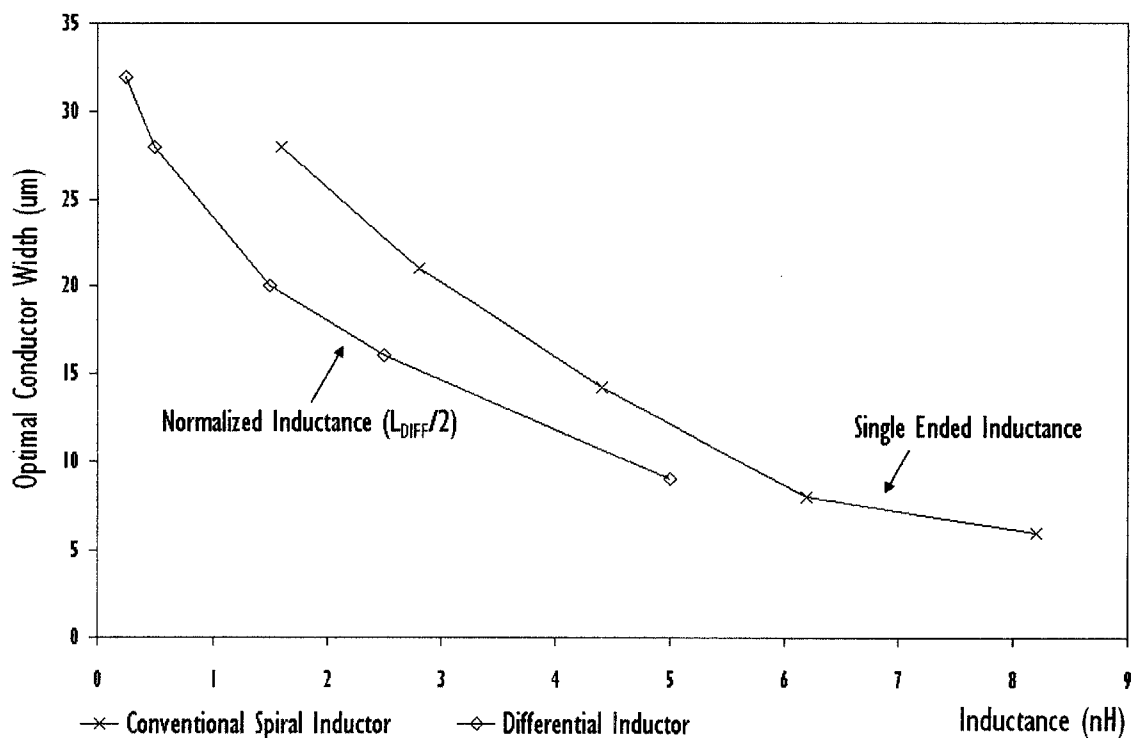


Figure 5.14 - Comparing optimal conductor width (for high quality factor) between differential and single ended spiral inductors (Chapter 3, Figure 3.23a) versus normalized inductance at 2.45 GHz.

5.5 Models Verification using Differential Giga-Hertz Amplifier

Accuracies and reliabilities of both the scalable symmetrical and differential inductor models are evaluated using a 2.4 GHz amplifier with an expected gain of about 15 dB in the same 0.18 μm RFCMOS technology. Circuit schematic of the differential amplifier for correlation studies between measured and simulated circuit characteristics is shown in Figure 5.15. Adopting inductive source degeneration input matching technique, gate-to-source capacitance of the input transistor T_1 is matched to the external 50 ohm system at 2.4 GHz with L_1 , L_2 and C_1 . V_{BIAS} provides the gate biasing to T_1 and R_1 isolates the RF input signal. T_2 and T_3 make up the second stage differential transistor pair with C_2 and C_5 as the DC blocking and AC grounding capacitors respectively. Differential inductor L_3 , together with C_3 and C_4 provides 50 ohm load matching at the output ports. Optimal conductor widths have been selected for L_1 , L_2 and L_3 , after evaluating design trade-offs between size and quality factor performance of the inductors at 2.4 GHz.

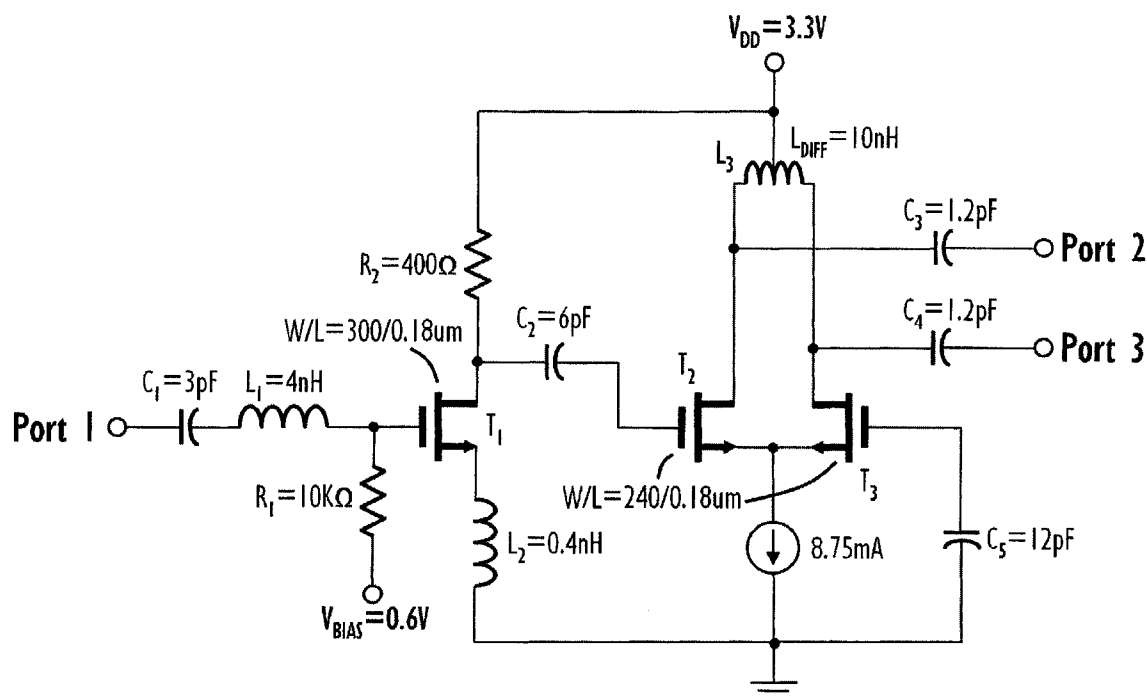


Figure 5.15 - Circuit schematic of a 2.4 GHz single-ended-to-differential amplifier with differential Inductor.

Pad capacitances have been taken into account during circuit simulations and hence, pad parasitic de-embedding is not required. RF interconnect model, which will be discussed in Chapter 6, is utilized to evaluate and tackle the post-layout effects contributed by metal interconnects routed between devices. Typical dies for circuit tests are selected based on full wafer map device characteristics obtained from RF scribe-line process monitoring test [57]. Cascade Microtech Dual Infinity GSSG probes, Agilent 4-Port Performance Network Analyzer (PNA) and hybrid calibration technique [77] are used for performing the on-wafer circuit characterization. Source power selection of -17 dBm on the network analyzer ensures that the differential amplifier is in the linear mode of operation. Die photo depicting the differential amplifier is shown in Figure 5.16(a). Figure 5.17 shows the simulated versus measured 3-port S-parameters of the amplifier. Acceptable circuit predictions of measured matching characteristics have been achieved at all input and output ports. At 2.4 GHz, a maximum error of 1.39 dB is observed between the measured and simulated S_{11} , S_{22} and S_{33} . Deviations for gain predictions at 2.4 GHz are kept within 2.7 % for both S_{21} and S_{31} . Excellent correlations between measured and simulated amplifier characteristics endorse the reliability, scalability and accuracy of the symmetrical and differential inductor models in this research work.

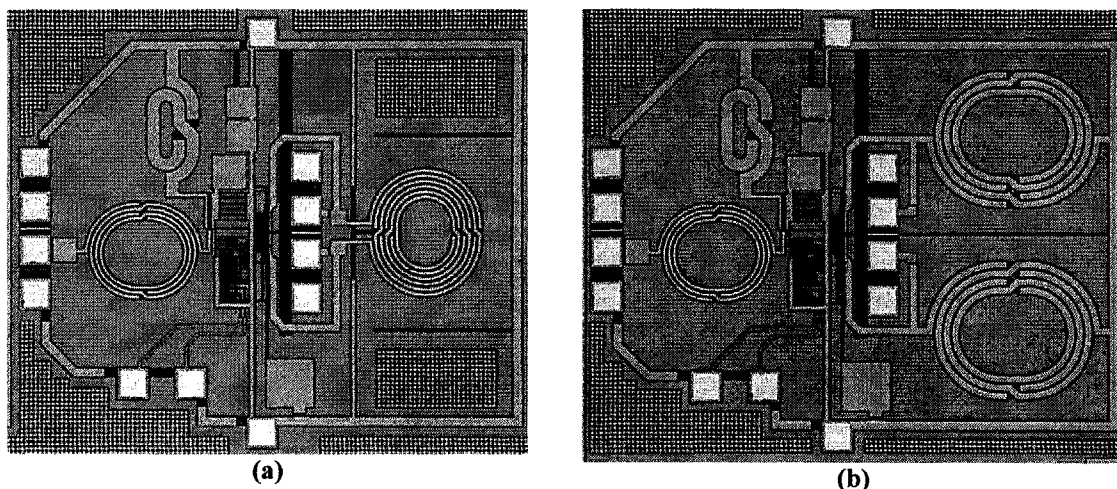


Figure 5.16 - Die photos showing on-wafer multi-port RF circuit measurements of differential amplifiers with differential inductor (a) and symmetrical spiral Inductors (b) using Cascade Microtech Infinity GSSG probes.

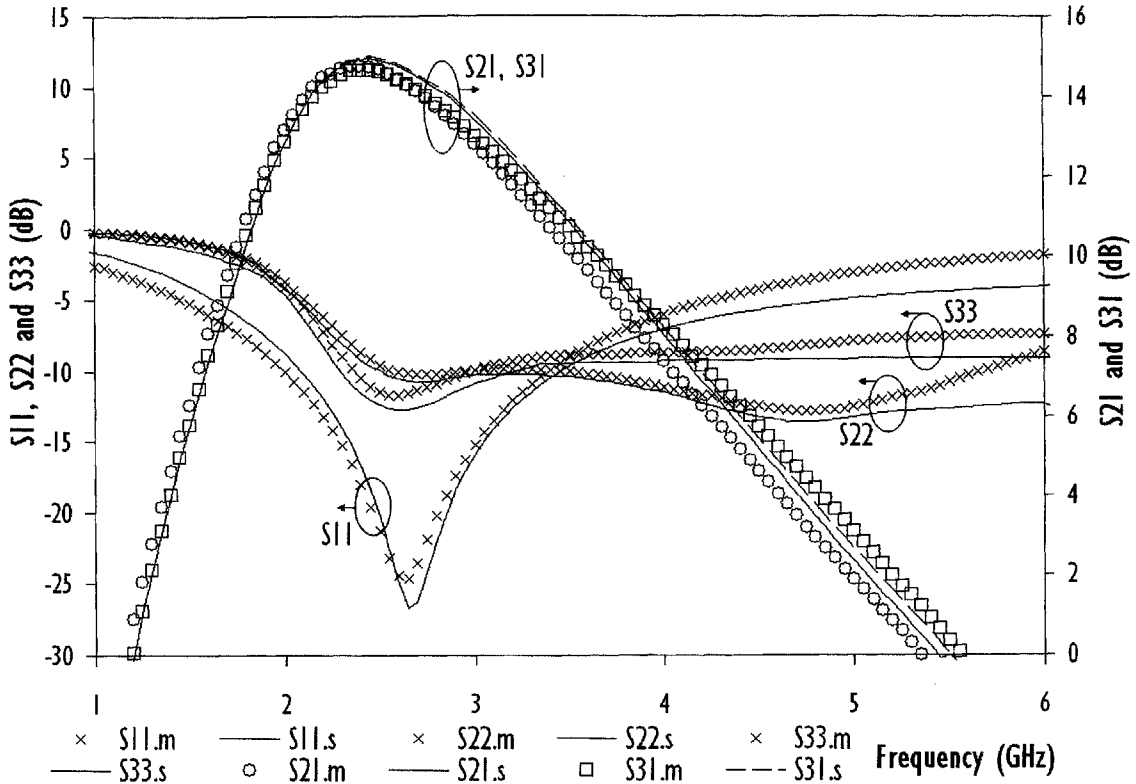


Figure 5.17 - Simulated (.s) and measured (.m) 3-Port S-parameters versus frequency characteristics for giga-hertz amplifier with differential inductor.

Figure 5.16(b) shows the die photo of a differential amplifier with two 5 nH symmetrical spiral inductors as output matching inductors instead of the differential inductor. Performance comparisons of measured mixed-mode S-parameters for the 2 differential amplifiers (Figure 5.16) are shown in Figure 5.18. Figure of merits used for benchmarking the 2 amplifiers in this experiment are S_{DS21} , S_{CS21} and CMRR, and they refer to the differential mode to single-ended gain, common mode to single-ended gain and common mode rejection ratio respectively, defined according to the following equations [78], [79]:

$$S_{DS21} = \frac{S_{21} - S_{31}}{\sqrt{2}} \tag{5.6}$$

$$S_{CS21} = \frac{S_{21} + S_{31}}{\sqrt{2}} \tag{5.7}$$

$$CMRR = \frac{S_{DS21}}{S_{CS21}} \tag{5.8}$$

Comparing performance of the two amplifiers, differential inductor clearly offers more advantages than the symmetrical spiral inductors. It has allowed an area reduction of more than 20 % in silicon real estate for the entire amplifier layout. In addition, larger differential mode to single-ended gain of more than 2 dB over the entire frequency spectrum and superior common mode rejection ratio of 13.5 dB at 2.4 GHz have both been observed for the amplifier with differential inductor as shown in Figure 5.18. On-wafer high frequency noise characterization also revealed that the use of differential inductor reduces noise figure of the amplifier, NF_{50} at 2.4 GHz from 3.43 to 2.85 dB. Huge improvements in circuit performance can be attributed to two main reasons: better AC grounding and higher quality factor for differential inductors. Layout of differential inductor promotes substantial amount of inductive mutual coupling. As such, the required total conductor length for differential inductor as compared to using two symmetrical spiral inductors for generating the same amount of inductance is much shorter, resulting in smaller resistive loss and higher quality factor, thereby translating to circuit level improvements in terms of better gain and noise performance.

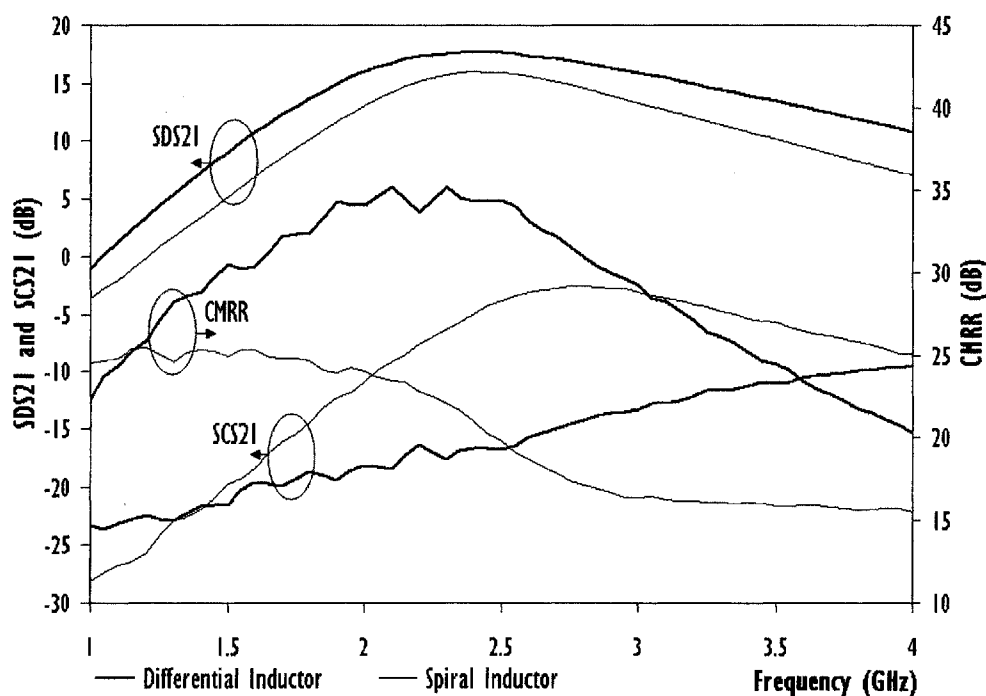


Figure 5.18 - Comparing measured performance of giga-hertz amplifiers using differential inductor and symmetrical spiral inductor as the output matching load inductor.

5.6 Comparing Research Works on Modeling Differential Inductors

Table 5.1 compares five other key research studies, which were published recently in internationally recognized conferences and journals, as an evaluation of the research contributions for this work. In contrast to most other research papers, more than one hundred test structures are designed in a single testchip and used to develop this differential inductor model. Although this research employs the second largest number of test structures for model development, the inductor model published by V. Blaschke [80] has a much larger model error of $\pm 20\%$ for differential quality factor. This work, on the other hand, achieves excellent model deviations for differential inductance and Q-factor of -3 to 4% and -4 to 8% respectively.

Most other research works do not design and fabricate RF circuits to verify their differential inductor model. In E. Ragonese's research paper [81], a down-converter circuit was used to verify the validity of their proposed model but huge errors of about ± 10 dB are observed when predicting the image rejection ratio of the down-converter. For this work, the differential inductor model accurately predicted the gain (2.7% error) and port matching characteristics (1.39 dB error) of a single-ended to differential output RF amplifier. The highly accurate and scalable differential inductor model was also used in ground-breaking trade-off studies between the inductor layout and its performance up to 10 GHz. It has also, for the first time, quantitatively compares the performance of differential inductors to those of the conventional spiral inductors.

Table 5.1 - Comparing various research works on modeling and optimizing the design of differential spiral inductors.

Author	Y. Z. Xiong	E. Ragonese	V. Blaschke	L. Zhang	J. Chen	This Work
Reference	[82]	[81]	[80]	[83]	[84]	
Journal/ Conference	IEEE TED	IEEE BCTM	IEEE CICC	IEEE EDSC	IEEE TED	IEEE TED
Year of Publication	2005	2006	2006	2007	2007	2008
Number of test structures used for model development.	3	4	166	17	1	120 (refer to Section 5.3)
How many elements are in the proposed model?	19	14	31	18	12+S×10 (S=no. of Segments in the inductor. Therefore, each inductor will have a different model)	23 (10 elements have to be extracted)
Is the extraction methodology published?	Yes	No	Yes	Yes	Yes	Yes
Is there a methodology to separate self and mutual inductance associated with the two coils?	Not published	No	No (Mutual coupling coefficient was not extracted from measurement data)	No (Mutual coupling coefficient was not extracted from measurement data)	No (Mutual coupling coefficient was not extracted from measurement data)	Yes (Section 5.2 outlined a methodology to handle this)
What is the operating frequency supported by the model?	10 GHz	20 GHz	20 GHz	8.5 GHz	10 GHz	10 GHz (or Self-resonant, whichever is lower)
What is the model error/deviation?	Not published	$L_{DIFF} : 7\%$ $Q_{DIFF} : 12\%$	$Q_{DIFF} : \pm 20\%$	9 % error for S-parameters	Not published	$L_{DIFF} : -3$ to 4% $Q_{DIFF} : -4$ to 8% (For all inductors at 2.45 and 5.05 GHz)
Is the model scalable to the inductor physical design parameters?	Only 3 inductors are presented in the paper	Only 4 inductors are presented in the paper	Not published	Only 17 inductors are presented in the paper	Only 1 inductors are presented in the paper	Yes (120 inductors, Scalable with Turns, Width, Diameter)
How is the performance of the model continuity?	Not published	Not published	Not published	Not published	Not published	Excellent (Model is continuous Figure 5.9)
Is the model SPICE- compatible?	Yes	Yes	Yes	Yes	Yes	Yes
Trade-off studies between performance, layout and operating frequency at same inductance value?	No	No	No	No	No	Yes (Recommended the optimal widths for different inductance values up to 10 GHz Figure 5.12)
Has the model been verified in test circuits?	No	Yes (Down- converter is used)	No	No	No	Yes (Amplifier was used, Results in Section 5.5)

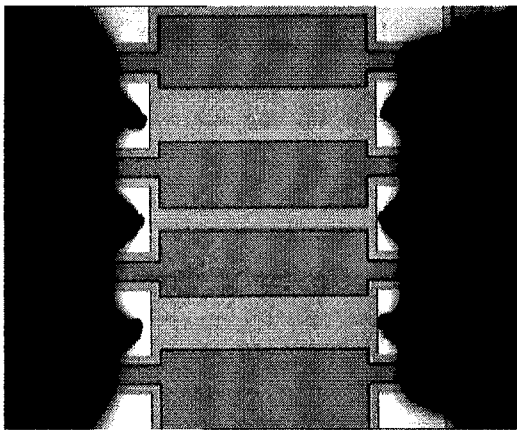
Chapter 6 - Accurate and Scalable RF Interconnect Model

6.1 Design of Test Structures and Experimental Setup

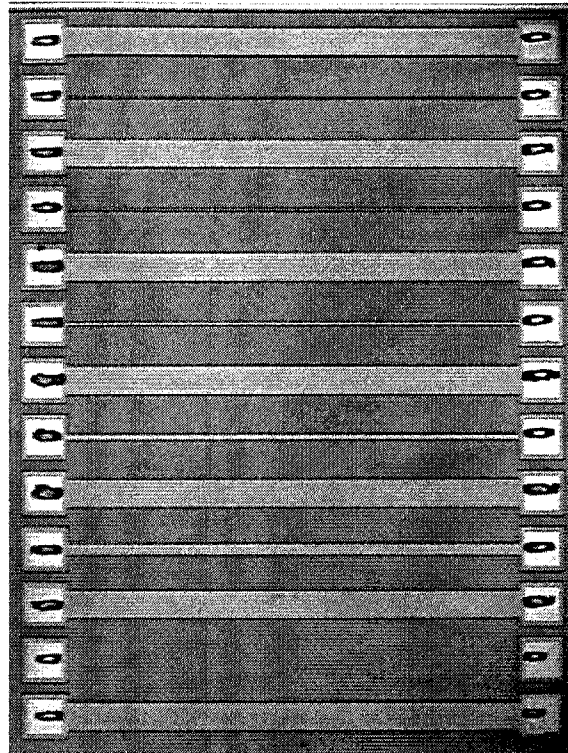
In this chapter, an accurate and scalable RF interconnect model is presented to understand and predict the degradation effects of interconnects on actual fabricated RF circuits. This sub-circuit model is developed using a streamlined set of 25 top metal (Metal 6) interconnect test structures designed with lengths of 50, 100, 200, 400 and 800 μm and widths of 1.5, 3, 5, 10 and 20 μm respectively. The test structures are fabricated using the same 0.18 μm RFCMOS processing technology. On-wafer RF device measurements are carried out using Agilent 8510C Vector Network Analyzer and Cascade Microtech RF Infinity probes. This work focuses on top metal layer because of the following reasons:

1. They have the largest metal thickness and therefore offer the lowest parasitic resistance and inductance.
2. They are furthest away from the silicon substrate and hence have the lowest substrate losses.

The wafer and RF probes are shielded within the Micro-chamber of Cascade Microtech 300 mm semi-automated probe station throughout the measurements. Two-port S-parameters of the interconnects are extracted over the frequency range from 50 MHz to 10.05 GHz. Substrate taps near the top metal lines are included in all ground pads of the 6-pad GSG configuration to ensure that the substrate is effectively grounded. To facilitate de-embedding of pad capacitance without the interconnect lines, open calibration structures are fabricated next to the device. Parasitics of the test pads are accurately de-embedded by subtracting Y-parameters of the open calibration structures from those test structures with the interconnects outlined in Section 2.3.4.1. Figure 6.1 shows die photos taken in the course of characterizing the interconnect test structures.



(a)



(b)

Figure 6.1 - Die -photos showing on-wafer RF characterization of interconnects. (a) Interconnect test structure with Cascade Microtech RF Infinity probes. (b) Interconnects 800 μm in length with different widths and open calibration structure.

6.2 Proposed Figure of Merit for RF Interconnects

To quantify the detrimental effects of interconnects on circuit performances, this research work has made pioneering attempts to define figure of merits which are useful to circuit designers when they decide on the interconnect dimensions for their RF circuits. The interconnect's figure of merits, parasitic inductance (L) and intrinsic factor (I_F) adopted for this research work are derived from the de-embedded Y-parameters in the following discussions. Although interconnects are not magnetic energy storage elements, they do possess non-negligible self-inductance at radio frequencies and hence can be regarded as on-chip inductors and their parasitic inductance, L (units in Henry) can also be evaluated using Equation 3.1.

Proceeding in this direction, the Q-factor shown in Equation 3.2 for an inductor, can also be used to correlate how interconnects would influence the circuit performance. L and Q are both extracted from Y_{11} and not Y_{12} parameter since it is important to include and consider the effects of the lossy silicon substrate when evaluating the performance of interconnects. Examining Equation 3.2, the Q-factor is defined as a ratio of imaginary[Y_{11}] over real[Y_{11}]. This suggests that at a fixed resistive loss, when the inductance increases, the Q-factor increases. However, for the case of interconnects, desirably low loss metallization should possess negligible parasitic inductance and resistance. In this work, for radio frequencies applications, a more suitable figure of merit to describe interconnects, Intrinsic Factor, I_F (units in S^2 , for frequency > 0), is proposed for the first time as follows:

$$I_F = \frac{1}{\text{Im ag} \left[\frac{1}{Y_{11}} \right] \times \text{Real} \left[\frac{1}{Y_{11}} \right]} \quad (6.1)$$

From Equation 6.1, interconnects with large intrinsic factors insinuate that they have small resistive and inductive parasitics. On the contrary, parasitic series resistance, R associated

with the metallization is extracted from Y_{12} parameter as shown in Equation 3.3 to show the skin effects of metallization at radio frequencies.

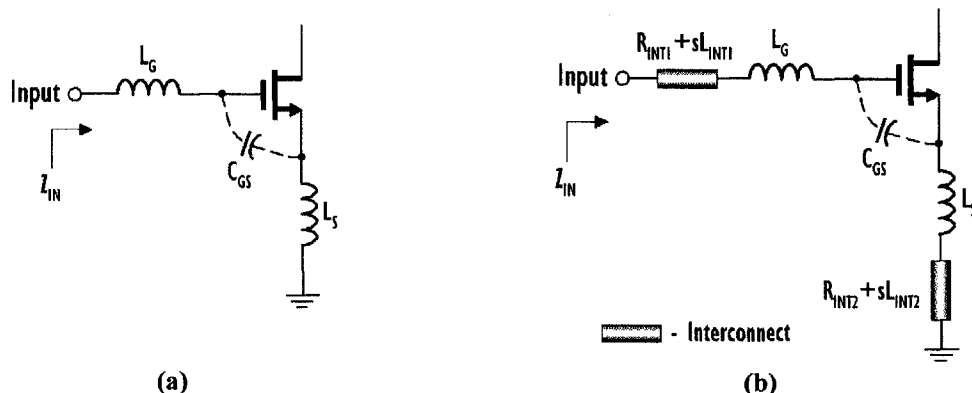


Figure 6.2 - Inductive source degeneration impedance matching without (a) and with (b) consideration of interconnect metallization.

Schematics in Figure 6.2 help illustrate with an inductive source degeneration impedance matching example, on how I_F can be utilized as a performance indicator for interconnects. Figure 6.2 (a) shows the ideal input matching circuit with lossless inductors, L_S and L_G providing optimal matching for the nMOSFET which only its transconductance and gate-source capacitance are considered [85] in the following discussions. As such, the input impedance Z_{IN} can be expressed as,

$$Z_{IN} = s(L_G + L_S) + \frac{1}{sC_{GS}} + \left(\frac{g_m}{C_{GS}} \right) L_S \tag{6.2}$$

where g_m is the transconductance of the nMOSFET, C_{GS} is the gate-source capacitance of the nMOSFET and $s = j*2\pi*$ frequency

For maximum power transfer to occur at the operating frequency, real $[Z_{IN}]$ have to match the source resistance, R_{SOURCE} , which is typically 50 ohm,

$$\left(\frac{g_m}{C_{GS}} \right) L_S = R_{SOURCE} \tag{6.3}$$

and the imaginary impedances must satisfy the following condition,

$$(L_G + L_S) = \frac{1}{C_{GS}} \quad (6.4)$$

From Equations 6.3 and 6.4, values of L_S and L_G are first determined so that the ideal impedance matching criteria can be fulfilled. In schematic design phase, effects from the interconnect structures required to provide necessary electrical continuity between devices are still not known and hence not taken into account. If say after the chip layout, their resistive and inductive parasitics are considered in the example of Figure 6.2(b), the new input impedance Z_{IN} can be formulated as,

$$Z_{IN} = s(L_G + L_S) + s(L_{INT1} + L_{INT2}) + \frac{1}{sC_{GS}} + \left(\frac{g_m}{sC_{GS}} \right) R_{INT2} + R_{INT1} + R_{INT2} + \left(\frac{g_m}{C_{GS}} \right) (L_S + L_{INT2}) \quad (6.5)$$

For impedance matching at the operating frequency, real $[Z_{IN}]$ will have to match to the source resistance,

$$R_{INT1} + R_{INT2} + \left(\frac{g_m}{C_{GS}} \right) (L_S + L_{INT2}) = R_{SOURCE} \quad (6.6)$$

and the imaginary impedance will have to satisfy the new condition:

$$(L_G + L_S) + (L_{INT1} + L_{INT2}) = \frac{1}{C_{GS}} + \left(\frac{g_m}{C_{GS}} \right) R_{INT2} \quad (6.7)$$

To achieve maximum power transfer, real $[Z_{IN}]$ must be matched to the source resistance but evaluating Equations 6.3 and 6.6 reveal that additional components of $(R_{INT1} + R_{INT2})$ and $L_{INT2} * (g_m/C_{GS})$ have impeded the performance of the original matching inductor, L_S . Comparing Equations 6.4 and 6.7, the resonant frequency of the impedance matching network differs by the extra components of $(L_{INT1} + L_{INT2})$ and $R_{INT2} * (g_m/C_{GS})$. These parasitic components from the interconnects contribute to unfavorable shifts in the frequency response of the circuit as opposed to when it was previously optimized with L_S

and L_G which excluded effects from the interconnects. Therefore, without prior knowledge of the parasitic resistances and inductances introduced by the interconnects, operating frequency in this narrow-band RFCMOS design is altered and power is not transferred efficiently into the nMOSFET. If both interconnects in Figure 6.2(b) are identical, i.e. $R_{INT1}=R_{INT2}=R_{INT}$ and $L_{INT1}=L_{INT2}=L_{INT}$, Equations 6.6 and 6.7 simplify to

$$2R_{INT} + \left(\frac{g_m}{C_{GS}} \right) (L_s + L_{INT}) = R_{SOURCE} \quad (6.8)$$

$$(L_G + L_s) + (2L_{INT}) = \frac{1}{C_{GS}} + \left(\frac{g_m}{C_{GS}} \right) R_{INT} \quad (6.9)$$

Using interconnects with large I_F will have less significant impact on circuit performances. In this example, for the interconnects shown in Figure 6.2, without having any shunt parasitic capacitances, from Equation 6.1, I_F can be extracted from Y_{12} parameters and therefore written as,

$$\begin{aligned} I_F &= \frac{1}{\text{Imag} \left[\frac{1}{Y_{12}} \right] \times \text{Real} \left[\frac{1}{Y_{12}} \right]} \\ &= \frac{1}{2 * \pi * \text{Frequency} \times L_{INT} \times R_{INT}} \end{aligned} \quad (6.10)$$

In Equation 6.10, when I_F is very large, it suggests that both R_{INT} and L_{INT} are negligibly small and hence, Equations 6.8 and 6.9 tends to the original matching conditions described in Equations 6.3 and 6.4,

$$\begin{aligned} 2R_{INT} + \left(\frac{g_m}{C_{GS}} \right) (L_s + L_{INT}) &\rightarrow \left(\frac{g_m}{C_{GS}} \right) L_s \text{ and} \\ (L_G + L_s) + (2L_{INT}) = \frac{1}{C_{GS}} + \left(\frac{g_m}{C_{GS}} \right) R_{INT} &\rightarrow (L_G + L_s) = \frac{1}{C_{GS}} \end{aligned}$$

Therefore, choosing high I_F interconnects allow fabricated circuits to have smaller frequency shifts and minimal degradation on the transfer of power previously optimized in

circuit schematic simulations when interconnects are not taken into considerations. Monitoring the parasitic resistance, inductance and capacitive substrate loss i.e. real and imaginary impedances individually is cumbersome and exploiting the proposed I_F provides a quick benchmarking indicator for circuit designers. More importantly, having accurate and scalable interconnect models which are SPICE-simulator compatible allow circuit designers to take evasive actions before product fabrication if post layout simulations reveal that additional metallization causes circuits to perform out of specifications.

6.3 Proposed Sub-circuit Model for RF Interconnects

The proposed scalable double- π RF sub-circuit model for RF interconnects is shown in Figure 6.3. L_S and R_S describe the parasitic self-inductance and resistive loss on the metallization respectively. L_{SK} and R_{SK} model the skin effects of the metallization at radio frequencies. Substrate loss for interconnect is modeled by the RC network that consists of C_{OX} , C_{SUB} and R_{SUB} . These 3 elements describe the oxide capacitance between the silicon substrate and metallization, the capacitive and resistive losses in the silicon substrate respectively.

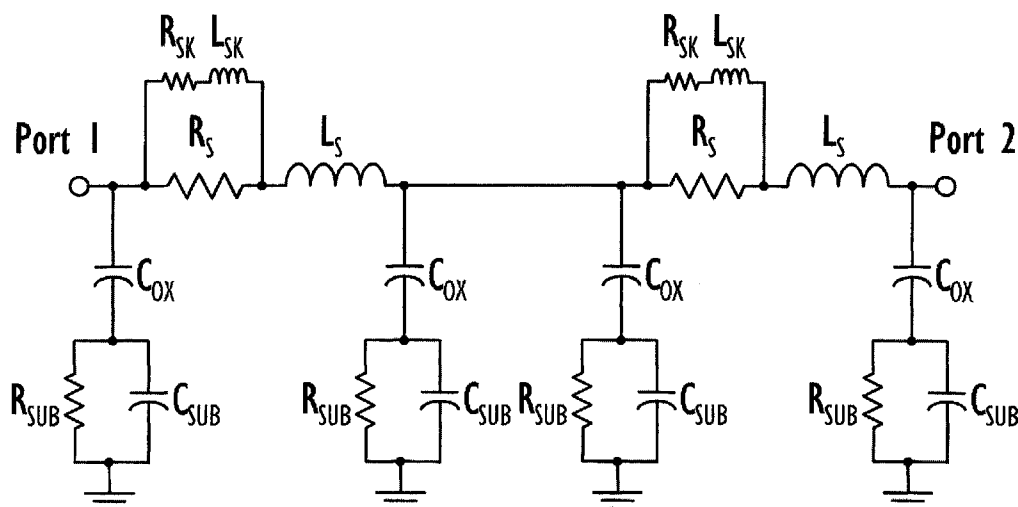


Figure 6.3 - Double- π RF sub-circuit model for interconnects.

Although the proposed double- π model is complicated with numerous RLC elements, this model is symmetrical and values for the model parameters are identical for the two π

networks. Figure 6.4 illustrates a flowchart that summarizes the extraction procedure for this double- π model. It is important to emphasize that the double- π model is SPICE-simulator compatible and does not contain any model elements, especially resistors, whose behaviors are modeled by frequency-dependent functions or equations. Such approach of modeling the inductors is currently not supported in commercial SPICE circuit simulators.

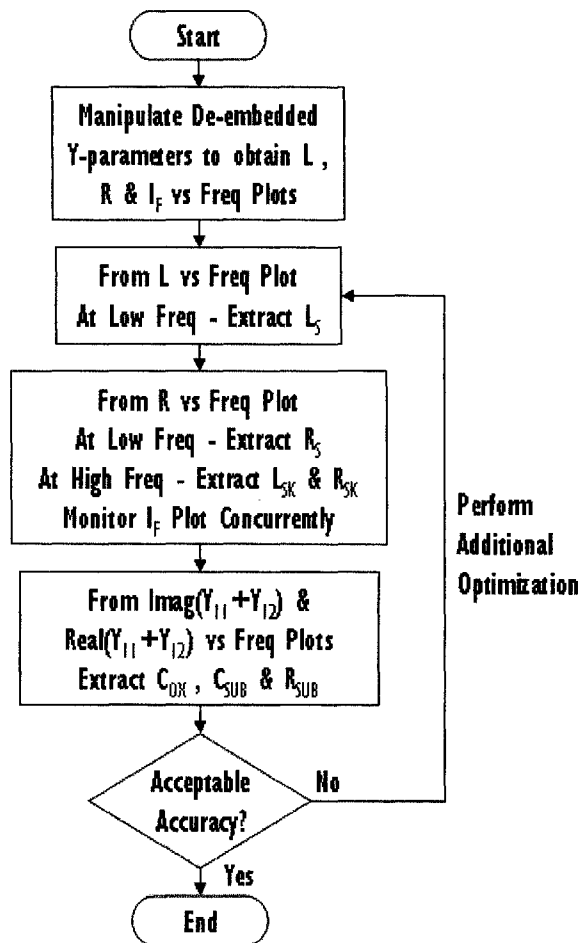


Figure 6.4 - Model parameter extraction procedure for double- π RF interconnect model.

6.4 Accuracy and Continuity of the RF Interconnect Model

Extraction routine described in Figure 6.4 is implemented in IC-CAP, Agilent's device characterization and modeling software, to obtain values of the components in the RF sub-circuit model. This scalable RF model is developed using the 25 interconnect test structures with 5 different sets of widths and lengths. As an example, Figure 6.5 demonstrates how well SPICE simulated two-port S-parameters of this double- π model can predict the measured L, R, Q and I_F , for an interconnect with length and width of 800 μm and 20 μm respectively. Comparing Figure 6.5(c) and 6.5(d) reveal that I_F is more appropriate to describe the performance of interconnects since it decreases as frequency increases, describing the proliferation of parasitic inductance, resistance and substrate losses associated with interconnects as operating frequency escalates.

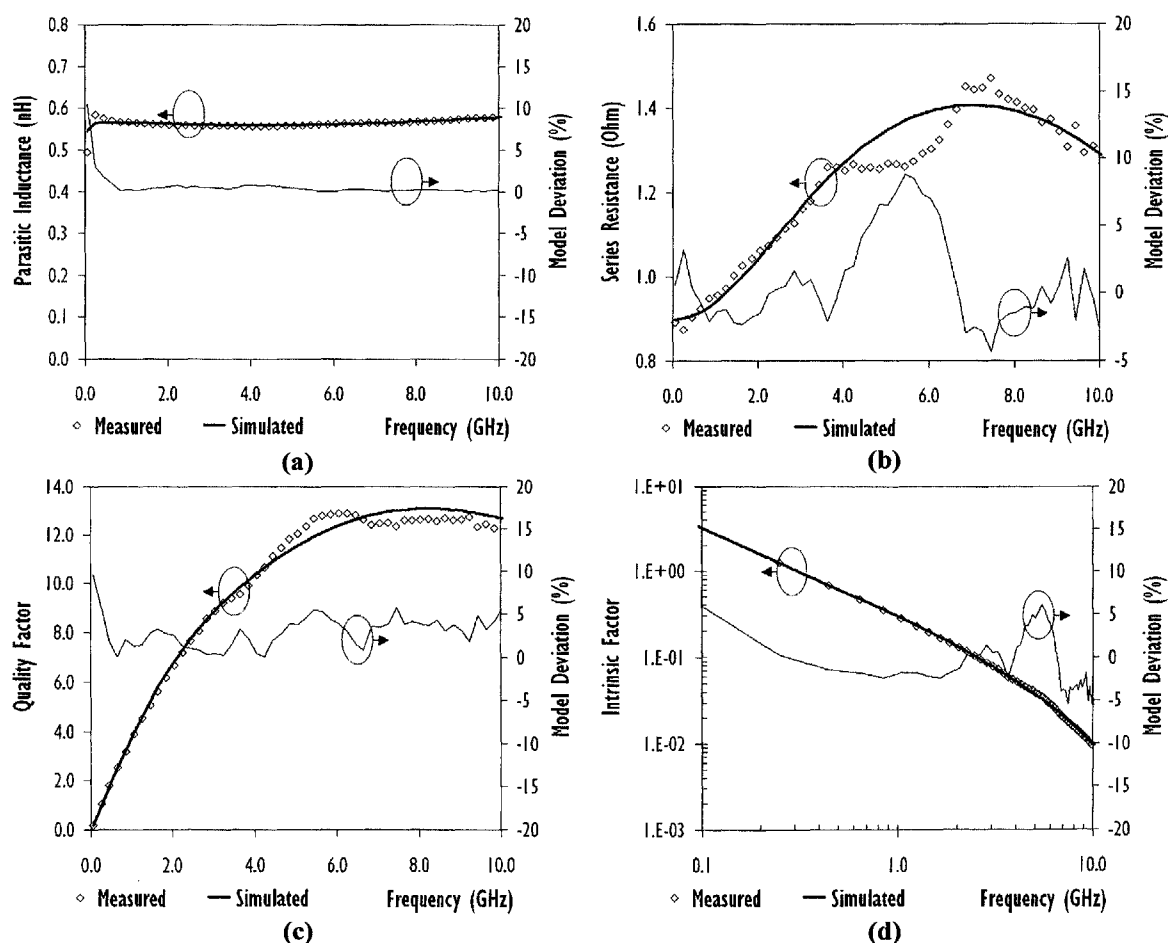


Figure 6.5 - Measured vs simulated parasitic inductance (a), series resistance extracted from Y_{12} (b), Q-Factor (c) and Intrinsic Factor, I_F (d) vs frequency for interconnect with length and width of 800 μm and 20 μm respectively using the proposed double- π RF interconnect model.

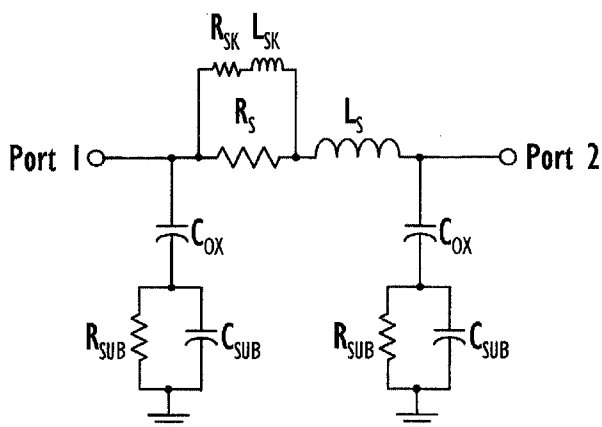


Figure 6.6 - Single- π lumped element RF sub-circuit model for interconnects.

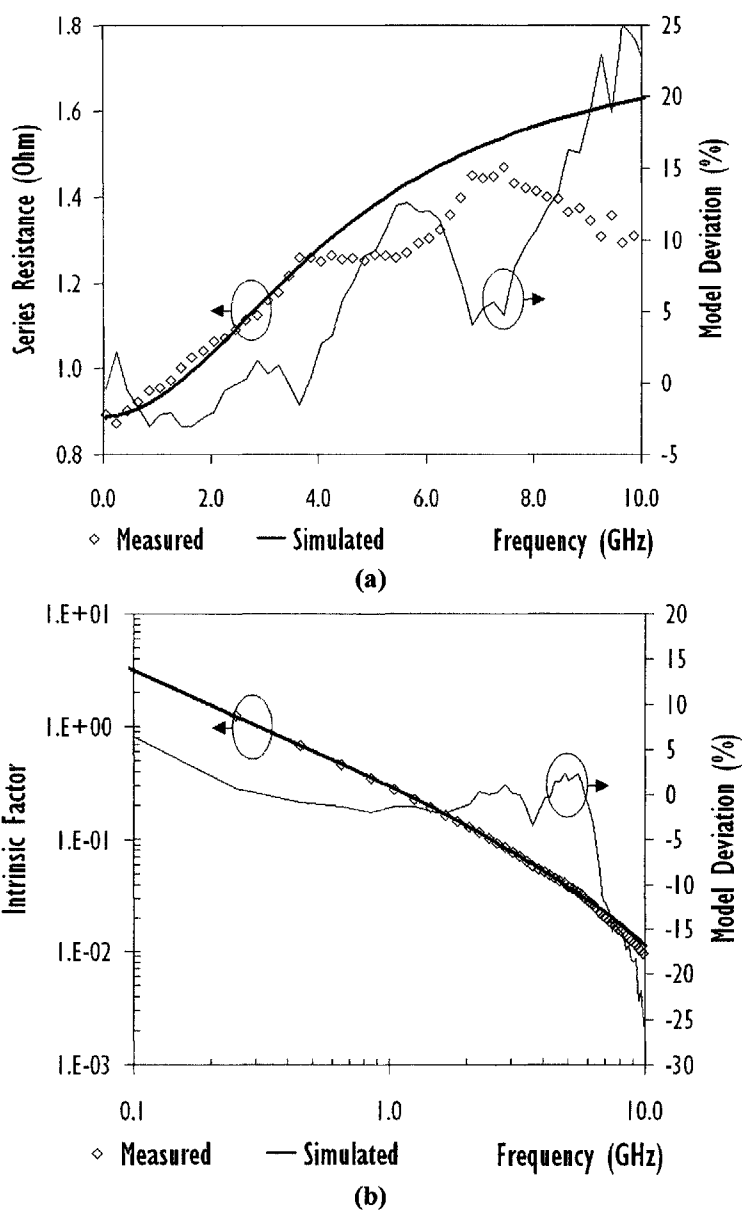


Figure 6.7 - Measured vs simulated series resistance extracted from Y_{12} (a) and Intrinsic Factor, I_F (b) vs frequency for interconnect with length and width of $800\ \mu\text{m}$ and $20\ \mu\text{m}$ respectively using a single- π lumped element RF sub-circuit model.

A single- π lumped element RF sub-circuit model shown in Figure 6.6 can also be used to model interconnects operating at radio frequencies. However, there is a limitation to this approach at the higher RF regime and this model-inadequacy is even more evident for long interconnect lines whereby the single- π model is not able to predict the reduction of the extracted series resistance, R , revealed in Figure 6.7(a). This phenomenon can be attributed to the fact that as frequency increases, interconnects behave like transmission lines with distributed characteristics and hence, a simple lumped element π model is insufficient to describe its behavior. When single- π lumped element model is adopted for the same interconnect in Figure 6.5, the model deviation between the measured and simulated values for R and I_F worsen from about $\pm 8\%$ to more than $\pm 25\%$ as shown in Figure 6.7.

As discussed in Section 2.2.1, if the interconnect line is less than $1/20^{\text{th}}$ of the wavelength, λ , of the signal, it is sufficient to use a lumped circuit model for the interconnect. When the interconnect is embedded within dielectric material, g , the velocity of the signal propagating in the interconnect will be reduced. Relative permittivity, ϵ_r , and permeability, μ_r , of material g have to be considered when calculating the wavelength, λ_g of the signal. Therefore, critical lengths of interconnects in silicon process will be smaller because they are embedded within silicon dioxide, resting on a lossy silicon substrate. The critical physical lengths for RF interconnects in silicon-based process with silicon and silicon dioxide as dielectric materials can be calculated as follows,

$$\begin{aligned} \text{Critical length} &< \lambda_g / 20 \\ \text{Critical length} &< \frac{c}{\sqrt{\epsilon_r} \times \sqrt{\mu_r} \times \text{frequency} \times 20} \end{aligned} \quad (6.11)$$

where, λ_g is the wavelength in material g , c = speed of light (in free air $\cong 3\text{e}+08$ m/sec), ϵ_r and μ_r refer to the relative permittivity and permeability of material g .

Computations of the critical lengths for interconnects embedded within silicon dioxide using Equation 6.11 have been presented in Table 2.2. These results further support that the double- π RF interconnect model will be more accurate compared to a simple lumped element π model in emulating behaviors of the interconnect structures, especially those that exhibit distributed effects.

Up to 10 GHz, employing models with multiple- π (> 2) networks are less likely to provide any significant improvement in accuracy for predicting these interconnects. Such complex models are more difficult to extract and the amount of simulation time required when they are used in circuit level simulation is most likely to increase. The simple double- π distributed model is adequate in corresponding high frequency effects without compromising the accuracy of the model. It is also scalable and continuous across various physical dimensions of the interconnects. Examining the model accuracy as well as continuity in predicting all the test structures at popular frequencies for applications such as Bluetooth and wireless LAN, box plot in Figure 6.8 consolidates the deviation between the measured and simulated parasitic inductances for majority of the 25 interconnect test structures to be within $\pm 1\%$ at 2.45 and 5.05 GHz. It also shows that the proposed double- π model has an intrinsic factor, I_F accuracy of within $\pm 5\%$ at 2.45 and 5.05 GHz.

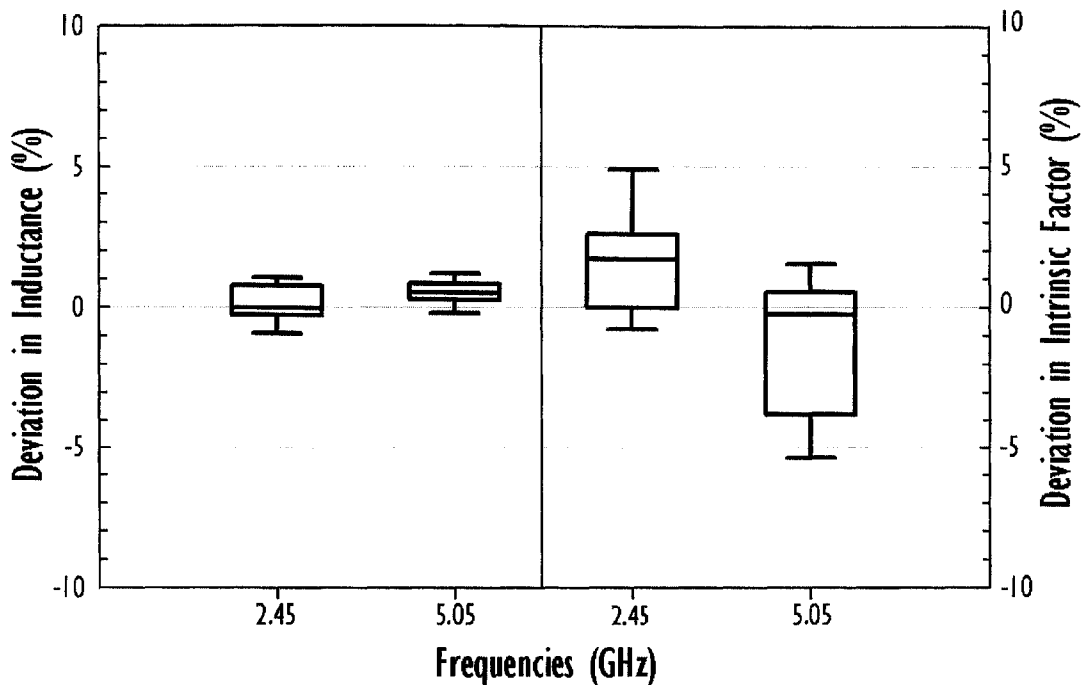


Figure 6.8 - Box plots showing deviation between simulated and measured parasitic inductance and Intrinsic Factor, I_F at 2.45 and 5.05 GHz for the metal-6 interconnect test structures.

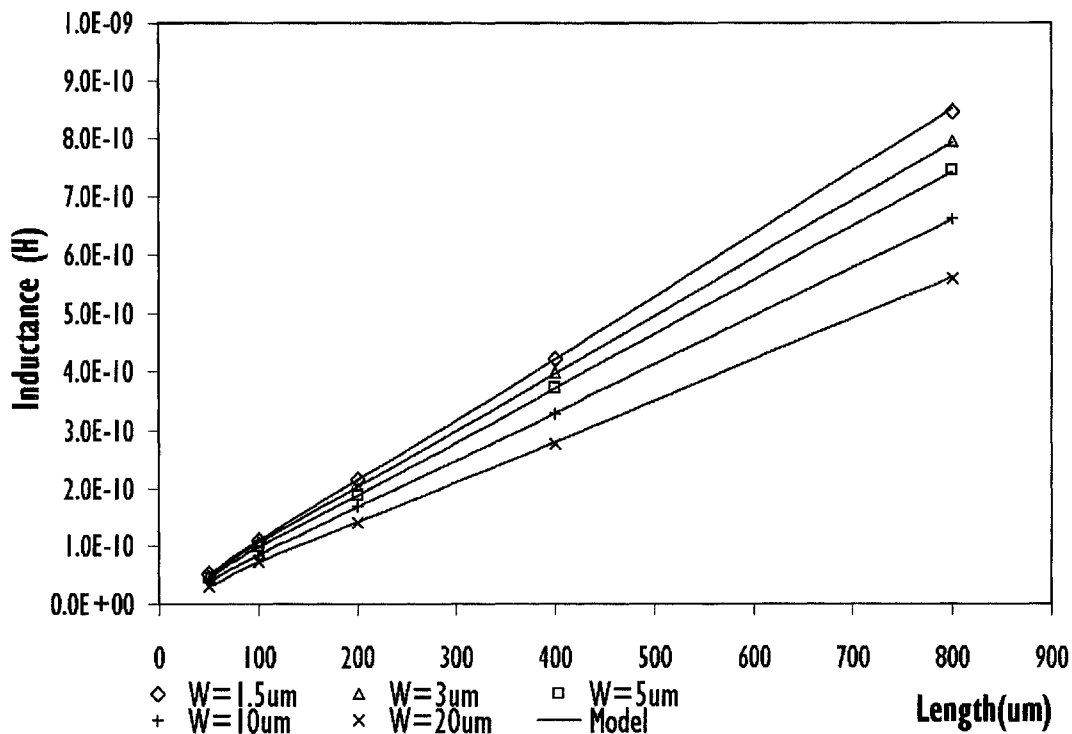


Figure 6.9 - Double- π RF interconnect model continuity – simulated and measured interconnect inductance versus length for different widths at 2.45 GHz.

Figure 6.9 demonstrates that at 2.45 GHz, the scalable interconnect model can accurately predict the measured inductances and is continuous for all the RF interconnects with various metallization widths and lengths. Figure 6.10 examines the simulated versus

measured interconnect intrinsic factor, I_F , for all the interconnects at 2.45 GHz and further assures that the scalable double- π model is incessant and precise. It also reveals that long narrow-width interconnects should be avoided in RFIC's since short wide-width interconnects are less lossy with relatively larger I_F values.

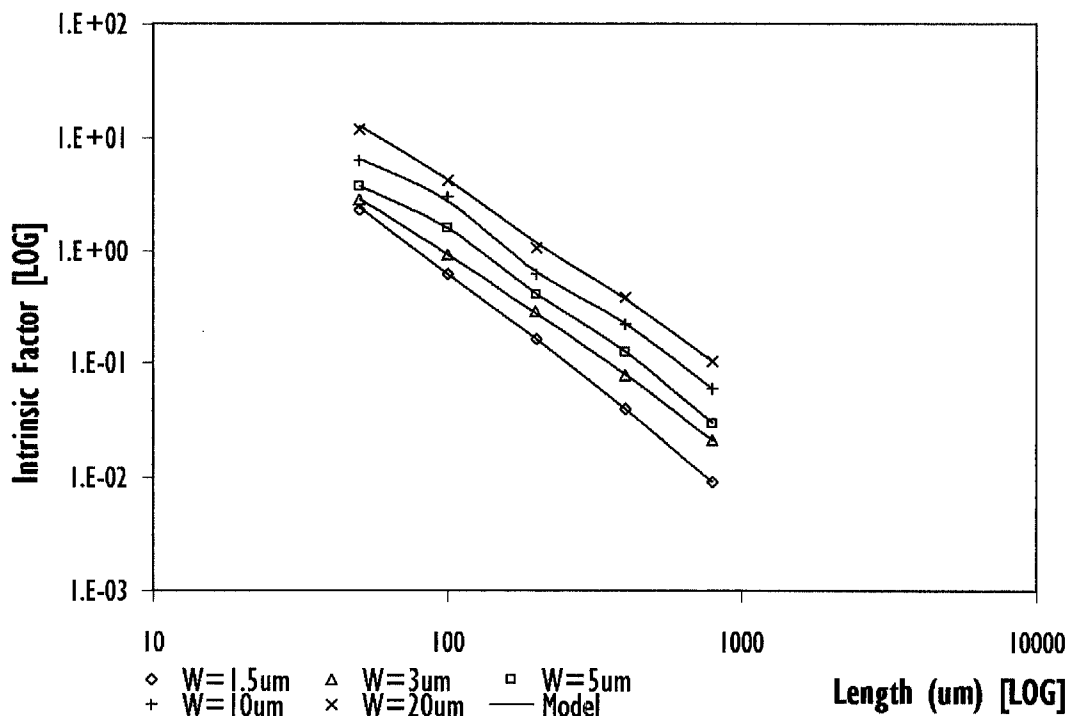


Figure 6.10 - Double- π RF interconnect model continuity – simulated and measured Intrinsic Factor, I_F versus length for different widths at 2.45 GHz.

6.5 Model Verification using Giga-Hertz Amplifiers

Conventional giga-hertz amplifier and voltage controlled oscillator circuits are designed and fabricated in the same 0.18 μm RFCMOS technology to demonstrate the accuracy, scalability and SPICE-simulator compatibility of the double- π RF interconnect model. The amplifier design consisting of a RF nMOS thin gate transistor with input and output matching networks is expected to operate at 2.45 GHz with a gain of about 10 dB. With reference to the giga-hertz amplifier circuit schematic shown in Figure 6.11, C_1 , C_2 , R_1 and L_1 are used to provide narrowband (2.45 GHz) 50 ohm input matching at the gate of the transistor, M_1 . R_1 is employed to marginally reduce the Q-factor of L_1 so that a large input matching bandwidth can be achieved. Output matching network to the external test system is made up of L_2 and C_3 . R_2 is used to isolate the DC biasing from high frequency signal path at the gate of the transistor. Last but not least, for amplifier to operate, 0.9V and 1.8V DC biases are applied to V_G and V_{DD} terminals respectively.

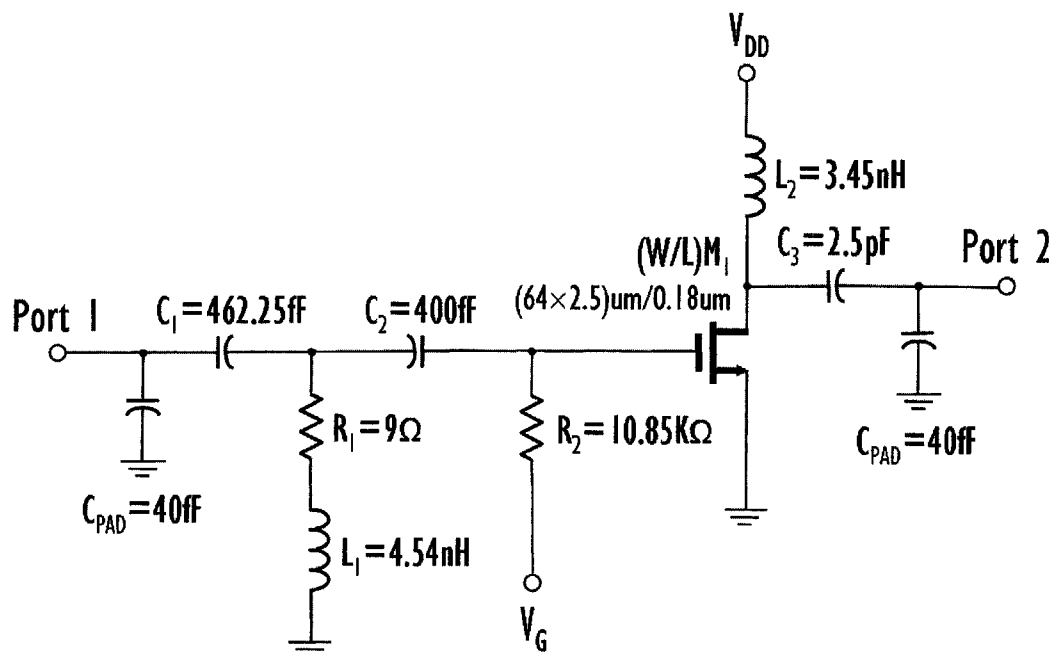


Figure 6.11 - Schematic of a simple giga-hertz amplifier circuit to verify the accuracy of the double- π RF interconnect model.

To verify the validity and precision of the proposed RF interconnect model, two device-identical giga-hertz amplifier circuitries were fabricated using the same interconnect

lengths but with interconnect widths of 1.5 and 10 μm . Experimental control of maintaining the same interconnect length helps minimize unfavorable differences of circuit performances associated with signal coupling and device layout placement which may lead to a biased experimental comparison. Figure 6.12 shows die photos of the device-identical amplifier circuits with different interconnect widths. On-wafer RF circuit performance characterization for the amplifiers are performed on a “golden” or typical die selected using data obtained from full wafer map device measurements of RF scribe line test structures to account for variations in the fabrication process [57]. Similar experimental setup described in Section 6.1 has been used, taking into consideration the selection of source power on the network analyzer. The two amplifiers’ measured two-port S-parameters consolidated in Figure 6.13 reveal that amplifier with interconnect width of 1.5 μm has a much smaller gain and lower peak gain frequency as compared to the amplifier with interconnect width of 10 μm .

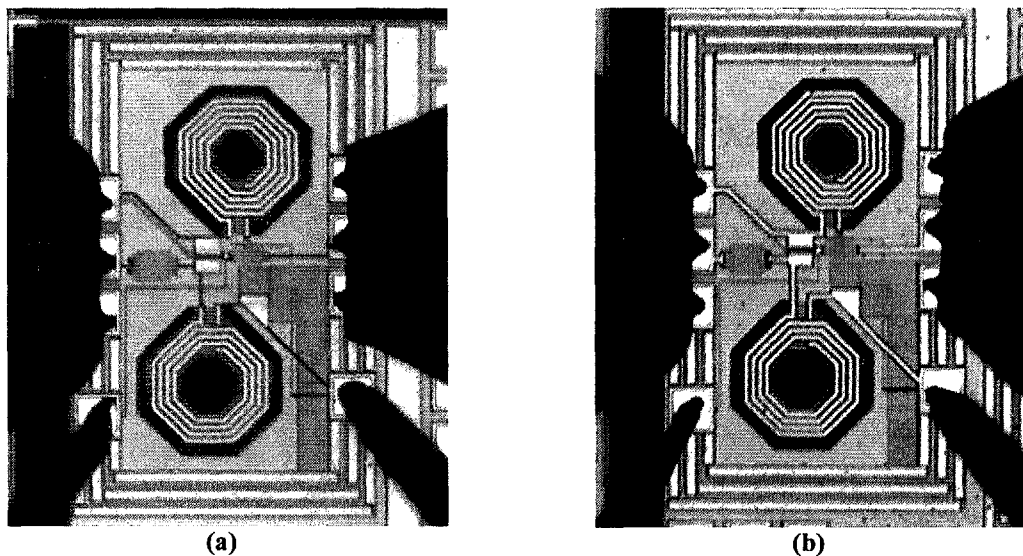


Figure 6.12 - Die photos showing on-wafer circuit characterization of giga-hertz amplifiers with different interconnect widths of (a) 1.5 μm and (b) 10 μm .

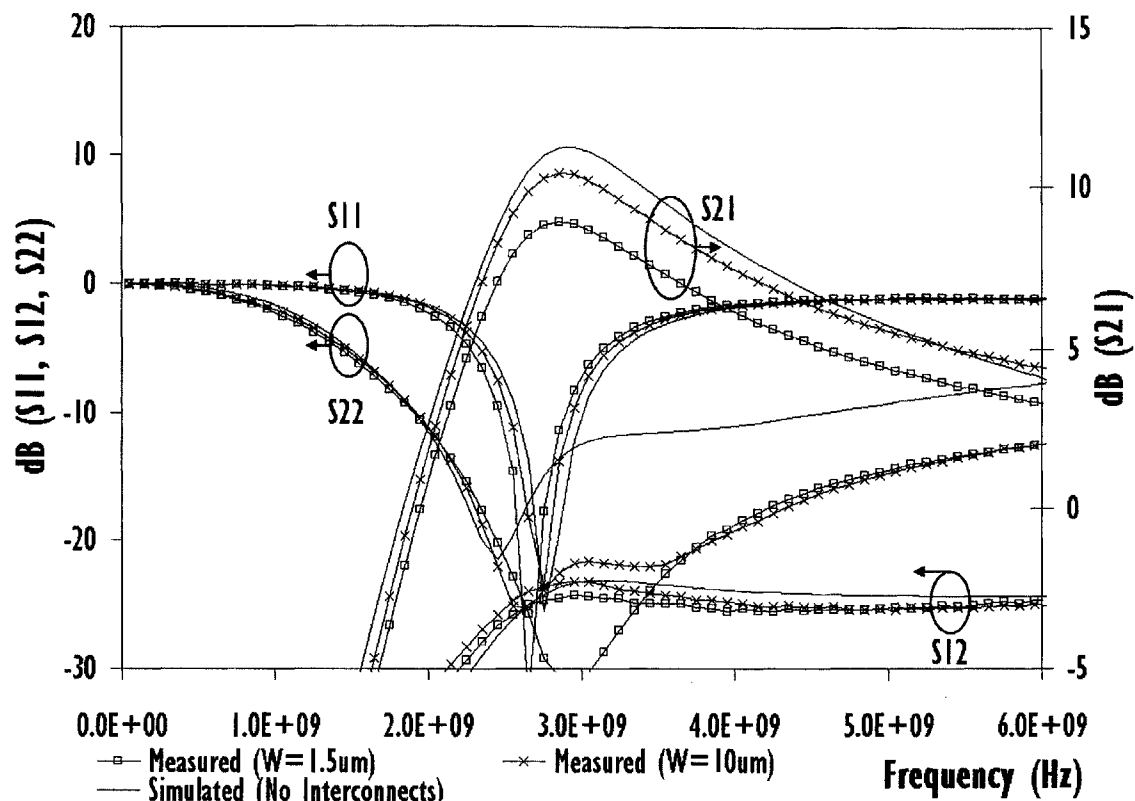


Figure 6.13 - Magnitude of measured S-parameters versus frequency for the 2 amplifier circuits with interconnect widths of 1.5 and 10 μm respectively.

These observations are attributed to the fact that 1.5 μm width metal lines have smaller I_F values as compared to interconnects with 10 μm width, as shown in Figure 6.10, suggesting that they have higher RF resistive loss and larger parasitic inductance. More notably, Figure 6.13 has disclosed the existence of intolerable discrepancies between simulated and measured circuit performances when interconnects are not considered during circuit simulations. The simulated circuit results are obtained from circuit schematic SPICE simulations of the amplifier in a commercial SPICE simulator.

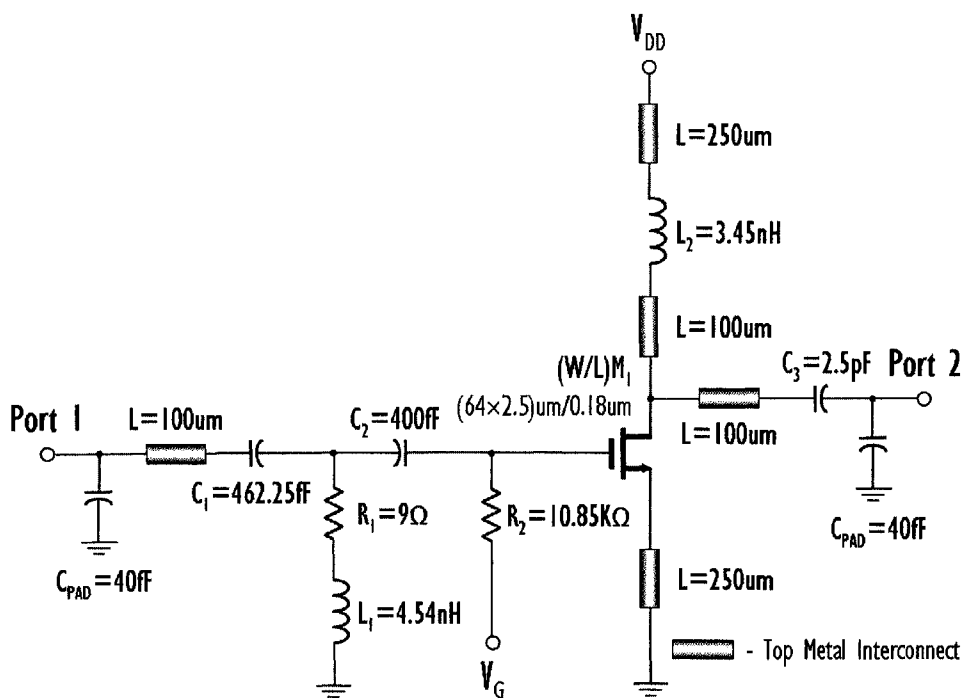
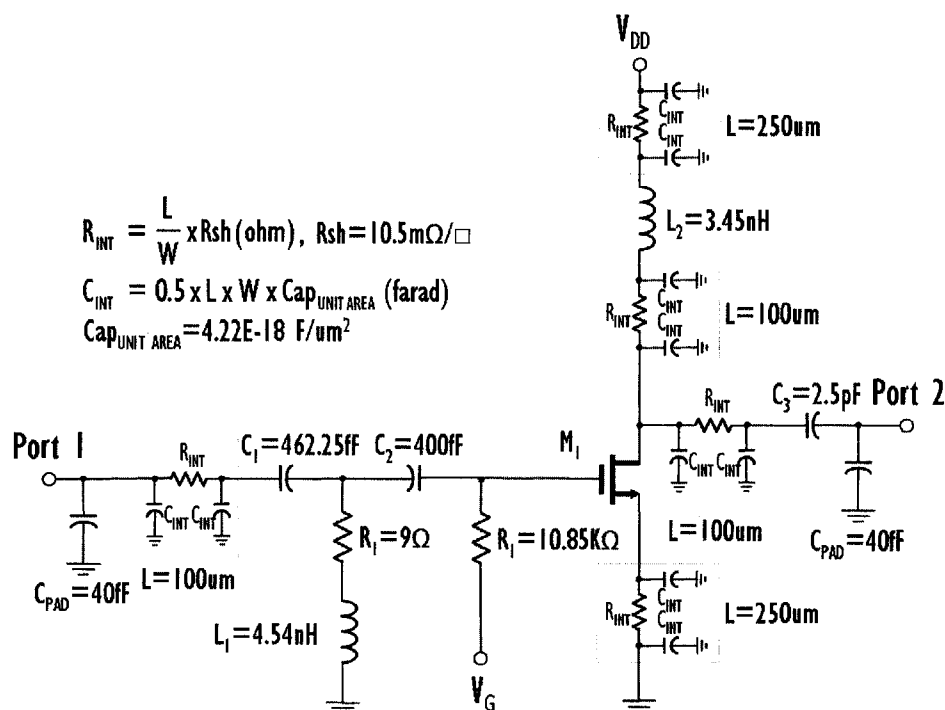


Figure 6.14 - Schematic of the giga-hertz amplifier circuit showing the lengths of metallization interconnects in various parts of the circuit.



$$R_{INT} = \frac{L}{W} \times R_{sh} \text{ (ohm)}, R_{sh} = 10.5 \text{ m}\Omega/\square$$

$$C_{INT} = 0.5 \times L \times W \times \text{Cap}_{UNIT \text{ AREA}} \text{ (farad)}$$

$$\text{Cap}_{UNIT \text{ AREA}} = 4.22 \text{E-}18 \text{ F}/\mu\text{m}^2$$

Figure 6.15 - Schematic of the giga-hertz amplifier circuit showing representation of metallization interconnects with conventional RC extraction.

Figure 6.14 illustrates a post-layout back-annotated schematic highlighting lengths of the interconnect metallization within the amplifier circuitry. With this information, the double- π RF interconnect model proposed in Section 6.3 is deployed to predict the overall Device Design. Characterization and Modeling of Inductors and Interconnects for RFIC Applications — 184

circuit degradation contributed by the interconnects at high frequencies. Figure 6.15, on the other hand, shows the amplifier schematic with a typical RC approach to investigate the effects of the interconnects. These 2 schematics allow multiple SPICE simulations of the amplifiers to be performed so that meaningful comparisons can be made between existing RC and the proposed RF interconnect modeling methodology. The measured and simulated S-parameters of the amplifier with interconnect width of $1.5 \mu\text{m}$ are evaluated in Figure 6.16. Simulated gain (11.25 dB) at peak gain frequency (2.93 GHz) of this amplifier without any interconnects is very much higher compared to the actual measured gain (8.93 dB) and peak gain frequency (2.85 GHz). With the RC interconnects, the simulated results only managed slight improvement in predicting the measured gain and the simulated peak gain frequency is still higher by 120 MHz.

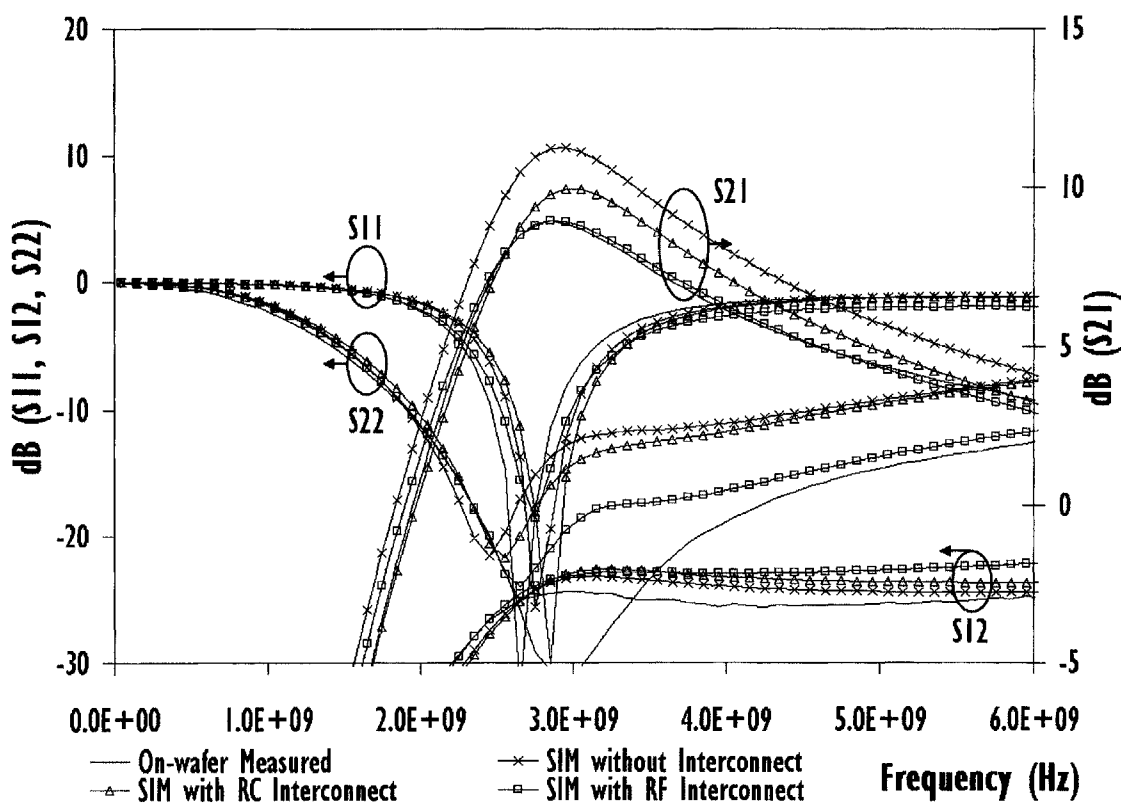


Figure 6.16 - Magnitude of measured and simulated S-parameters versus frequency for giga-hertz amplifier circuit with interconnect width of $1.5 \mu\text{m}$ using different interconnect schemes.

Nevertheless, when the double- π RF interconnect model is used, the simulated results correlate well with the measured amplifier performance in terms of absolute gain and peak

gain frequency with the input and output matching characteristics also within acceptable limits, even so when the interconnects have 45 and 90 bends. This outstanding agreement is possible because the parasitic inductance as well as high-frequency resistive loss associated with the interconnects are well emulated by the double- π RF interconnect model. Similar improvements between the measured and simulated S-parameters are also noted for the amplifier with 10 μm -width interconnects in Figure 6.17. RC interconnect approach is inadequate in predicting the measured gain and peak gain frequency of the amplifiers. Utilizing the RF interconnect models generate excellent agreement between the measured and simulated two-port characteristics for the amplifiers with different interconnect widths, demonstrating proficient model accuracy, continuity and scalability. Table 6.1 summarizes and compares the measured versus simulated maximum gain and peak gain frequency for the 2 amplifiers using the RC and RF interconnect models.

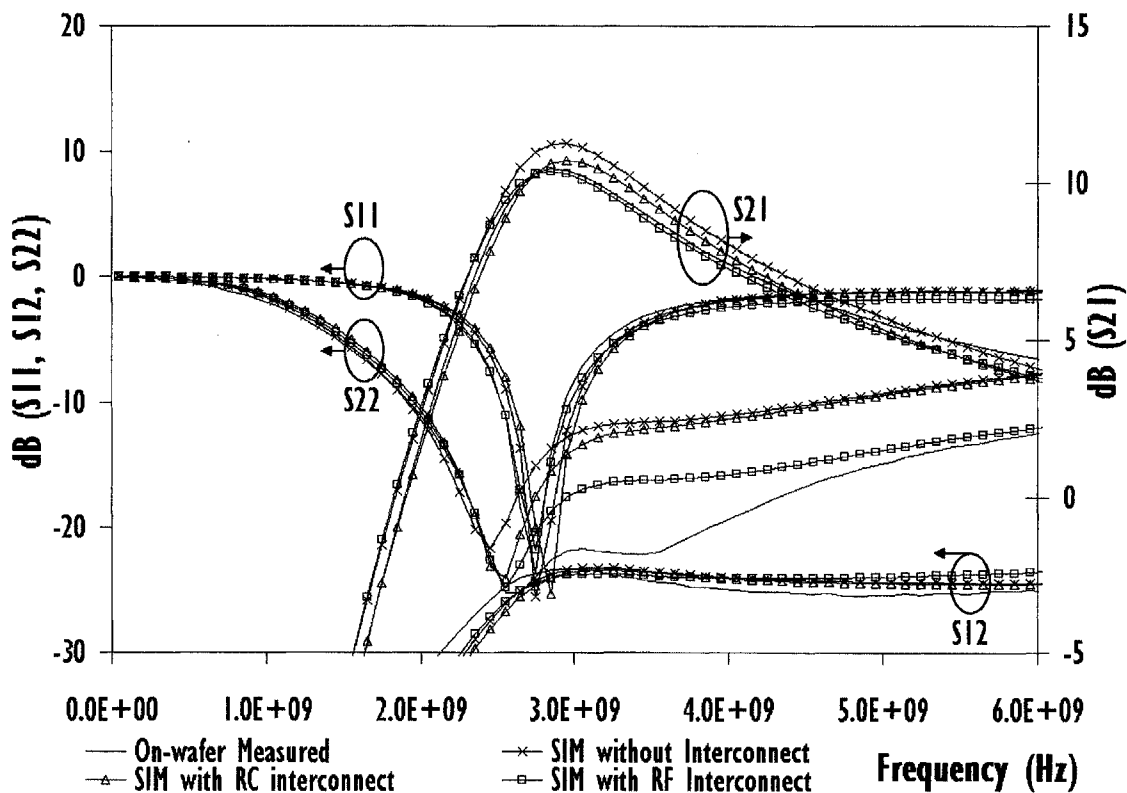


Figure 6.17 - Magnitude of measured and simulated S-parameters versus frequency for gigahertz amplifier circuit with interconnect width of 10 μm using different interconnect schemes.

Table 6.1 - Measured vs simulated gain and peak gain frequency for giga-hertz amplifiers with different interconnect widths.

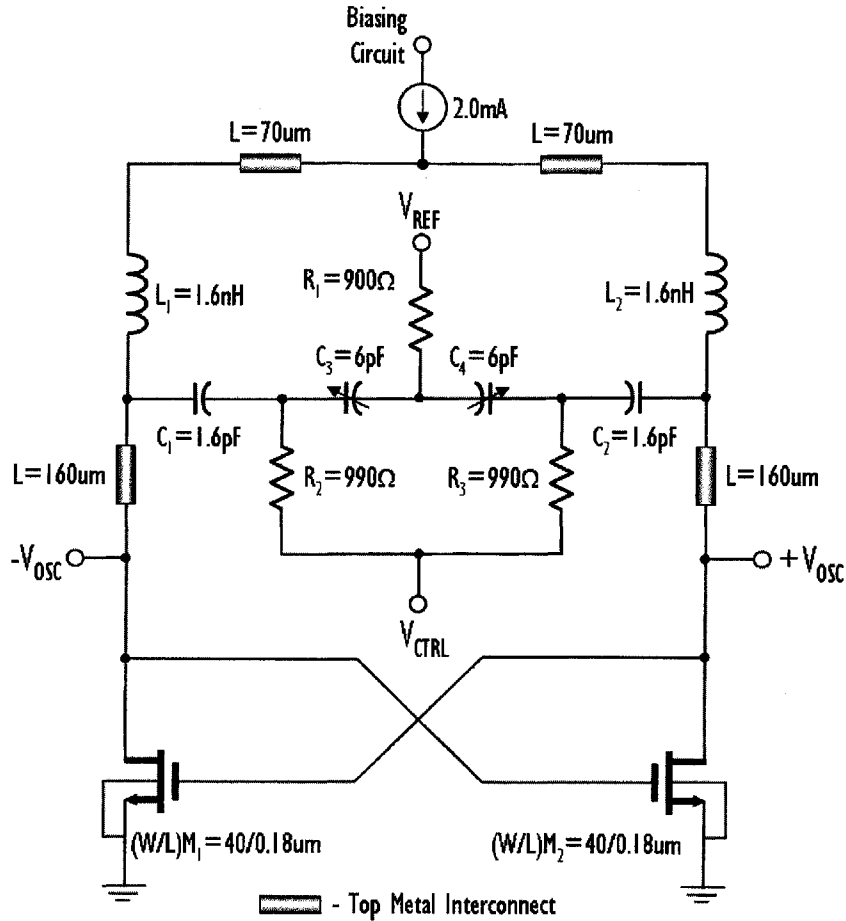
Interconnect Width in the Amplifiers Layout (μm)	Amplifiers' Measured Max. Gain(dB) [Peak Gain Frequency (GHz)]	Simulated Gain at Peak Gain Frequency Using Different Interconnect Modeling Schemes					
		No Interconnect Model		With RC Interconnect Model		With Double- π RF Interconnect Model	
		Simulated Max. Gain [Peak Gain Freq]	Deviation From Measured Gain (%)	Simulated Max. Gain [Peak Gain Freq]	Deviation From Measured Gain (%)	Simulated Max. Gain [Peak Gain Freq]	Deviation From Measured Gain (%)
1.5	8.93 [2.85]	11.25 [2.93]	25.98	9.95 [2.97]	11.42	8.92 [2.85]	-0.11
10	10.43 [2.87]	11.25 [2.93]	7.86	10.70 [2.95]	2.59	10.34 [2.87]	-0.86

6.6 Model Verification using Voltage Controlled Oscillator

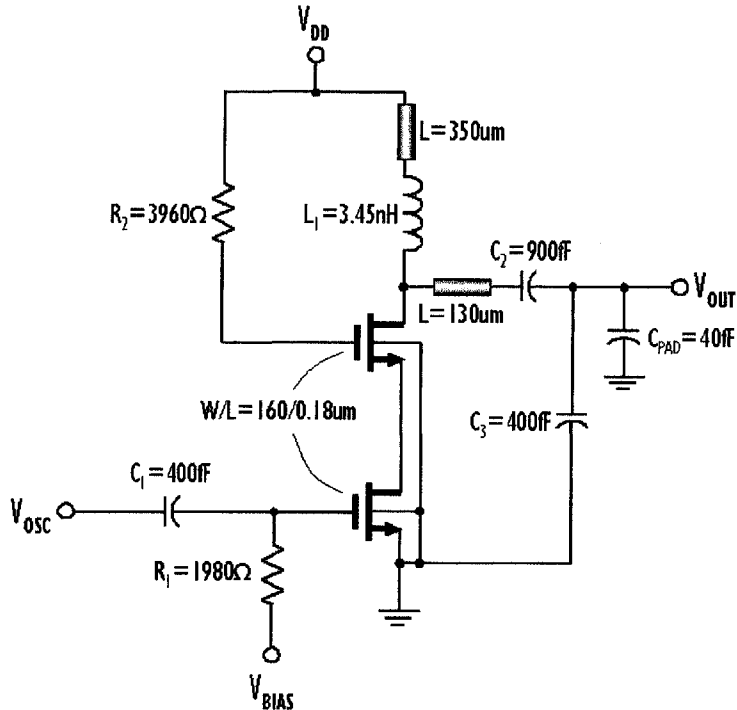
Accuracy and reliability of the double- π RF interconnect model is further scrutinized using a conventional giga-hertz voltage controlled oscillator (VCO) design. The post-layout back-annotated schematics illustrating the addition of interconnect metallization in the VCO and buffer amplifier designs are summarized in Figure 6.18 (a) and (b) respectively. In Figure 6.18 (a), the VCO tank circuitry comprises of L_1 , L_2 , C_1 , C_2 , C_3 and C_4 to define the oscillation frequency of the differential signal pair at terminals $-V_{\text{OSC}}$ and $+V_{\text{OSC}}$. These two terminals are then each connected to a separate buffer amplifier with low output impedance for higher load driving capability shown in Figure 6.18 (b).

In Figure 6.18 (a), the crossed-coupled nMOSFETs for the VCO design, M_1 and M_2 generate negative resistance to counteract the resistance from the LC tank thereby launching the VCO into oscillation. MOS Varactors, C_3 and C_4 , operating in the accumulation mode, are used to vary the oscillating frequency of the VCO. Reference and control DC voltages, applied on terminals V_{REF} and V_{CTRL} respectively, are utilized to change the capacitances of the MOS varactors. Finally, isolation of the DC biasing from the RF oscillating signal is achieved using R_1 , R_2 and R_3 . Die photo capturing the VCO with the RF and DC probes for on-wafer circuit characterization is shown in Figure 6.19.

VCO circuit simulations with and without RF interconnect model are performed. With the RF interconnect model, the SPICE simulated oscillation frequencies with respect to the control voltages have excellent associations with the on-wafer measured results. From Figure 6.20, it is observed that the percentage error between the simulated and measured oscillating frequency for the VCO has improved from about 5.6 % when interconnects are not considered to within 3 % when RF interconnect models are utilized, indicating excellent reliability of the proposed double- π RF interconnect model even for transient circuit simulations.



(a) Voltage Controlled Oscillator



(b) Buffer Amplifier

Figure 6.18 - Schematics of voltage controlled oscillator (a) and buffer amplifier (b) of a simple giga-hertz voltage controlled oscillator with interconnect width of $10\mu\text{m}$ to verify the accuracy of the double- π RF interconnect model.

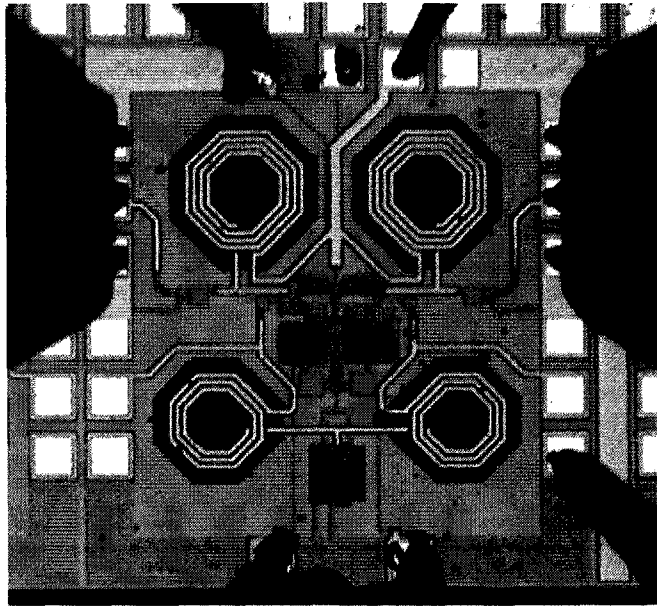


Figure 6.19 - Die photo of the giga-hertz voltage controlled oscillator with interconnect width of 10 μm to verify the accuracy of the double- π RF interconnect model.

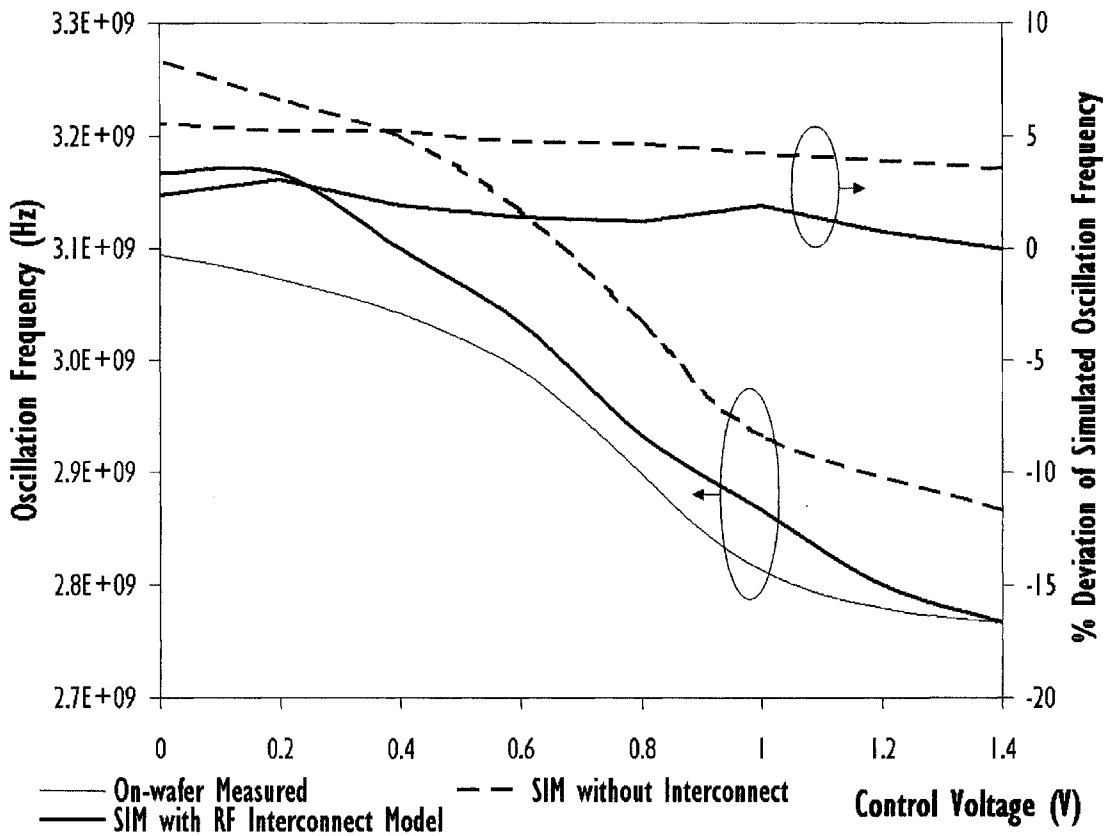


Figure 6.20 - Measured and simulated (SIM) oscillation frequency versus control voltage for gigahertz voltage controlled oscillator using double- π RF interconnect model.

6.7 Comparing Research Works on Interconnect Modeling

Five other key research studies on RF interconnects are tabulated in Table 6.2 as an evaluation of the research contributions for this work. A new figure of merit, the intrinsic factor, I_F has been proposed in this research to help circuit designers conveniently understand the RF performance of interconnects. Compared to most research papers, this study employs the most number of test structures to develop the RF interconnect model, achieving excellent model deviations in inductance and intrinsic factor of $\pm 1\%$ and $\pm 5\%$ respectively.

Unlike other publications, this work utilizes practical RF circuits to validate the double- π interconnect model. The effects of interconnect designs on the performance of RF circuits are also shown quantitatively, comparing the performance of two giga-hertz amplifiers that have identical device placements and interconnect routing but different interconnect widths. Last but not least, the scalability and accuracy of the interconnect model have been demonstrated with good circuit simulation predictions for two giga-hertz amplifiers and a voltage controlled oscillator.

Table 6.2 - Comparing various research works on modeling RF interconnects.

Author	J. Wee	Y. Eo	G. Wang	Y. Cao	X. Shi	This Work
Reference	[86]	[87]	[88]	[89]	[90]	
Journal/Conference	IEEE TMTT	IEEE TAdvPackaging	IEEE TED	IEEE TVLSI	IEEE TVLSI	IEEE TMTT
Year of Publication	1998	2000	2001	2005	2005	2005
Number of test structures used for model development.	5	10	1	2	5	25 (refer to Section 6.1)
Is there new figure of merit Proposed for Interconnects?	No (R, L, C, Propagation and Attenuation constants are used)	No (L, signal delay and Transient Response)	No (R, L, C and Attenuation constant are used)	No (Paper just evaluate based on low frequency L and R. No information on High frequency substrate loss)	No (Paper just compare fitting of S-parameters. Circuit designer would not know which interconnects will have the best design)	Intrinsic Factor (Conveniently allow researchers and circuit designers to compare the RF performance of interconnects)
How many elements are in the proposed model?	4	30	6	5	20	20 (10 elements have to be extracted)
Is the extraction methodology published?	Yes	Yes	Yes	Yes	Yes	Yes
What is the operating frequency supported by the model?	20 GHz	20 GHz	6 GHz	< 30 GHz	25 GHz	10 GHz
What is the model error/deviation?	Not Published	Not Published	Not Published	< 10 %	Average error of 2 % for S-parameters	L : ± 1 % I _F : ± 5 % (For all interconnects at 2.45 and 5.05 GHz)
Is the model scalable to the inductor physical design parameters?	Unknown (Only 5 structures of widths from 1 - 20µm and length of 5 mm)	Unknown (Only 5 structures of widths from 0.8 - 10µm and length of 8 mm)	Unknown (Only 1 structure is used)	Unknown (Only 1 structure of 5 µm width and 3 mm length used)	Yes (Demonstrated with 6 structures)	Yes (Scalable with Length and Width)
How is the performance of the model continuity?	Unknown (Only 5 structures of widths from 1 - 20µm and length of 5 mm)	Unknown (Only 5 structures of widths from 0.8 - 10µm and length of 8 mm)	Unknown (Only 1 structure is used)	Unknown (Only 1 Structure of 5 µm width and 3 mm length used)	No continuity plots against length and widths of interconnects	Excellent (Model is continuous Figure 6.9 and 6.10)
Is the model SPICE-compatible?	Yes	Yes	Yes	Yes	Yes	Yes
Has the model been verified in test circuits?	No	Yes (A simple transmission line terminated with a capacitive load is used)	No	No	No	Yes (Two Amplifiers and a VCO, Results in Section 6.5 and 6.6)

6.8 RF Interconnects in Aluminum and Copper Technologies

Previous sections have presented the development of an accurate double- π interconnect model that is continuous and scalable across physical dimensions of interconnects. This model has been demonstrated to offer excellent predictions to the measured performance of RF circuits which will significantly reduce costly design iteration cycle. Intrinsic factor has also conveniently guided engineers to choose interconnects with the smallest parasitics for device routing. In this section, the performance of interconnects in the 0.13 μm RFCMOS copper technology will be evaluated and compared against the 0.18 μm RFCMOS aluminum-based interconnect technology. The fabricated copper-based interconnects are characterized by the same procedure outlined in Section 6.1. Differences in materials and physical dimensions for these two interconnect processing technologies have been described in Section 2.2.2. There will also be discussions on how to extend the interconnect model for 0.18 μm RFCMOS technology to copper-based interconnects in the advanced RFCMOS technologies.

Figure 6.21 illustrates the low frequency resistance for 24 interconnect test structures having different lengths (from 100 to 800 μm) and widths (1.5, 5 and 10 μm), utilizing both top metal copper and aluminum metallization. Figures 6.22 and 6.23, on the other hand, consolidate the interconnects' extracted inductance and intrinsic factor at 2.45 GHz respectively. In Figure 6.21, copper-based interconnects are noted to have much smaller series resistance compared to aluminum-based interconnects primarily due to lower resistivity and thicker top metallization. Therefore, for top metal interconnect with the same design, smaller R_S , R_{SK} and L_{SK} interconnect model parameters (refer to Figure 6.3) are required to predict the behavior of copper-based interconnects beyond the 0.13 μm RFCMOS technology (refer to Table 4.1).

Aluminum and copper have almost identical permeability ($\mu_{Al} = 1.2566650 \times 10^{-6}$ H/m and $\mu_{Cu} = 1.2566290 \times 10^{-6}$ H/m [60]). The thicker top metallization for the 0.13 μm RFCMOS technology implies both larger cross-sectional area and lower current density, justifying the smaller parasitic inductance observed in Figure 6.22 for the copper interconnects. As such, for top metal interconnect of the same length and width, a correspondingly lower L_S model parameter value is expected for interconnects in the copper backend technology. Comparing the intrinsic factors for both technologies, Figure 6.23 revealed that the copper-based interconnects have much better RF performance compared to aluminum-based interconnects across all lengths for widths of 1.5, 5 and 10 μm . This is expected since copper interconnects have smaller parasitic resistance and inductance as indicated in Figures 6.21 and 6.22. Also, the dielectric constant of IMD in the copper-based interconnects are much lower compared to aluminum based interconnects, suggesting smaller substrate losses (refer to Figure 2.21). The value of model parameter, C_{OX} will be much smaller and no significant differences in C_{SUB} and R_{SUB} values are expected to model the copper-based interconnects even though substrate resistivity is to be reduced to prevent latch-up occurrences (refer to Figure 6.3). To sum up, copper metallization would be the preferred choice if degradation effects on RF circuit performance due to the interconnects is a critical factor for circuit designers.

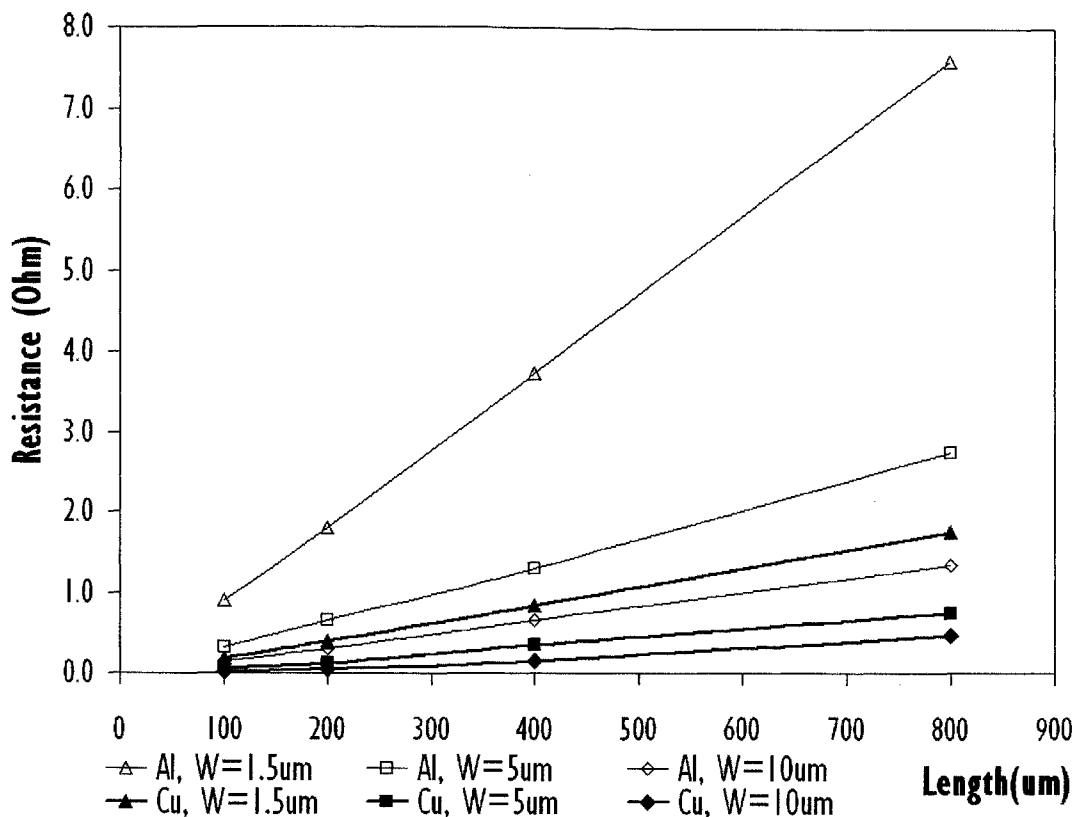


Figure 6.21 - Comparing extracted low frequency resistance for aluminum (Al) and copper (Cu) top metal interconnects with conductor lengths from 100 to 800 μm and widths of 1.5, 5 and 10 μm .

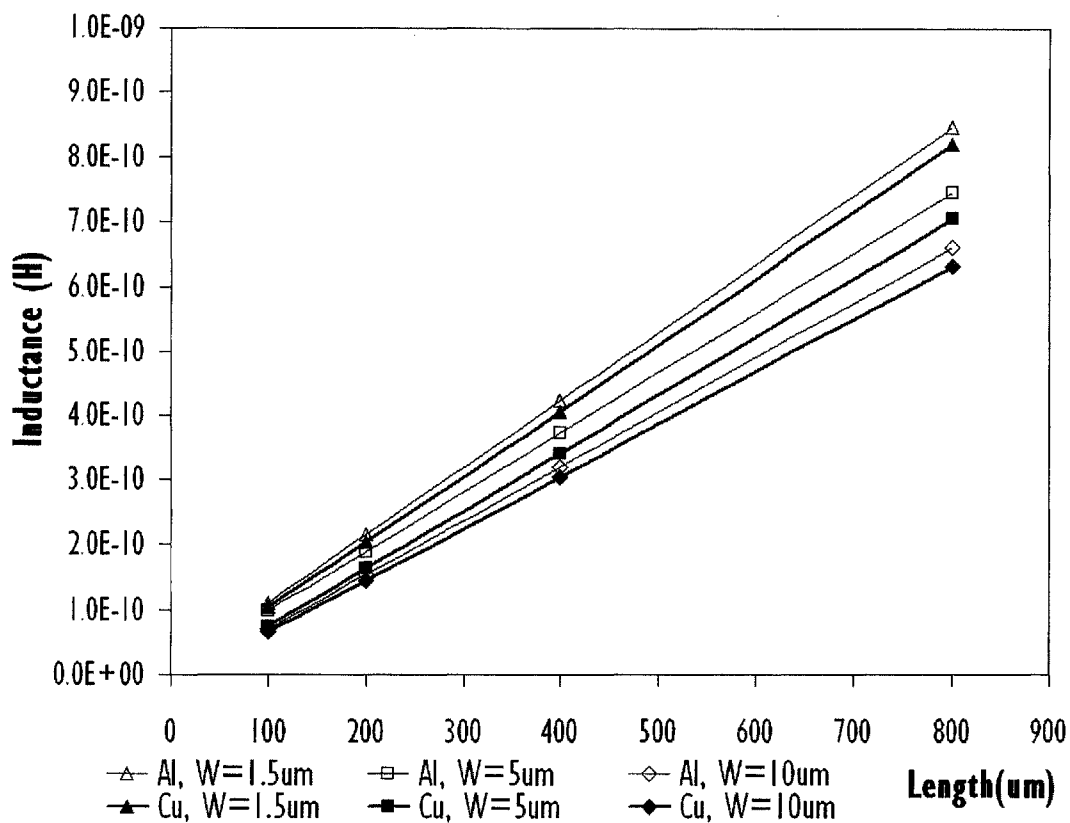


Figure 6.22 - Comparing extracted inductance at 2.45 GHz for aluminum (Al) and copper (Cu) top metal interconnects with conductor lengths from 100 to 800 μm and widths of 1.5, 5 and 10 μm .

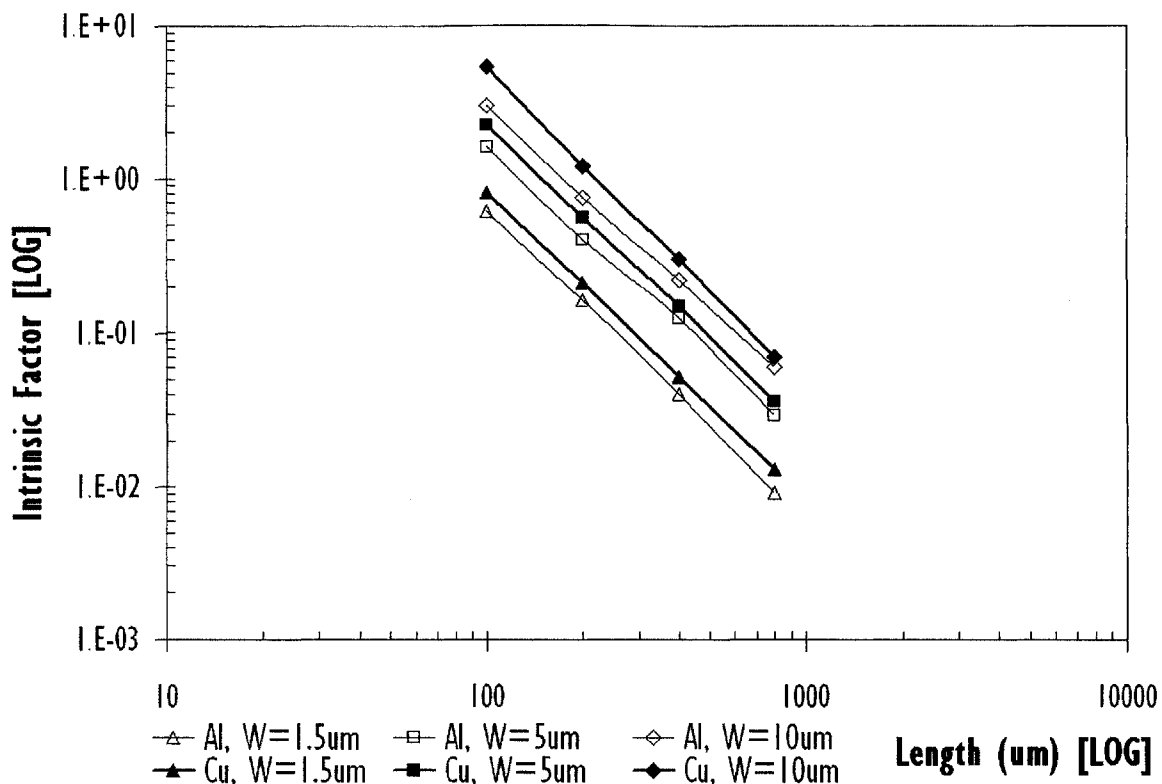


Figure 6.23 - Comparing extracted Intrinsic factor at 2.45 GHz for aluminum (Al) and copper (Cu) top metal interconnects with conductor lengths from 100 to 800 μm and widths of 1.5, 5 and 10 μm .

Chapter 7 - Conclusions and Recommendations

7.1 Conclusions

The soaring demands for personal wireless communication equipment motivated an urgent need to develop inexpensive, small size, low power consumption and low noise level RF SoCs. With an established technology, low fabrication cost, larger possibilities and ease of achieving SoC integration with RF front-end and digital/analogue baseband coexisting on a common platform, silicon is recognized as the most suitable material for satisfying the demands of this rapidly growing wireless communication market. Enhanced device characteristics such as higher cutoff frequencies for transistors have allowed the traditional digital technologies to cope with stringent RF specifications set forth in popular communication standards. Nevertheless, low resistive bulk silicon which helps improve latch-up immunity at tighter design rules and high resistive loss associated with the back-end-of-line metallization limit the performance of on-chip inductors and interconnects making them major road blocks to achieving high circuit performance at giga-hertz frequencies.

In this thesis, a comprehensive literature review on silicon-based spiral inductors and transmission lines is presented. The advantages of using on-chip inductors are discussed. Figure of merits and various loss mechanisms for silicon-based spiral inductors have been defined and analyzed. Numerous techniques such as novel processing technologies, use of active circuitries, varying physical dimensions and optimization through inductor device model, proposed to improve the performance of on-chip inductors are critically reviewed in this report. The concepts of transmission lines and existing techniques to tackle post-layout parasitics have also been discussed. The need to perform calibration for RF measurements and the various calibration methods are explained and evaluated. Past and present RF probe technologies are documented and the procedures of extending

measurement reference planes to the devices for on-wafer RF characterization are also covered in this research work.

Evaluating the pros and cons of various approaches published in the literature, physical design parameter optimization of spiral inductors offers huge impact and benefits the industry since these passive integrated inductors are widely adopted in commercial products. All other known techniques, in general, require either expensive non-standard fabrication flows or active devices that consume additional power and introduce noise sources to the RF circuits. For the first time, spiral inductors are designed to achieve similar inductance values as an experimental control to investigate how its core diameter, conductor spacing and width affect their performances quantitatively. It is found that the inductor's core diameter has immense influence on its performance and must be larger than 100 μm to minimize the formation of conductor eddy current. On the other hand, small inductors with narrow conductor widths, such as 4 μm , are less susceptible to conductor eddy current effect and hence using small core diameters will reduce the circuit silicon real estate required. Conductor spacing should be small as it offers larger inductance value and consume smaller silicon area. Optimization of conductor width allows peak Q-factor of spiral inductors to be tuned at the circuit's operating frequency and in doing so, permits inductors over a wide range of inductance values to have much larger Q-factors at that particular frequency of interest. It has been found that inductors of large inductance values actually require smaller width to adjust their peak Q-factor at 2.4 GHz achieving both performance enhancement and reduction in silicon area consumed by the inductor. The proposed design methodology of achieving alignment between the inductors' peak Q-factor frequency and circuit operating frequency allows a giga-hertz amplifier with optimized inductors to out-perform the amplifier with non-optimized inductors by a larger gain (26.6 % larger) and a lower noise figure (2.5 dB lower).

Based on the findings from optimizing conventional spiral inductors, streamlined sets of symmetrical and differential inductor test structures for developing scalable RF SPICE models are designed and fabricated in the 0.18 μm RFCMOS technology. The scalable RF models developed in this work has enabled ground-breaking analysis of trade-offs between inductor performance and design layout by comparing inductors with identical inductance values at frequencies of interest up to 10 GHz. Large-width designs are found to favor inductors with small inductance values due to huge reduction in resistive loss and large performance improvements. On the other hand, as inductance increases, trade-offs between resistive and substrate loss result in optimal widths such that using much larger widths would only waste chip area and not improve Q-factor. Such optimal width for differential inductors when compared to symmetrical spiral inductors is reported, for the first time, to be about 30 % smaller. As operating frequency increase, the optimal conductor width will decreased, reducing size of the symmetrical and differential inductors and improves their performances significantly. These findings together with the aggressive downscaling of feature size in silicon-based transistors continue to bolster silicon technologies as preferred design platforms for cost-sensitive mobile communication products.

Model verifications with a giga-hertz differential amplifier revealed good correlations between SPICE simulated and on-wafer measured circuit characteristics demonstrating high accuracy and scalability of the two proposed scalable RF inductor models. Use of differential inductor instead of two symmetrical spiral inductors as the output matching inductors lead to considerable amount of chip size reduction, higher differential gain, larger common mode rejection ratio and smaller noise figure for the differential amplifier. These results reinforce the fact that inductors must be supported by scalable models, offering designers libraries of inductors with fine variations in inductance values as well as flexibilities to choose between small size-driven or high performance-driven inductors

for their RF circuits. Without such libraries, they remain handicap with limited techniques to improve circuit performance or reduce the cost of their RFIC.

Experimental circuit results have shown that without considering interconnects' parasitics in the design phase, fabricated RF circuits deviates from simulated circuit results, exhibiting characteristics such as power losses and shifts in circuit operating frequencies. To address this issue and to minimize the iteration cycle for silicon-based RFIC design, RF interconnect test structures are designed, characterized and modeled to predict their inductive and resistive characteristics as well as substrate losses at radio frequencies. A new figure of merit, interconnect intrinsic factor, I_F , has been proposed in this research work to serve as a convenient quantitative indication for circuit designers as to how interconnects affect the performance of RFICs. The SPICE-simulator compatible double- π interconnect model proposed in this work can accurately emulate the RF characteristics of metal lines, exhibiting continuity and scalability across physical dimensions of the interconnects. Circuit verifications using giga-hertz amplifiers and voltage controlled oscillator show that RF interconnect model out-perform conventional RC approach, achieving excellent correlations between SPICE simulated and on-wafer measured circuit characteristics. Deviations from the measured gain of not more than 1 % is achieved when RF interconnect model is used to predict the circuit characteristics for amplifiers with different interconnect widths. The RF interconnect model has also accurately predict measured oscillation frequency for a voltage controlled oscillator to within 3 % error. The proposed methodology of tackling backend interconnects has demonstrated that it is possible to achieve cost-effective one-pass design success for silicon-based RFICs when accurate device as well as interconnect SPICE models are adopted in RFIC design flows.

7.2 Recommendations for Further Research

In most silicon-based RF circuits, top metallization interconnect is the preferred choice that RF circuit designers would use to provide electrical connections between devices. Designers would also, as much as possible, use straight interconnects (not with 45° or 90° bends) and avoid placing 2 interconnects carrying RF signals too close to each other such that inductive and capacitive coupling would affect circuit performance. In every new technological node, more metallization levels are implemented for higher device integration density and advanced active devices having exemplary RF performances are being developed. The future of silicon processing technology is promising and will be used in millimeter-wave applications such as automotive radars. These automotive radar applications include automatic cruise control 'long-range radar' operating at 77 GHz which enables a vehicle to maintain a cruising distance from a vehicle in front; anti-collision 'short-range radar' operating at 79 GHz that warns drivers of a pending collision, enabling avoiding action to be taken [91], [92].

In view of these technological trends and needs, the following topics should be investigated:

1. To develop interconnect models for lower level metallization such as metal 1-metal 5.
2. To investigate the capacitive and inductive mutual coupling effects between the interconnects, from a circuit level perspective.
3. To study the effects of having 45 degree and 90 degree bends on interconnects and model these effects up to 110 GHz.
4. To extend the physical design optimization and modeling of interconnects, symmetrical and differential inductors up to 110 GHz, beyond the 90 nm RFCMOS technological nodes. For these models, to also include capabilities to predict over-temperature device behaviors.

Author's Publications

Journal Publications

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2. **C. B. Sia**, B. H. Ong, K. S. Yeo, J. G. Ma and M. A. Do, "Accurate and Scalable RF Interconnect Model for Silicon-based RFIC Applications", *IEEE Trans. Microwave Theory and Tech.*, vol. 53, no. 9, pp. 3035-3044, Sep. 2005.
3. **C. B. Sia**, B. H. Ong, K. W. Chan, K. S. Yeo, J. G. Ma and M. A. Do, "Physical Design Optimization of Integrated Spiral Inductors for Silicon-Based RFIC Applications", *IEEE Transactions on Electron Devices*, vol. 52, no. 12, pp. 2559-2567, Dec. 2005.
4. **C. B. Sia**, B. H. Ong, W. M. Lim, K. S. Yeo and T. Alam, "Modeling and Layout Optimization of Differential Inductors for Silicon-based RFIC Applications", *IEEE Trans. Electron Devices*, vol. 55, no. 4, pp. 1058-1066, Apr 2008.
5. A. F. Tong, W. M. Lim, **C. B. Sia**, K. S. Yeo, Z. L. Teng and P. F. Ng, "RFCMOS Unit Width Optimization Technique", *IEEE Trans. Microwave Theory and Tech.*, vol. 55, no. 9, pp. 1844-1853, Sep. 2007.

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